AD7280 Capability Demonstration

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Abstract

This report presents a demonstration product created for Analog Devices, Inc.'s AD7280. The AD7280 is a lithium ion battery monitoring system that typically uses several chips in series. This design makes use of an array of current mirrors to allow the AD7280s to be used in parallel. A GUI was also created to allow user interaction. Finally, a battery simulation was created so that adjustable inputs could be applied to the system, thus greatly improving the effectiveness of the demonstration.

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Executive Summary

It is known that the world's fossil fuel supply is running out. There are also many environmental hazards associated with the use of and drilling for fossil fuels. One solution to these problems is hybrid cars. Hybrid cars run on a combination of gasoline and rechargeable batteries. This increases fuel mileage and reduces the total amount of fossil fuels that is needed per hybrid car. One new and efficient kind of rechargeable battery that can be used in hybrid cars are lithium-ion batteries. However, these batteries are not perfect and need to be monitored due to certain complications that can result from low charge, over charge, low temperature, or high temperature.

The company Analog Devices, Inc has come up with a device called the AD7280 that serves exactly this purpose. The AD7280 is an analog to digital converter that can monitor the temperature and charge of six lithium-ion battery cells. A typical hybrid car would use one hunderd of these lithium-ion battery cells to help power the vehicle. A fully charged lithium-ion battery cell has up to a four-volt potential meaning the series addition of all 100 battery cells can be up to 400 volts. The AD7280 is capable of monitoring up to 5000 of these cells using its ability called the *daisy chain*. In typical applications, such as in a hybrid car, 100 battery cells are used. In the daisy chain mode, the devices are connected in a series configuration and communicate on seven data lines using current as signals. They run on a differential voltage with the total absolute voltage being 400 volts. This means that when Analog Devices tries to demonstrate the AD7280 to potential customers, a 400-volt supply is required to present the product's full capabilities. Such a high voltage supply causes complications with safety and portability. Our project is to create a system that can show off the capabilities the AD7280 and eliminate the safety and portability complications.

The solution to this high-voltage demonstration problem, and the major design problem of this project, is to rearrange the configuration and put the AD7280s in parallel, meaning all of them run on the same, lower voltage. This was accomplished using a current mirror circuit that allows the current signal data to be mimicked across different voltage levels. Two AD7280s would remain in series to prove that the concept works while the next two AD7280s are in parallel with the previous two, communicating through the current mirrors. Since the parallel configuration only requires enough voltage to run two AD7280s plus the current mirrors, a supply of only 51 volts is needed to operate an arbitrary number of AD7280s. The two AD7280s in series will use 45 volts as Vdd while the current mirrors operate at three volts outside of ground and Vdd, totaling 51 volts. This is a great improvement over the 400 volt supply required for the series configuration with respect to both safety and portability as a much smaller supply is possible.

Another major part of our system was designing a *graphical user interface* (GUI). The GUI needed to be presentable and easy to read to maximize the effectiveness of a demonstration. The final GUI was designed using the National Instruments LabVIEW software. The design can be displayed and interfaced with on a computer. It is capable of displaying all the capabilities of the AD7280s in a user friendly manner. This GUI shows all the voltages being read from the battery cells, their temperature readings, all of the control registers, and some alert indicators. This GUI allows the user or the presenter to modify and read all the control registers to show the behavior of the AD7280s under any conditions

desired. The software communicates to the AD7280s through the USB and a development board. The development board is connected to a demonstration board containing the AD7280s, which was also designed for this project, through a 96-pin connector.

The demonstration board is a PCB that was designed to have the AD7280s in the parallel configuration as previously described. It has a total of ten AD7280s and four current mirror circuits connecting the AD7280 series pairs together. Along with an additional driver board, the demonstration board can perform the previously stated functions with all of the functionality and components consolidated into two boards. The driver board connects to the demonstration board through a 64-pin connector. It acts as the lithium-ion battery cells that the AD7280 monitors by controlling the voltage that is read by the AD7280s using resistors. There are also a set of potentiometers on the driver board that are used to adjust resistances to show the AD7280's ability to read a range of voltages. It also has the ability to measure current going through the system. Figure 1 shows a top level block diagram of the whole system.

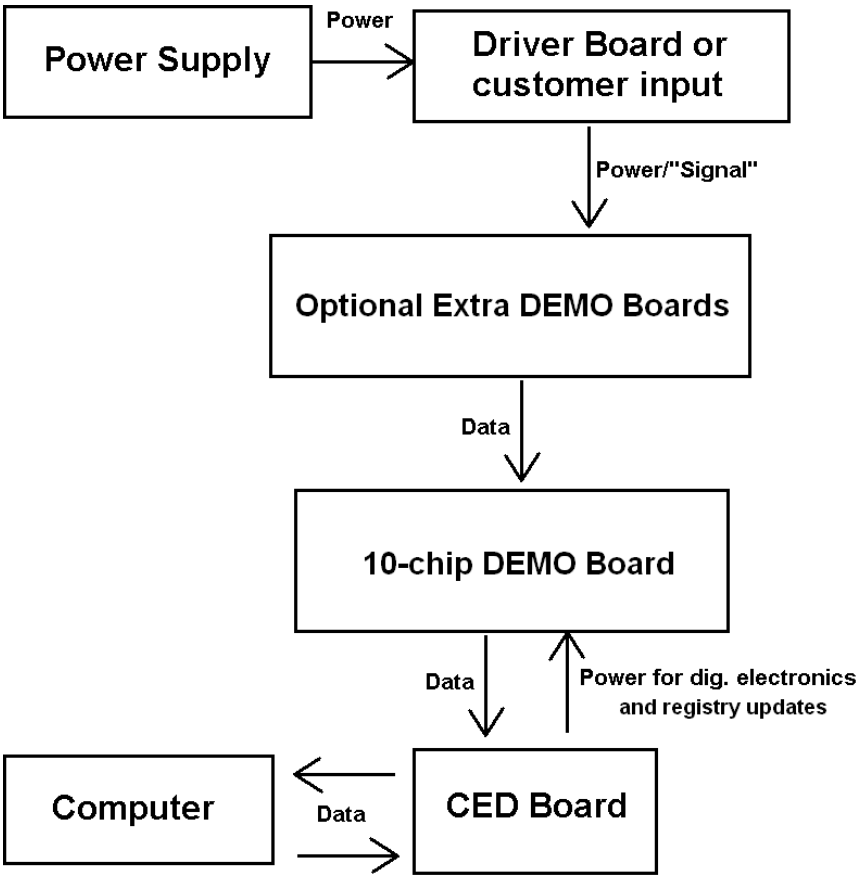

Figure 1 – System-level block diagram of our project

With the demonstration PCB and driver board, an effective showcase of the AD7280's capabilities can be done.

The DEMO board PCB was received late in the project. The procedure in Section 9.6 was modified before testing the board. It worked with two AD7280s immediately but troubleshooting was required when introducing more chips. After this was done, the DEMO board was able to function correctly with four AD7280s. Due to time constraints, four was the highest number of chips that were

tested. Since each of the current mirrors and AD7280 pairs are in parallel, the DEMO board will work with ten AD7280s, as intended. The driver board that was built to drive the DEMO board inputs was successfully completed and enclosed in a box with potentiometer knobs and a 64-pin connector. This had to be converted to drive the AD7280 EVAL board for two reasons. First, time constraints prevented the DEMO board from being fully tested, and second, post-manufacturing rework which caused the DEMO board to no longer be as presentable as would be required for a marketing presentation. The converted driver board, EVAL board, and GUI were then all used into the system. When this was done, the software correctly read the adjustable voltages given to it by the driver board and the GUI performed as intended.

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1. Introduction

Over the past several years, it has become evident that the Earth's natural fossil fuel resources are starting to reach what is known as *peak oil*, [6] or *Hubbert's Peak* [7]. M. King Hubbert first proposed in 1956 that eventually, due to the irreplaceability of fossil fuels, we would eventually reach a point where oil production drops off not because of reduced demand for energy, but because of physical limits on how much can be extracted from the ground. Crude oil prices have skyrocketed over the past ten years, climbing close to 700% in 2008 dollars [8]. Additionally, environmental concerns have begun to encourage conservation efforts both in the United States and abroad.

Environmental concerns exist for both the use of, and drilling for, fossil fuels. A fossil fuel is defined as "An energy source formed in the Earth's crust from decayed organic material. The common fossil fuels are petroleum, coal, and natural gas" [9]. They are drilled for and mined in various locations throughout the world. There are several environmental concerns regarding the drilling for fossil fuels. For one, it is possible to corrupt the ground water supply as "drilling can break the barrier between fossil fuel and groundwater reserves" [10]. It can also harm the physical environment and existing plants and wildlife because "when oil and gas are removed from a reserve under the earth, this leaves what is essentially a large hole underground. When there is no longer anything to support the land above, the land can collapse" [10]. Additionally there have been known to be complications and oversights with the handling of fossil fuels as "oil can enter the sea from spent drilling sites [and] oil refineries can also discharge oil into the environment as waste" [11]. These concerns with the actual acquiring of fossil fuels are not the only ones that exist when is comes to the overall use of fossil fuels.

There are also environmental concerns with the burning and combustion of fossil fuels. The combustion of fossil fuels emits carbon dioxide which "is considered a greenhouse gas as it traps heat (infrared energy) radiated by the Earth into the atmosphere and thereby contributes to the potential for global warming" [12]. Additionally, "burning fossil fuels also releases sulphur (sic) dioxide and nitrogen oxides. These gases contribute to the greenhouse effect, form acid rain, and can make the air unhealthy to breathe in urban areas where their concentrations are normally highest" [11]. All of these environmental concerns are on top of the fact that the world fossil fuel reserves are running low. At the rate of consumption in 2003 and with the amount of fossil fuels left on the planet, there remains approximately 1,000 billion barrels of oil, enough to last 38 years, 5,400 trillion cubic feet of natural gas, enough to last 59 years, and 1,000 billion metric tons of coal, enough to last 245 years [10]. Obviously with these supply concerns in addition to the environmental hazards, a solution needs to be found. One of the solutions is hybrid vehicles.

It is a known fact that hybrid vehicles use fuel more economically then a standard car. Of the three most common forms of fossil fuels, petroleum, the fuel used by cars, "ranked a close second (behind coal) as a source of carbon dioxide emissions from the consumption and flaring of fossil fuels in 2005, accounting for 39.0 percent of the total" [13]. This total is 28192.74 million metric tons [14] of carbon dioxide emitted worldwide in 2005. In a study done at the *Massachusetts Institute of Technology* (MIT), it was found that "hybrids, plug-in hybrids, and other advanced vehicle systems could be incorporated into the U.S. fleet rapidly enough to make a significant dent in total fuel use by 2035" [15].

This has the caveat that great efforts are made to “increase the [emphasis on reducing fuel consumption], increase the market penetration rate of advanced propulsion technologies, and find ways to reduce the rate of growth in demand” [15]. If these things are done, say the MIT researchers, the “total fuel use in 2035 could end up being less than half what it would be if we take no action, with greenhouse gas (GHG) emissions reduced by almost as much” [15].

It is anticipated that as the population continues to grow and demand for energy climbs ever higher, gas prices and environmental concerns will play increasingly more important roles in modern society. One of the most visible solutions in American society is the *hybrid electric vehicle* (HEV) that came into prominence in August 2000 with the launch of the Toyota Prius. The 2008 model of the Prius gets 48 miles per gallon (mpg) city driving, 45 mpg highway [16], while the 2008 national average in the United States is 24.8 mpg [17]. With such a large gap in mpg between the average car and the possibilities of hybrid cars, it follows that hybrid vehicles can potentially help to solve the world's energy crisis.

While there are several different variations on exactly how it is achieved, all HEVs rely upon a gasoline engine to supplement power to a battery-powered electric motor, and also to recharge the battery when the energy stored in it has become depleted. See Figure 2 for a pictorial description of the power train of a hybrid vehicle. Note that electric motors are at their most efficient at low speeds [18], while gasoline internal combustion engines are very efficient at high speeds [19], so combining the two allows for maximum gas mileage. Additionally, HEVs are able to partially recharge their batteries during braking by effectively running the electric motor in reverse, thus producing a current into the battery [20].

Given that HEVs are reliant upon batteries, and that moving a mass as large as a car requires a large amount of energy, a high capacity, fast-recharging, stable, safe battery is required. For the moment, the industry has decided upon *lithium ion* (li-ion) battery technology to fulfill this need. Li-ion technology has relatively lightweight materials, high energy density, provides large instantaneous power supply, does not exhibit a *memory effect*[1], and allows for many charge/discharge cycles without aging.

[1] A *memory effect* is a term generally used to describe how NiMH and NiCd batteries lose capacity when they are not completely discharged before being recharged. A memory-like effect can also be seen when batteries are overcharged, which causes them to experience what is known as a voltage depression where the voltage provided by the battery drops quickly over time, even at low current draw. Overcharging and the resulting voltage depression does not actually reduce the energy capacity of the battery, but devices monitoring the batteries will falsely indicate that they need to be recharged before they are truly out of energy.

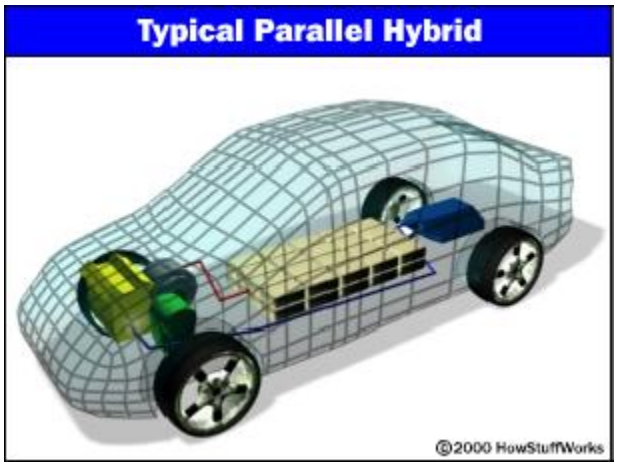


Figure 2 – Hybrid car. The blue section in the back of the car is the gas tank. The large yellow and black box block in the center of the vehicle is the battery bank. The grey cylindrical object is the electric motor. The yellow block represents the gas engine. Finally, the green object represents the transmission of the vehicle. Reprinted with permission from [1].

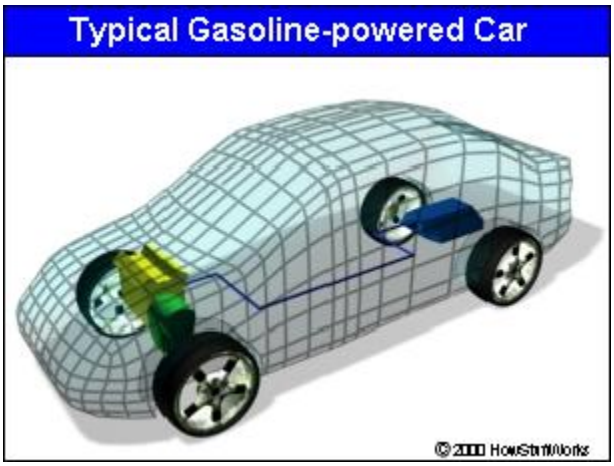


Figure 3 – Gas car. The colored sections of the vehicle represent the same objects as in Figure 2. Note the lack of the battery, as well as the electric motor it would power if either were present. Reprinted with permission from [1].

However, there are several disadvantages to li-ion technology. First, due to the high energy density, if manufacturing errors or high stresses occur, li-ion cells are prone to catching fire, and even explosions [21]. In an automotive application, this is to be avoided at all costs. Additionally, while there is no memory effect associated with lithium-based batteries, they do lose capacity as they age. At higher temperatures, the aging process is particularly damaging [22]. Finally, there is no such thing as a *deep discharge*[2] li-ion battery. If the cells are discharged too far, they become unstable when recharged, and again, they can explode. As a result, while li-ion batteries carry great potential, they need to be monitored constantly to ensure that they are not damaged. For our project, we attempt to design a device intended to demonstrate the capabilities of the AD7280, a chip manufactured by Analog Devices, Inc., which is capable of monitoring both the voltage and temperature of up to six cells in a li-ion battery [3].

[2] *Deep discharge batteries* are designed to be discharged to 20% or less of their total capacity.

1.1. Project Objectives

The objectives of this project are to create a li-ion battery simulator that can effectively demonstrate the capabilities of the AD7280 battery monitoring system during trade shows and in other customer-sensitive environments. The AD7280 is manufactured by *Analog Devices, Inc.* (ADI). The true application of this system uses 400 volts to monitor 100 individual 4-volt battery cells in a HEV. This voltage is too high to be safely worked within a demonstration setting. In order for ADI to effectively and safely demonstrate the capabilities of this product to potential customers, a lower voltage needs to be used. To do this, the series configuration that builds up to a 400-volt or greater potential needs to be converted to a parallel configuration that uses a much lower (and safer) voltage. Referring to Figure 4, notice that in the actual application each consecutive AD7280 is given inputs which are at a higher voltage than the previous chip. Contrast this with Figure 5, the parallel configuration of AD7280s, which allows us to monitor many cells at a safe voltage. Due to user interface, size, and weight considerations, this project monitors only 60 cells instead of the anticipated 100 or more that would be used by an automotive company. This new configuration will be laid out on a printed circuit board and will be portable, with its own on board power supply to both power the monitoring system, and simulate the battery voltages. The use of a USB interface between the system and computer software will be investigated and applied if possible. The interface will be used to set the simulated voltages, as well as to transmit data about the voltage and temperature outputs from the AD7280s. That data will then be displayed on the computer screen. If a USB interface is not found to be feasible, another means will be realized to control the voltage inputs to the AD7280s.

1.2. Vision

These objectives, when realized, will allow Analog Devices to demonstrate the full capabilities of the AD7280. Our mission is to achieve these objectives by creating and designing a stand-alone *printed circuit board* (PCB) that requires a voltage supply of less than 60 volts to monitor 60 cells and uses a presentable GUI that will make the product appealing to the customer. The market base of the hybrid and plug-in car industry continues to broaden, and by achieving our objectives we can contribute to the growth of an evolving and globally important industry. In order to make inroads into the marketplace, though, a working product needs to be developed and effectively marketed to major automotive suppliers. In our case, a "working product" will be in the form of a device that can be brought to a trade show, or to a customer's headquarters, and will demonstrate the ability of the AD7280 to monitor li-ion battery cell voltage and temperature.

1.3. Specific Technical Goals

The goals we intend to fulfill follow. Our completed design must meet each of the following design objectives:

Ability to be Safely Demonstrated - The final design will use no more than 60 volts. To do this, the series of 60 cells application will be converted to a parallel application, which will allow each individual board to have sufficient voltage and still be safe for demonstration.

Durability - This device is going to be frequently transported and manipulated by non-experts (customers and managers, among others). As such, it needs to be able to take a beating and still perform to specification. We intend to accomplish this by having the board built professionally.

Clarity – Clarity is important for our project in two ways. First, after being introduced to the topic there should be no question about what is being demonstrated. Second, the GUI should be easily understood, including both the *human computer interaction* (HCI) and data output sections. This means that people should not have difficulty understanding what the buttons on the GUI do, and they should be able to understand what the GUI is displaying at all times.

Presentable Design - The PCB should be as small and as well laid out as possible. It should also be able to use a portable power supply. Additionally, the device should appear professionally made.

User Interface - The battery monitoring device GUI should be presentable and appealing to potential customers. To do this, the interface that was previously developed in LabVIEW will be modified to account for both the new parallel configuration, as well as to show off the performance of the AD7280 in an eye-catching manner.

Adjustable voltage inputs - One major feature required by ADI is the ability to show off the alarm features of the AD7280. If the cell voltage or temperature goes outside of the allowable ranges, the AD7280 is supposed to raise alarm flags so that an outside micro-controller can take appropriate actions. This is especially important when talking about li-ion batteries in the automotive industry, as li-ion batteries have been known to catch fire. Obviously, this is to be avoided when driving down the highway at 100 kph. The adjustable voltages are supposed to simulate both normal and alarm conditions, which should be reflected by the GUI flashing warning lights. These voltage inputs are going to be supplied from what will be referred to as a *driver board* from now on.

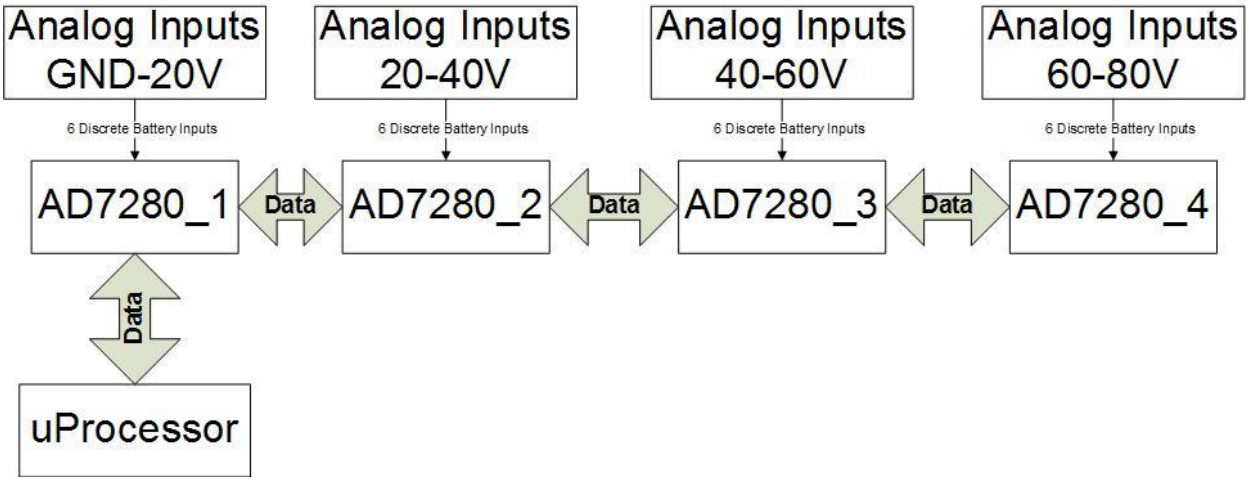


Figure 4 – Series configuration of the AD7280. This is the configuration that will be used in a real-world application.

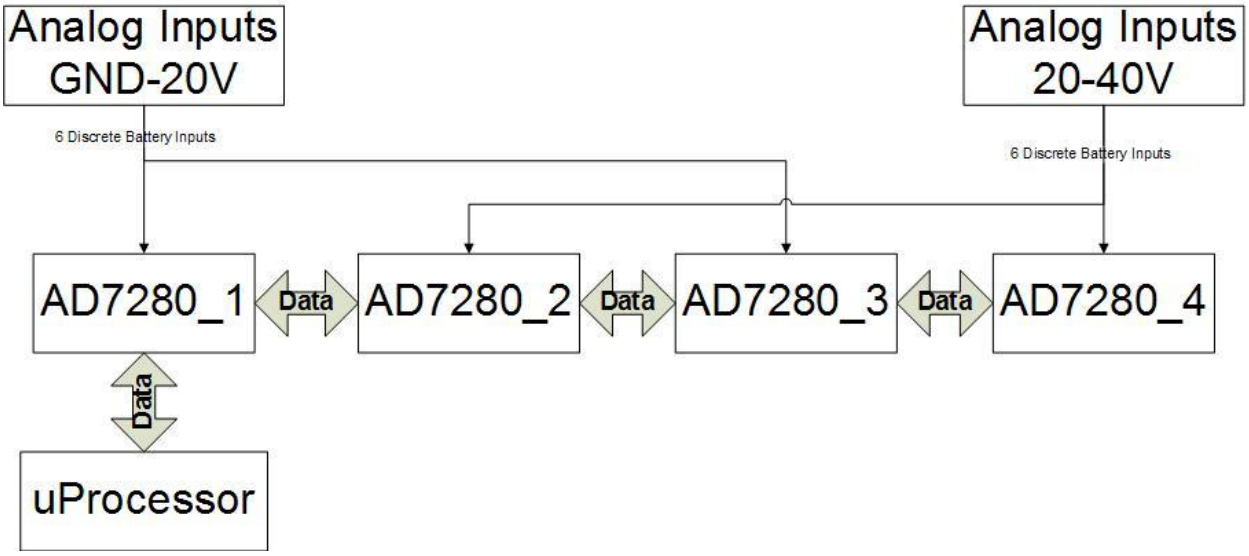


Figure 5 – Parallel configuration of the AD7280. This is the configuration that our project intends to utilize.

2. Background Research

This chapter lists the various underlying technology of which our project makes use. It describes each technology in sufficient detail that a person unfamiliar with the concept will be able to understand the rest of the paper. Readers who are familiar with a given topic can feel free to move on to the next without fear.

2.1. Li-ion Battery Technology

Batteries are an electrochemical energy storage system. They came into existence in the year 1800, created by Alexander Volta [23]. Batteries are made of one or more cells, each of which has the basic elements of an anode, a cathode, and an electrolyte or separator which prevents the anode and cathode from coming into direct contact. When discharging, electrons flow from the anode, though the load, to the cathode. In a rechargeable battery, the opposite holds true during the charging cycle [24]. Including Volta's original battery, batteries have been created using such varied anode/cathode pairs as zinc/silver [23], sponge metallic lead/lead dioxide (lead acid), cadmium/nickel oxyhydroxide (NiCd), rare earth metal/nickel oxyhydroxide (NiMH), and many other chemicals [25].

Each combination has its own particular advantages and disadvantages. Some chemistries have higher voltages (corresponding to higher energy density), some are able to provide higher currents for longer periods of time without voltage drop, and some are lighter or can be manufactured more easily than others. Of course, depending on the materials and processes used to construct the batteries, different batteries will have higher costs [25].

Batteries based upon lithium metal were first proposed in 1912 [26]. These batteries were non-rechargeable, and did not even become commercially available until the 1970's [26]. When rechargeable lithium metal batteries were investigated during the 1980's, safety problems plagued the research, and the products were never successfully released [26]. The problem with lithium-based batteries is that, along with being the lightest metal, lithium metal has the single highest energy density. When repeated charging and discharging of the batteries caused changes on the lithium anode, which in turn reduced the thermal stability of the battery [26]. Quoting from [26], "When this occurs, the cell temperature quickly approaches the melting point of lithium, resulting in a violent reaction called 'venting with flame'."

In 1976, around the same time that lithium metal batteries were first commercially offered, the lithium ion chemistry was put forth as another alternative [27]. The first commercial li-ion battery appeared in 1991 [26]. While li-ion batteries have slightly lower energy density than lithium metal batteries, they are much safer. Protection circuitry attached to each cell during manufacturing guarantees that the cells will not overheat violently, thus preventing a safety hazard [24]. Example circuitry is a temperature controlled switch that opens if the temperature grows too high. The opened switch does not allow further current to flow, which reduces the heat buildup inside the battery. Alternatively, the battery can be fitted with a membrane which punctures after a pressure buildup inside the battery. If this ever happens, the battery is permanently damaged and cannot be used [22]. Some cells are believed to be damaged during manufacture by small metal fragments puncturing the separator between the anode and cathode. Growth of these puncture holes over time, many charge/discharge cycles, and many thermal

expansions is believed to be the cause of the frequent reports of li-ion batteries catching fire or exploding in laptops [21].

On top of limiting manufacturing errors, correct charging/discharging schemes are vital to the safety and length of life of li-ion batteries. A nominally full li-ion cell will put out approximately 3.7V (citation needed). If the cell is discharged below 2.5V, the internal protection on the battery will open and cause the battery to appear dead [22]. Some specialized chargers are able to correct this phenomenon, but if the cell voltage is below 1.5V, even special equipment such as this cannot be used for safety reasons [22]. Additionally, for safety reasons, most protection circuitry on a li-ion cell does not allow a charge over 4.2V [22].

As stated above, discharging li-ion batteries below a certain threshold is detrimental to their lifetime. Additionally, it is very difficult to know when this threshold is approaching, as the capacity/voltage curve has a very sharp knee, shown in Figure 6. A similar, though less drastic, trend can be seen in NiMH batteries. On top of that, li-ion and NiMH batteries tend to have longer service lives when they are not stored at full charge [22] [28]. As a result of this, and going back to the Prius example given in the introduction, Toyota uses an electronic monitoring system to guarantee that does not allow the Prius' NiMH batteries to vary outside of the 45-75% capacity limits [28]. It seems logical that a similar occurrence can be expected for when li-ion batteries are used in place of the NiMH ones currently in the prius.

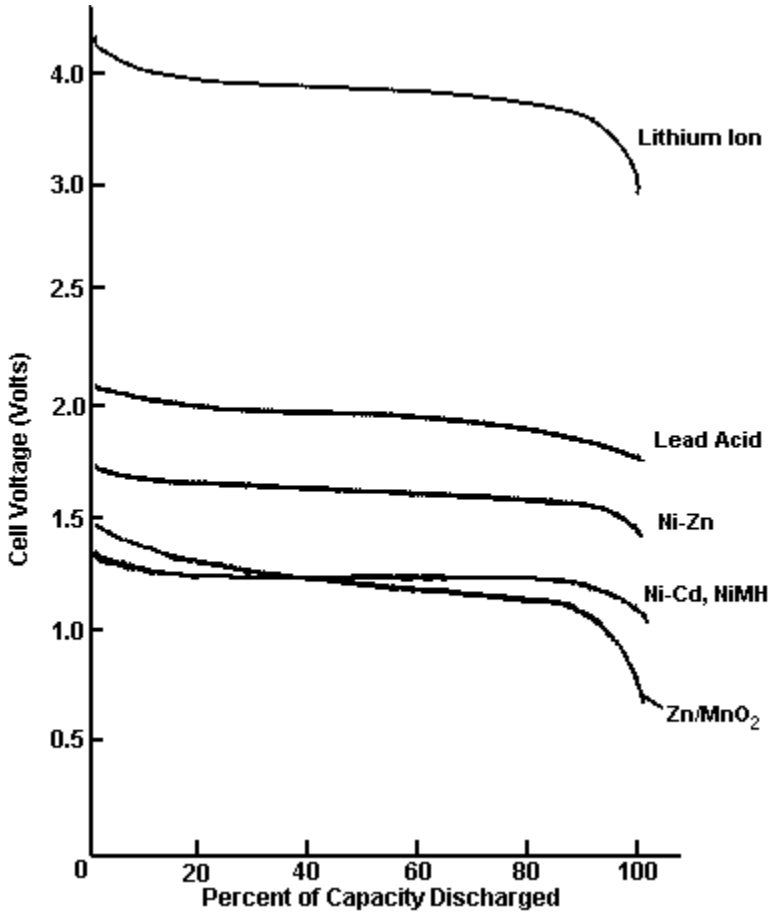


Figure 6 – Chart of capacity vs. cell voltage. Note the particularly sharp knee on the li-ion cell as it nears full discharge compared with other technologies. Reprinted with permission from [2].

2.2. Thermistors

Thermistors are resistive devices whose resistance changes with temperature [29]. They can be created with either positive or negative temperature coefficients. This makes them useful devices for sensing temperature if the relationship between temperature and resistance is well known. For instance, a voltage divider can be created using a resistor with a fixed value and a thermistor, as shown in Figure 7. Assuming a positive temperature coefficient, as the temperature increases the thermistor resistance increases, and so the voltage output will also increase proportional to the ambient temperature. This output voltage can then be sent to a controller or microprocessor which can respond accordingly.

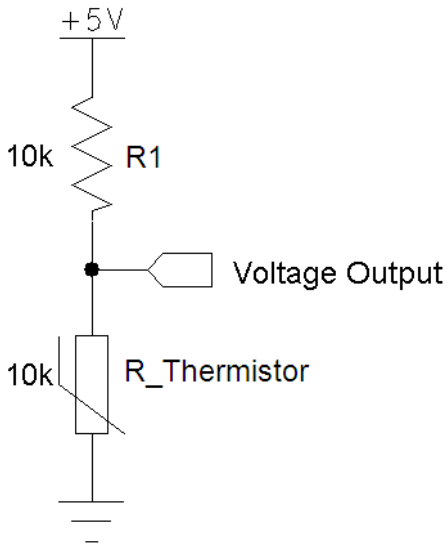


Figure 7 – Simple voltage divider network with a resistor and a thermistor. As the temperature of the thermistor varies, so too will it's resistance, and thus the voltage output will fluctuate. Note that the indicated value of 10k on the thermistor is a nominal resistance, and will vary as described in the product's datasheet.

2.3. Analog to Digital Converters

The primary purpose of an *analog to digital converter* (ADC) is to convert analog signals to discrete digital numbers in forms of bits [30]. This digital format can then be read by a microcontroller or a computer. This device is seen in many monitoring systems such as battery voltage monitoring, temperature monitoring, and others [3].

Some important concepts about the ADC include full scale voltage range, and resolution. Full scale voltage range is the maximum analog input that can be placed upon the ADC [30]. Some typical values on full scale voltage range ranges from 3 to 10 volts. Resolution is the number of discrete representation the number of discrete values the ADC can produce over the range of analog values which is based on the number of bits the ADC is capable of processing [30]. For example, a 2-bit ADC has 4 or 2^2 possible representations. If the full scale range of the ADC is 3 volts, this ADC will recognize analog inputs of 0 volt, 1 volt, 2 volt, or 3 volts. Anything in between those 4 discrete points will be rounded to the nearest level [30].

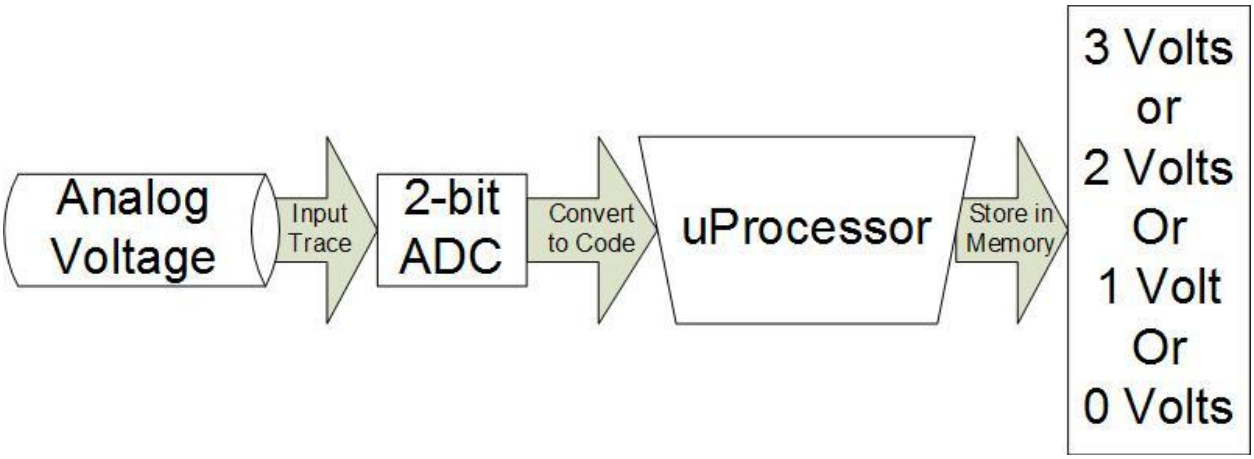


Figure 8 – Block diagram describing an ADC.

So if the analog input is 2.7 volts, the 2 bit ADC will return a value of 3 Volts. And if the Analog Input is 0.9 volts, the 2 bit ADC will return a value of 1 Volt.

The value that the ADC returns is usually in form of a code which represents a certain voltage. Given a 3 bit ADC, the number of possible return values are 2^3 or 8 [30]. These values are 000, 001, 010, 011, 100, 101, 110, and 111. Figure 9 shows a plot of these codes vs. the fractions of the full scale resolution.

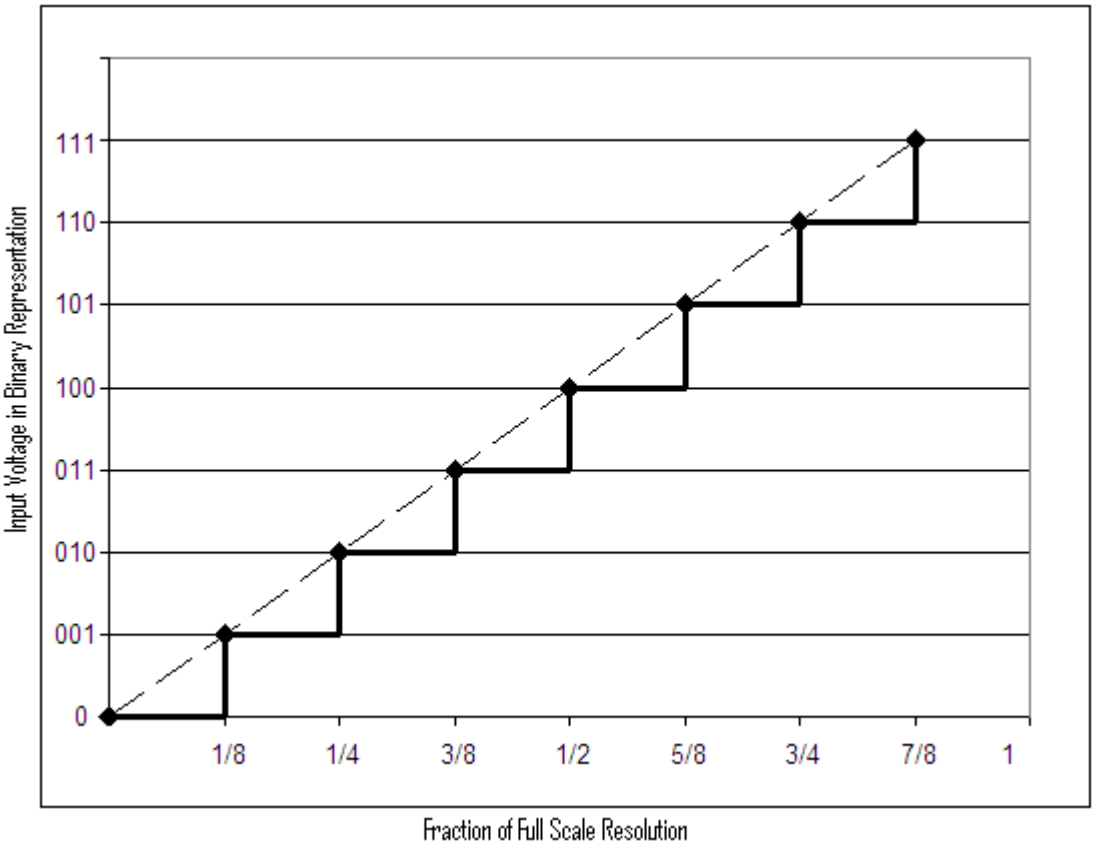


Figure 9 – Three-bit ADC output. Compare the dotted line, indicating an ideal transfer function, with the solid black line that indicates the actual output code with three-bit accuracy.

The dotted line in Figure 9 shows an ideal transfer function in which every representation in code corresponds exactly to the appropriate analog input if the accuracy was infinite. The solid black line indicates the actual output code for a given input at three-bit accuracy. However, since the accuracy is limited, this transfer function rounds everything down causing a quantization error. For example when the analog input voltage in Figure 9 is 1/9 of the full scale voltage range, the ADC will code this reading 000. However, because 1/9 is much closer to 1/8 than 0, we need the ADC to code this reading as 001. Therefore we introduce to the ADC a bit shift offset to deal with this. Figure 10 illustrates an example of this offset.

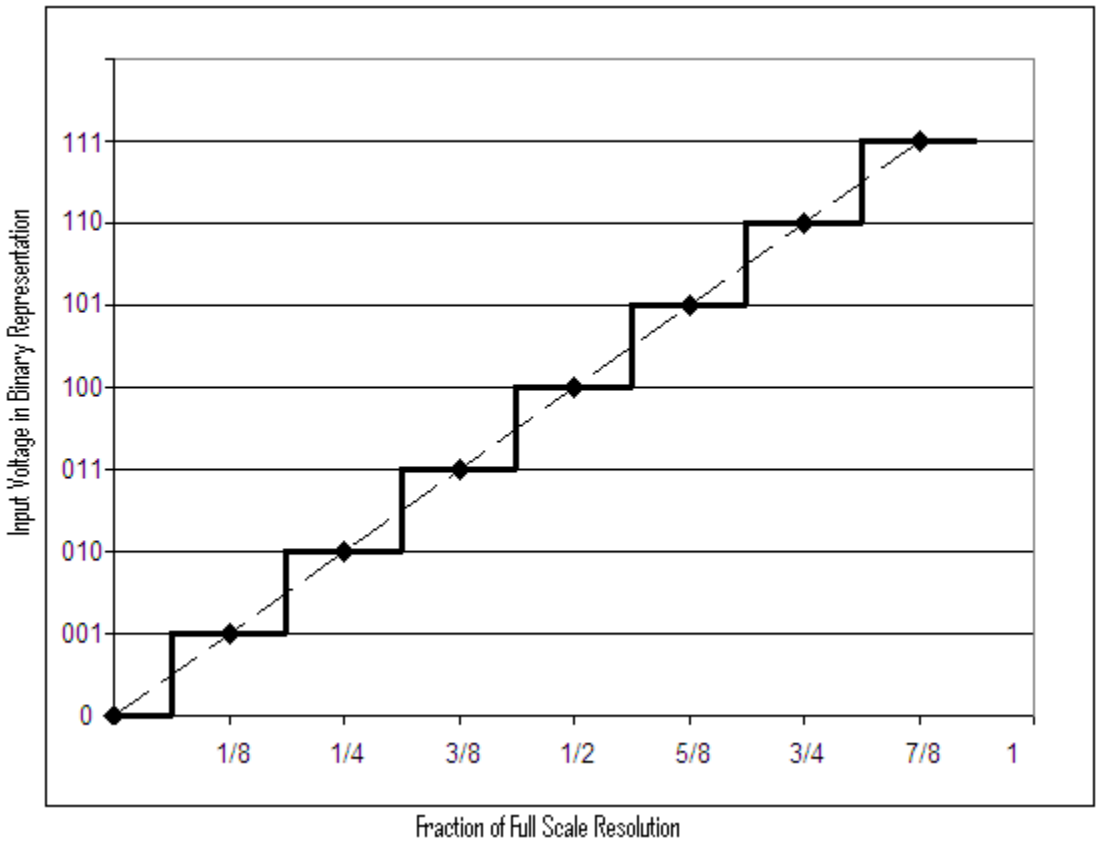


Figure 10 – Three-bit ADC with a ½ bit offset inherent in the design. The dotted line is an ideal transfer function, as in Figure 9, and the solid line indicates the code interpreted by the ADC.

Using the ½ bit shift, when the analog input voltage in the theoretical ADC indicated in Figure 10 is 1/16 and 3/16 of the full scale voltage range, the ADC will code this reading as 001. Similar readings are made throughout the input range. The output of this theoretical ADC introduces a rounding of the input to the nearest discrete representation.

Another important characteristic about ADCs is sampling to acquire data of the analog input signal. The frequency at which the ADC samples at determines the rate at which new digital values are acquired from the analog input signal. The higher the frequency with which the input signal changes, the higher the sampling frequency is required by the ADC. The Nyquist theorem states that the ADC sampling frequency must be at least twice the highest frequency inside the analog input signal [31].

2.4. The AD7280

The AD7280 is a 12-bit ADC from ADI [3]. Its purpose is to monitor li-ion and NiMH batteries. The AD7280 has six voltage inputs for six cell voltages as well as 6 thermistor inputs for temperature monitoring of the cells. The analog inputs are ranged from 0 to 5 volts. The device has configurable alert output which gives warning for situations in which the cells are not desired to be in such as low voltage or over voltage, and high temperature. The device is powered by the input voltages stacked together and it operates from 7.5V to 30V. The AD7280 communicates with a microcontroller through serial interface via the SDIN and SDOUT pins [3].

The AD7280 also has an ability called the daisy chain. The daisy chain ability allows multiple AD7280 to communicate with each other. Up to 50 devices can be linked together allowing for the monitoring of 300 cells, up to 1110 volts (3.7 volts each cell) [3]. See Figure 11 for a block diagram representation of the AD7280, and Figure 12 for a visual representation of the daisy chain.

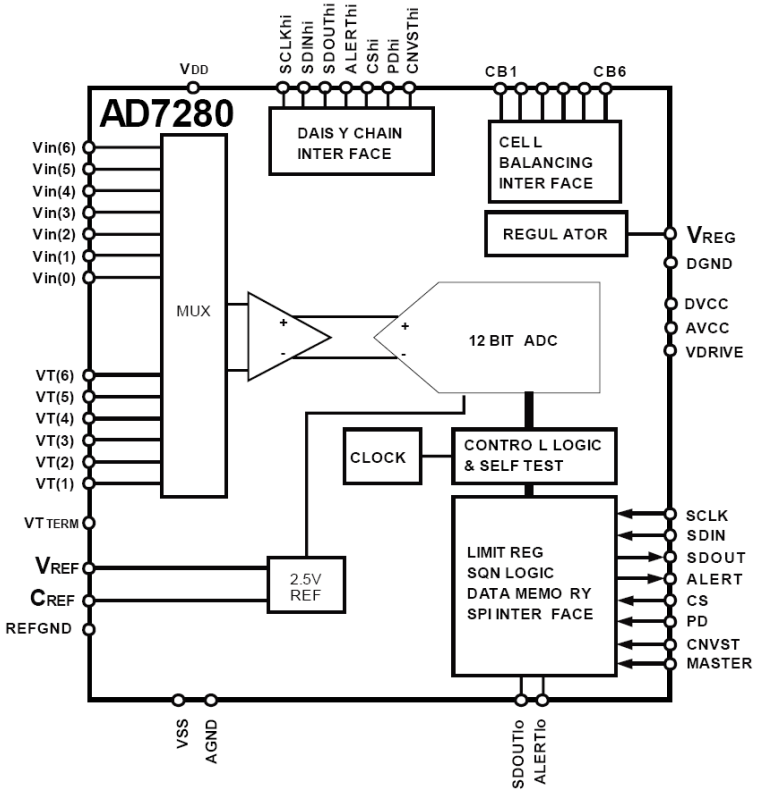


Figure 11 – Block diagram representation of the AD7280, including inputs and outputs. Reprinted from [3] with permission.

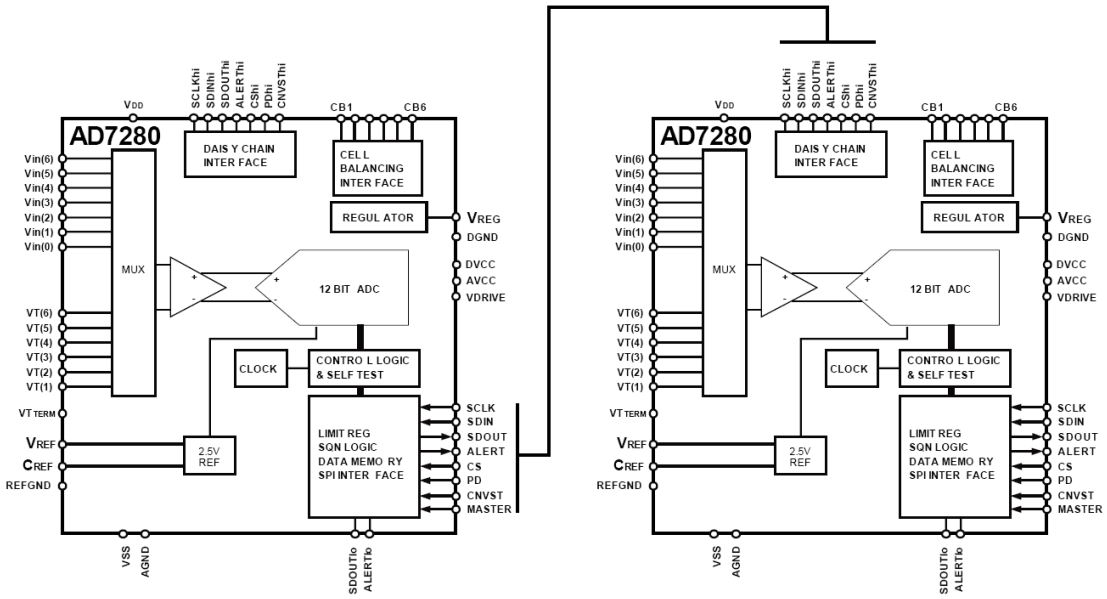


Figure 12 – Functional representation of the daisy chain interface used by the AD7280. Modified from [3] with permission.

Table 1 – Listing of the AD7280's daisy chain communication pins.

Pin Abbreviation	Pin Name	Pin Function
SCLK	Serial Clock	Input from the uProcessor which is transmitted from master to slave. Used to synchronize the AD7280s.
SDIN	Serial Data Input	Input from the uProcessor which is transmitted from master to slave. Used to set registers in the AD7280s.
SDOUT	Serial Data Output	Output containing information about the voltage and temperature of the battery cells the AD7280 is monitoring.
ALERT	Alert	Output indicating over-voltage, under-voltage, over-temperature, or under-temperature.
CS	Chip Select	Input indicating whether or not the relevant AD7280 is the active chip.
PD	Power Down	Input indicating that the chip should shut itself off.
CNVST	Convert Start	Input indicating when the AD7280 should begin a conversion sequence.

The AD7280s communicate through a 7-pin parallel bus. The pins are named to help provide understanding to the user. See Table 1 for a listing of the communication pins. When the master strobes

CNVST, the slave converts the data from the inputs attached to the slave and sends this data from the SDOUT pin to the master.

Each AD7280 device has the registers listed in Table 2.

Table 2 – List of registers in the AD7280. Table continues on next page.

REGISTER MAP			
Register Name	**Register Address**	**Register Data**	**Read/Write Register**
Cell Voltage 1	0h	D11 to D0	Read Only
Cell Voltage 2	1h	D11 to D0	Read Only
Cell Voltage 3	2h	D11 to D0	Read Only
Cell Voltage 4	3h	D11 to D0	Read Only
Cell Voltage 5	4h	D11 to D0	Read Only
Cell Voltage 6	5h	D11 to D0	Read Only
Cell Temp 1	6h	D11 to D0	Read Only
Cell Temp 2	7h	D11 to D0	Read Only
Cell Temp 3	8h	D11 to D0	Read Only
Cell Temp 4	9h	D11 to D0	Read Only
Cell Temp 5	Ah	D11 to D0	Read Only
Cell Temp 6	Bh	D11 to D0	Read Only
SELF TEST	Ch	D11 to D0	Read Only
CONTROL	Dh, Eh	D15 to D8, D7 to D0	Read/Write
OVER VOLTAGE	Fh	D7 to D0	Read/Write
UNDER VOLTAGE	10h	D7 to D0	Read/Write
OVER TEMP	11h	D7 to D0	Read/Write
UNDER TEMP	12h	D7 to D0	Read/Write
ALERT	13h	D7 to D0	Read/Write
CELL BALANCE	14h	D7 to D0	Read/Write
CB TIMER 1	15h	D7 to D0	Read/Write
CB TIMER 2	16h	D7 to D0	Read/Write
CB TIMER 3	17h	D7 to D0	Read/Write
CB TIMER 4	18h	D7 to D0	Read/Write
CB TIMER 5	19h	D7 to D0	Read/Write
CB TIMER 6	1Ah	D7 to D0	Read/Write
PD TIMER	1Bh	D7 to D0	Read/Write
READ	1Ch	D7 to D0	Read/Write

Registers CELL VOLTAGE 1 to CELL VOLTAGE 6 gives the voltage readings in code for cells 1 through 6, respectively. Similarly, registers CELL TEMP 1 to CELL TEMP 6 gives the thermistor readings in code for cells 1 through 6. The registers OVER VOLTAGE, UNDER VOLTAGE, OVER TEMP, and UNDER TEMP are user configured for conditions that the user feels the need to set off the ALERT register. The CB TIMER 1 to CB TIMER 6 allows to the user to program individual ON times for each of the Cell Balance outputs between 0 to 30 minutes with 1 minute resolution. Lastly, the PD TIMER allows the device to power down after a certain period of being ON.

During the use of the daisy chain, bits D23-D18 are used to select devices. Device select address should be written and read LSB first [3]. Reference Table 3 for a complete listing of addressing information.

Table 3 – Address labels for AD7280

Device Address	Register Address	Data	Address All Parts	Additional Zero's
D23-D18	D17-D12	D11-D4	D3	D2-D0

2.5. LabVIEW

LabVIEW is a platform for graphical programming developed by National Instruments that allows the programmer to program embedded systems graphically [32]. A LabVIEW program is called a VI, and a VI call other VIs during its runtime [32]. When a VI is called by another VI, the called VI is named a SUBVI [32].

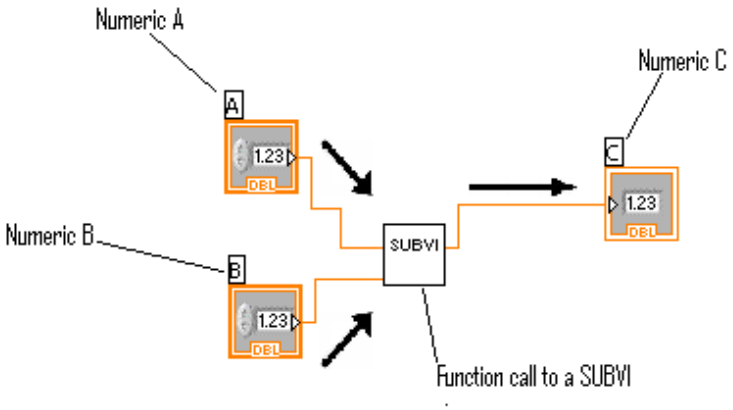


Figure 13 – SubVI call

Figure 13 shows that in the main VI, there are 3 variables (called Numeric in LabVIEW nomenclature) A, B and C. The SUBVI named “SUBVI” is called in this main VI and this SUBVI takes 2 inputs and gives 1 output. So the 2 variables, A and B are provided as inputs for the SUBVI and the output of the SUBVI is stored in the variable C.

Like other programming languages such as Java or C++, a platform compiler parses the LabVIEW code and generates machine code that the platform CPU can execute.

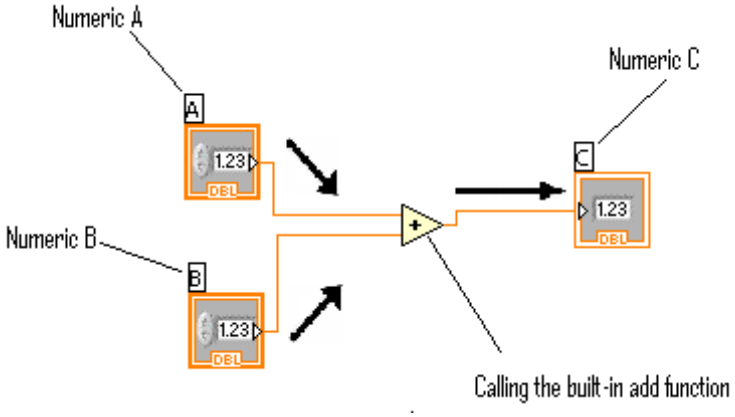


Figure 14 – LabVIEW adder code

Given the LabVIEW code shown on Figure 14, the equivalent C code for that would be int C, A, B; C = A + B;. Basically the code in Figure 14 and the C code both tells an interpreter to take the value stored in memory A and the value store in B and sum those 2 values and store the result to memory C.

The compiler would compile the LabVIEW code shown on Figure 14 to something that the CPU can run the same way the C compiler compiles C code [33]. For our project, we used an X86 architecture on a windows platform, so our compiler would create executable files from the LabVIEW code.

Similar to other programming languages such as C, C++, and Java, LabVIEW has a runtime library. According to [33], the LabVIEW runtime library

> contains approximately 750 exported functions that offer UI features like graphing, memory management functions for the dynamic arrays, and yes, even string formatting libraries similar to printf. This runtime library servers the same function for LabVIEW executables that the MFC libraries offer to executables built in C. The applications that you build in LabVIEW call into this runtime library to access helper functions and use routines and graphics that are commonly used. The applications that you build in LabVIEW call into this runtime library to access helper functions and use routines and graphics that are commonly used. The only difference between C and LabVIEW is that with C programs you often don't have to install these libraries because they are included with the OS, but with LabVIEW, your installer must include these libraries. LabVIEW executables are roughly the same physical size on disk as an equivalent C application, but because the LabVIEW runtime libraries need to be installed, the LabVIEW installers look like they are larger.

The reason that LabVIEW is used for this project is its ability to easily generate image objects.

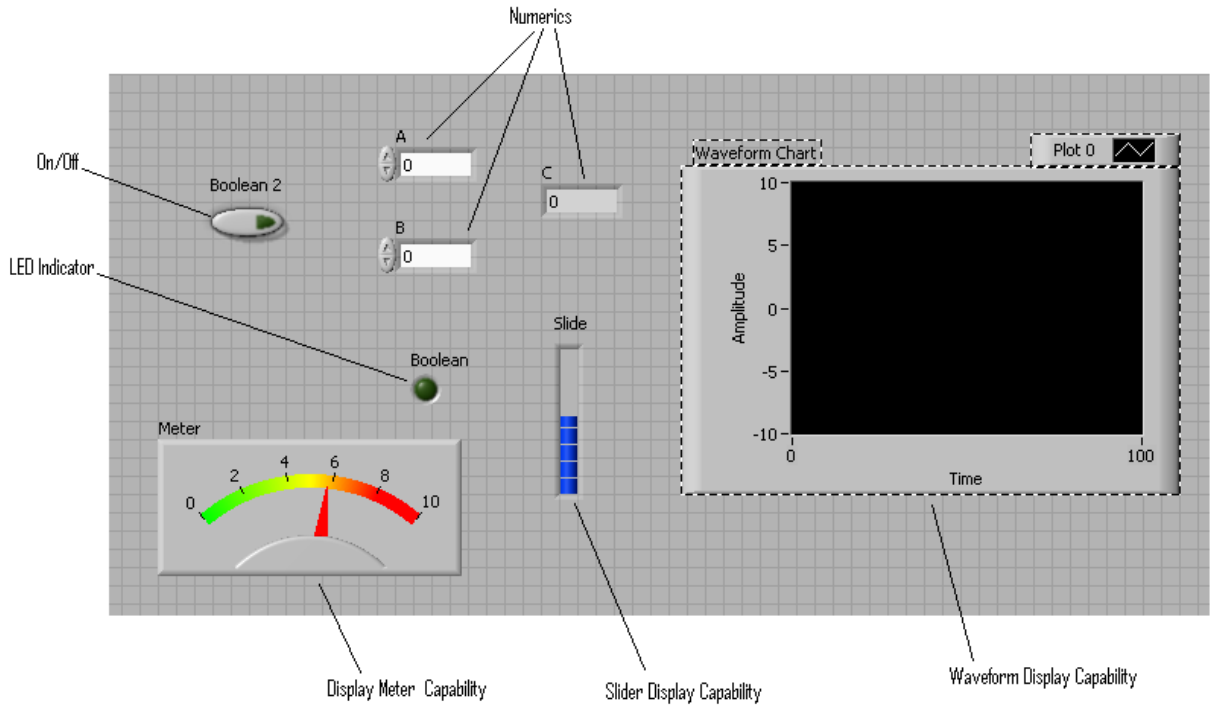


Figure 15 – Some LabVIEW displays

Figure 15 shows some of the capabilities of LabVIEW. On this figure we see LEDs, some variables, meters and slide indicators, and a graph. All these items are part of a library that the programmer can grab from at will. Therefore, due to the ease of interacting with graphical objects, LabVIEW is used for the presentation software.

2.6. Converter Evaluation & Development Board

Usually, a development board with USB capability and some I/O capability is provided so that a computer running LabVIEW can interface with a specific device, like the AD7280. National Instruments sells some of these boards. For this project, we are using a board called the *Converter Evaluation & Development* (CED) board developed by analog devices. "The CED1 board is part of a next generation platform from Analog Devices Inc., intended for use in evaluation, demonstration and development of systems using Analog Devices precision converters. It provides the necessary communications between the converter and the PC, programming or controlling the device, transmitting or receiving data over a USB link." [4].

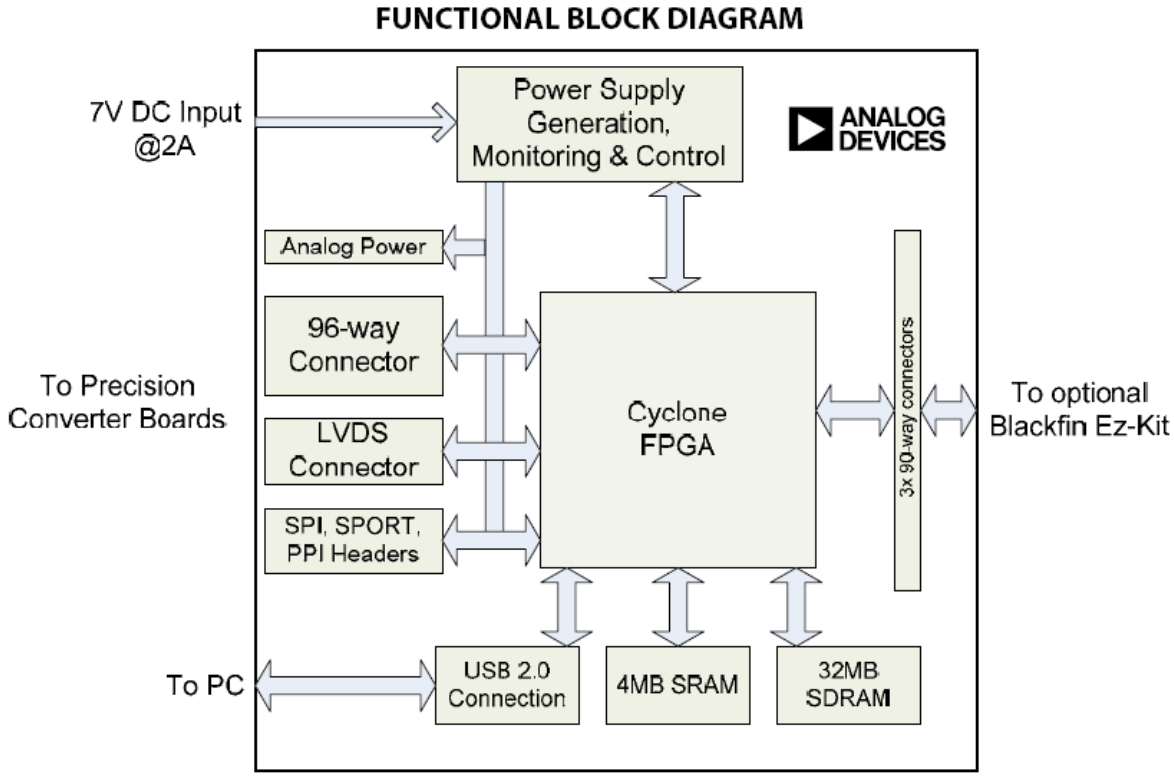


Figure 16 – Block Diagram for the CED Board. Reprinted from [4] with permission.

As shown in Figure 16, the CED board uses a 7 volt power supply and takes serial inputs and outputs to the PC through USB. It has a Cyclone FPGA to regulate this task. We connected board through the 96-way Connector to the *Evaluation Board* (EVAL board) which has 2 AD7280s in daisy chain in series so that a PC can talk to the AD7280s.

2.7. AD7280 Evaluation Board

The EVAL board contains 2 AD7280s linked in serial daisy chain as shown on figure 2. The master chip is connected to the 96-way edge connector which connects to the CED board as

previously stated. This connection has CS, SCLK, SDI, SDO, CNVST, ALERT, PD and a 7 volt power supply. All these data and control lines communicate to the SPI interface of the CED [5].

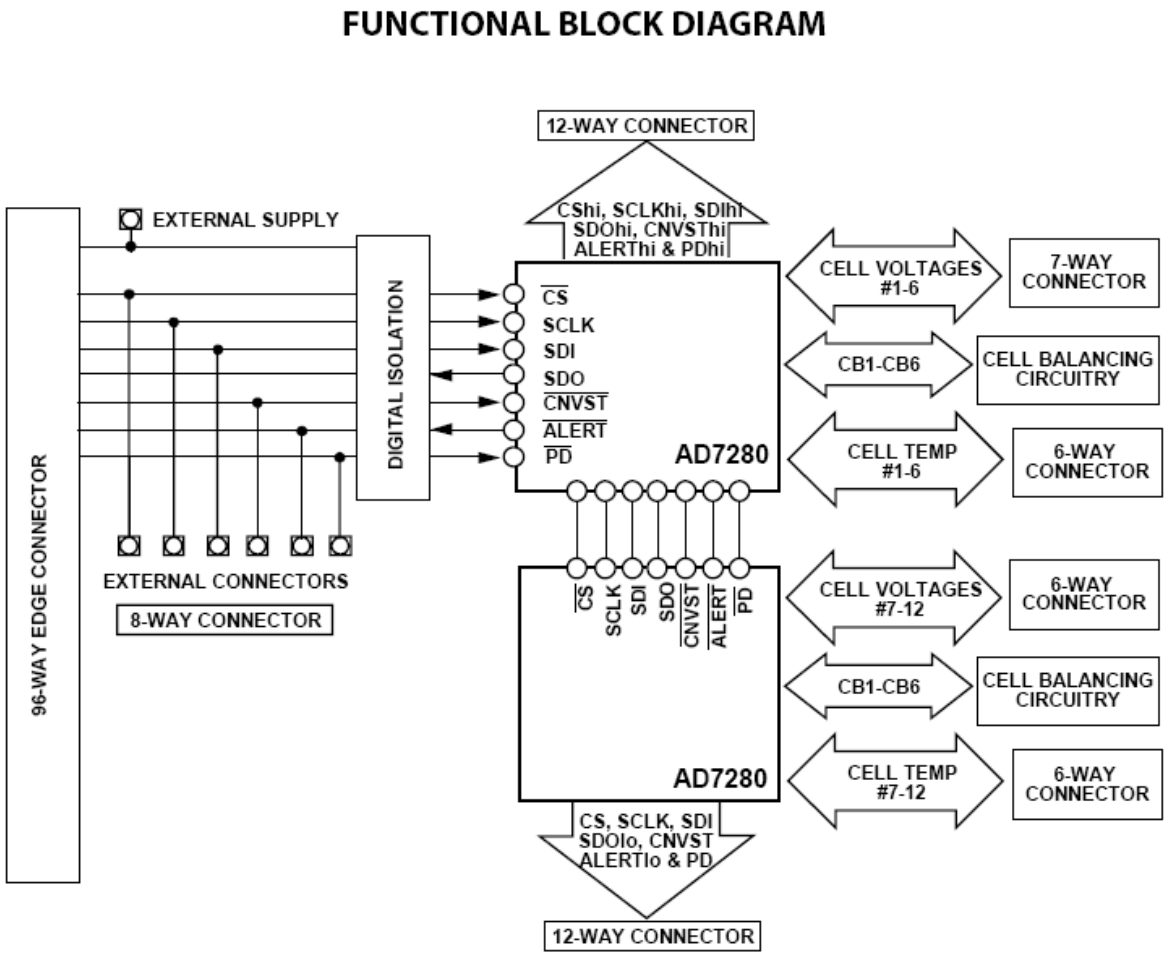


Figure 17 – Block diagram of the EVAL board. Figure reprinted from [5] with permission.

The slave device is connected to the master device in a standard daisy chain; therefore the master can know what inputs go into slave. The master device has a 7-way connector (J2 on EVAL Board Schematic) for cell voltage inputs and the slave device has a 6-way connecter (J3 on EVAL Board Schematic) for cell voltage inputs. This board also supplies both these devices with thermistor inputs as well as cell balancing circuitry [5].

The EVAL board can also be placed in a daisy chain with other EVAL boards. This is done by turning the master chip of an EVAL board to be a slave by moving a resistor R88 to the slot R89 (from EVAL Board Schematic) turning the board to be a slave board. Then connect the bottom 12-way connector (J15 on EVAL Board Schematic) shown on figure 2 of the slave board to another EVAL Board's top 12-way connector (J16 on EVAL Board Schematic) [5].

Additionally, the EVAL Board provides several test points that are useful for debugging purposes. These test points are: Alert1, SDO1, SDI1, CNVST1, SCLK1, PD1, CS1, VREG1, VREF1, Alert2, SDO2, SDI2, CNVST2, SCLK2, PD2, CS2, VREG2, and VREF2. These points can be probed with an oscilloscope from the analog ground of the whole board. Also the way that the CED reads conversion

data from the AD7280s is by grabbing a chunk of addresses of the AD7280s and sends that data value of these addresses to the PC [5].

2.8. Current Mirrors

One interesting concept that will be very important to the success of the project is current mirrors. A current mirror is an “electronic circuit that generates, at a high-impedance output node, an inflowing or outflowing current that is a scaled replica of an input current flowing into or out of a low-impedance input node” [34]. It is used to mimic the current in active devices regardless of voltage and loading. They are a set of matched transistors, in this case *bipolar junction transistors* (BJTs), that are connected as shown in Figure 18:

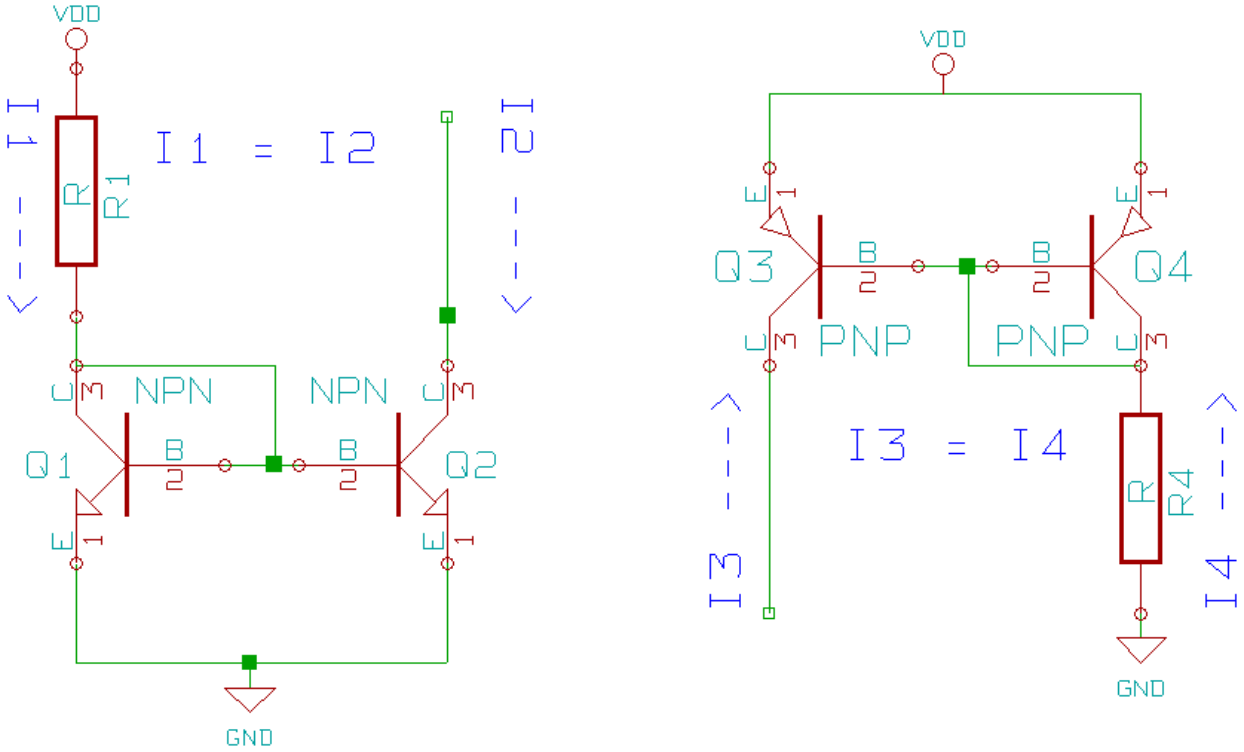


Figure 18 – NPN (left) and PNP (right) current mirrors.

The NPN mirror is said to be a “current-sinking type, because the regulating transistor [Q1] conducts current to the load from ground” [35]. The PNP mirror is said to be in a “current sourcing configuration, where the regulating transistor [Q2] connects the load to the positive terminal of the DC power supply” [35]. The way that these current mirrors work is the transistors Q1 and Q4 draw current from resistors R1 and R4, respectively. This causes a certain emitter-base voltage due to what is essentially a diode drop. Since the bases of the Q1 & Q2 and Q3 & Q4 are connected, and assuming the transistor pairs are matched, the same emitter-base voltage will appear at the output transistors Q2 and Q3. This means the same current flows in I2 and I3 as flows in I1 and I4, respectively. This current is ideally independent of the voltage across the input resistors, R1 and R4 because the base-emitter voltages of the transistors is largely unaffected by these voltages [36]. This behavior for the NPN current mirror, and similarly for the PNP current mirror can be derived in the following way:

The current I1 can be found using Ohm's Law: I1 = (Vb – Vbe)/R. Using Kirchhoff's Current Law at the collector of Q1: I1 = Ic1 + Ib1 + Ib2. It is given from the diagram that the base-emitter

voltage for both Q1 and Q2 are the same so it can be said that I1 = (β +2)Ib2, where β is the transistor gain, which is equal in Q1 and Q2 because they are matched. It can also be said that Ic2 = β * Ib2 = (β)*I1/(βf + 2) = Ir1/{1 + (2/β)} because of the same base-emitter voltages. Since β is assumed to be much greater then 2, as it should approach infinity, the conclusion can be drawn that Ic2 = I1, which is the same as I1 = 12 [37]. This would hold in an ideal case but in reality the currents are not the same. They are, however, nearly the same.

The current mirrors will be used to convert the series implementation of the AD7280 evaluation boards to a parallel configuration. One of each of the NPN and PNP current mirrors will be used for each of the seven data lines. The configuration of these current mirror pairs is shown in Figure 19.

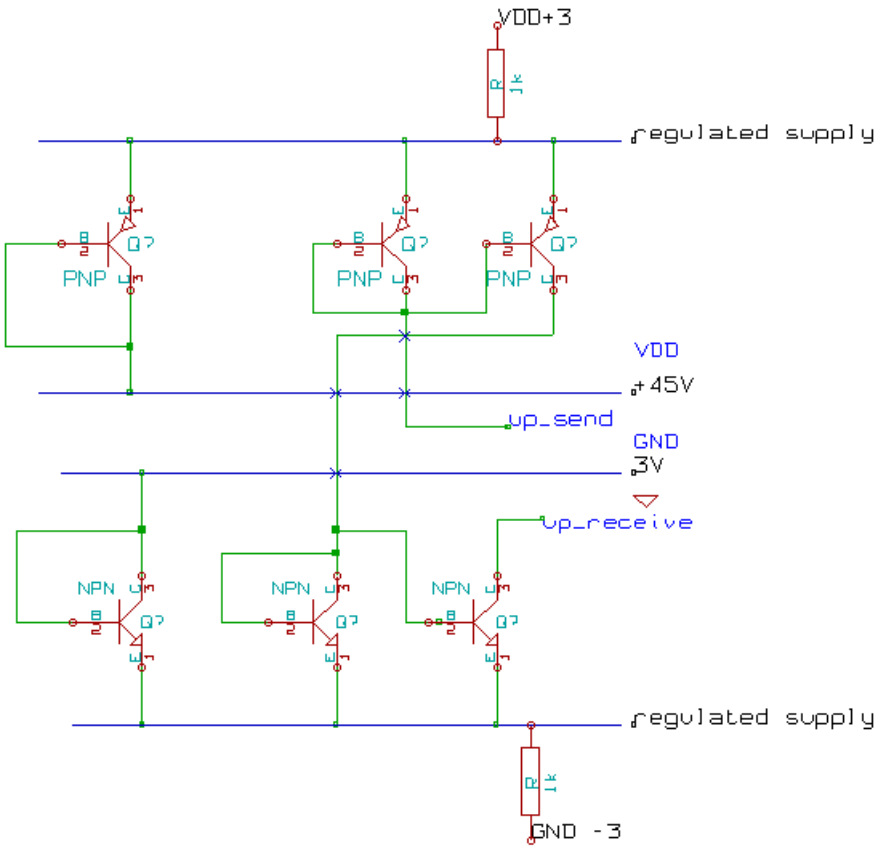


Figure 19 – Current mirror pair.

As Figure 19 shows, the current mirrors operate outside of ground and Vdd. This is because the collector voltage must be higher the emitter voltage for the NPN current mirror for current to flow, and vice-versa for the PNP current mirror. Using the same logic as stated previously, it can be similarly derived that the current that is seen at the up_send node will also be seen at the up_receive node. This is the key to our projects goal of changing the series configuration of the AD7280 evaluation boards to a parallel configuration as the current mirror scheme does not require sequential evaluation boards to operate at different voltages.

2.9. Chapter Summary

In this chapter we have presented the fundamental building blocks which are used in our project. Li-ion batteries are obviously the critical input of our project, although we simulate them for the

demonstration board. This simulation is critical, because a demonstration cannot be allowed to last for the duration of multiple charge/discharge cycles of a li-ion battery.

3. Project Planning

To determine the best approach for completing all of the project requirements with respect to both the product itself and the report, much thought was put into prioritizing and logistics. As with most group efforts, it was decided that several components of the final product should be developed simultaneously. The Gantt chart shown in Figure 20 illustrates the different components of the project and the relative timing of their execution.

The Gantt charts shows there were four main phases of the project in addition to the final report. The four phases were research, design, test and implementation, and integration. At times these phases did overlap, which was necessary to further understanding of the concepts. These phases were further broken down into two divisions, hardware and software. The hardware included designing, testing, and implementing the current mirror circuit, designing the PCB for the demonstration board, and designing and testing the driver board. Each of these needed to be individually tested, verified, and scrutinized as the components were inserted into the system. The software included learning, developing, and implementing software in LabVIEW. This also included designing the GUI. This component was continuously developed throughout the project to accommodate further advances in hardware.

The Gantt chart above shows many components of the project were executed in parallel. Each component had a person assigned to the task. In some cases, however, more then one person was assigned a task due to the specialties that were involved in completing the task. Both the hardware and software portions could be developed simultaneously as one did not always rely on the other. At certain points during the project, integration of hardware and software had to be done to continue progress. An example of this is testing the integration of the current mirrors into the system to troubleshoot the concept. This was required to complete the demonstration board design.

Using these planning strategies, the group was able to complete tasks in the most efficient manner. Additionally, assigning responsibility to each task allowed for effective communication of goals and accountability. The parallel structure of completing tasks lead to productive use of time, and a successful team effort.

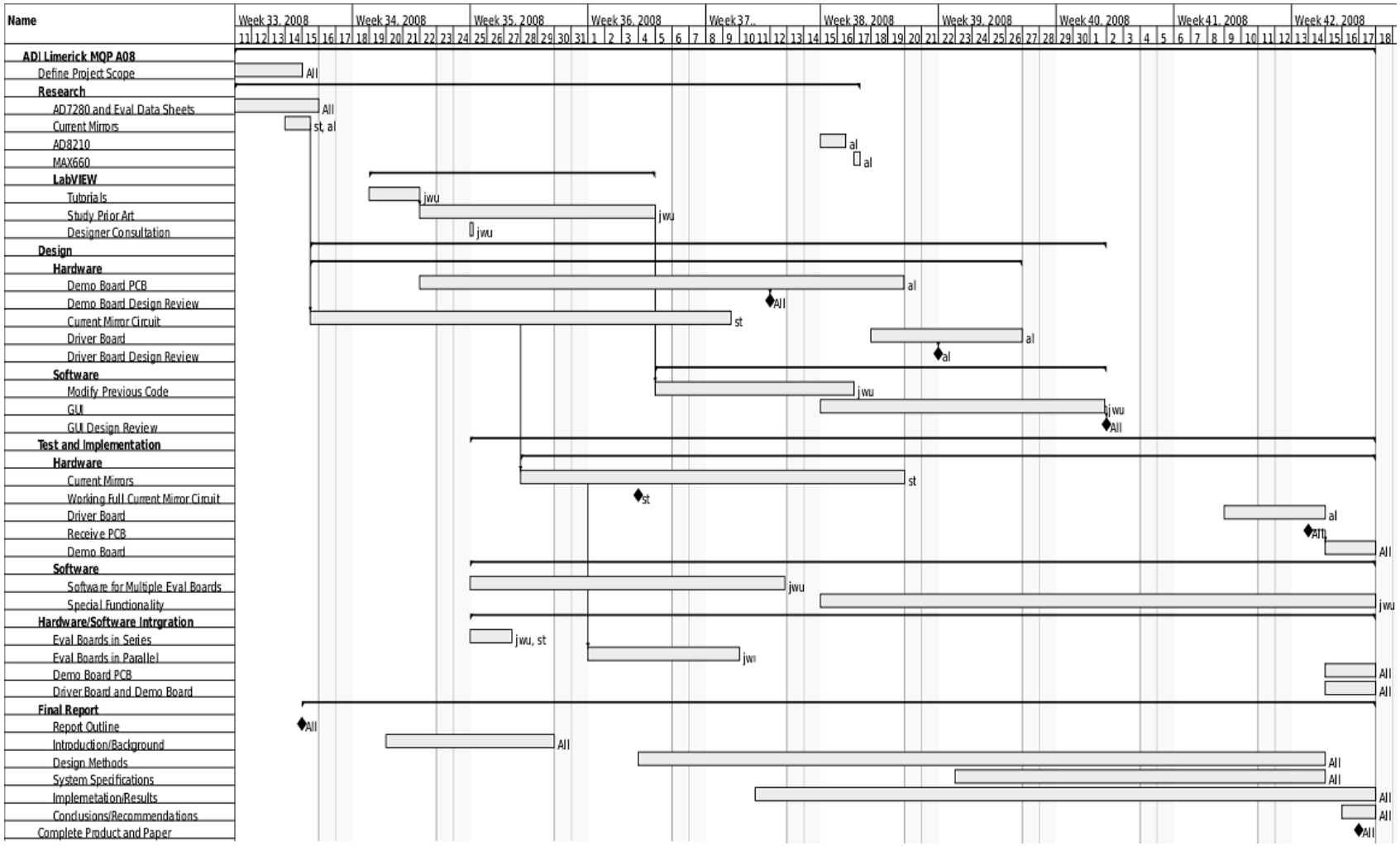


Figure 20 – Gant chart showing the progress of our project over time

4. System Specifications

This section is devoted to detailing a broad overview of our project in terms of both hardware and software. We first present a top-level description of what is happening, and then break each major system into smaller, more detailed, components.

4.1. Overview

With the end goal of having this project provide a *demonstration board* (DEMO board) for use by both the marketing department of ADI at a trade show, and the engineering departments of potential customers, we first need to define what is going to be of use to each of these groups. For instance, when taking the DEMO board to trade shows, there is a need for low voltages to promote safety in an uncontrolled environment. However, when testing the AD7280, engineering groups need the full voltage range that is required in the real application. As a result, the boards need to be able reconfigurable to achieve either goal. The engineering teams also have a higher number of required AD7280s than the marketing teams would, so smaller boards need to be built with the option of connecting them together. The reason the marketing department needs the lower chip count is to be able to effectively get their point across with as little information as possible. This is made easier if there are fewer data points to examine. This does not help the engineering department, though, because they need to test the setup as it is intended to be used in the real world. One final distinction between the two departments is how the data should be presented. The marketing department requires an effective GUI, as explained previously, but the engineering team is going to need to store the data in numeric form. We therefore needed to develop both of these methods in the software. These results are summarized in Table 4.

Table 4 – Listing of requirements for ADI and potential customers.

ADI Marketing Dept	**Customer Engineering Dept**	**Conclusion**
Safety (low voltage)	Realistic product representation (full voltage range)	Reconfigurable board necessary
10 chips	20+ chips	Ability to link multiple copies of the board together
Effective/attractive GUI	Good data acquisition	Selectable graphical or spreadsheet output

To aid in giving the reader an understanding of how the boards we're developing are intended to be used, refer to Figure 21. Figure 21 shows that we have a computer controlling a *Converter Evaluation & Development* (CED) board, which communicates with the primary DEMO board. The DEMO board may or may not be connected with additional DEMO boards during the engineering process. This last DEMO board in the chain is driven by the driver board.

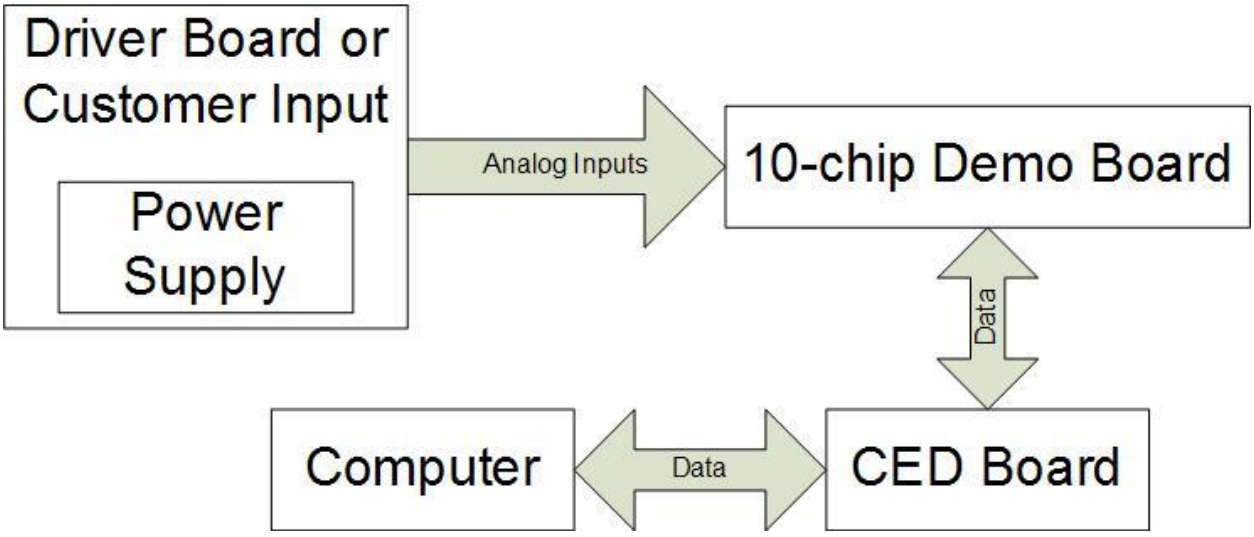


Figure 21 – System-level block diagram of the project.

4.2. System-Level Inputs

The AD7280 is intended to measure both battery voltages and temperatures. The voltages are taken differentially across each battery the chip is monitoring. The temperatures are typically monitored using a voltage divider circuit where one of the resistors is a thermistor located very close to the battery, as explained in Section 2.2. For our purposes, we have simulated batteries coming from the driver board. To simulate the battery temperatures, we have thermistors mounted so that a cup of hot coffee can be placed on top of them, causing the ambient temperature to rise, thus lowering their resistance, and changing the voltage input to the AD7280.

Most of the inputs to the DEMO boards are battery voltages. When the ADI marketing department is demonstrating the AD7280s, these inputs are going to be simulated by the driver board. Customers will have to create their own boards to provide inputs to the DEMO board. The driver board's schematic can be seen in Section 9.3. It can be seen that the driver board connects to the DEMO board through the use of a 64-pin DIN-41612 connector. Note that many of the outputs from the driver board are electrically identical, and provide a constant DC voltage to the majority of the inputs on the DEMO board. In fact, on the DEMO board there are only two chips which receive a varying voltage. The voltage on these chips can be varied by turning potentiometers located on the case of the driver board. The rationale for this is that the customer wants to be able to see that identical inputs result in identical outputs (thus, we have eight chips with the same inputs), but they also want to see that the chips respond to changing voltages appropriately. When the customer's engineering department uses the DEMO board, they will be applying different voltages to each input.

There is one special output from the driver board. This input is used to send a small voltage to a current monitoring chip, the AD8210. The AD8210 is not a major part of our project, but we were requested to include it on our DEMO board so that we could demonstrate it's capabilities in addition to the AD7280. The AD8210 works by placing a shunt resistor in series with the load. Normally, the expected load is inductive, such as an electric motor. For our simulations, however, we've placed a variable

resistance in series with the shunt resistance. The voltage is sensed by the AD8210, which then reports a voltage output on a scale of 0-5V. Because we needed a way to communicate the voltage output to the computer for display, we have replaced one of the temperature measurement inputs of the AD7280 with the AD8210 output. Luckily for our project, the output from the AD8210 is on the same voltage range (0 to 5V) as the input to the AD7280 thermistor measurement.

4.3. System-Level Outputs

Our project has several subsystems. We consider each EVAL board equivalent (two AD7280s and a set of current mirrors), the driver board, the CED board, and the GUI to be a subsystem. Each of these subsystems communicates with the others, but the actual outputs from the system are fairly simple. For the purposes of our demonstration, the only outputs are LED indicators and the laptop monitor. The LEDs indicate alarm conditions, as well as cell balancing outputs from the AD7280. The laptop monitor provides more detailed information, such as exactly what voltage each input to the AD7280s is currently reading, the temperature at the thermistors, and a software alert flag.

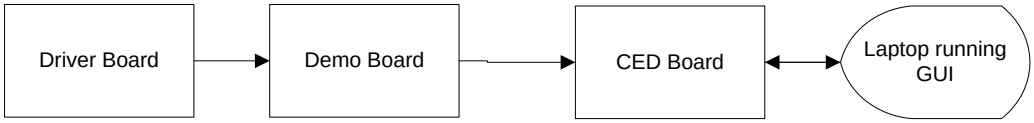


Figure 22- System Level Diagram

4.3.1. Driver Board Outputs

On the driver board there are three resistor networks, each of which outputs to the DEMO board. The first resistor network provides twelve constant voltages, linearly increasing from GND to +45V. The second resistor network also provides twelve voltages, but these are adjustable by making use of the potentiometers on the box of the driver board. The final resistor network has one output voltage which is sent to the current sensing chip on the DEMO board.

4.3.2. DEMO Board Outputs

The DEMO Board has five sets of two AD7280s operating in parallel. The devices communicate with each other by means of current mirror circuits placed between the higher-potential chip of one set and the lower-potential chip of the other set. As shown on Figure 23, this board provides outputs in the form of an Alert LED, Cell Balancing circuitry, and Serial Communication.

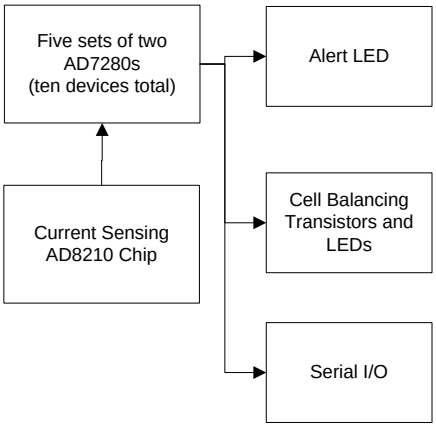


Figure 23 – DEMO Board Block Diagram

4.3.3. CED Board Outputs

As shown on Figure 24, the CED Board has a Cyclone FPGA on it that acts as a translator between the AD7280s and the USB port on the laptop.

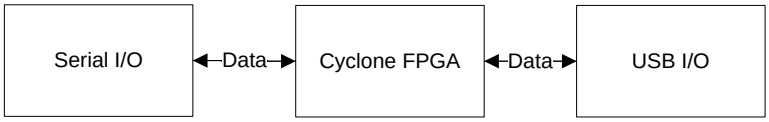


Figure 24 – CED Board Block Diagram

4.3.4. Laptop Running GUI

The laptop communicates with the CED using its integrated USB I/O port. Based on the data that comes from the CED board, the laptop will display voltage and temperature readings from the AD7280s, the alert LED, and the current reading from the current sense chip. The laptop also has the ability to write to and read from the AD7280 control registers.

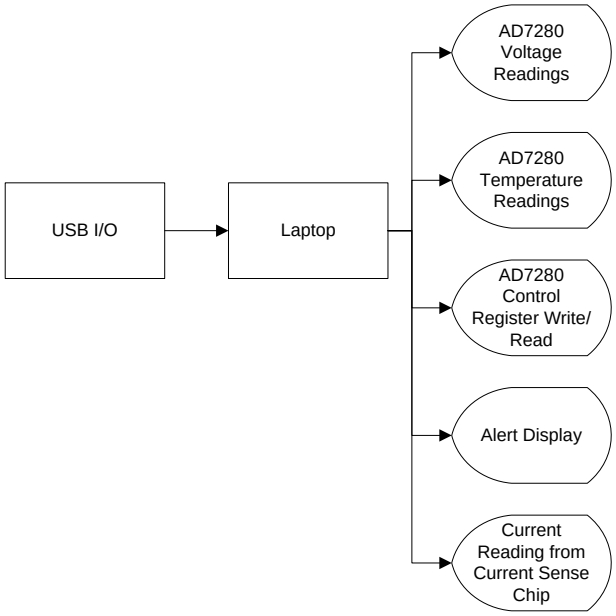


Figure 25 – System Block Diagram of GUI and Computer

5. Design Methods

This chapter describes the thought process and preliminary steps that were taken to design the final product. It is broken down into three sub-sections: product requirements, parts selection, and software development. Each of these sub-sections details the thought and reasoning that went into making each decision. They also describe the methods that were used to determine that something was to be included in the final design.

5.1. Product Requirements

When designing the overall system and thinking of what it needed to do, a number of requirements were determined to be important and needed to be especially considered in the design. Our ultimate goal is to effectively demonstrate the capabilities of the AD7280 to potential ADI customers. This means it needs to not only be fully functional, but also appealing to the eye, easy to understand, and easy to use. These factors were broken down into two main categories: appeal and ease of use. A great deal of focus was put on these factors when designing the product.

To make the product the most appealing as possible, several things had to be taken into consideration. The first of these is the GUI that is used to display the product's functionality. The GUI should be visually appealing so it catches the eye of a customer viewing the demonstration. This involves an attractive and professional design with a color scheme and information that is easily read and interpreted. In addition to this, the product must operate on a safe voltage potential to ensure the customer would be safe using the product. The ability to be safely used adds to the appeal of the system. Finally, the system needs to be visually pleasing. In order to satisfy this requirement the driver board needs to be enclosed in a box that highlights the demonstration board and can be easily connected to. The demonstration board should also be visually pleasing and the system should be designed to visually display its capability in the most appealing way possible.

To add to its charm, the system should be easy to use and its operation and outputs should be easy to read and interpret. To accomplish this, the GUI should have an intuitive display that highlights important aspects of the demonstration. The information that is being displayed should be easily read and interpreted. Since the board is likely to be used by customers with only a basic knowledge of the system, it should be easy to teach someone how to use the product. This is accomplished by designing intuitive and user friendly software. The software should be well documented and easy to understand. Since the demonstration board does not use the AD7280s in the way they will be used in their full application, the board should be easily reconfigurable to switch between series and parallel configurations as needed.

These characteristics that enhance the appeal and ease of use of the system needed to be considered when designing the system. They had to be included to accomplish the goal of effectively demonstrating the AD7280. By defining these product requirements a concrete direction could be determined and the system could be further developed.

5.2. DEMO Board

The DEMO board grew as an extension of the EVAL board. The EVAL board was designed for customers to gain an understanding of the functionality of the AD7280. The DEMO board is intended to show that larger numbers of AD7280 chips can be used, as well as reduce the amount of off-board interconnects that are required between sets of AD7280 chips. For instance, with one DEMO board, the same functionality can be shown as with using five EVAL boards. With those five EVAL boards, however, four sets of headers need to be installed, whereas one DEMO board could exhibit this functionality without any off-board connections. The DEMO board does have the ability, however, to use headers to connect multiple copies together, but the number of times this is required is greatly reduced. See Section 9.1 for the full schematic of the DEMO board.

Due to the fact that the DEMO board was extending the EVAL board, most of the design was copied directly from the EVAL board. For instance, on the DEMO board, the digital logic communications to the CED board, the digital logic power supplies, all digital/analog isolation, the first two AD7280 chips, and the passive components associated with the first two AD7280s are exact duplicates of the EVAL board. Each subsequent set of two AD7280s (and their associated passive components) is also a copy of the first set. The biggest difference in schematic design is the ability to configure the sets of AD7280s to be either in series or in parallel.

The reconfigurable nature of the AD7280s is a result of having two options during the assembly of the board. One PCB is made for both options, but only certain components are inserted for either option. The most prominent example of this is the current mirror section of the circuit. The components on those pages of the schematic all have notes associated with them stating that they should only be inserted if a series of parallel configuration is desired.

When a parallel configuration is desired, a set of seven NPN and seven PNP current mirrors are inserted such that they act as voltage level shifters. The AD7280 is only designed to operate with each subsequent chip receiving voltages at ever-increasing potentials. The chips communicate by sending varying amounts of current instead of setting high or low voltages. Normally, that would be very clever, but when the chips are in parallel, it means that they do not work properly because the voltages in subsequent chips are lower, not higher. By using the current mirrors, we are able to allow the AD7280s to source and sink current normally, regardless of whether they are at a higher or lower potential than the next chip.

If, on the other hand, a series configuration is necessary, the current mirror setup is easily bypassed by simply not inserting the current mirrors, and instead placing 0Ω resistors between the relevant communication pins. This configuration is electrically the same as if five EVAL boards were placed in series with one another.

5.3. Driver Board

The driver board was designed so as to easily integrate with, and supply the correct voltage inputs to, the DEMO board. To do this, we first established a voltage range on which it would operate. As we discuss in Section 5.4.2, we chose to power the driver board using a 48V DC power supply. This

power supply was used to provide appropriate voltages to the 64 outputs that were needed to drive the DEMO board. The schematic showing the driver board is shown in Section 9.3.

To begin the design of the driver board, we first decided that we would provide the inputs to the DEMO board from three resistor networks, one constant, and two variable. The constant network has the +45V rail as the input (the other end is grounded), and the outputs are sent to eight of the ten AD7280 chips on the DEMO board. The reason for sending the same voltages to so many chips is that we wanted to show that the output from the AD7280 is consistent when the same input is applied.

The second output is sent to the current monitoring circuit using the AD8210. This circuit has fewer components than the other two, consisting of only two fixed resistors and a potentiometer in series with each other. The first fixed resistor shall be referred to as the *protection resistor*, and the second will be called the *sensing resistor*. The sensing resistor is a relatively small shunt resistor tied to ground on one side. The other end of the sensing resistor is where the output from the circuit is taken. The protection resistor is a relatively large resistance, and is in place to make sure that the total resistance stays high. We wanted to guarantee that the +3.3V regulator that was supplying the input would be able to supply enough current, and did not want to load it down. When the pot is set to a high resistance, relatively little voltage is dropped across the sensing resistor, and the output is low. Similarly, when the pot is set to low resistance, the sensing resistor would have a large voltage drop across the terminals, and a high signal is sent to the AD8210.

The outputs from the final variable resistor network are sent to the remaining two AD7280 chips. These outputs are used to show that the AD7280s can dynamically react to input voltage changes. This circuit is significantly more complicated than the other two. The input, first of all, to the resistor network is not a voltage from one of the rails, but rather a pseudo-constant current. We made a constant current source by using another current mirror, as shown in Figure 26. The off-page connector labeled “I_INPUT” is the current input node attached to the variable resistor string.

The next step in the design was to overcome the challenge of providing sufficient current to the V_{DD} pins of the AD7280s without causing the voltage to sag in the resistor networks. We achieved this goal by buffering the voltage outputs of the V_{DD} outputs using opamps. The opamp buffers work to keep the output stable under any load. Each resistor network had two opamps on it, one supplied with +48V and +24V, the other supplied with +24V and GND, for the positive and negative supplies respectively. The higher-potential opamp supplied the current to the higher-potential chip in each set of AD7280s, and the lower-potential opamp similarly supplied the power for the lower-potential chip. The non-inverting inputs to the opamps were guaranteed to never exceed their power supplies, and by connecting the inverting inputs directly to the outputs, we were able to guarantee that the correct output would be applied to the AD7280 inputs.

In order to provide the +24V rail needed for the opamps, we inserted an adjustable output voltage regulator with a high voltage input capability. To adjust the output, we were able to use the formula $V_{OUT}=V_{REF}(1+R2/R1)$, where V_{REF} is the voltage difference between the output and ADJ pins on the device, R1 is the resistance between those same pins, and R2 is the resistance to GND from ADJ [38].

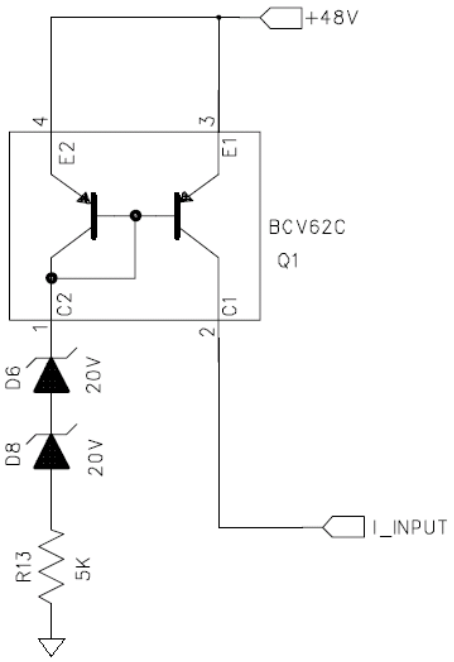


Figure 26 – Current mirror input to the adjustable resistor network. The supply to the system is +48V, which is much higher than the current mirror can accept. We bring the effective voltage down by using two 20V zener diodes in series, and then dropping the remainder of the voltage across a resistor. This ensures that the current going through I_INPUT is constant. Second order effects add non-idealities that were small enough for our project that we ignored them.

Finally, the communications between sets of AD7280s in parallel need some biasing voltages both greater than the highest input and lower then the lowest input. As a result, we supply the resistor networks with +45V and GND, and bias the communications sections of the DEMO board with +48V and -3.3V. Achieving the +48V and GND rails was a simple matter of connecting the DEMO board straight to the power supply connector. We realized the +45V rail by using a 3.3V regulator which had it's GND pin connected to zener diodes which biased up the voltage by approximately 42V. The -3.3V rail was made by first using a +3.3V regulator, which had it's output tied to the input of a charge-pump voltage inverter. All of these regulators together enabled us to have access to +48, +45, +24, +3.3, 0, and -3.3V anywhere we needed them in the system.

5.4. Parts Selection

In any system such as the one we developed, many different components are required to interoperate effectively. Here, we discuss some of the highest profile, and most important individual components that made up the subsystems of our DEMO and driver boards. In fact, the majority of the components that were used on the DEMO board were directly copied from the EVAL board upon which we were expanding. The exception to this is listed in Section 5.4.1. On the other hand, the driver board was being designed from scratch, so all components needed to be selected individually.

5.4.1. Current Mirrors

The current mirrors that were selected were found at *Farnell Electronic Component* (FEC, or alternately, Farnell) Distributor's Irish web page. They are the BCV61 and BCV62 current mirrors made by Infineon Technologies[3]. See Figure 27 for a schematic of the *integrated circuit* (IC).

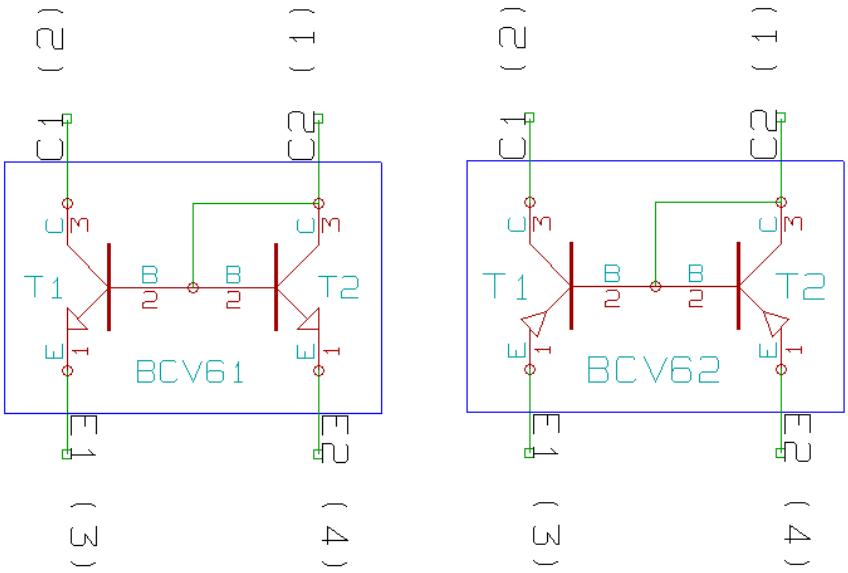


Figure 27 – Current mirror schematics for the BCV61 and BCV62, manufactured by Infineon.

The BCV61 is an NPN current mirror and the BCV62 is a PNP current mirror, they were made to be complements of each other by the manufacturer. These particular current mirrors we chosen first because the transistors inside are a one-to-one match, within the 30% tolerance specified . This means the current in should be exactly the current out. In addition to the perfect matching, these current mirrors operate in the voltage, current and temperature ranges that will be used for this project. Those ranges are up to 30 volts across transistor T1, a collector current of 100 milliamps, and an operating temperature of up to 150 degrees celcius. The voltage rating of 30 volts, however, proved to be a miscalculation on our part as the distribution of voltage in our application was not as we expected. Details of this are in Section 6.1. Though these current mirrors technically meet our demands and specifications, they did raise some logistical concerns. They are surface mount IC's which have a footprint of about 2.9mm by 1.3 mm. This led to issues with testing as the pins were too small to fit into a solder-less bread board. To compensate, the current mirrors needed to be soldered onto prototyping board and wires soldered to the board. The soldering of such a small component led to some burnt out IC's but when successful, the current mirrors were tested and they worked to within a tolerable amount of error.

5.4.2. Driver Board Components

The driver board we developed needed to be able to supply a large number of voltage outputs. In order to have that capability, we used a commercially available voltage supply, four kinds of voltage regulators, high current opamps, and two resistor networks. The specifics are outlined below. See Section 9.3 for the driver board schematic.

[3] See Section 9.4 for the datasheets of all parts listed in Section 5.4.

5.4.2.1. XP Power AED36US48 Power Supply

The power supply we selected for our driver board was the AED36US48, manufactured by XP Power. This is a 48V, 36W DC power supply that can be provided with either 50 Hz 240V, or 60 Hz 120V AC power. The reason we selected this particular supply are because of the high voltage output and relatively low cost of the product. The AD7280s require voltage inputs between 7.5 and 30V [3]. Our DEMO board has two AD7280s in series, so the driver board needed to output at least 15V, and at most 60V. Given that we did not want the output voltages to be too dangerous, we selected the 48V output.

Additionally, we knew that in the worst case scenario, the ten total chips we were using on the DEMO board would require 10mA each at the same time. Other parts of the circuit, of course, would also be drawing power at that time as well, such as the resistor network we set up to provide voltage inputs from the driver board. When we took all such factors into account, plus a safety factor of 25%, we realized that the AED36US48's specified output of 750mA would easily fit our needs without any worries about reaching current limits or blowing fuses.

5.4.2.2. AD817 High Current Opamp

Most of the voltage inputs to the AD7280s from the driver board were voltages across a series of resistors on the driver board. The AD7280 chip has high impedance inputs, so this was not a problem. The issue was that the driver board also needed to supply V_{DD} for the chips, which can take as much as 10mA during an A/D conversion [3]. If we were to use the same scheme of taking the voltage from the resistor chain, it would get loaded down by the low impedance, we would lose regulation, and the product would not work as we wanted. As a result, we buffered the inputs to the V_{DD} pins of the AD7280 using the AD817. The AD817 is a high speed, low power, side supply range amplifier capable of outputting 50mA [39]. The high current output was critical for this project because we had ten chips, and in a worst-case scenario, they could draw a total of 100mA. Realistically, this will never happen because they are designed to not all convert at the same time, but we decided to be very careful with our requirements. Note that we used four AD817 chips on our driver board, as shown in Section 9.3. Two of the chips were on a string of resistors that provided constant voltage outputs to eight chips. The other two AD817 chips supplied power from a string of adjustable resistors to two AD7280 chips This resulted in a design that never needs more than 80% of the maximum output current capability from the AD817.

5.4.2.3. TL783 Adjustable Voltage Regulator

In order to supply the AD817 opamps with the necessary +24V rail shown in Section 9.3, we used the TL783. The TL783 Adjustable Voltage Regulator is a high voltage input, variable voltage output regulator supplied by Texas Instruments. It is capable of accepting up to 125V between the input and ADJ pins, and the output can be adjusted depending on the resistances between the output and ADJ pins, and between the ADJ pin and circuit GND [38]. This was very convenient for our project, as it meant we could fine tune the output to exactly what we wanted using a trim pot. As was discussed in Section 5.3, the output voltage followed the equation $V_{OUT}=V_{IN}(1+R2/R1)$. We kept R1 constant at 82Ω and varied R2.

5.4.2.4. ADP3338 3.3V Voltage Regulator

The inputs to the AD7280 were never going to reach +48V because we needed some voltage to bias the current mirror circuit on. We needed approximately 3V on both the high and low ends of the

voltage scale to do this. ADI supplies a 3.3V regulator with sufficient current capability for our needs, the ADP3338. We were working with ADI, and so were able to get these components for free. Due to the fact that we needed both +3V and +45V, we needed two of these chips. The first problem we had, though, is that the ADP3338 cannot accept +48V as an input. To get around this issue, for the +45V regulator we placed zener diodes between the GND pin and actual circuit GND. This allowed us to input the 48V directly from the AED36US48 and achieve +45V output. In reality, the output voltage was +44V due to the zeners we had selected, which was close enough for our purposes. In the case of the +3.3V regulator, we put the zeners in series with the inputs to reduce the effective voltage input. Note that, because we wanted GND on the driver board to be the same as GND on the DEMO board, we did not use the +3.3V to GND as our biasing voltage, but instead used GND to -3.3V.

5.4.2.5. MAX660 Voltage Converter

In order to achieve the -3.3V mentioned in Section 5.4.2.4, we used the MAX660, a Monolithic CMOS Voltage Converter. The MAX660 is capable of taking any positive voltage between +1.5 to +5.5V and invert it to the respective negative voltage -1.5 to -5.5V [40]. On our driver board, we supplied the MAX660 with the +3.3V output from one of the ADP3338 chips mentioned in Section 5.4.2.4 to enable an output of -3.3V. This -3.3V was then sent to the DEMO board to be used for biasing the current mirrors on, as described previously.

5.5. Software Development

We need to create a software that can show that many AD7280s can be placed in a Daisy Chain and communicate with each other. This software also needs to be able to show the thermistor and voltage inputs for all the devices that are connected. Also, this software needs to show off the ability for the user to access the control registers of the AD7280s such as alert, power down, under voltage, over voltage, under temperature, over temperature and cell balance. Therefore, we came up with the following solution.

The software was written to communicate with the AD7280 evaluation boards through the CED board and to show off the capabilities of the AD7280. The primary purpose of this software is to display the capability of the AD7280s. For details of how this software is created, refer to Section 6.3 Software Implementation of this report. The software can perform the following functions.

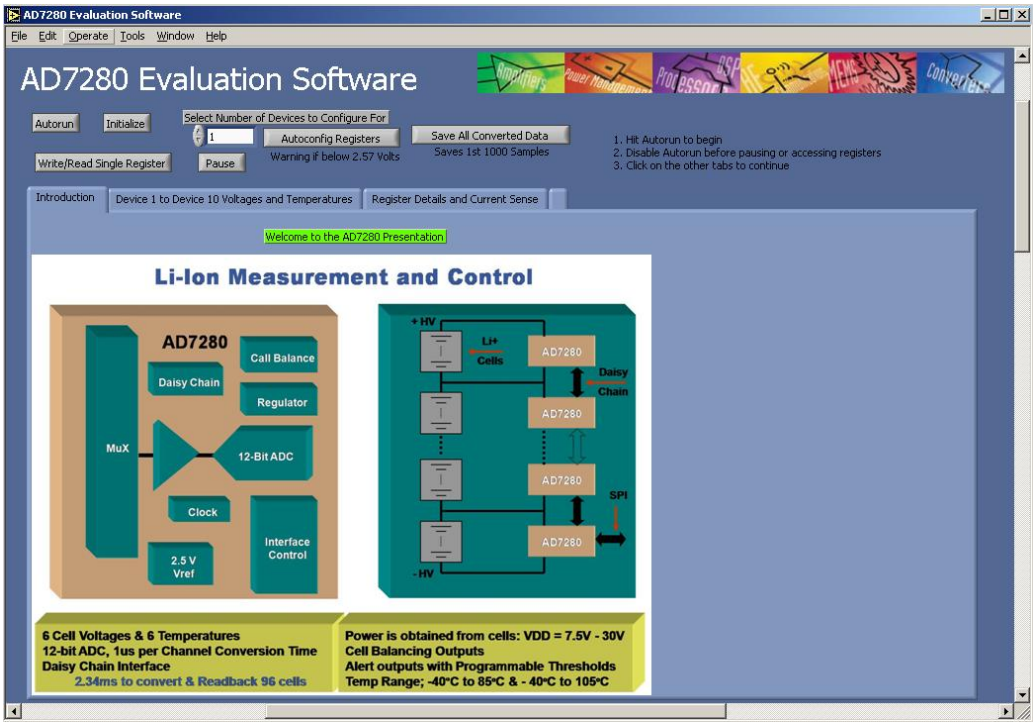


Figure 28 – GUI Main Screen

Figure 28 shows the screen as you open the program. To Start using the program, click the button Initialize and then click the button Autorun. The Initialize button downloads the software to the AD7280 through the CED board. The Autorun button starts the reading of convertion data from the AD7280s. While the program is in Autorun mode, hit Stop Board Actions shown on Figure 28 before configuring registers, writing/reading to registers or saving data.

5.5.1. Board Selection

On the left side, there are 11 Buttons, Activate Board 1 to Activate Board 11. Clicking any of these buttons will show the apropriate board data. For example on figure 3, when the Activate Board 2 button is clicked, a screen pops up showing the data for the devices on board 2. Each board has 2 devices, hence each tab on the Show Board screens will have 2 graphs.

5.5.2. Voltage Readings

Shown on board 2 on Figure 29 is the voltage readings for all the inputs for board 2 in form of a plot and their coresponding numerical indicators. There are 2 devices on each board and each device has 6 voltage inputs, therefore there are 12 numerical indicators shown in volts on this screen.

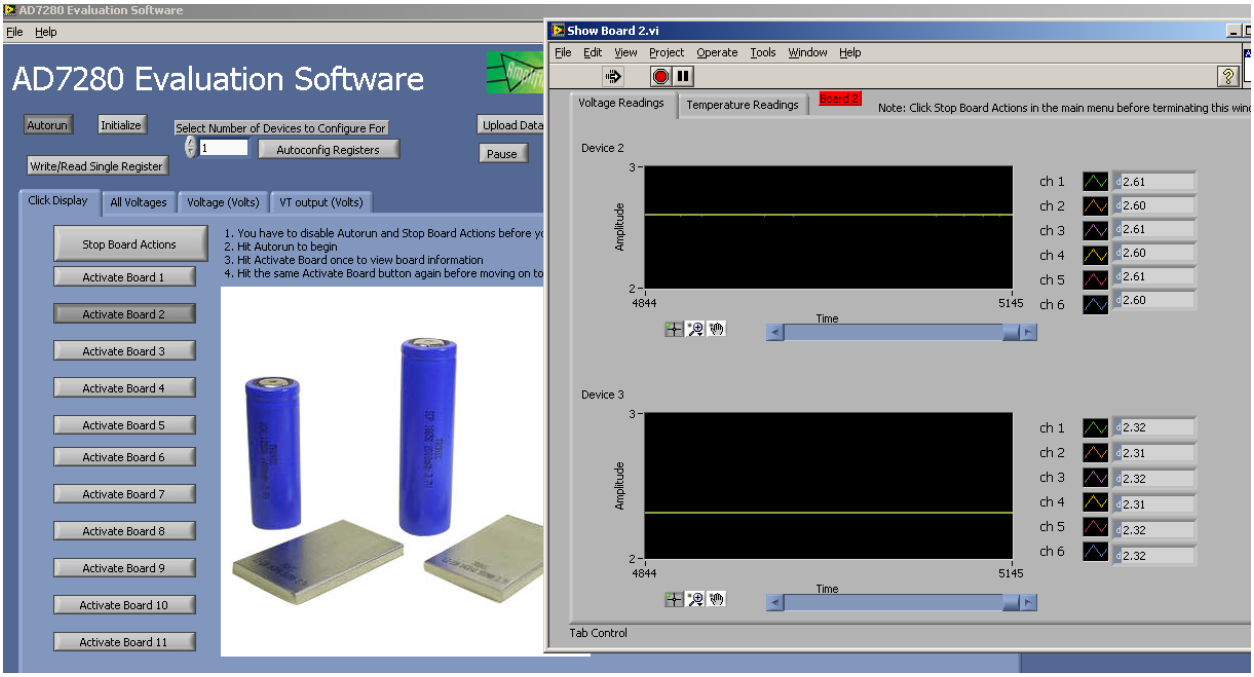


Figure 29 – Cell Voltage Value Screen

5.5.3. Temperature Readings

Each board screen has 2 tabs, Voltage Readings and Temperature Readings. Figure 30 shows what happens to the Show Board 2 screen when the Temperature Readings tab is clicked.

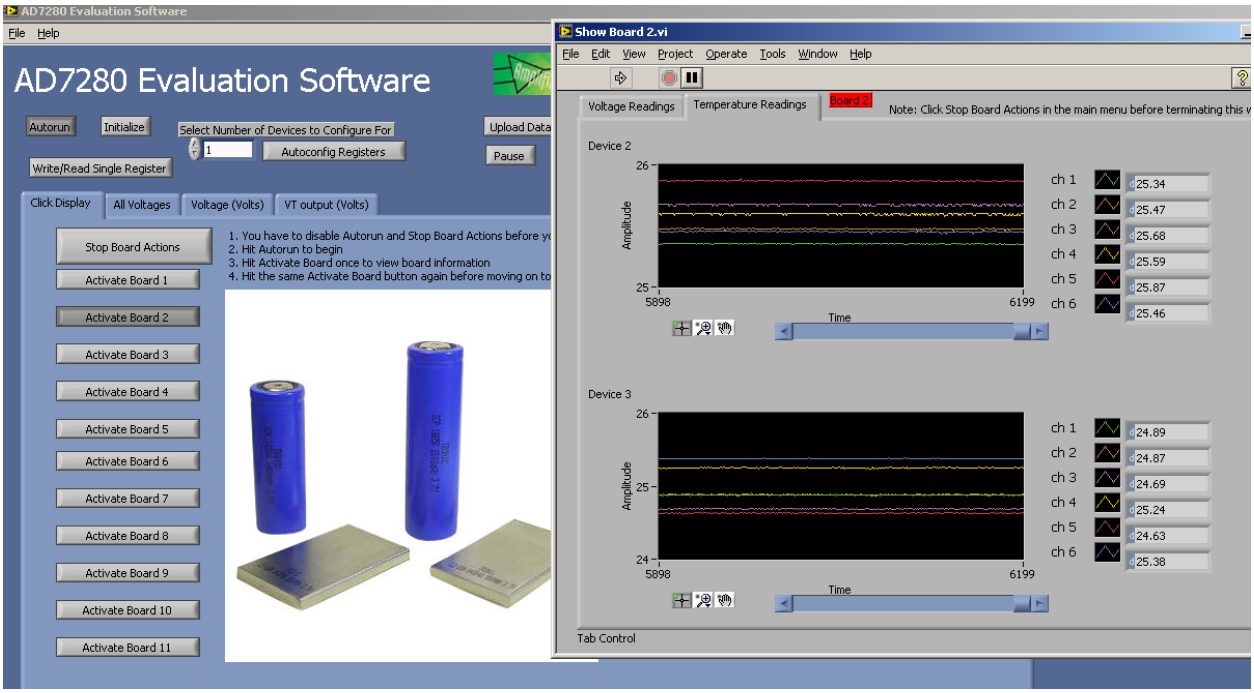


Figure 30 – Temperature Screen

After that tab is clicked the screen shows the thermistor readings in Celsius for the thermistor that are attached to board 2.

5.5.4. Reading from and Writing to all the AD7280 Registers

Before using this function, Stop All Board Actions should be clicked for safety measures. To use this function, click on the button on the upper left hand corner called Write/Read Single Register and a screen shown on Figure 31 should popup.

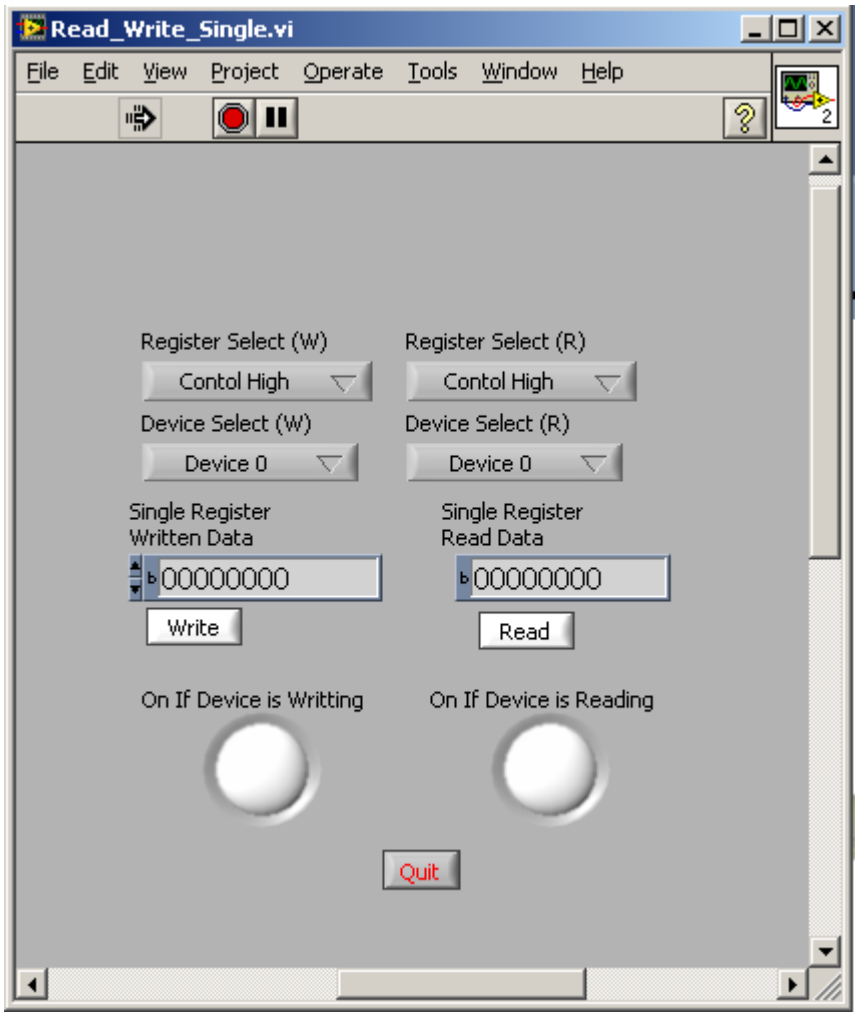


Figure 31 – Register Read/Write Screen

This function allows the user to read from and write to any device for up to 11 boards. That is Device 0 to Device 22. The buttons labeled Device 0 on Figure 31 are drop down menus. Figure 32 shows what happens when the user clicks on them. The buttons on the right side are for reading and the buttons on the left side are for writing.

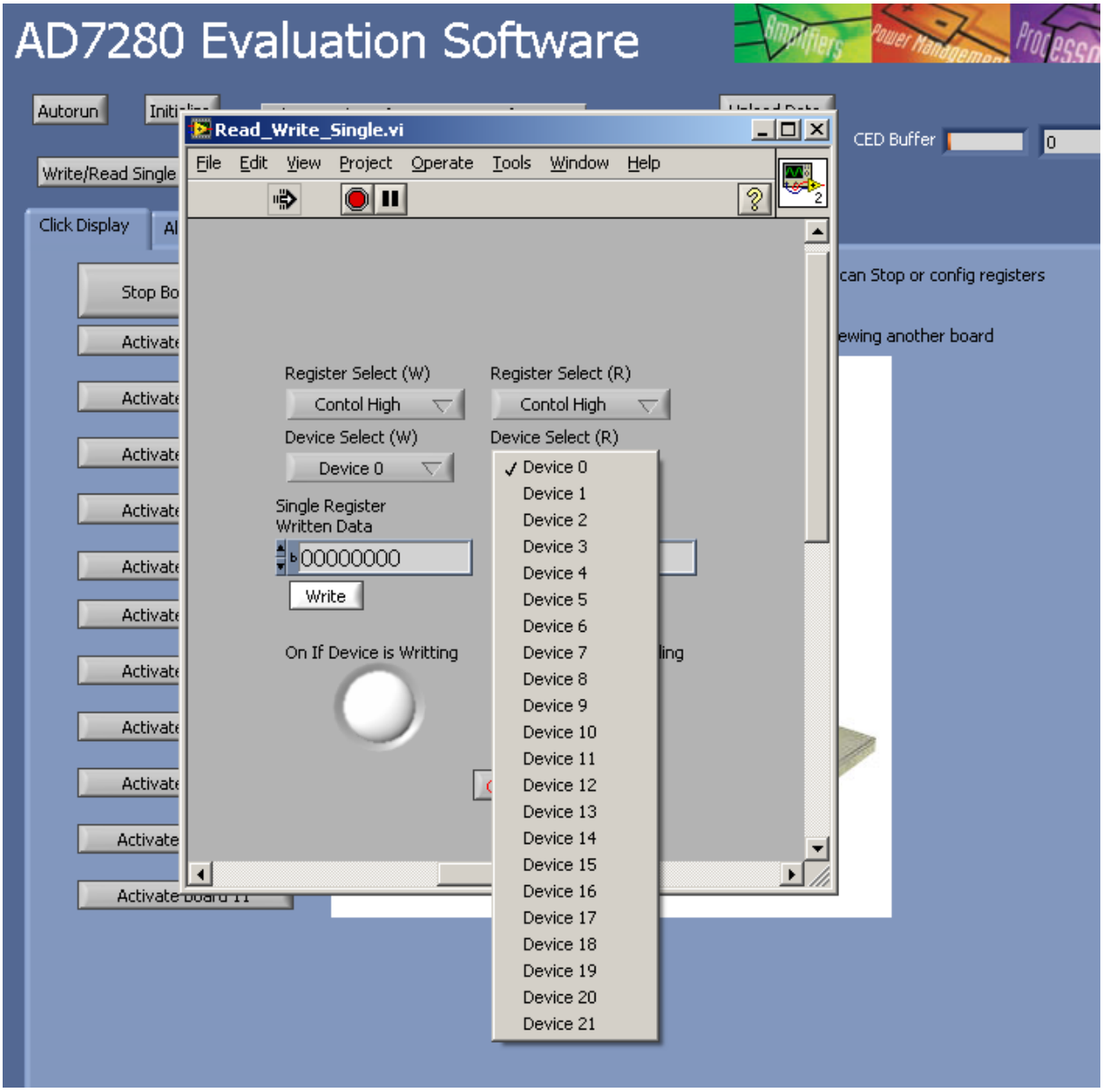


Figure 32 – How to select a device

After clicking on the drop down menu, the user can select which device to write to or read from.

The button Control High is also another dropdown menu. Figure 33 shows what happens when that button is pressed.

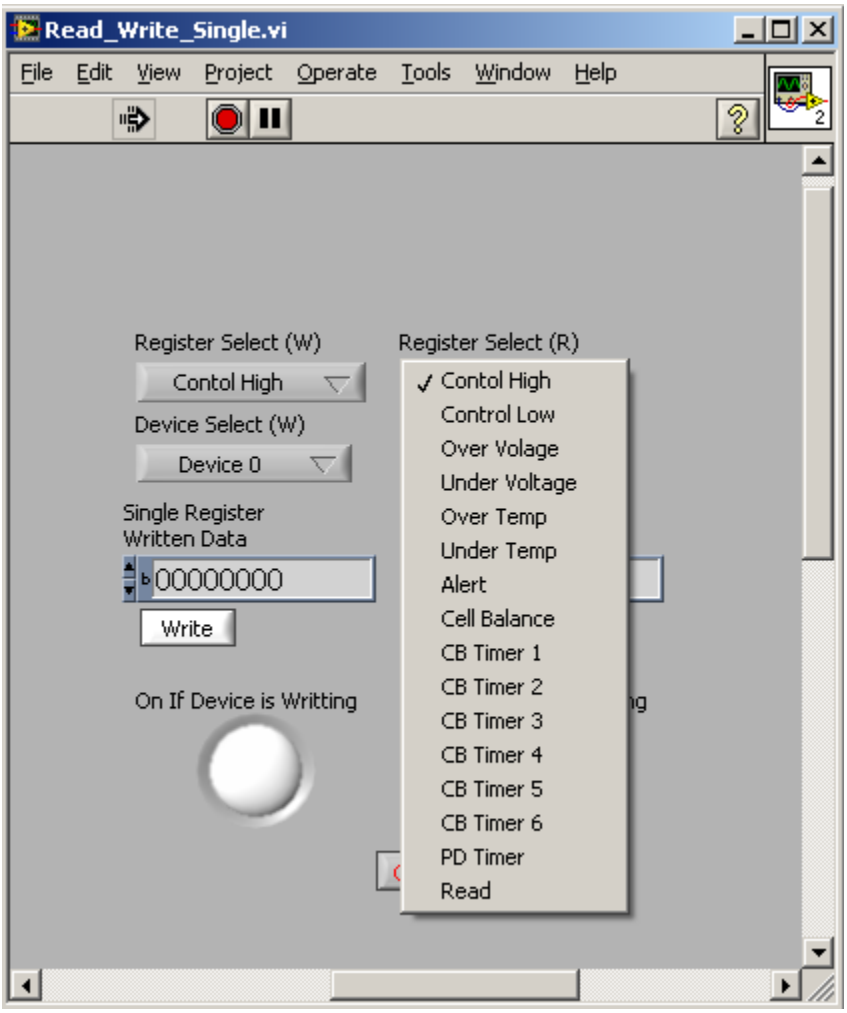


Figure 33 – How to select a register

The button indicated in Figure 33 selects a specific register that the user wants to write to or read from.

Lastly, after a specific device is selected and a specific register is selected, clicking the Read button shown on Figure 31 will read the value of that register on that device. The user can also use the Device Select (W) and Register Select (W) buttons shown on Figure 33 and click on the Write button on figure X5 to write to that specific Register on that device.

5.5.5. Automatically Configuring the Alert Function

The AD7280 has a user-configurable alert function. The user can configure the voltage inputs and thermistor inputs in which an alert flag is set by using the Write/Read Single Register function.

Figure 34 shows a button called Autoconfig Registers and a numeric indicator circled in red. This button allows the user to automatically setup the alert condition with a single click. The user needs to enter the number to devices that are being used on that numeric indicator before clicking on Autoconfig Registers.

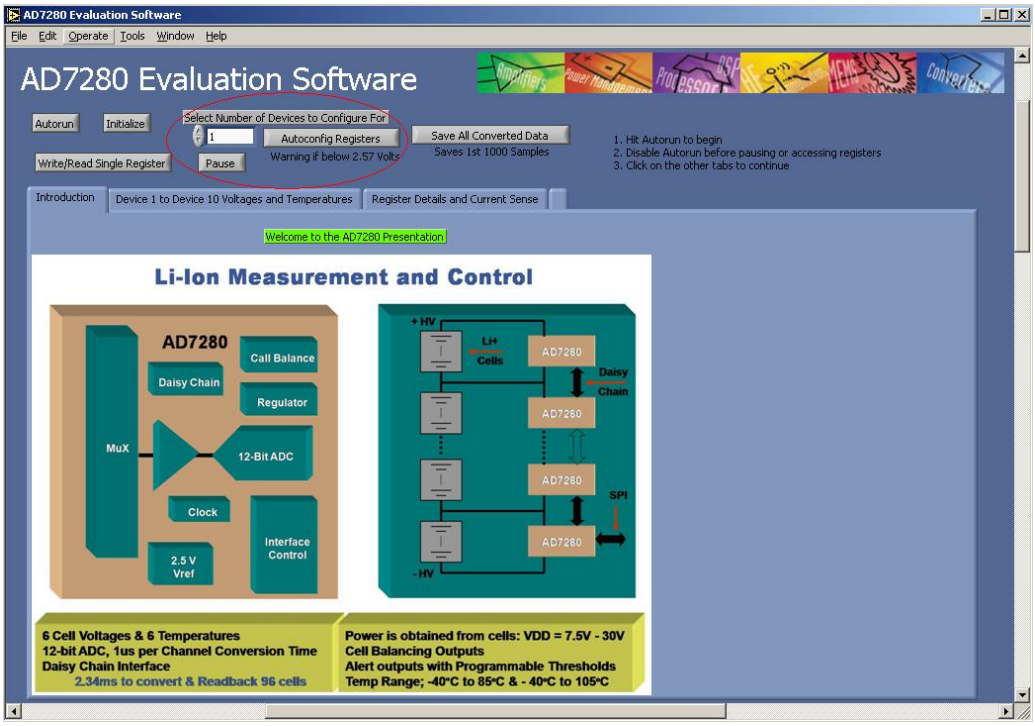


Figure 34 – Button to click on to configure alert condition

Currently, this function is set in such a way that if any input cell voltage is less than 2.5 volts and greater than 5 volts, then the alert flag gets set. This also triggers the LED, D10 on the evaluation board indicating that the alert flag is set. Temperature conditions in which the alert flag is set is not part of this function so the thermistor alert triggering is set to default which is alert when temperature is outside of this range -50 degree C to 150 degree C.

Once Autoconfig Registers is pressed, a screen will show up confirming that the button has been pressed. Press the Write button on that screen for this function to take effect.

5.5.6. Save All Converted Data

Before pressing the button, remember to toggle Autorun and Stop Board Actions off. Pressing the Save All Converted Data indicated in Figure 35 button will prompt you to save to a directory that you select. It is recommended to open the saved file as an excel spreadsheet.

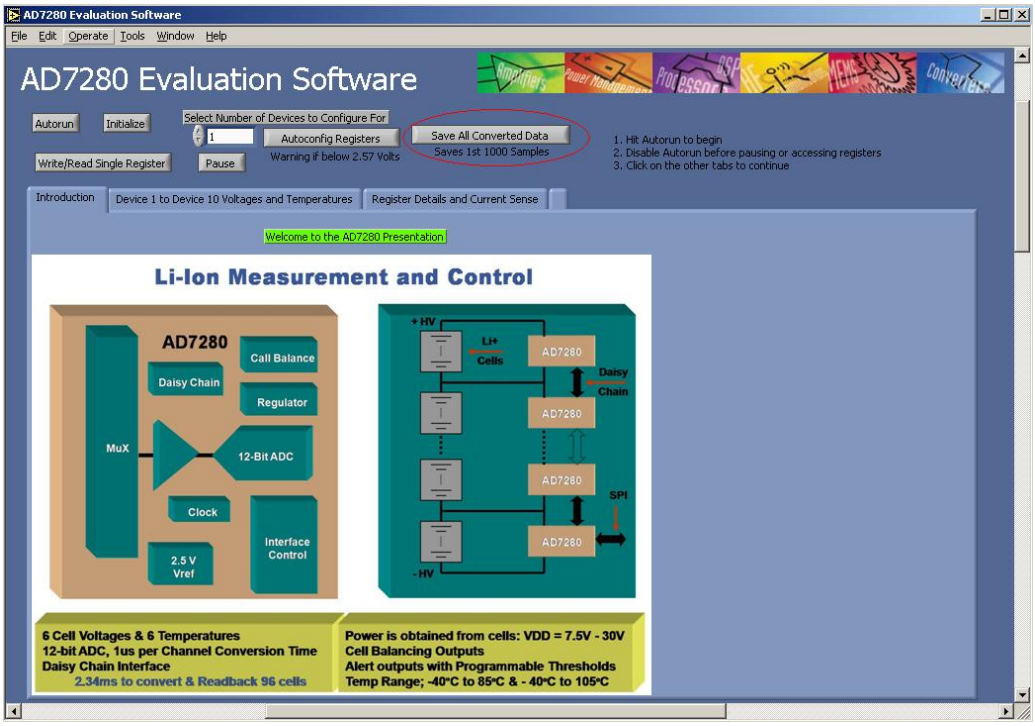


Figure 35 – Button to click on to save data

The saved file has the format shown in Table 5.

Table 5 – How to read the saved data

Device 1												Device 2
Cell 1 Volt	Cell 2 Volt	Cell 3 Volt	Cell 4 Volt	Cell 5 Volt	Cell 6 Volt	Cell 1 Temp	Cell 2 Temp	Cell 3 Temp	Cell 4 Temp	Cell 5 Temp	Cell 6 Temp	…
Data Point 1	Data Point 1	Data Point 1	Data Point 1	Data Point 1	Data Point 1	Data Point 1	Data Point 1	Data Point 1	Data Point 1	Data Point 1	Data Point 1	…
Data Point 2	Data Point 2	Data Point 2	Data Point 2	Data Point 2	Data Point 2	Data Point 2	Data Point 2	Data Point 2	Data Point 2	Data Point 2	Data Point 2	…
Data Point 3	Data Point 3	Data Point 3	Data Point 3	Data Point 3	Data Point 3	Data Point 3	Data Point 3	Data Point 3	Data Point 3	Data Point 3	Data Point 3	…
…	…	…	…	…	…	…	…	…	…	…	…	…

5.5.7. Show 10 Chips

Figure 36 shows a display of 10 devices with their voltage inputs and their temperature readings as well as a battery bar indicator.

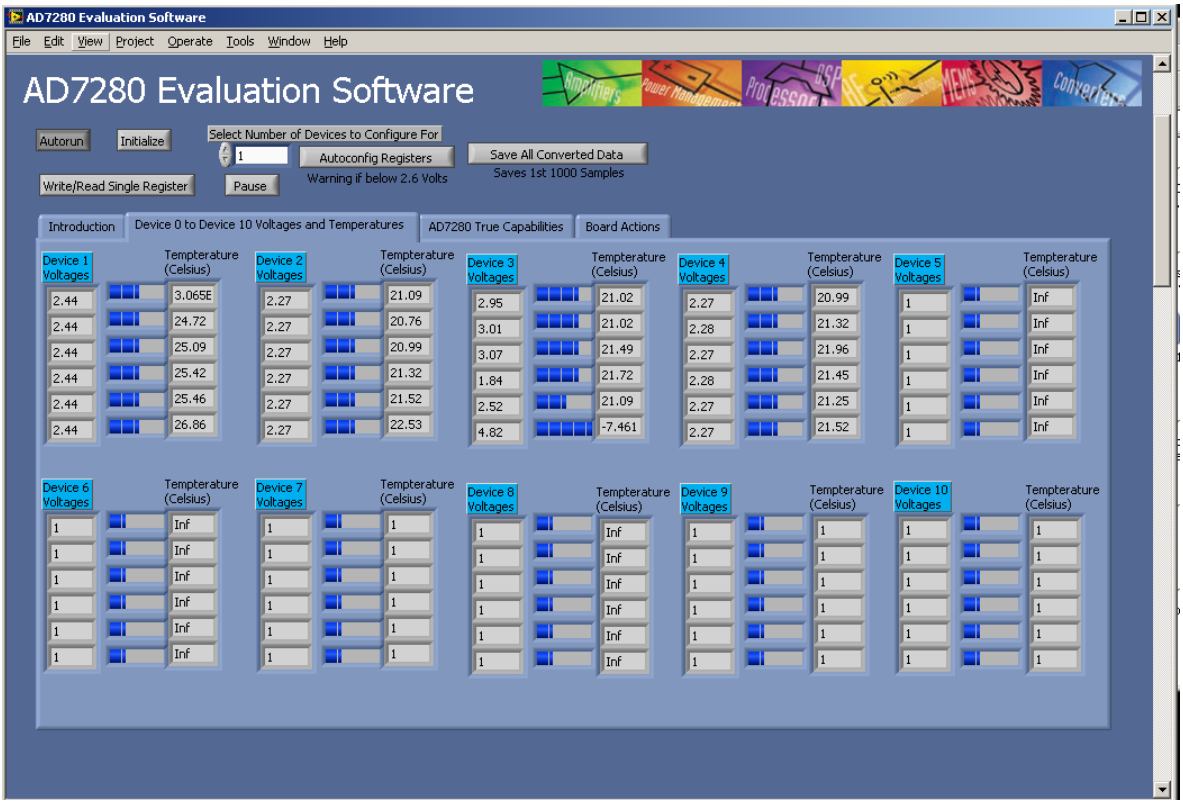


Figure 36 – showing 60 cell voltage and temperature readings

5.5.8. Selectable Detailed Display of all Devices

Figure 37 shows a screen that displays all the function of an AD7280 displaying all its control registers, alert indicator, temperatures, and voltages. It even has a selector to select between difference devices in the daisy chain and a current sense display that shows the current readings coming out of the current sense chip. A special button to note is the Invert Temp Reg button. Since the thermistor readings decrease in voltage drop as temperature goes up, the alert conditions are inverted. Pressing this button will correct this condition by inverted all input values the user sets to the registers.

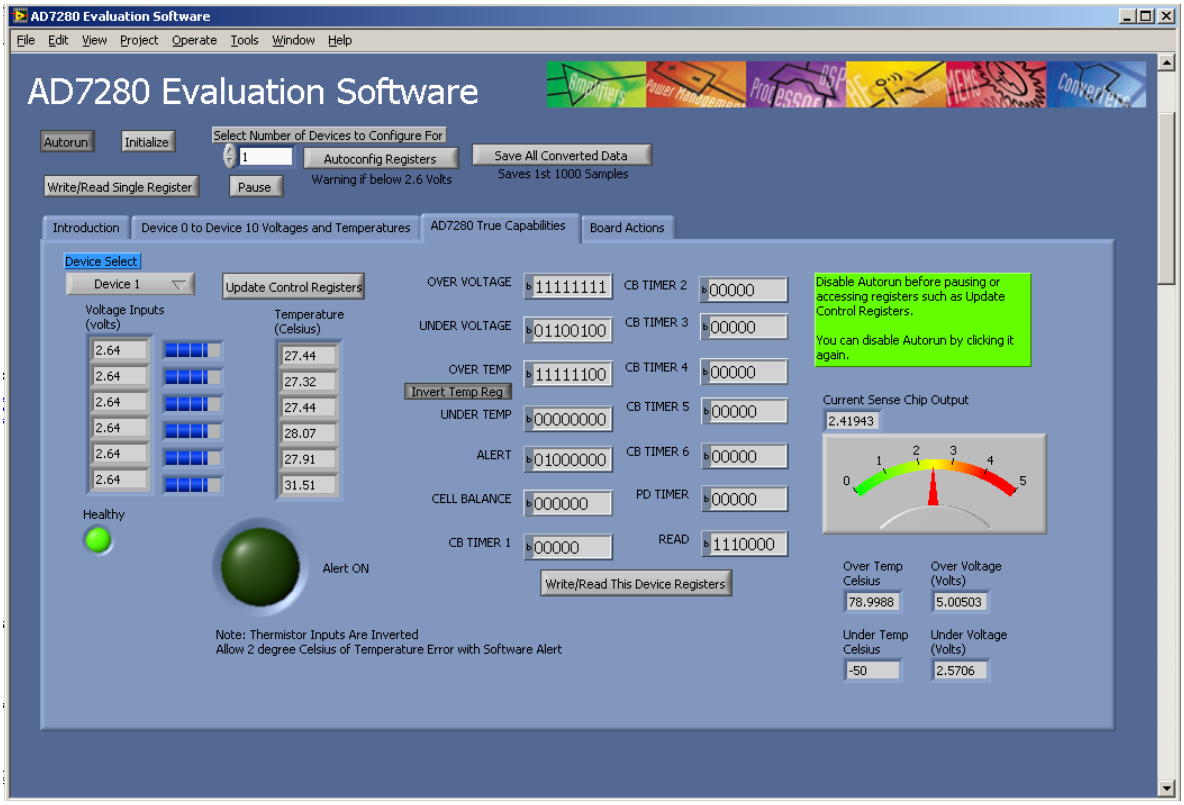


Figure 37 – All capabilities of the AD7280 are displayed on this screen.

6. Implementation/Results

This section covers the steps we took to make this project work. This will include how we wrote the software, details of current mirror behavior for different configurations, steps we did to get the AD7280s to work in series, how we designed the PCB, and how we tested each subsystem.

6.1. Testing

This section details how each block of hardware and software was prototyped. We also explain particulars about troubleshooting and the revision history of various blocks. In cases where we were stuck for extended periods, several different revisions were attempted until a successful solution was found.

6.1.1. Initial Series Testing

To test the daisy chaining capability of two boards, we connected the J15 connector of a slave EVAL board to J16 connector of a master EVAL board. We then used a configuration that we were told that allows the software to see all four devices (two devices per board). This configuration is turning off temperature readings this supposed to cause voltage readings from the slave board to show up in place of the temperature readings of the master board.

We were not getting any readings for the second board despite implanting this configuration. So we checked to see if there is a hardware issue by probing the test points to the communication signals between the two boards. The following are pictures we took of the waveforms of the signals that communicates between the two boards.

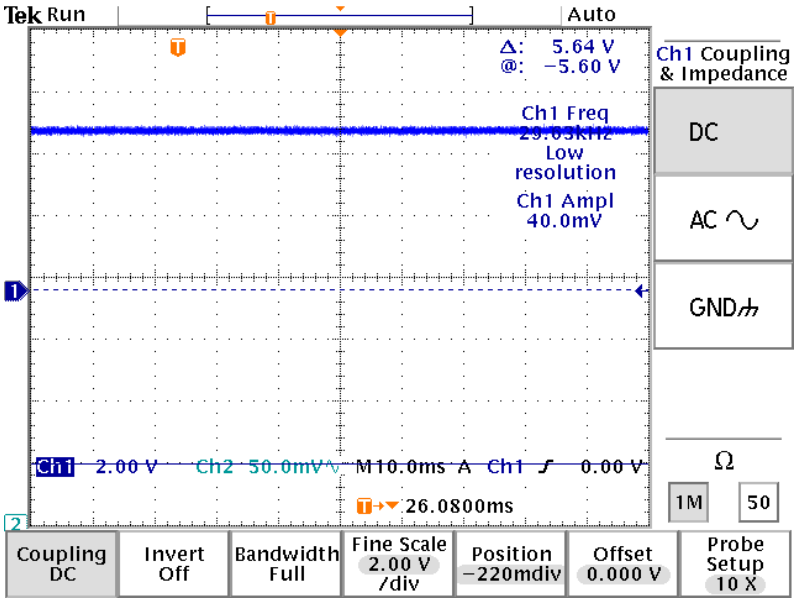


Figure 38 – This picture shows what happens when the Alert Test Point Is Probed. Alert can either be a high or low, and on this picture it is a high.

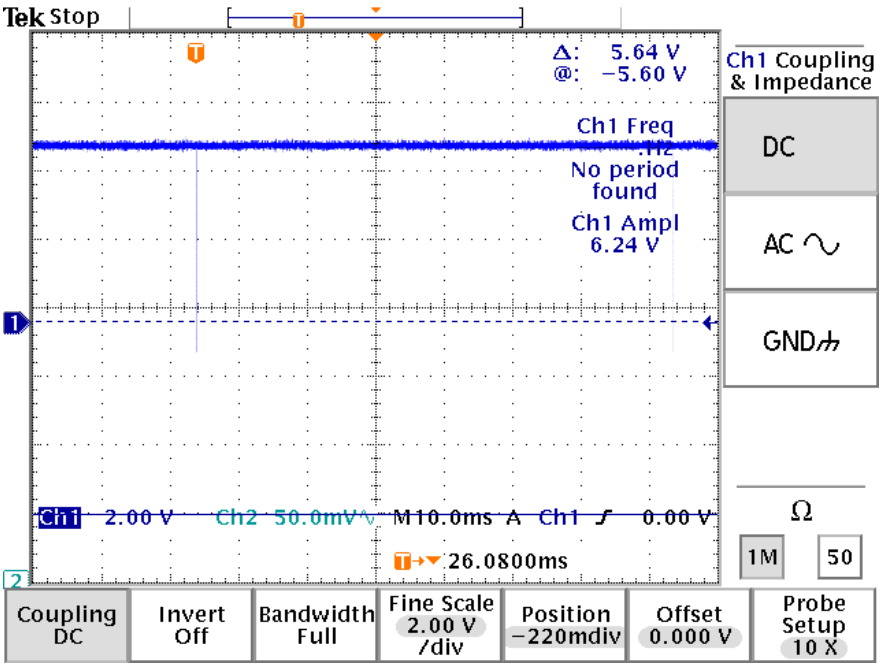


Figure 39 – This picture shows what happens when the CNVST Test Point Is Probed. CNVST is either a high or a low, and in this picture it is a high.

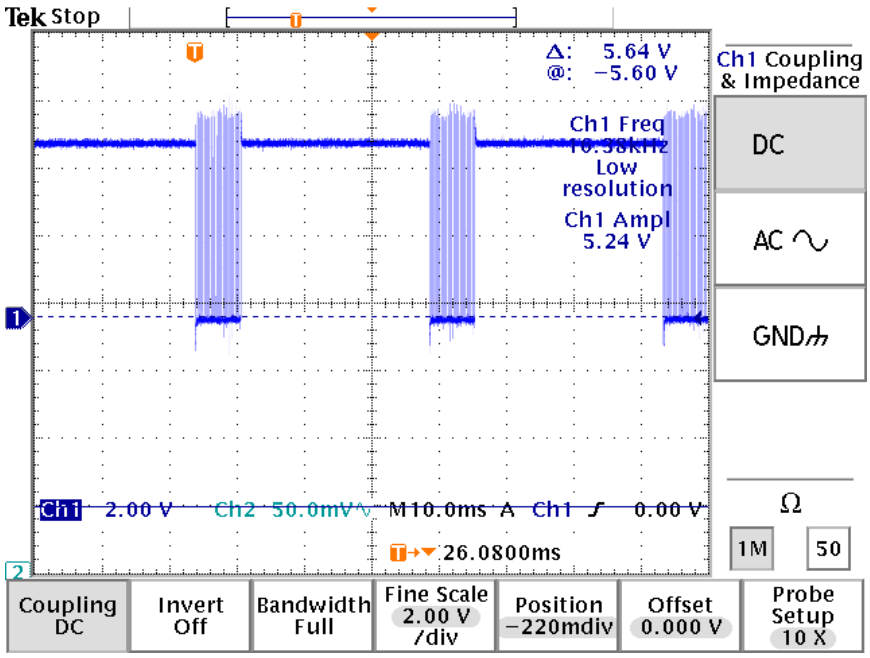


Figure 40 – This picture shows what happens when the CS test point is probed. Chip Select is active low and is pulled low periodically.

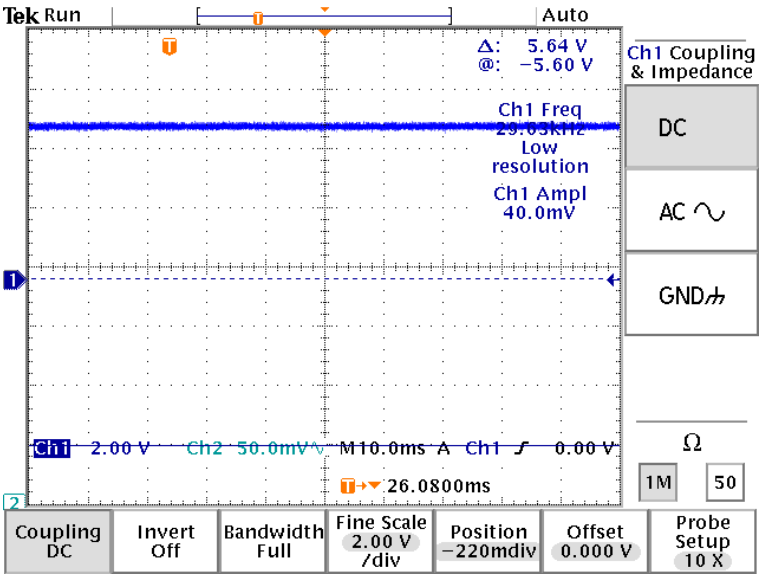


Figure 41 – This picture shows what happens when the PD Test Point Is Probed. PD is either a high or a low and is active high, and in this picture it is a high.

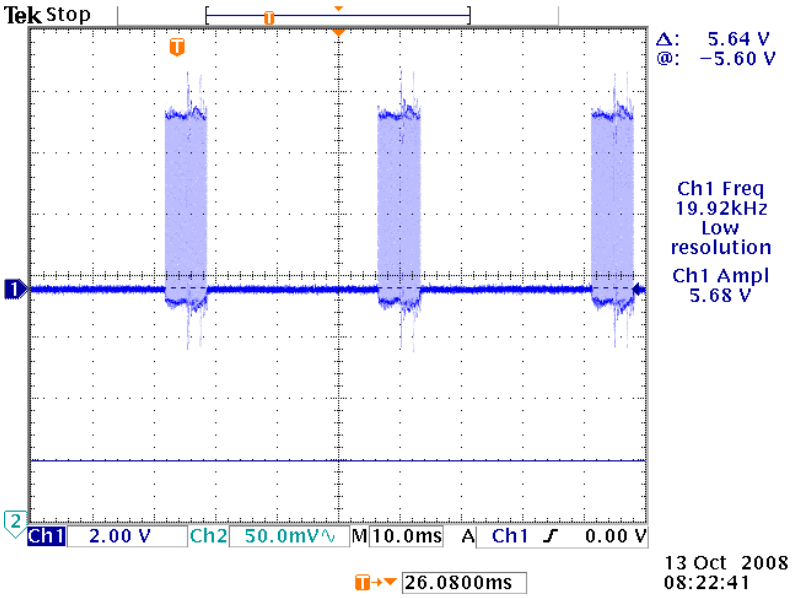


Figure 42 - This picture shows what happens when the SCLK Test Point Is Probed. During operation, the PFGA sends bursts of clocks periodically. We see that a 1 MHz clock is being busted every approximately. 30ms

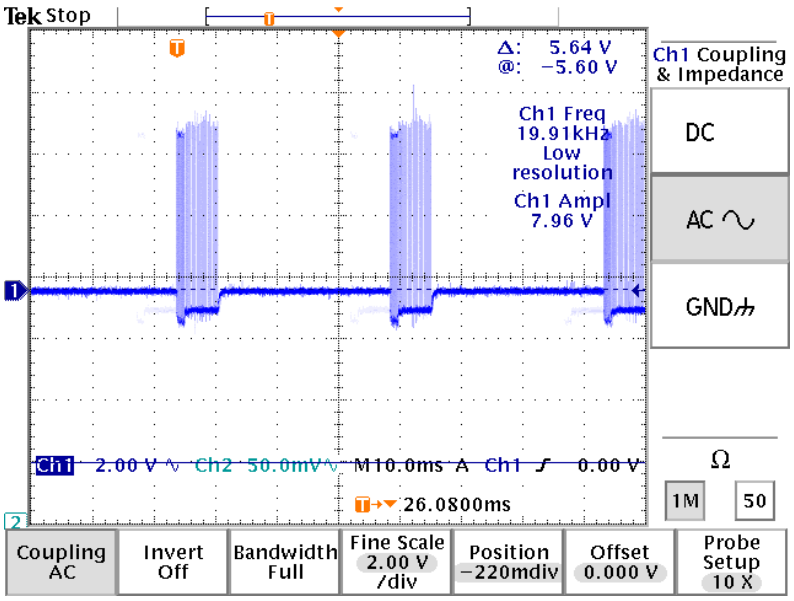


Figure 43 – This picture shows what happens when the SDIhi SDOlo Test Point Is Probed with 10ms time scale with 10ms time scale. Every few 20 to 30ms, a stream of bits is sent.

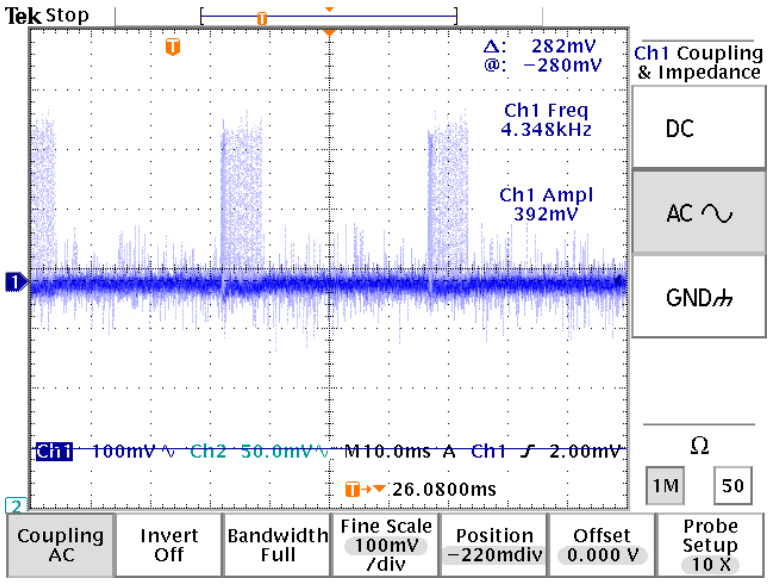
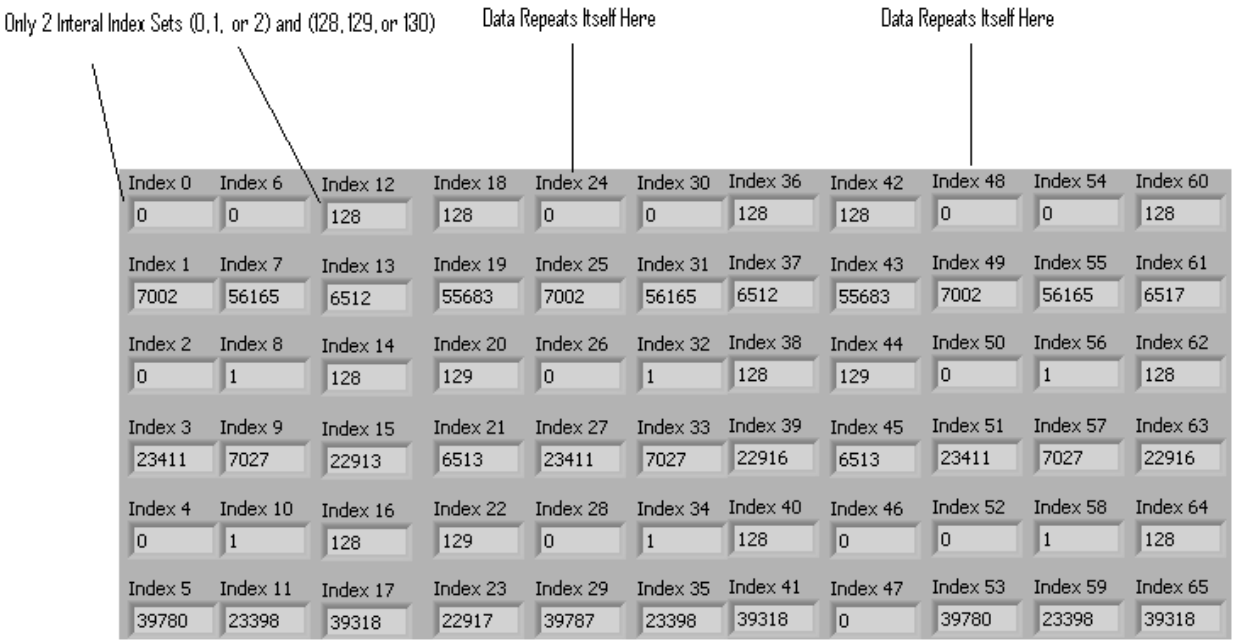


Figure 44 – This picture shows what happens when the SDIlo SDOhi Test Point Is Probed with 10ms time scale. Every few 20 to 30ms, a stream of bits is sent.

Looking at Figure 43 and Figure 44, we see that SDIhi SDOlo and SDIlo SDOhi are sending data signals between the two boards, so the two boards are talking to each other and therefore it was not a hardware issue. We next move to test the software.

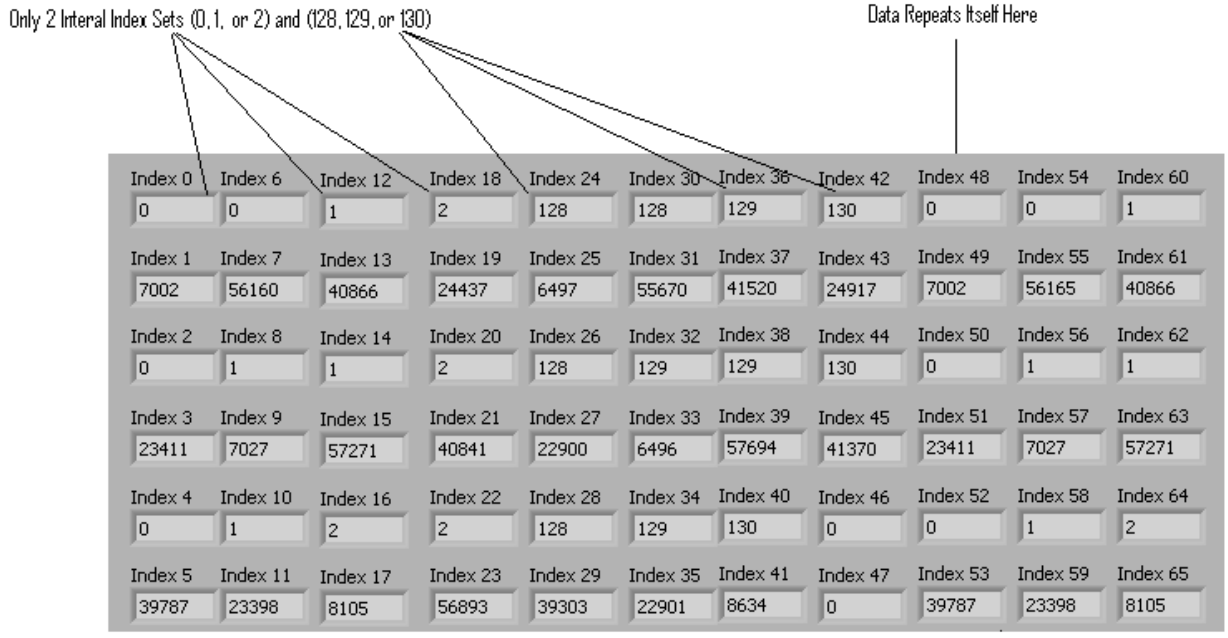
We figured that a good starting point in figuring out what is wrong would be to see what the data array from the VI Manual Receive from CED is reading. Figure 45 shows the values of this array.



Index 0	Index 6	Index 12	Index 18	Index 24	Index 30	Index 36	Index 42	Index 48	Index 54	Index 60
0	0	128	128	0	0	128	128	0	0	128
Index 1	Index 7	Index 13	Index 19	Index 25	Index 31	Index 37	Index 43	Index 49	Index 55	Index 61
7002	56165	6512	55683	7002	56165	6512	55683	7002	56165	6517
Index 2	Index 8	Index 14	Index 20	Index 26	Index 32	Index 38	Index 44	Index 50	Index 56	Index 62
0	1	128	129	0	1	128	129	0	1	128
Index 3	Index 9	Index 15	Index 21	Index 27	Index 33	Index 39	Index 45	Index 51	Index 57	Index 63
23411	7027	22913	6513	23411	7027	22916	6513	23411	7027	22916
Index 4	Index 10	Index 16	Index 22	Index 28	Index 34	Index 40	Index 46	Index 52	Index 58	Index 64
0	1	128	129	0	1	128	0	0	1	128
Index 5	Index 11	Index 17	Index 23	Index 29	Index 35	Index 41	Index 47	Index 53	Index 59	Index 65
39780	23398	39318	22917	39787	23398	39318	0	39780	23398	39318

Figure 45 – Data array from CED with Turning off Temperature Readings to Collapse the Data Stack

We noticed on Figure 45 that starting from the column of index 48; the data repeats itself as if it was from index 0. Also the first row of Figure 45 has a repetition of 0, 0, 128, 128, 0, 0, 128, 128, 0, 0… The value 128 has to do with device select, and since there are 4 devices attached and there are only two different device select values, we concluded that something in the software is not telling the CED to **upload** the data from the other two devices.



Index 0	Index 6	Index 12	Index 18	Index 24	Index 30	Index 36	Index 42	Index 48	Index 54	Index 60
0	0	1	2	128	128	129	130	0	0	1
Index 1	Index 7	Index 13	Index 19	Index 25	Index 31	Index 37	Index 43	Index 49	Index 55	Index 61
7002	56160	40866	24437	6497	55670	41520	24917	7002	56165	40866
Index 2	Index 8	Index 14	Index 20	Index 26	Index 32	Index 38	Index 44	Index 50	Index 56	Index 62
0	1	1	2	128	129	129	130	0	1	1
Index 3	Index 9	Index 15	Index 21	Index 27	Index 33	Index 39	Index 45	Index 51	Index 57	Index 63
23411	7027	57271	40841	22900	6496	57694	41370	23411	7027	57271
Index 4	Index 10	Index 16	Index 22	Index 28	Index 34	Index 40	Index 46	Index 52	Index 58	Index 64
0	1	2	2	128	129	130	0	0	1	2
Index 5	Index 11	Index 17	Index 23	Index 29	Index 35	Index 41	Index 47	Index 53	Index 59	Index 65
39787	23398	8105	56893	39303	22901	8634	0	39787	23398	8105

Figure 46 – Data array from CED before problem fixed without with Turning off Temperature Readings to Collapse the Data Stack

We then turn the temperature readings back on as Kate's trick had not worked. We noticed that the first row of Figure 46 showed 0, 0, 1, 2, 128, 128, 129, 130, 0, 0, 1… The values 1 and 2 are 0+1, and 0+2 which is an offset from device select which indicates temperature readings. The same can be said for the values 129, and 130 which is 128+1, and 128+2. We are however still seeing only two devices being read. This confirms that the software is not telling the CED to **upload** the data from the other two devices.

Next we noticed that each device holds twelve data values. For example the data values for device one is contained in indexes 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23 from Figure 11. The data values for device two are contained in indexes 25, 27, 29, 31, 33, 35, 37, 39, 41, 43, 45, 47 from Figure 46. That makes a total of 24. So we looked into the **upload** data code for any value of 24, and we saw the value conversion results per set are set to 24. We changed this value to 48.

We tried running the code again and there have been no changes. We looked further again and it turned out that there were 2 variables that we needed to change in order to change conversion results as there was another value that was 24 in the **start real time** function that tells the CED the number of frames it needs to grab. So we changed the number of frames to 48 and all four devices are seen by the software.

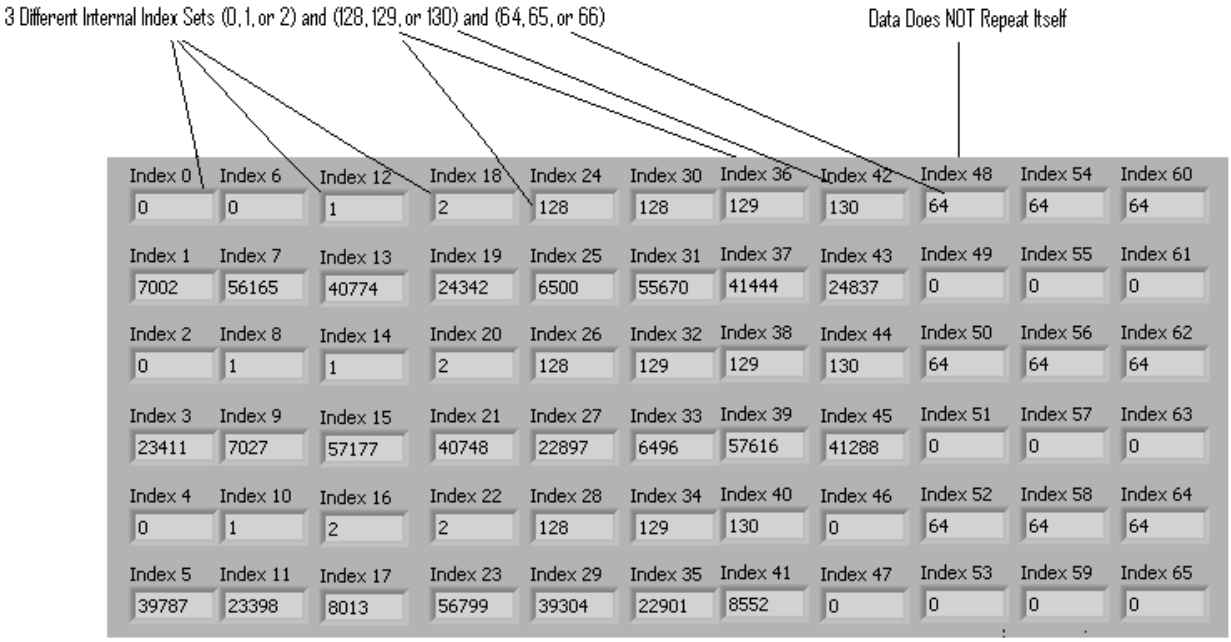


Figure 47 – Data array from CED after problem fixed

Figure 47 shows a 3rd device select value in the data array after increasing the number of frames that the CED grabs. Therefore, we now have the software to test the current mirrors.

6.1.2. Current mirror verification.

After the current mirrors were soldered to a prototyping board and they were capable of being placed into a bread board, they were tested to verify their operation. Figure 48 is the circuit that was used to perform this test.

The resistors R1 through R4 were not always the same for the duration of the project. However, in a single set of tests they did remain the same, R3 would always equal R4 and R1 would always equal R2. This was needed to prove that the current flowing through the current mirror to ground was the same on both ends with the highest efficiency. A test was performed by applying a Vdd to two of the pins of the current mirror, pins 1 and 2 of the NPN current mirror and pins 3 and 4 of the PNP current mirror. The voltage is applied at these pins due to the nature of NPN and PNP transistors. In both cases the other two go through a resistor to ground. The voltage needs to be higher at the collector then the emitter for NPN transistors and vice-versa for the PNP transistors. The voltage was measured across the two resistors with a digital multimeter. A current mirror was proclaimed acceptable if the voltage readings were within 10%, meaning the current flowing through the resistors were within 10% because Ohm's law says that V=IR and in this experiment R is constant. The 10% error was deemed acceptable because in the application of these current mirrors the values that will be used are 200 micro amps to represent a high signal and 20 micro amps to represent a low signal. If the current mirror is off by the maximum 10%, a high signal can still not be misinterpreted as a low because the cutoff between high and low is close to 100 micro amps. An example of a test done on a pair of current mirrors, one NPN and one PNP, and using the symbols from above, is the following: Vdd = 5V, R1 = R2 = R3 = R4 = 5kΩ. The voltage measured across R3 and R4 was 4.463V and 4.465V, respectively. This is a good current mirror and the error is less the a tenth of one percent. The voltage measured across R1 and R2 was 4.457 and 4.624, respectively. This current mirror is also good as it is only off by 3.61 percent. Each of the current mirrors used was tested in this manner to verify good operation before it was placed into a more advanced circuit.

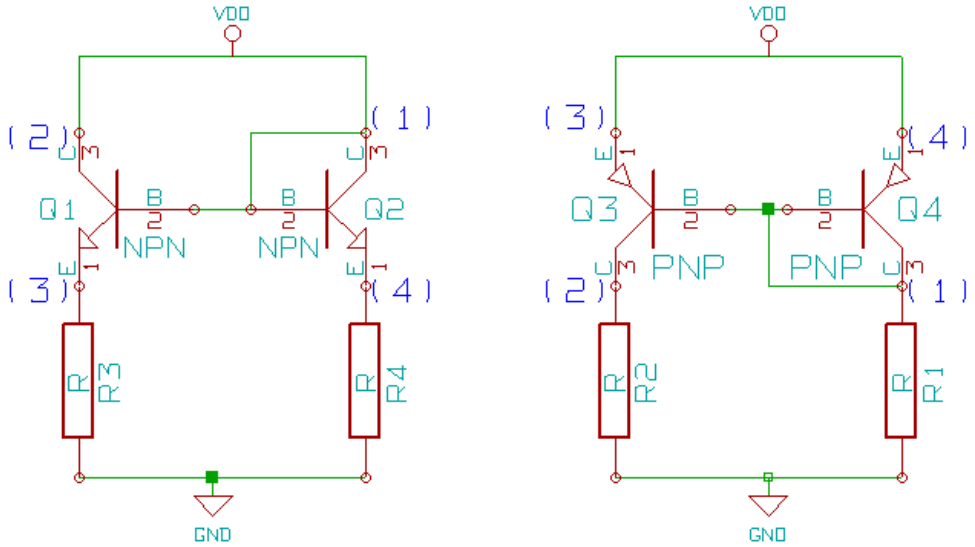


Figure 48 – NPN (left) and PNP (right) current mirror test circuits

After it was certain the current mirrors were working properly, a circuit had to be designed to use them as a level shifter that can draw and supply the same current from the 45-volt level to the 3-volt level. The 45V and 3V are relative to earth round and are used as Vdd and GND, respectively. The first circuit that was tested for this purpose is shown in Figure 49:

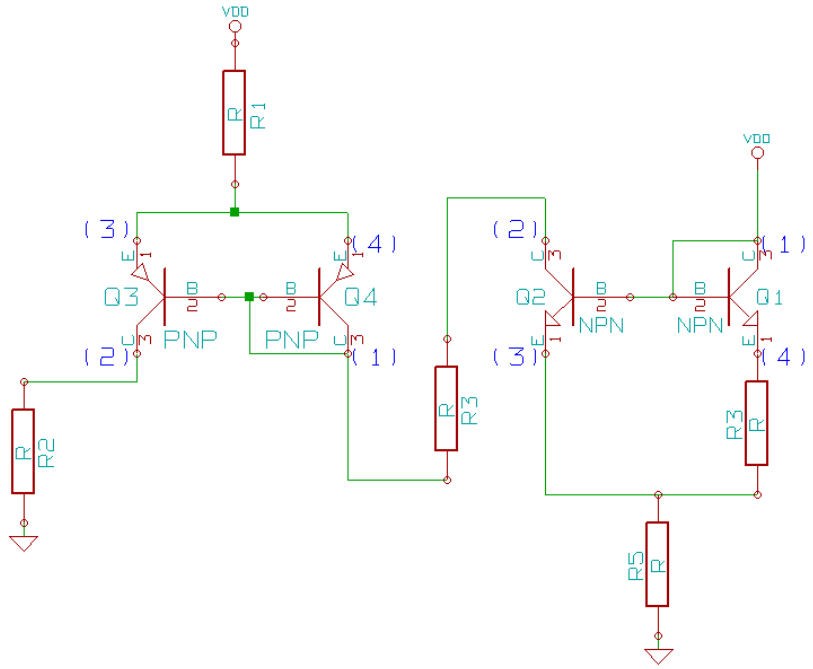


Figure 49 – First full current mirror experiment

This test was done with Vdd = 10, R1 = R5 = 22kΩ, and R2 = R3 = R4 = 1.5kΩ. A successful experiment would result in the voltages across R2, R3 and R4 all being the same. This would show that the current flowing through the input ad output parts of the circuit are the same. The voltages were measured across R2, R3 and R4 and were 0.008V, 0.006V, and 0.134V, respectively. These values are not within the allowable amount of error. Additionally, they are not consistent with the higher voltages that were expected in this experiment. It was fount that most of the voltage was dropped across R5, 9.30V. A second experiment was done on this circuit with the resistors changed. They were changed to R1 = R5 = 5kΩ, and R2 = R3 = R4 = 1kΩ. The experiment had the same goal as the previous one and, similarly, was not a success. The voltages measured across R2, R3 and R4 were 1.23V, 0.204V, and 1.392V, respectively. These voltages are not a successful result. Most of the voltage in this case was dropped across R1, with 7.97V. These experiments did not work because the voltage at the collectors of the transistors was not regulated, meaning neither was the current, and the resistor R3 was connected to the wrong pin. The voltage at the collectors needed to be regulated and R3 needed to be connected from pin 1 to Vdd.

The next experiment that was done had the resistors in the correct place but was still not the correct circuit. The schematic of the circuit is shown in Figure 50.

This test was done with Vdd = 5V and R1 = R2 = R3 = R4 = 5kΩ. In a successful experiment the voltages across R2 and R3 would be the same. Vdd was applied and the voltages across all of the

resistors were measured with a digital multimeter. The voltges were found to be 3.071V, 1.414V, 1.609V, and 3.272 across R1, R2, R3, and R4, respectively. This means the percent error between the currents going through R2 and R3 is 12.1% which immediately makes the test unsuccessful. A few minor changes were made to the circuit to further the understanding of the concepts. First, all of the resistors were changed to 1kΩ. In this case, the voltages across R1, R2, R3, and R4 were found to be 3.065V, 1.379V, 1.587V, and 3.273V, respectively. This resulted in a higher error of 13.1% relative to the error of 12.1% found in the previous experiment. This shows that the decrease in resistance resulted in a higher error. Additionally, it showed that the voltages across R1 and R4 remained very close to the same, meaning the voltage at the collectors of the transistors was close to the same in both experiments. The next change that was made to the experiment in Figure 50 was Vdd was changed to 10V and the -5V supply was changed to -10V. This resulted in readings of 6.76V, 2.575V, 2.856V, and 7.04V across R1, R2, R3, and R4, respectively. The error between the currents was 9.8%. This would seem be a good experiment but the increase in voltage spread across the whole circuit is the reason it appeared to be a success. Taking the readings from R1 and R4, it was revealed that the error in those readings was 4.0%. In the first two experiments the error in these voltage readings was 6.1% and 6.4%, respectively. It appears that the reduction in error between the voltages at the collectors of the transistors is what reduced the error in the voltage readings across the resistors R2 and R3. This means that the voltages across R1 and R4 should be the same in the circuit for the current mirrors to work as desired which suggests regulating the voltage at the collectors of the transistors.

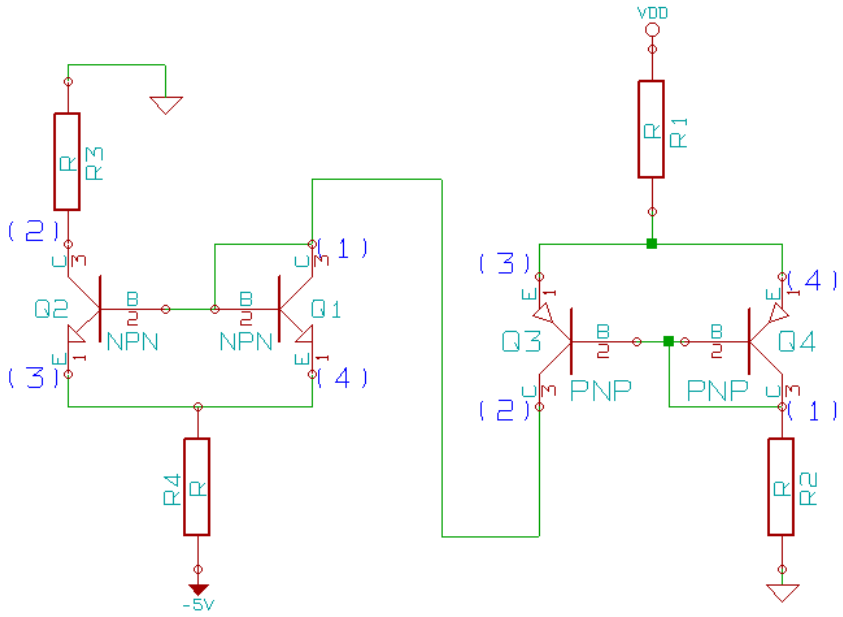


Figure 50 – Second full current mirror experiment

The next test that was attempted includes two additional transistors that are used for their diode drop properties. This will regulate the voltages at the collectors of the transistors to the fixed value of a diode drop. The schematic of this circuit is shown in Figure 51.

This test was done with Vdd = 5, R1 = R2 = 1kΩ, and R3 = R4 = 660kΩ using a resistance of two 330kΩ resistors in series. The resistances were measured with a digital multimeter and found to be closer to 664kΩ. Such a high resistance was used to simulate a high impedance input and output that the application of this current mirror circuit will use. The two transistors Q5 and Q6 act as diodes and therefore drop a diode voltage. This means that the collectors of the PNP current mirror transistors are at a diode drop above Vdd and the collectors of the NPN current mirror transistors are at a diode drop below ground. A successful experiment would result in the voltages across R3 and R4 being the same. The voltage across the the resistors R1,R2, R3 and R4 were measured and were 4.325V, 4.235V, 5.250V, and 5.663V, respectively. The percent error between R3 and R4 was 7.3%. To verify the successful operation of this circuit, the 664kΩ resistors were replaced with 330kΩ resistors. The voltages were measured and found to be 5.247V across R3 and 5.668 across R4, off by only 7.4%. This is determined to be a successful experiment. As a result, our current mirror circuit block was modeled after this circuit. A point of significance is the voltages across R1 and R2 were off by only 2.1%. This is the reason for the smaller error of 7.3% between the voltage measurements across R3 and R4. The diode drops across the transistors Q5 and Q6 are the closest relative to each other that can logistically be obtained so this is how it will be done in the final applications.

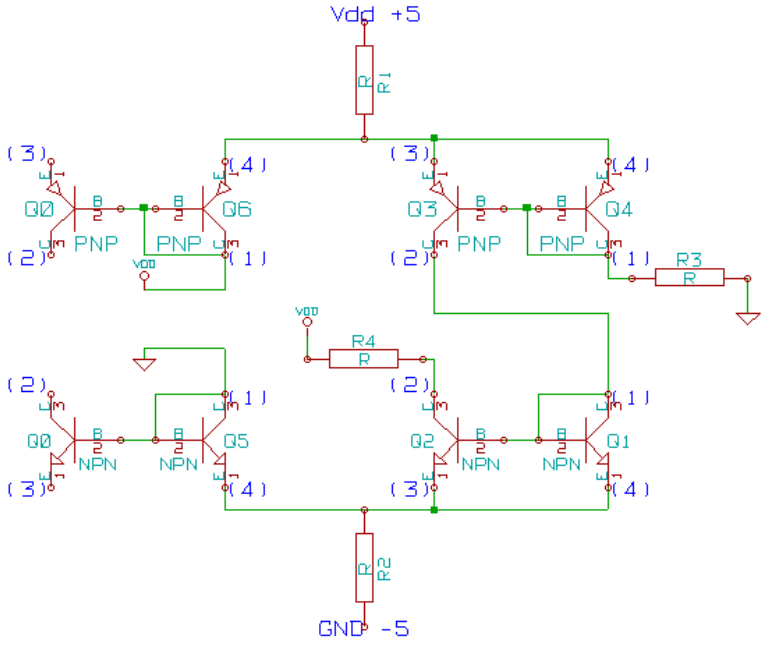


Figure 51 – Third full current mirror experiment.

After determining a current mirror circuit that would operate as desired, a fixture of seven of these circuits had to be built. Seven because there are seven data lines going from one set of AD7280s in parallel to the next set. Of these seven data lines, five of them are up sends, meaning the data is sent from the master to one of the slave boards. The other two data lines are down sends, meaning the data is sent from one of the slave boards to the master. The schematic for the first circuit that was designed and soldered to prototyping board is shown in Figure 52.

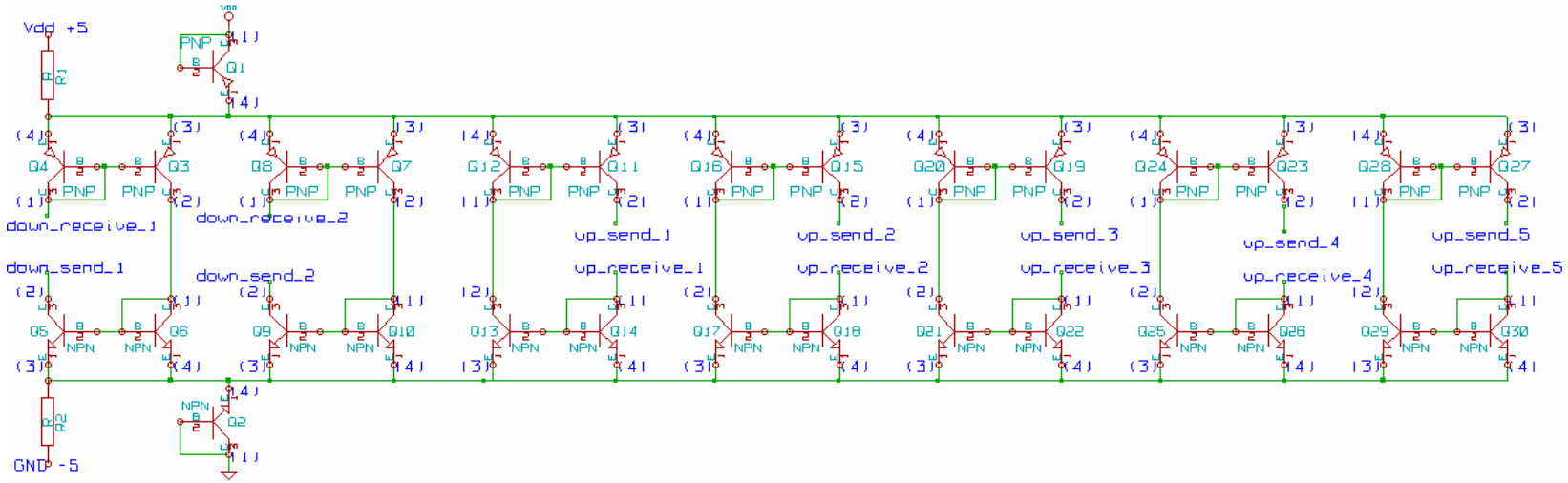


Figure 52 – First current mirror circuit using all seven data lines.

This circuit shown in Figure 52 uses the diode-drop transistors and pins 3 and 4, the collectors, are all connected to the corresponding diode-drop transistor. This regulates the voltage at the collectors of the transistors as explained previously. This circuit was tested using down send and up receive terminated at Vdd and down receive and up send terminated at ground. The Vdd that was used was 5V and the terminating resistors in both cases were 664kΩ. The complete results of this experiment can be seen in Table 6. This circuit was tested successfully as each of the current mirror pairs yielded an error of less then 10%, in fact, the average error was only 3.67%. However, before this circuit was attempted in the parallel configuration, it was realized that there was a problem. The connections of all of the pins 1 and 2 for all of the current mirrors needed to be switched. This is because in our application the send signal must be the one that is directly connected to the bases of the transistors in the current mirrors. This ensures that the current in a current mirror is the current out as both of the base currents are the same. The reason it worked in the test is because the resistors were a passive load so there was no defined send signal and receive signal. In the application the load will be active so the send signal must be connected to the transistor bases.

Table 6 – Results of the experiment shown in Figure 52

	Pin 1	Pin 2	% error
Data Line 1	down_receive_1	down_send_1	8.70%
	5.745V	5.245V	
Data Line 2	down_receive_2	down_send_2	7.70%
	5.685V	5.245V	
Data Line 3	up_send_1	up_receive_1	0.80%
	5.246V	5.290V	
Data Line 4	up_send_2	up_receive_2	3.00%
	5.246V	5.410V	
Data Line 5	up_send_3	up_receive_3	0.90%
	5.246V	5.292V	
Data Line 6	up_send_4	up_receive_4	2.40%
	5.237V	5.379V	
Data Line 7	up_send_5	up_receive_5	2.20%
	5.246V	5.363V	

A second current mirror circuit was designed and soldered on to prototyping board. The circuit is the same as Figure 52 except each of the pins 1 and 2 of the current mirrors are switched. This new circuit schematic is shown in Figure 53.

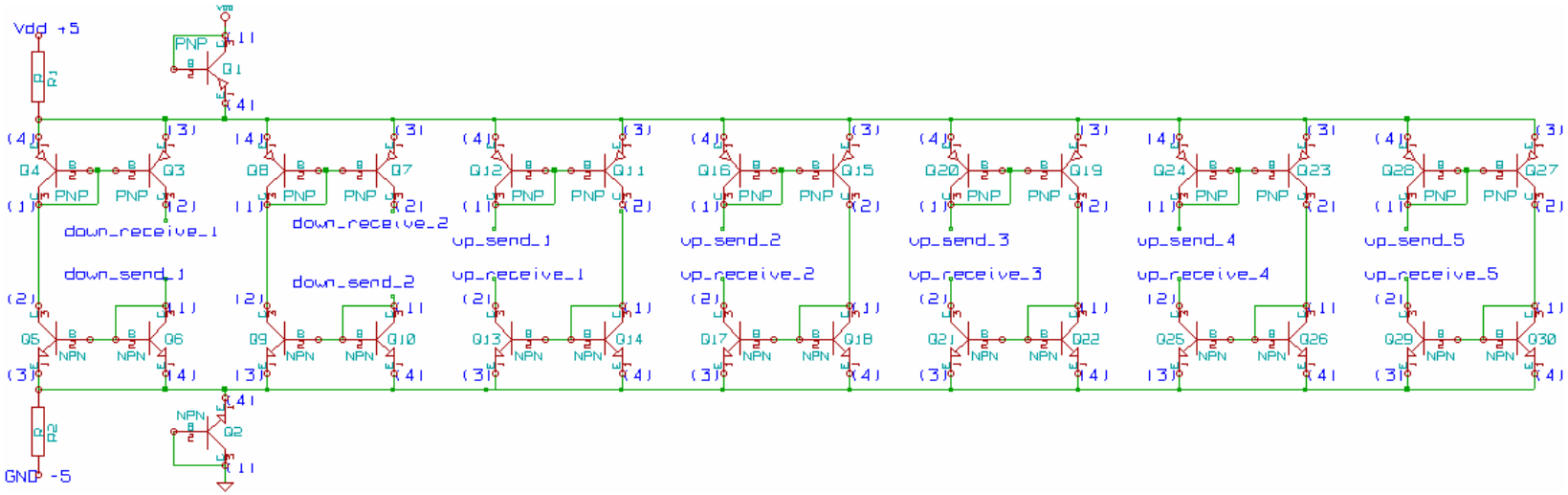


Figure 53 – Second current mirror circuit using all seven data lines. Send signal connected to the base of the receiving current mirror transistor

The circuit in Figure 53 was fabricated and tested. It was tested in the same way as previous, with V_{DD} = 5V and the down send and up receive terminated at V_{DD} and down receive and up send terminated at ground, each through 664kΩ resistors. For the complete results of this experiment, see Table 7. This board was tested successfully as all of the readings were off by less the 10%. The average error was 5.9% which is slightly higher than the average error in the previous circuit but still well within specifications. Since the send signal is connected to the transistor bases, as stated previously, this is the circuit that will be inserted into the parallel configuration

Table 7 – Results of the experiment shown in Figure 53.

	Pin 1	Pin 2	% error
Data Line 1	down_receive_1	down_send_1	3.30%
	5.427V	5.244V	
Data Line 2	down_receive_2	down_send_2	0.50%
	5.273V	5.244V	
Data Line 3	up_send_1	up_receive_1	7.30%
	5.246V	5.660V	
Data Line 4	up_send_2	up_receive_2	7.50%
	5.245V	5.673V	
Data Line 5	up_send_3	up_receive_3	7.40%
	5.246V	5.664V	
Data Line 6	up_send_4	up_receive_4	7.70%
	5.245V	5.683V	
Data Line 7	up_send_5	up_receive_5	7.60%
	5.246V	5.680V	

6.1.3. Initial Parallel Testing

After finding a current mirror circuit that will work as desired and designing the software to be capable of handling the new parallel configuration, the current mirror circuit was inserted into the system. The seven data lines from the master board were connected to the PNP current mirrors and the seven data lines from the slave board were connected to the NPN current mirrors. Figure 54 is a block diagram of the parallel test configuration:

There is one current mirror pair for each of the seven data lines. The arrows in Figure 54 show the flow of current going from the slave towards the master. According to the test data that was obtained in the individual tests, this circuit will output a current that has better than 10% error compared with its input. The power rails were set up using two dual rail power supplies, allowing for four different voltage levels and a ground. The power rails were 0V, 3V, 23V, 43V, and 46V. The symbolic representations of those voltages are GND-3, GND, $V_{DD}/2$, V_{DD}, and $V_{DD}+3$. A block diagram of the circuit is the shown in Figure 55.

Initially when the voltage was applied to this system the current limit indicator on the power supplies would activate. This would seem to mean there is a short somewhere in the circuit. Because of this, the circuit was rewired several times in an attempt to eliminate the short circuit. At one point in the rewiring a short was actually created and the AD7280s on the slave evaluation board were destroyed. At this point new AD7280s were obtained and professionally mounted to the evaluation board. The new board was tested and it was confirmed to function properly on its own. With the new board in and the system verified to be wired correctly, the current limit indicator on the power supplies still activated when the voltage was applied. The current limit was set to 20mA for the entire system. When the limit was relaxed to 22mA the indicator would flicker on and off. This would seem to mean that 22mA is close to how much current the system actually draws. The limit was then relaxed to 30mA and the indicator did not go on after that point. The current drawn by the entire system was about 22mA at the given voltage, as indicated by the power supply reading. There was no short.

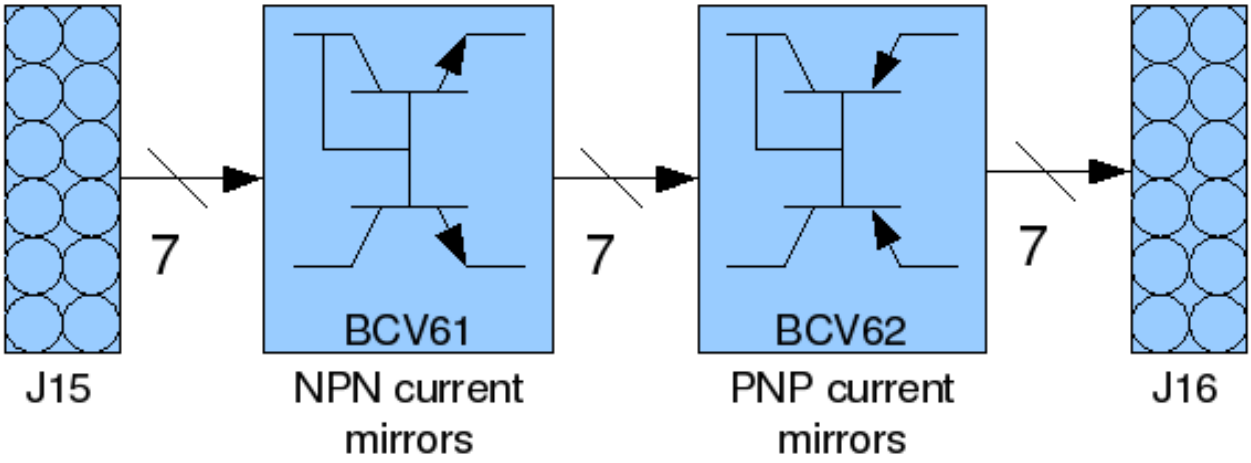


Figure 54 – Test integration of current mirrors.

When the voltage was applied to the system at the levels previously indicated and there were no setbacks, an attempt was made to download the code to the board and attempt to read data. The software showed that the first board was reading data but the second board, connected through the current mirrors, was not.

This contrasted the results from the series test where both boards and all four AD7280s would read data correctly. This means that the error must be related to the current mirrors being introduced into the system. An analysis of the data line SCLK was done due to the nature of a clock signal being a periodic square wave that is easily identifiable. Probing was done with an oscilloscope through a diode on the send signal, a test point on the receive signal, and through a resistor in between the current mirrors.

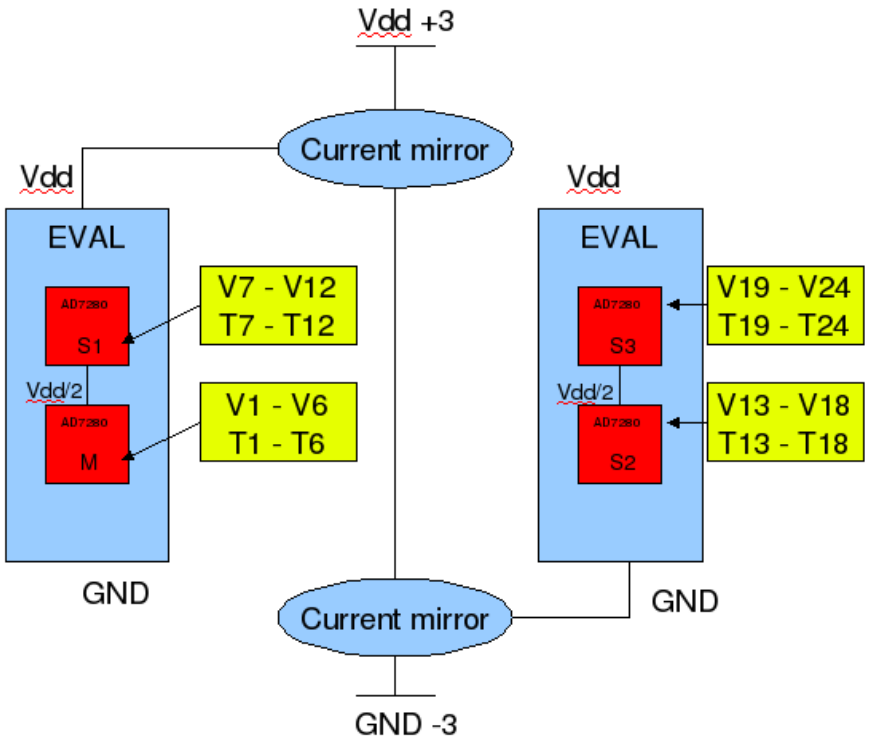


Figure 55 – Block diagram of the parallel test setup.

The diode that was probed to obtain an SCLKhi signal on oscilloscope s D15. This is because the oscilloscope can only read voltage so the wire itself can not be used as a test point, there must be an impedance. At the master board J16, pin 5, which is SCLKhi, the signal seen on the oscilloscope can be seen in Figure 57.

Figure 56 – Data from the master board (top) and the slave board (bottom). Note that the slave is not receiving data.

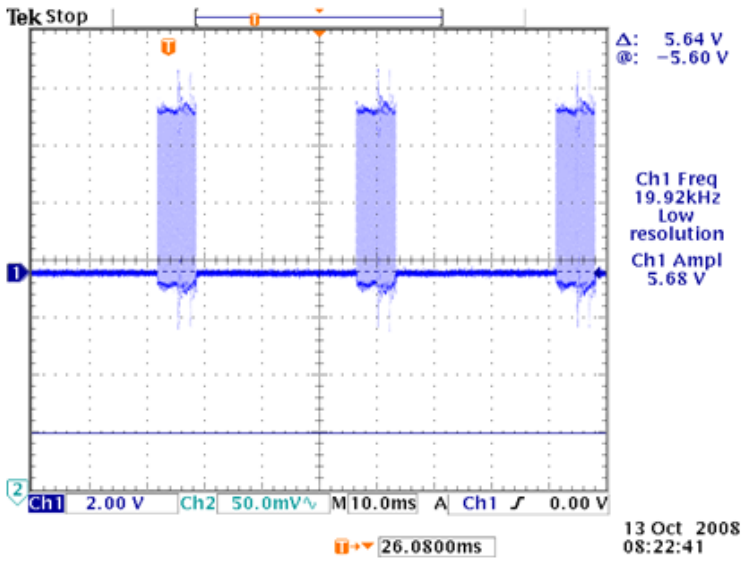


Figure 57 – Signal of SCLK from Test Point on Master Board

Figure 57 is a healthy looking clock signal meaning the problem with the system does not lie in the master board send signal. Next, the bridge wire between the NPN and PNP current mirror was probed with an oscilloscope through a resistor. Figure 58 shows the location that was probed to obtain the signal:

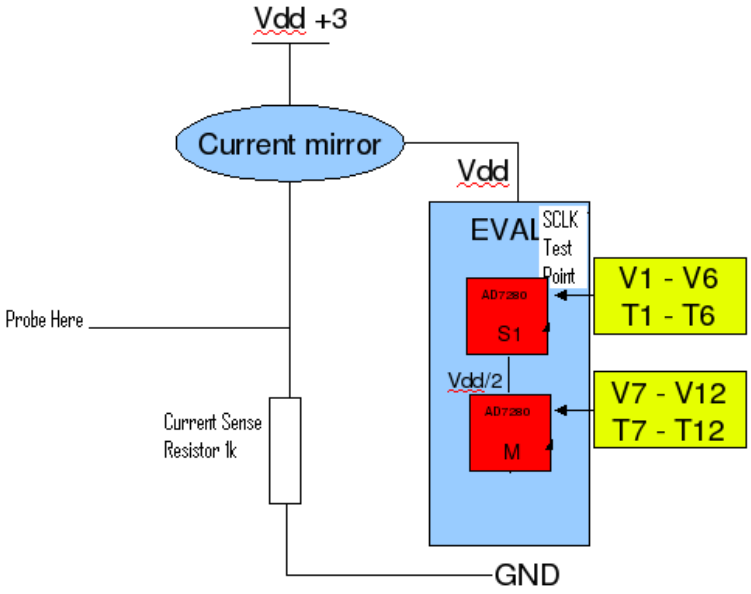


Figure 58 – Probe of SCLK signal after one current mirror

The obtained signal should be the same as the signal that was sent from the master board because the current in the current mirror circuit should be the same throughout.

The signal displayed in the output of the first current mirror is not what was expected as a signal similar to Figure 57 should have been what was seen. The obtained signal just looks like noise. This result means either the signal has been corrupted after coming through the first current mirror or the probe location is invalid. Since the signal is being measured from a resistor it is known the signal obtained should be a scaled version of what was seen at the master board meaning the probe location is valid. A probe after the second current mirror was done to verify the result. The SCLK signal was measured at the test point on pin 5 of J15, the input to the slave board.

The probe was placed on the SCLK test point on the PCB. The received signal should a scaled version of Figure 57. This data line was probed at the test point shows the signal coming from the second current mirror.

The signal coming from the second current mirror does not look like the signal that was seen at the output of the master board or the signal that was seen between the two current mirrors, but rather a signal that is nothing much more then ambient noise. After seeing these results of the AC analysis of the current mirror circuit, a new approach had to be devised to gain a better understanding of the system. The main concern was the current mirror data sheets specified the use of both AC and DC current mirroring but the tests to verify the current mirror operation were all done using DC supplies. There was no initial test done to verify operation using AC supplies which is what is used in the application of the current mirrors. Further investigation needed to be done.

We looked closer into the current mirror data sheet and noticed that the current mirrors can only operate up to 30 volts across the transistor at pins 2 and 3. The voltage across them in the full test that was done with all seven data lines was close to 44 volts on the sending current mirror. This voltage is well out of specification and is the reason that the current mirror circuit did not perform as expected in the test.

A new current mirror circuit was built because the previous one had been destroyed due to the over-voltage. The circuit was tested with the DC analysis as before and passed with similar results. The voltage across the system was setup lowered to 26 volts with the rails on the power supplied set at 0V, 3V, 13V, 23V, and 26V that are represented by GND-3, GND, Vdd/2, Vdd, and Vdd+3, respectively. Again, the SCLK was chosen for AC analysis because of its predictability. The same locations as the previous test were probed. The signal measured from the master board at pin 5 on J16 is shown in Figure 59.

As before, Figure 59 shows a healthy clock signal. The goal is for the rest of the probe locations to result in the same display. The next probe was taken off of a resistor between the two current mirrors. Figure 60 shows the display of the oscilloscope.

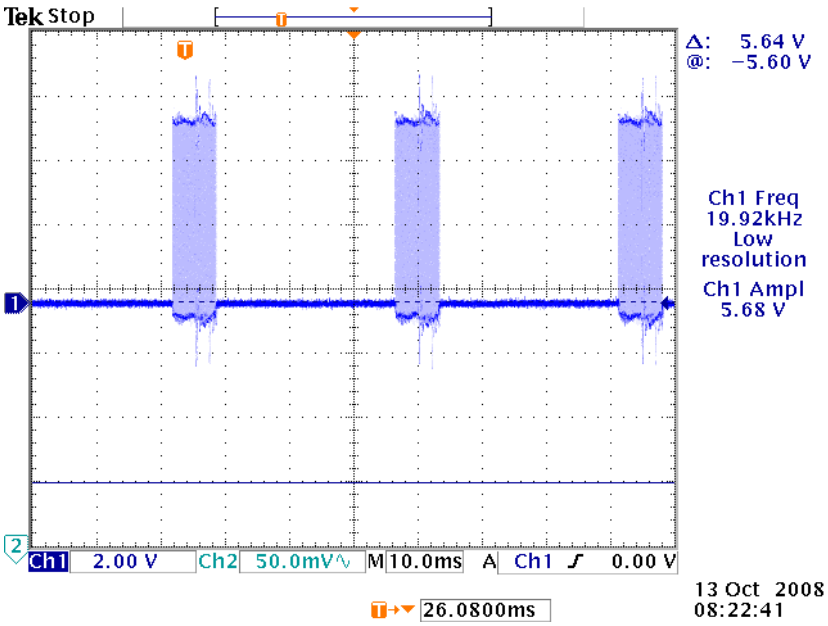


Figure 59 – Picture of SCLK test point output from the Master Board

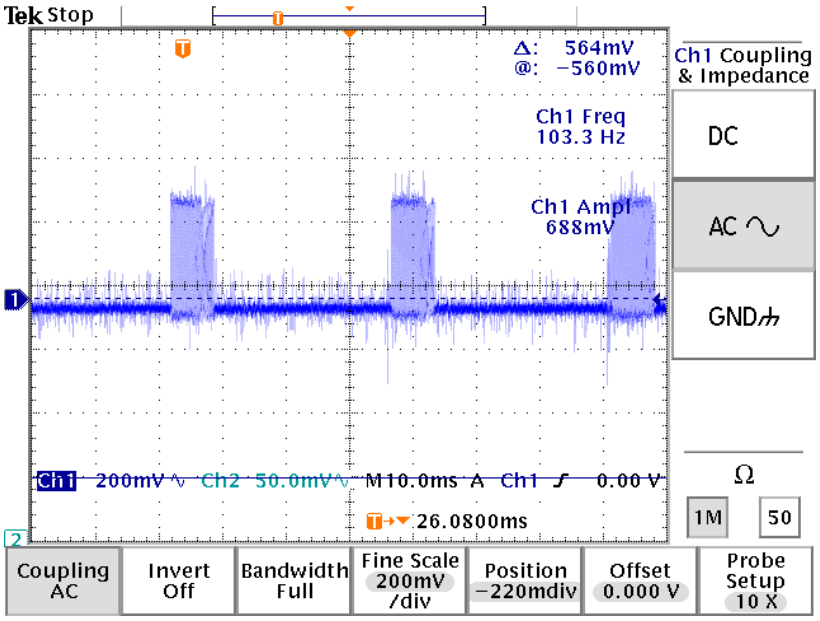


Figure 60 – Signal of SCLK Signal after One Current Mirror

This signal is what was expected and desired. It is a bit attenuated but that is also expected because the oscilloscope reads voltage and the output is a current. The oscilloscope cannot account for the difference in impedance between the diode probe and resistor probe so a scaled version is acceptable. Since this signal is good, it should also be what is seen at the output of the second current mirror. Figure 61 shows the reading from the test point on pin 5 of J15 on the slave board, which is the

signal after going through the current mirror circuit, as well as the diode on pin 5 of J16 on the master which is the signal that is sent to the input of the current mirror:

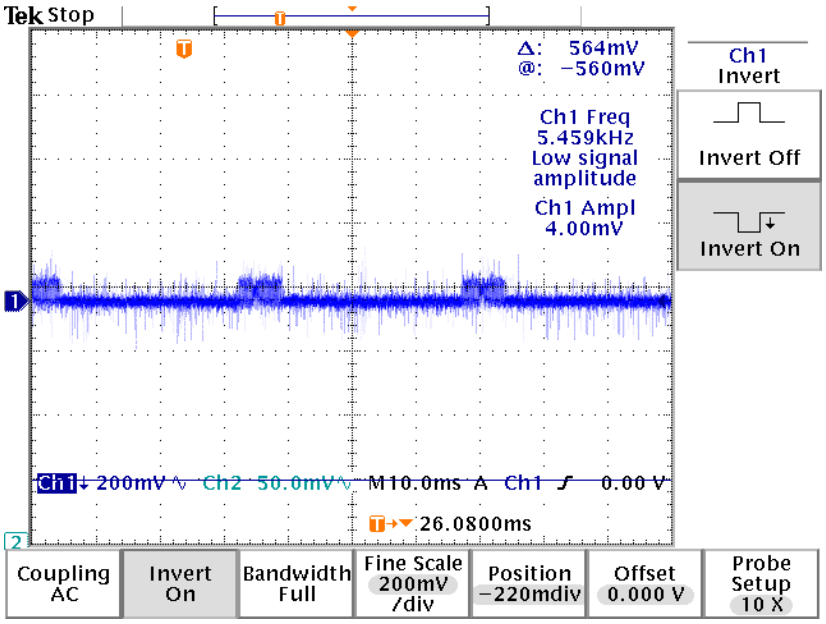


Figure 61 – SCLK from the slave board

Note the difference in scale of the oscilloscope in this figure versus the previous figures. This is a good signal. Also not the attenuation of the signal received by the slave board. This is, again, a result of different impedances on the test points which is acceptable. The figure shows that the output of SCLK from the master is very similar to the input of SCLK to the slave coming from the current mirrors. This is when it was realized that the current mirrors being used before had been destroyed due to their being used out of specification.

We then tested the four additional current mirror pairs in the up send configuration using the SCLK signal. This is because the master device has five send pins, which send data from low potential to high potential, and 2 receive pins which receive signals from a higher potential to a lower potential. The five send signals worked as desired as results similar to the previous experiment were seen from each current mirror pair. The same test could not be done on the two receive pins because it is not known what signal to expect when only one of them are connected in the system. Instead, the whole current mirror circuit was connected after verifying the voltage on the power supplies were low enough to safely operate the current mirrors. The devices were connected and an attempt to read data was made. At the low voltage and using the thoroughly tested current mirror circuit, data was successfully read from both the master board and slave board in the parallel configuration for the first time.

6.1.4. EVAL Board Final Testing

During the testing of the system in parallel with the current mirrors, the received signal through the current mirrors would break down at a certain voltage rendering is useless. This voltage at which the received signal breaks down is 20.5V across pins 2 and 3 on the PNP current mirrors in the up send

signals and across the NPN current mirrors in the down send signals. That is not consistent with the absolute maximum voltage of 30V allowable by the current mirrors according to the data sheet. This can be attributed to the fact that very small signals, 200 micro amps for a high, are being used and the 30V rating is an absolute maximum meaning operation at that voltage is unstable. This breaking down of signals can be seen on all data lines. The first test of this was on the data line SCLK which is an up send signal, from master to slave. A healthy SCLK signal would look Figure 62.

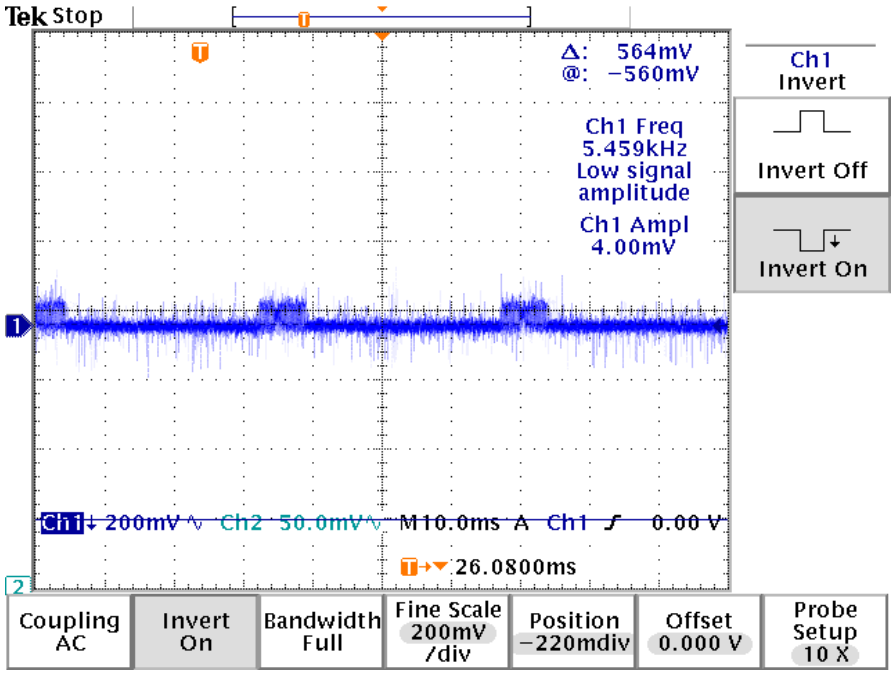


Figure 62 – Healthy SCLK Signal

This is the signal that was sent and measured from the master board through a diode at pin 5 of J16 regardless of the voltage put across the system. It is also the signal received at the pin 5 of J15 test point on the slave board before the voltage across pins 2 and 3 of the PNP current mirrors reaches 20.5V. When the voltage across the entire system rose above 26V, the voltage across pins 2 and 3 of the current mirror reached 20.5V. At that point the SCLK signal received by the slave board at pin 5 of J15 looked like Figure 63.

Figure 63 shows that there is a limit to the voltage that can be across the system. After this limit the SCLK signal is corrupted which means the rest of the system cannot function properly. To verify, the SDOlo signal was measured at pin 8 on the J15 test point on the slave board. When the voltage across the system is low enough and the SCLK signal is functioning properly, The SDOlo signal looks like Figure Figure 64.

Figure 64 shows a *down send* signal data line, meaning that the data flows from slave to master. Down send signals measured at the slave should look like the above signal unless there is some kind of corruption in the entire system. Knowing this, and the point at which SCLK becomes corrupted, the signal

was measured again with a voltage across the system known to corrupt SCLK. The signal obtained is seen in Figure 65.

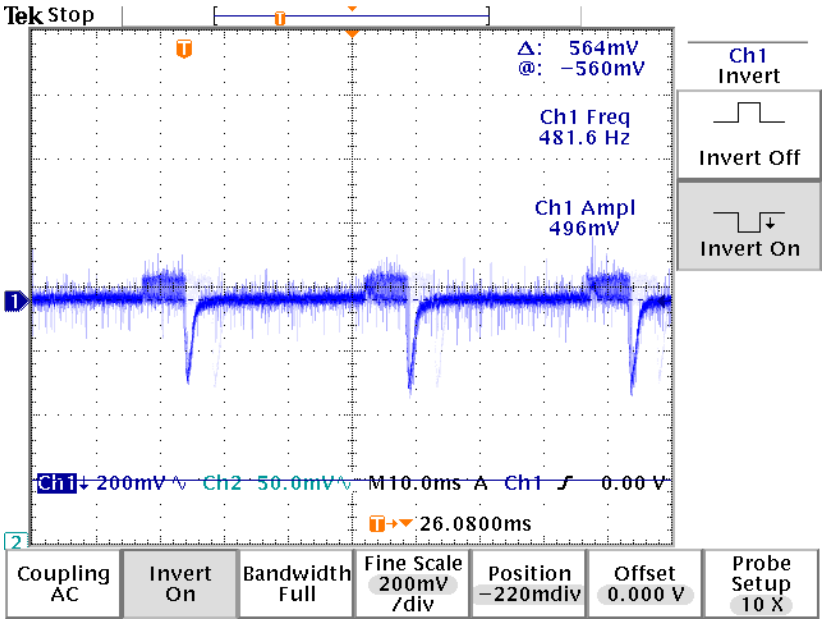


Figure 63 – Corrupted SCLK signal

The figure shows that the SDOlo signal has been corrupted by the high voltage and therefore the entire system data communication becomes corrupted when the voltage rises above 26V across the system. This also explains the failure of the first test. The first test was done at a voltage of 48V across the system. Not only is this much higher than the 26V at which the data signals become corrupted, it would also result in a voltage of about 44V across pins 2 and 3 of the current mirror which is 14V more across the transistor then the absolute maximum according to the data sheet.

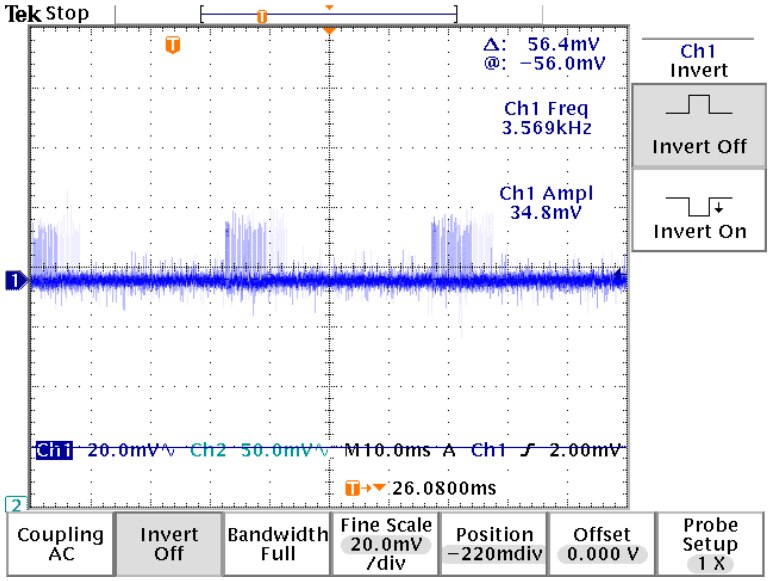


Figure 64 – Healthy SDOlo Signal

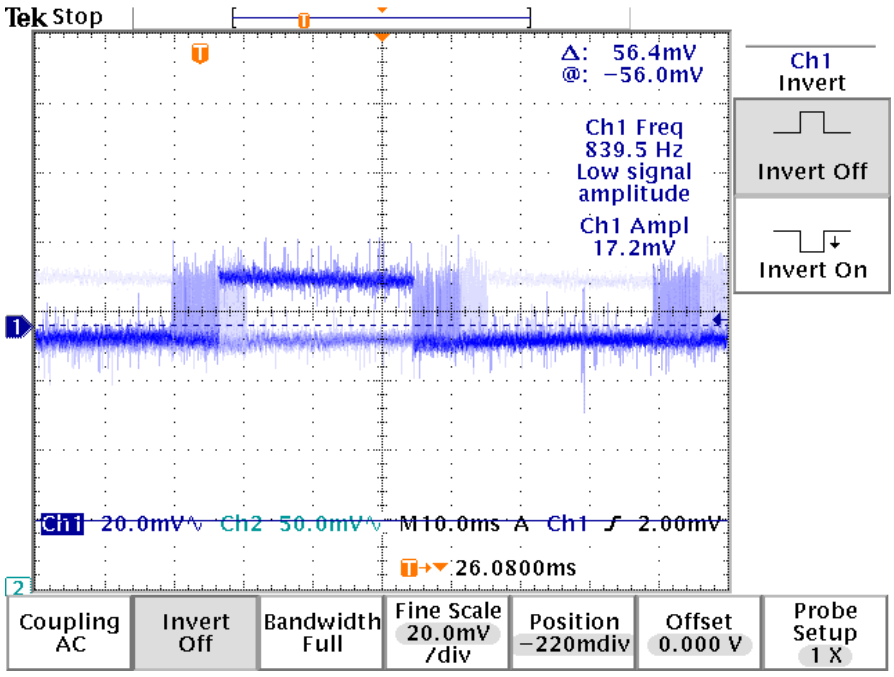


Figure 65 – Corrupted SDOlo Signal

The voltage across the system in our application needs to be 51V which, if not compensated for, will result in the same failure as the first test on the current mirrors where the absolute maximum rating is surpassed and the signals were corrupted. To solve this problem a zener diode was placed in between the two current mirrors. The schematic of a single current mirror is shown in Figure 66.

The zener diode that was used in the test was 20V. This value means the first 20V across the system has to be dedicated to the zener diode but the system would be able to operate at a higher voltage then it was previously able to. When the 20V zener diode was inserted, a test was performed on SCLK to find out at what voltage the signal breaks down. The break down voltage was found to be 42V. This is a better result as it is now known that the zener diode increases the amount of voltage that the system can handle. There is, however, now a higher minimum voltage that can be put across the system. This voltage is 26V, giving a 16-volt resolution. If the system was given a voltage under 26V there would be no reading by the software because it would be below the threshold. The 16V resolution is still an improvement over the circuit with no zener diode, however. The resolution in that case was 5 volts as each AD7280 needs at least 7.5V to operate and the current mirrors operate 3 volts out of ground and Vdd meaning the system could only operate between the voltages of 21V and 26V. In the application of this system the zener diode will need to be higher than 20V to be able to raise the total voltage across the system to 51V but the tests show that the concept of inserting a zener diode works.

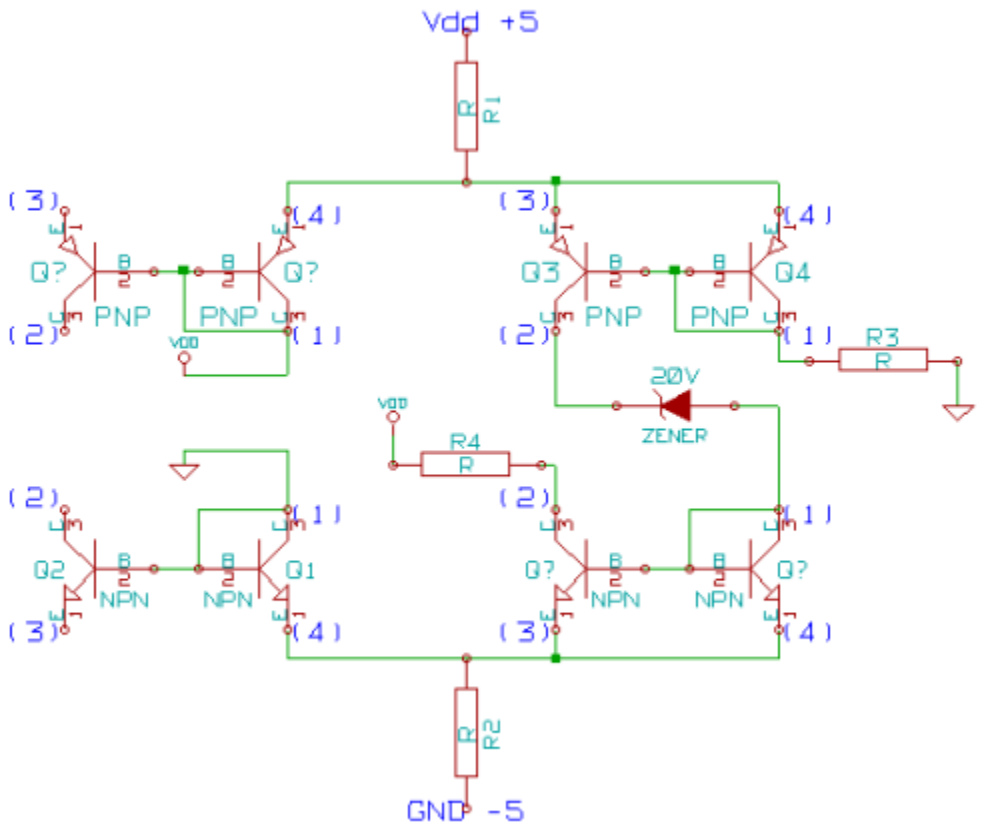


Figure 66 – Schematic of current mirror with zener.

6.2. Software Implementation

This software is based on Kate O'Riodan's AD7280 Evaluation Software. Some of her code is left here for debugging purposes, however if this document does not mention it, the programmer should just ignore it because it's not used. Her software was designed for two AD7280s on one EVAL Board and there were some issues involving memory refresh. The CED buffer is directly linked to the memory of the Cyclone FPGA. Some of the changes from Kate's software include the characteristic in which this software refreshes the CED buffer every 10 seconds so that it can run indefinitely, allowing for register access for 22 devices, a popup board screen to see conversion data for 22 devices, and an auto configuring of alert settings. The idea behind this software is to communicate through USB with the CED board as the CED board reports data from the AD7280s.

The AD7280 DEMO Software uses a button triggered interrupt type of actions. What this means is, whenever a button is pressed, a variable is set and depending on the numeric value of that variable a specific action is performed.

For example, for the Read/Write Single Register button is pressed then the Read/Write Single Register variable is triggered to a value of "true" and that activates a block of code is run shown on Figure 67. All this block of code does is to set a value 4 to the variable num.

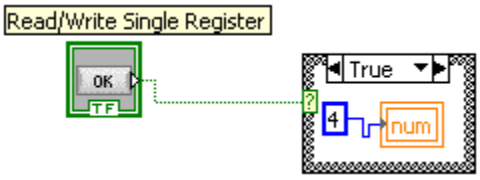


Figure 67 – Read/Write Single Register triggering

This software is also hierarchical based, which means that there is a VI called AD7280main.VI that is always running and it calls on other VIs during its operation as shown on Figure 68. These VIs when called can do anything from modifying the AD7280 registers to displaying conversion data. The VIs on lowest level are used for FPGA communication through the USB to the CED board. These VIs are shown in green and blue and they are **Configure Power Supplies**, **Program Board**, **Search for Boards**, **Manual Receive From**, and **Manual Send to**. All other VI, the ones shown in blue and white are higher level VI that takes the data from the FPGA VI and does parsing and plotting with it. Parsing is extracting required data from information returned from a lower level VI that is not in a useful form. For example, if a lower level VI returns a stream of bits, another function is required to break down the stream of bits and acquire useful information from just a stream of bits. Plotting is displaying the information on a chart.

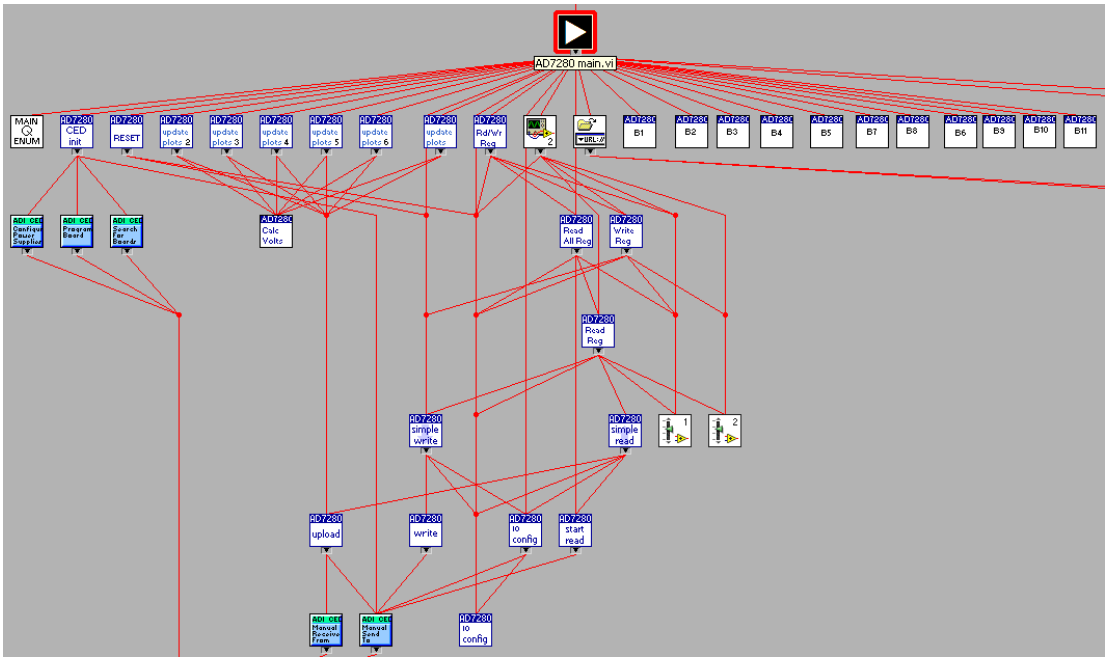


Figure 68 - VI Hierarchy

6.2.1. Examining the Lower Level Code

The following is documentation of how the button pressing relates to certain actions being triggered as well as what the code does as it runs continuously. As stated before, this software has a main VI always running in the background and events get triggered based on the user pressing certain buttons causing interrupts.

6.2.1.1. Event Triggering

There are a few event triggering variables, namely Numeric 5, and num.

num has the highest level of control for it controls how the program behaves.

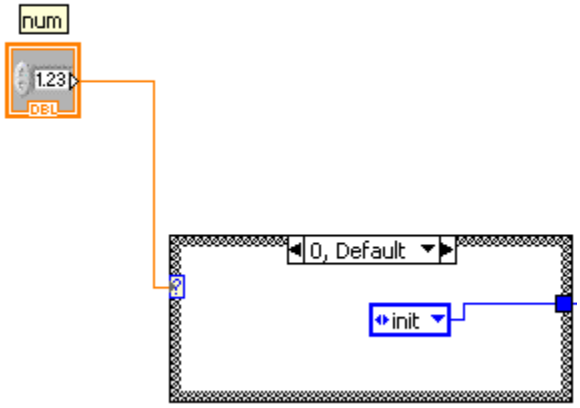


Figure 69 - num triggering

If num = 0, a function is triggered to initialize the AD7280s through the CED.

If num = 1, a function is triggered to download the code to the AD7280s through the CED.

If num = 2, a function is triggered to **upload** the conversion data continuously from the AD7280s.

If num = 3, a function is triggered to stop the program from running.

If num = 4, a function is triggered to allow the user to write/read all critical AD7280 registers.

If num = 5, a function is triggered to automatically configure the alert settings AD7280 registers by auto-writing to certain registers.

Numeric 5 governs which DEMO-board is active.

Figure 70 - Numeric 5 Triggering

If Numeric 5 = 0, all functions from devices on all the boards are stopped.

If Numeric 5 = 1, a function is triggered to **upload** data from the devices on Board 1 and a screen pops up showing all the data from Board 1.

If Numeric 5 = 2, a function is triggered to **upload** data from the devices on Board 2 and a screen pops up showing all the data from Board 2.

If Numeric 5 = 3, a function is triggered to **upload** data from the devices on Board 3 and a screen pops up showing all the data from Board 3.

If Numeric 5 = 4, a function is triggered to **upload** data from the devices on Board 4 and a screen pops up showing all the data from Board 4.

If Numeric 5 = 5, a function is triggered to **upload** data from the devices on Board 5 and a screen pops up showing all the data from Board 5.

If Numeric 5 = 6, a function is triggered to **upload** data from the devices on Board 6 and a screen pops up showing all the data from Board 6.

If Numeric 5 = 7, a function is triggered to **upload** data from the devices on Board 7 and a screen pops up showing all the data from Board 7.

If Numeric 5 = 8, a function is triggered to **upload** data from the devices on Board 8 and a screen pops up showing all the data from Board 8.

If Numeric 5 = 9, a function is triggered to **upload** data from the devices on Board 9 and a screen pops up showing all the data from Board 9.

If Numeric 5 = 10, a function is triggered to **upload** data from the devices on Board 10 and a screen pops up showing all the data from Board 10.

If Numeric 5 = 11, a function is triggered to **upload** data from the devices on Board 10 and a screen pops up showing all the data from Board 11.

6.2.1.2. Button Triggering Event

The way to trigger these numeric variables is by the use of buttons as discussed in the previous section. These seventeen buttons are Autorun, Auto Config Registers, Write/Read Single Register, Initialize, Stop Board Actions, and Activate Board 1 to Activate Board 11. The buttons can be seen as boolean variables, and when they are pressed they are true and when they are unselected, they are falese.

When Autorun is true as shown on figure 20 the variable, Numeric 4 is incremented until Numeric 4 = 500. If Numeric 4 = 500 then Numeric 4 is set to 0. If Numeric 4 is less than 498 then num is set to 2, which triggers a function to **upload** the conversion data continuously from the AD7280s. If Numeric 4 is less than 500 and is greater than 498, num is set to 1 which triggers a function to re-download the code to the AD7280s through the CED.

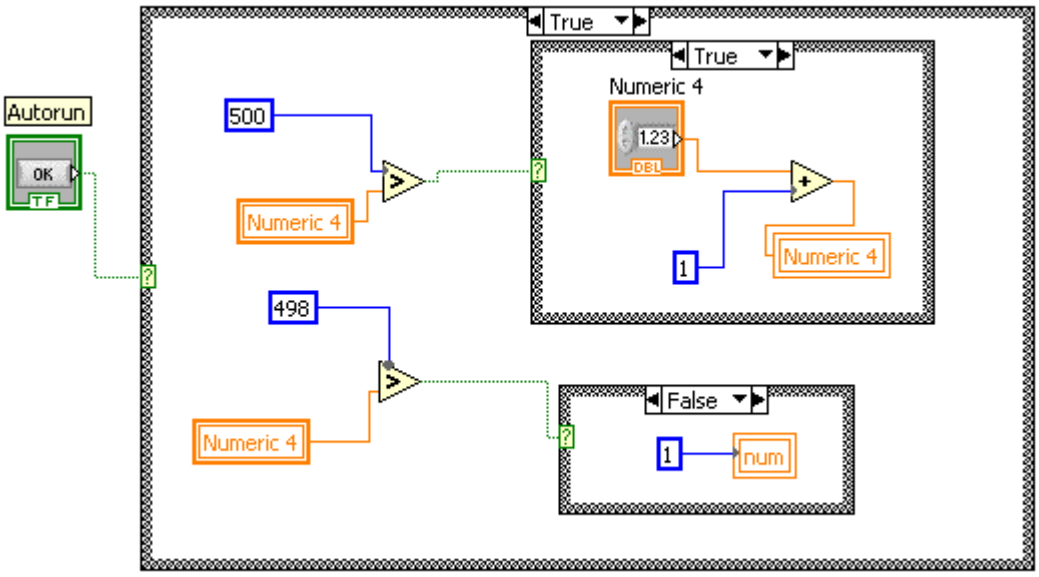


Figure 71 - Autorun Triggering

The reason for this to toggling is if the CED continuously **upload** data then it will the CED buffer will be full thus causing the device to stop working. Therefore, re-downloading the code once in a while will clear up the buffer. Another reason for setting num = 1 periodically is to ensure that the CED is ready to **upload** data after each refresh.

If Initialize is true, then num is set to 0 as shown on Figure 61.

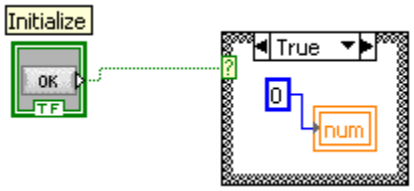


Figure 72 - Initialize Triggering

If Autoconfig Registers is true then num is set to 22.

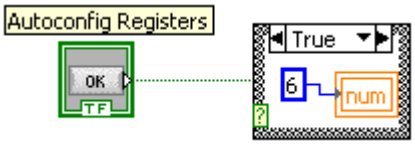


Figure 73 - Autoconfig Registers Triggering

If Write/Read Single Register is true then num is set to 23.

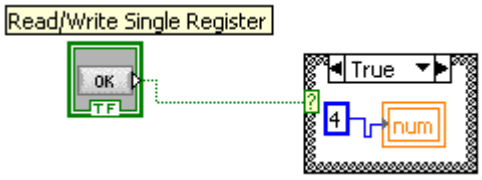


Figure 74 - Read/Write Single Register Triggering

If any of Activate Board 1 to Activate Board 2 and Stop Board Button is true then Numeric 5 will be set to the appropriate value shown on figure 24.

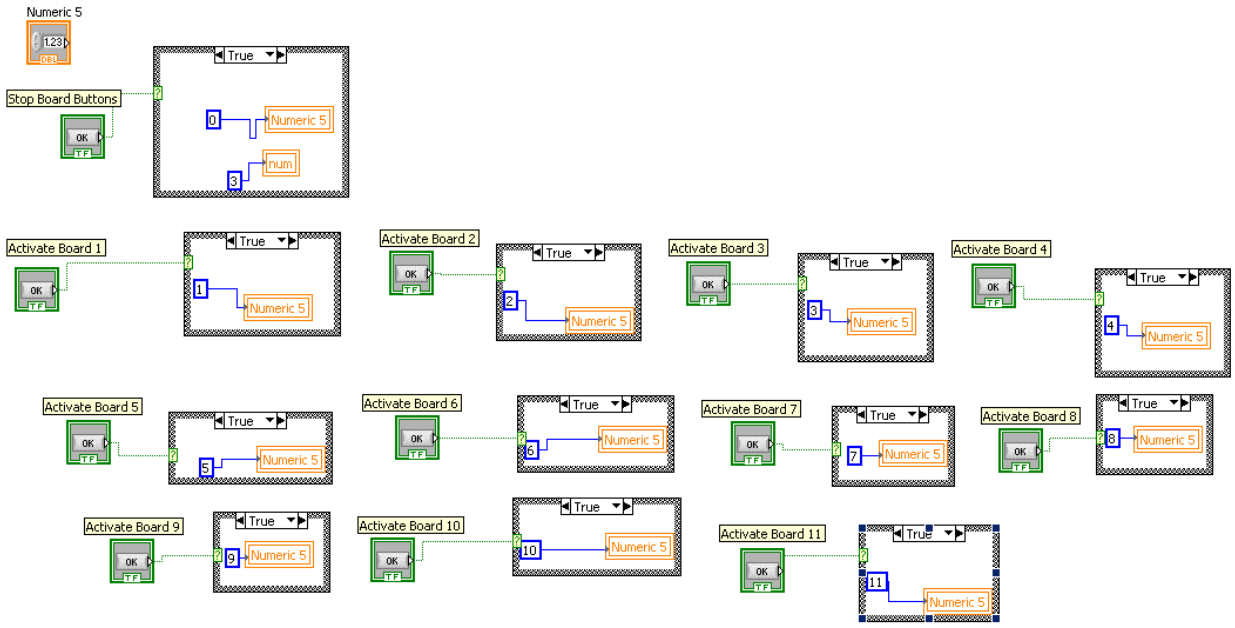


Figure 75 - Board Action Buttons Triggering

6.2.1.3. Runtime-Actions

The way that the CED reads conversion data from the AD7280s is by grabbing a chunk of addresses of the AD7280s and sends that data value of these addresses to the PC.

As the program starts, num = 0, therefore the SUBVI, **CED init** gets called.

Figure 76 - **CED Init**

As the code steps into CED init, as shown by Figure 77, four other sub-VIs are called.

All the SUBVI in this VI are FPGA communicators. As stated above, the VIs in blue are for FPGA communication. As shown on figure 26, this VI uses the functions to **Search for Boards**, then **Program the Board**, then **Configure Power Supply**, and then enables the board to output with **Manual Send to**. In most practical application, this VI and all its SUBVIs should be left unchanged.

Stepping out of CED init is shown in Figure 78.

We set 1 to num because since the board is initialized, we can prepare the board to **upload** data.

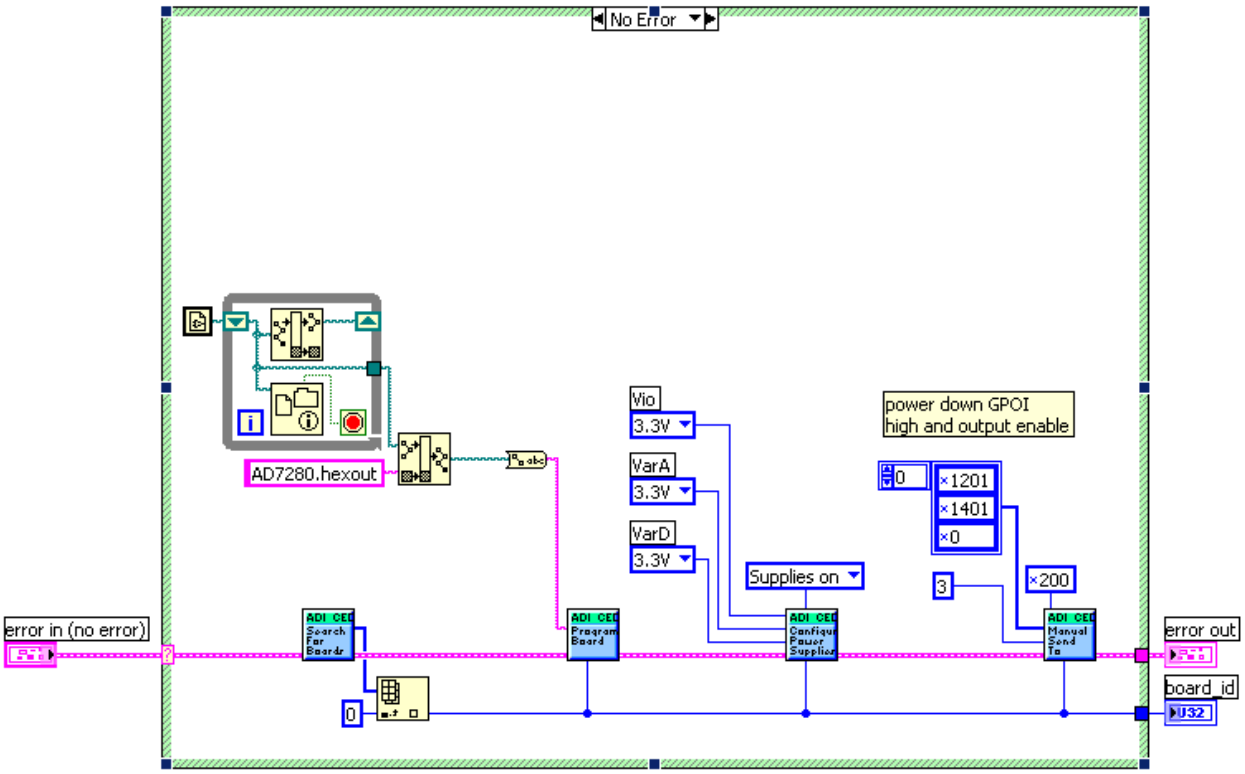


Figure 77 - After CED Init

Figure 78 - Prepare Data

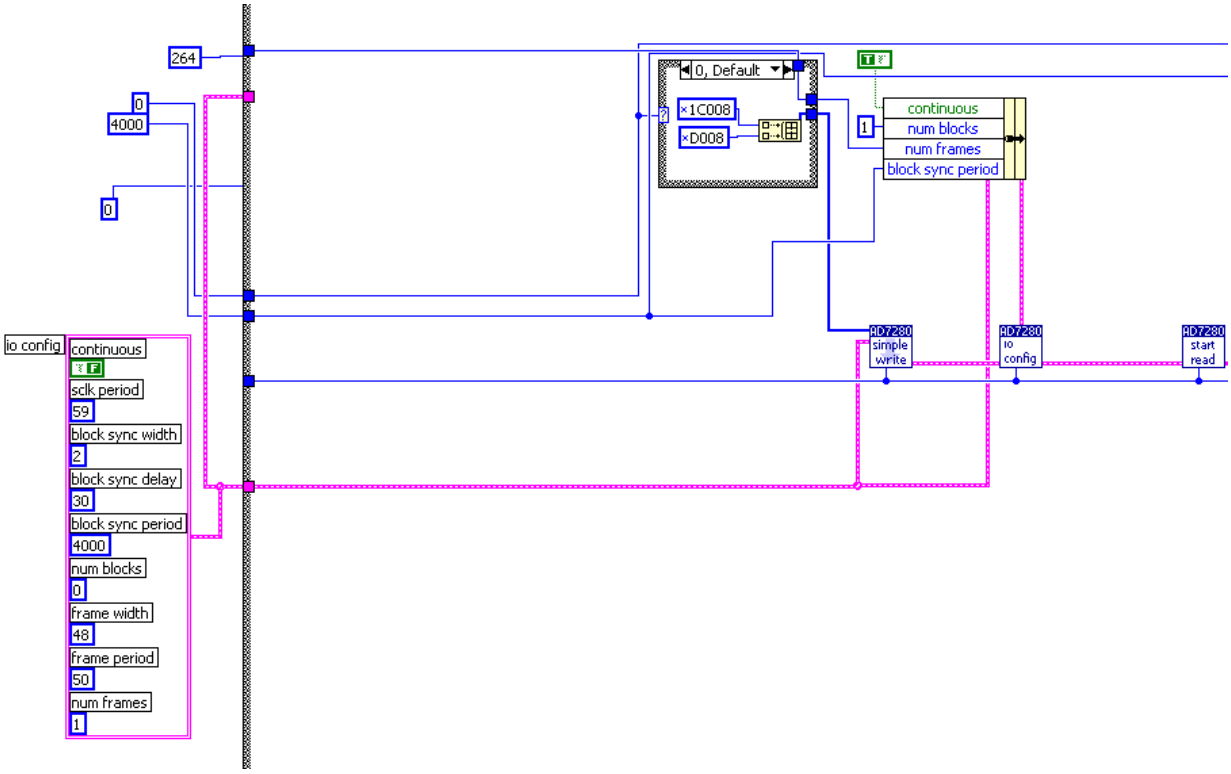


Figure 79 - **I/O config**

The function in Figure 79 first configures the I/O as shown on figure 28 on the left side. It is recommended this **I/O config** be left unchanged.

continuous: If true it causes the CED to read continuously from the AD7280. It does not stop after num frames / num blocks.

sclk period: Controls the period of the serial clock - the actual sclk period achieved is: 120Mhz / (2 * (sclk period + 1))

block sync width: The number of half sclk periods form the falling edge of convert start to the rising edge of convert start.

block sync delay: The number of half sclk periods from the falling edge of convert start to the falling edge of cs.

block sync period: The number of half sclk periods form the falling edge of convert start to the next falling edge of convert start.

num blocks: The number of convert starts in a burst. If zero there is a burst of chip selects with out a convert start and the convert start timing parameters are ignored.

frame width: The number of half sclk periods form the falling edge of chip select to the rising edge of chip select.

frame period: The number of half sclk periods from the falling edge of chip select to the next falling edge of chip select.

num frames: The number of chip selects in following each convert start (or in a burst if num blocks is zero).

A very important thing to note is the number 264 shown on the left side of Figure 79. This shows the number of frames of registers that the CED grabs. Each device uses 12 frames, so 264 frames means this software is currently used for 22 devices. Therefore, to tell the CED to get more addresses, just increment this number in steps of 12.

After that the SUBVIs **Simple Write**, **I/O config**, and **Start Read** is called as shown on figure 28. The VI start read causes the CED to start reading from the AD7280 according to the configuration of the serial I/O circuitry of the CED provided in the most recent call to **I/O config** VI. The values are stored in the RAM of the CED which is configured as a FIFO.

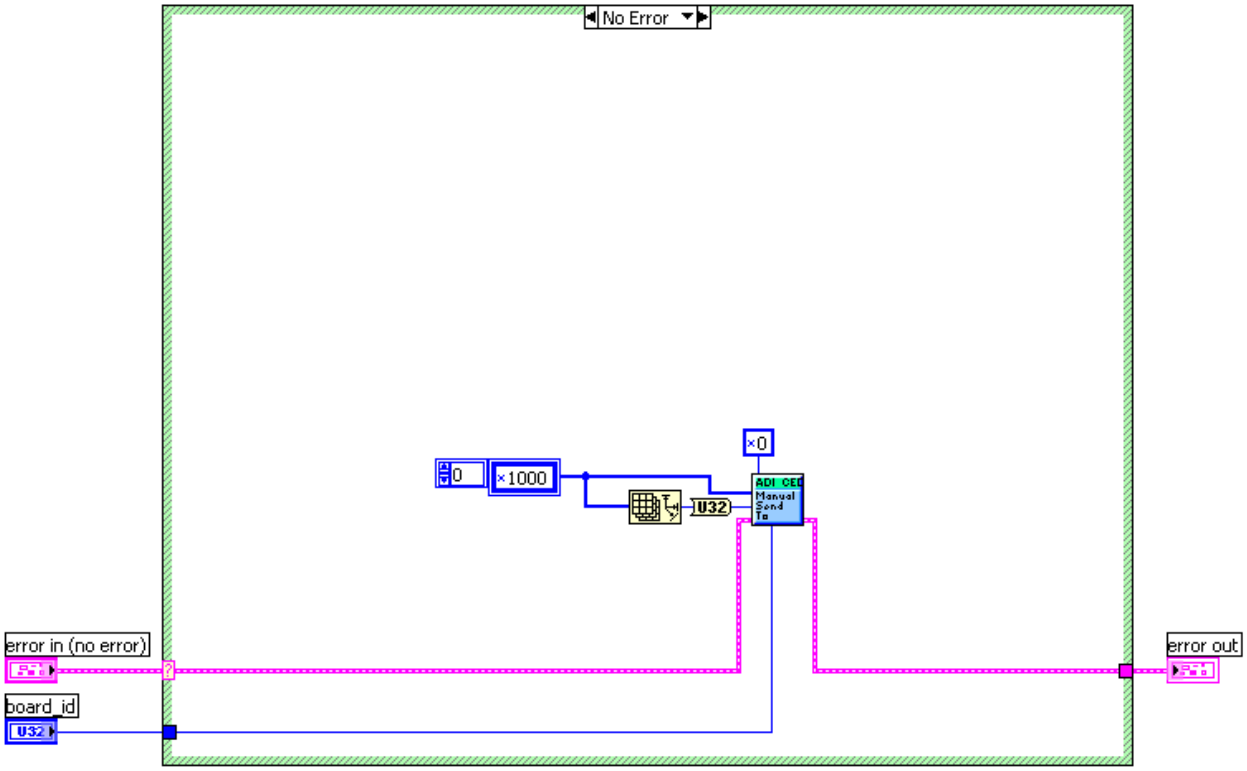


Figure 80 - **Manual Send to**

Stepping into start read, we see the FPGA communication VI, **Manual Send To**, being called on Figure 29. And a value of 1000000000000ob is sent to the CED telling it to start grabbing registers.

Figure 28 also shows the VI, **Simple Write** being called. **I/O config**.VI configures the serial I/O circuitry in the CED according to the parameters contained in the **I/O config** control.

Stepping into **I/O config**, we see the FPGA communication VI, **Manual Send To**, being called on Figure 28. And a values of **I/O config** as an array is sent to the CED telling it to start grabbing registers.

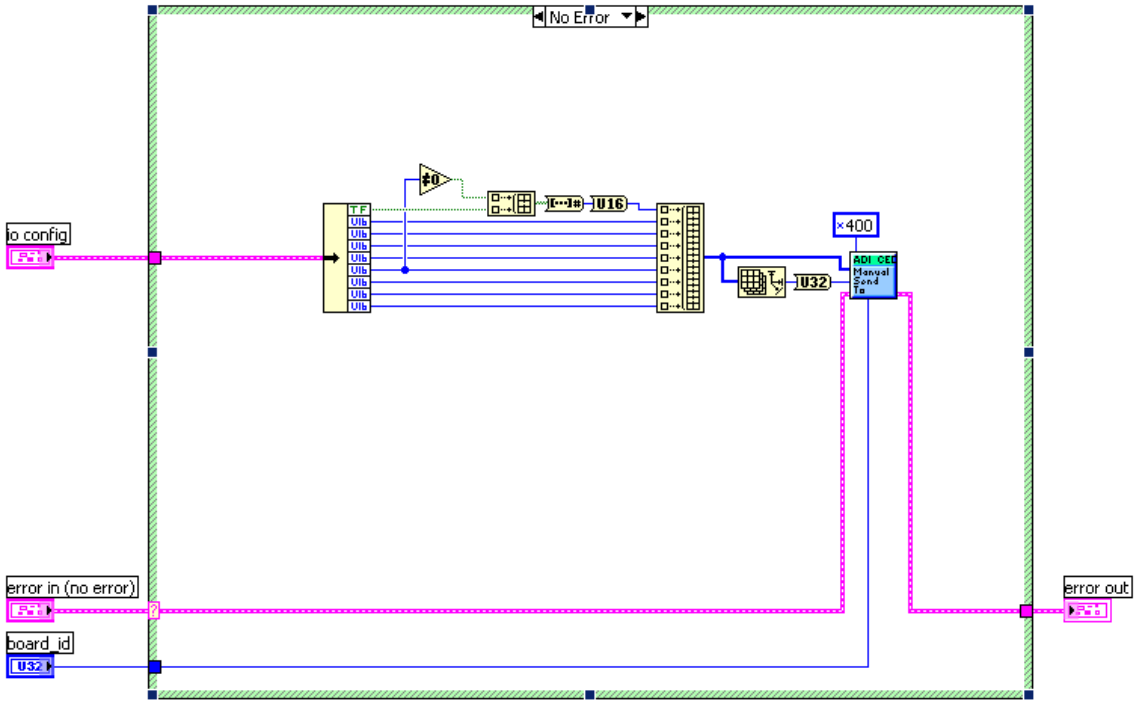


Figure 81 - **Simple Write**

Figure 28 also shows the VI, **Simple Write** being called. As shown in Figure 81, **Simple Write** configures the serial I/O circuitry for the CED to burst for the correct length and writes the 24 bit data words contained in data to the AD7280. The **I/O config** parameters are used except for num frames, continuous and num blocks which are over written with the number of data words, false and zero respectively. **Simple Write** calls the SUBVIs **Write** and **I/O config**.

As shown on Figure 83, **write** writes the 24 bit data words contained in the data array to the AD7280 according to the configuration of the serial I/O circuitry of the CED provided in the most recent call to **I/O config** VI using the FPGA communication VI, **Manual Send To**.

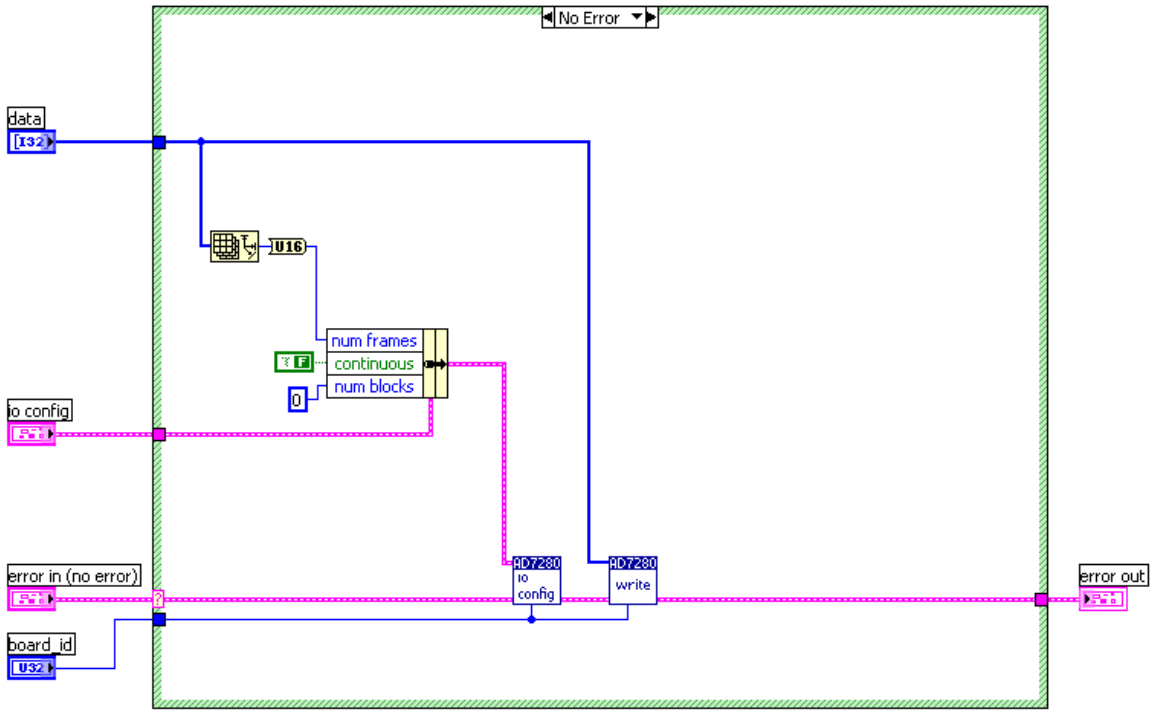


Figure 82 -– Simple write

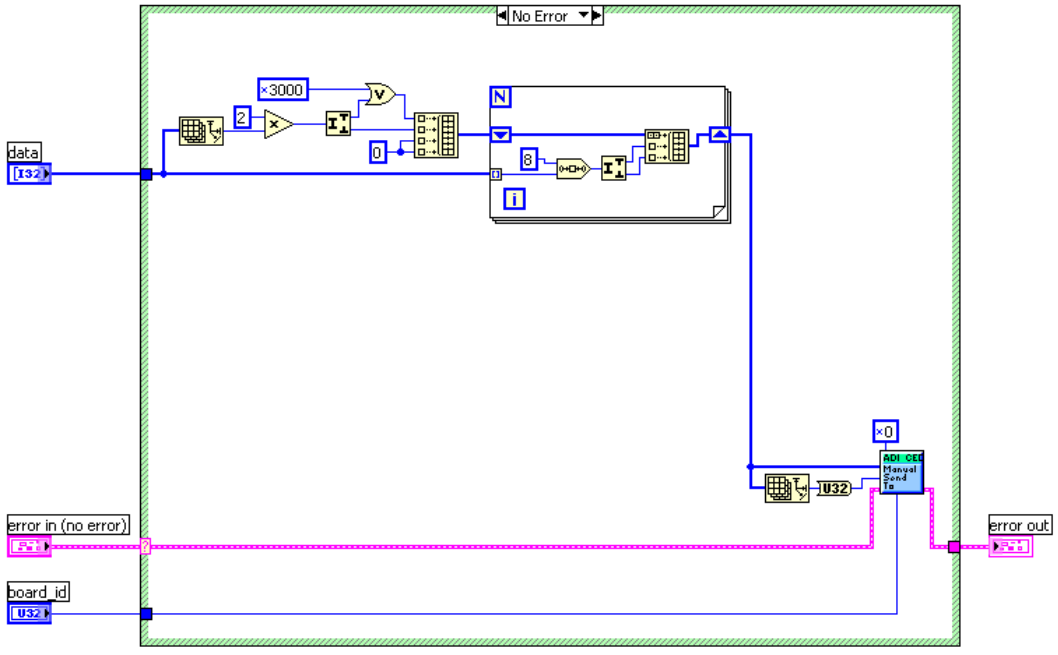


Figure 83 - **write**

After the CED is prepared for data upload, the user is allowed to choose to do a few things: 1) Read and Write certain registers, 2) Autoconfig the Alert condition, 3) Autorun and show the boards that are running, or 4) Save the conversion data

Clicking the Write/Read Single Register button will set num to 4. This will call the VI **Read Write Single**, shown as a scope icon in Figure 84.

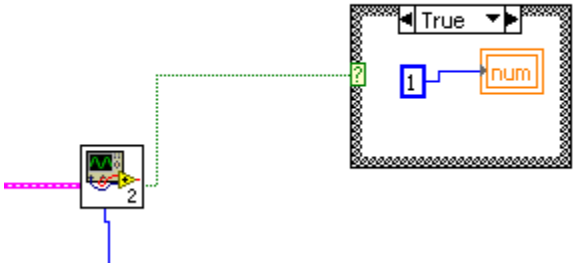


Figure 84 – Calling **Read Write Single**

This VI has 2 buttons indicated by the green TF Booleans shown on Figure 85 and Figure 86. There are also selectors also shown on Figure 85 and Figure 86 for device select and register select.

If the read Boolean shown on Figure 85 is true then the VI **Read Reg** is called to read the data of a specific register and a specific device. The other part of Figure 85 is just bit shifting certain readings to make the readings more user-friendly.

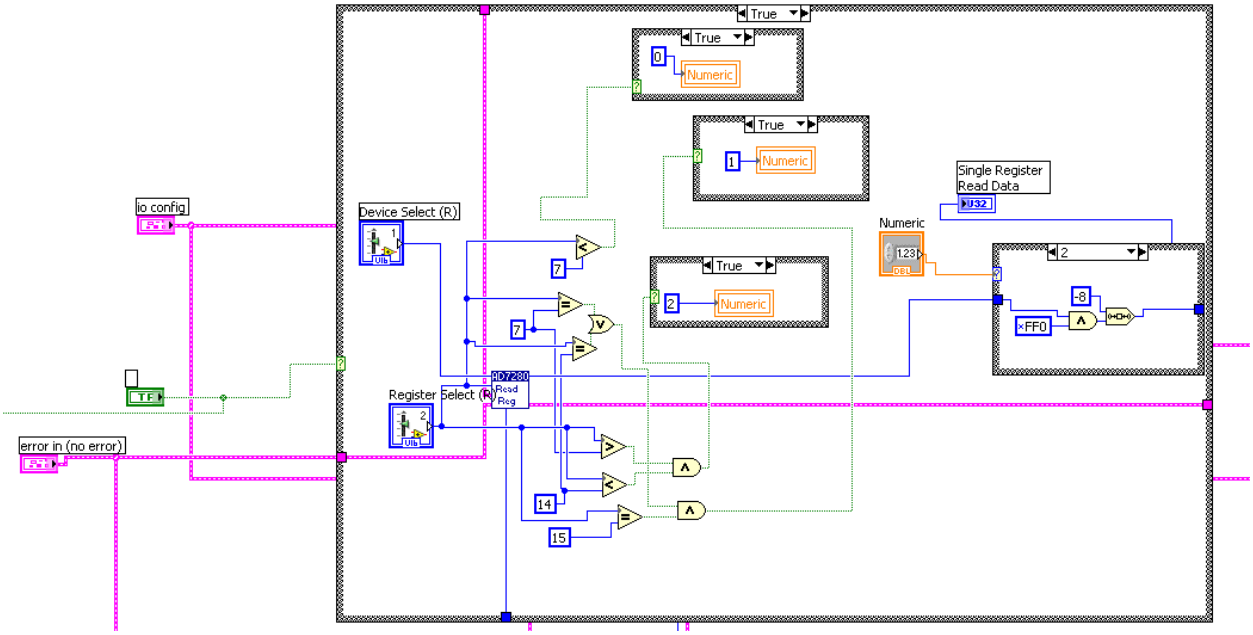


Figure 85 – Read part of **Read Write Single**

If the read Boolean shown on Figure 86 is true then the VI **Write Reg** is called to read the data of a specific register and a specific device. This VI exits after a **write** is performed.

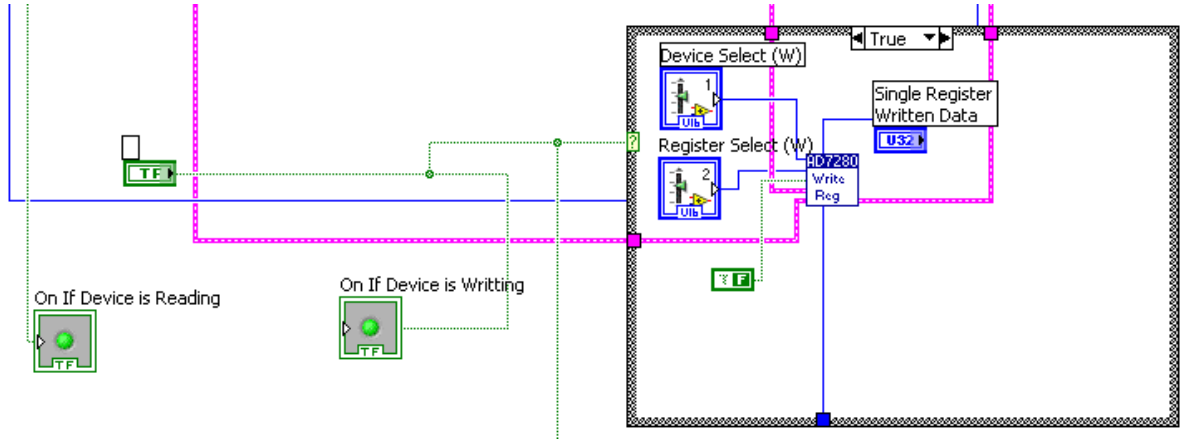


Figure 86 – Write part of **Read Write Single**

Stepping into **Write Reg** on Figure 87, we see that this VI just writes a 24-bit word array with address select, device select, and data to the subVI **Simple Write**.

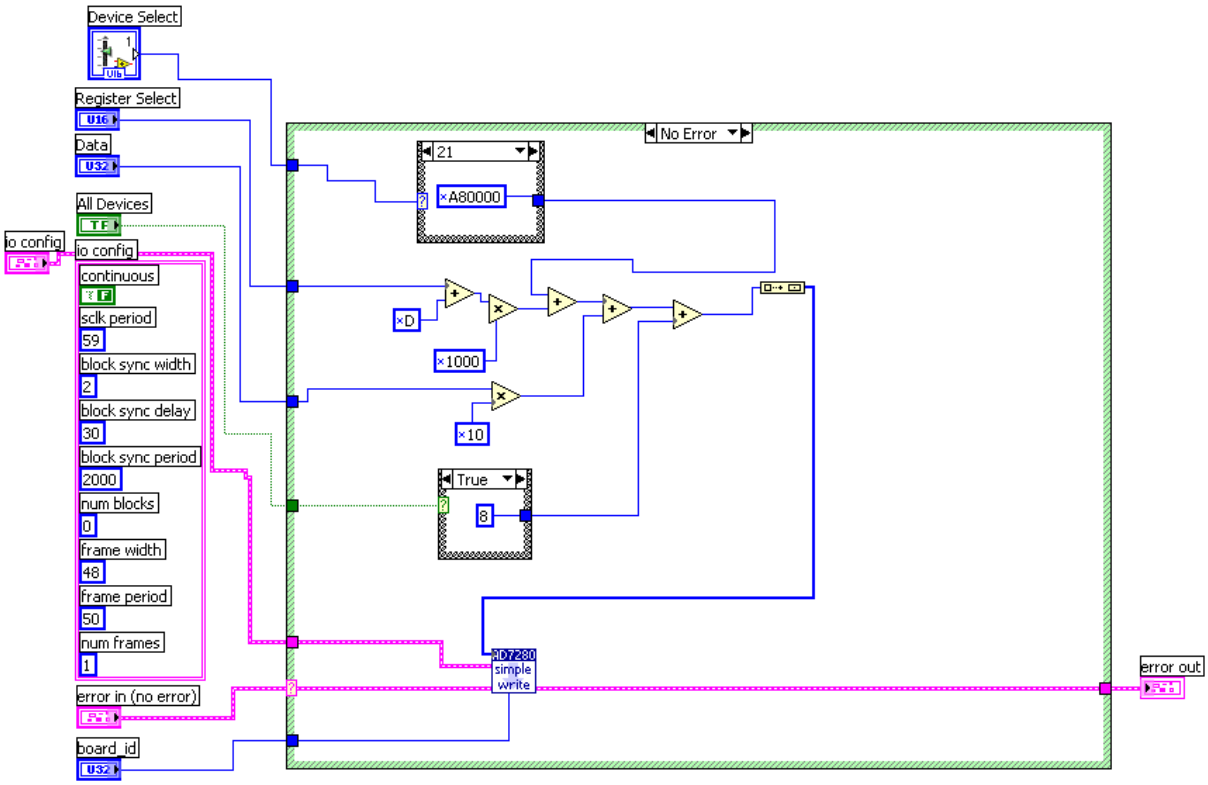


Figure 87 – **Write Reg**

Stepping into **Read Reg** on Figure 88, we see that this VI just writes a 24-bit word array with address select, device select, and a few bits that configure the device to return data, to the subVI **Simple Write**. The returned data is then acquired by calling the SUBVI **simple read**.

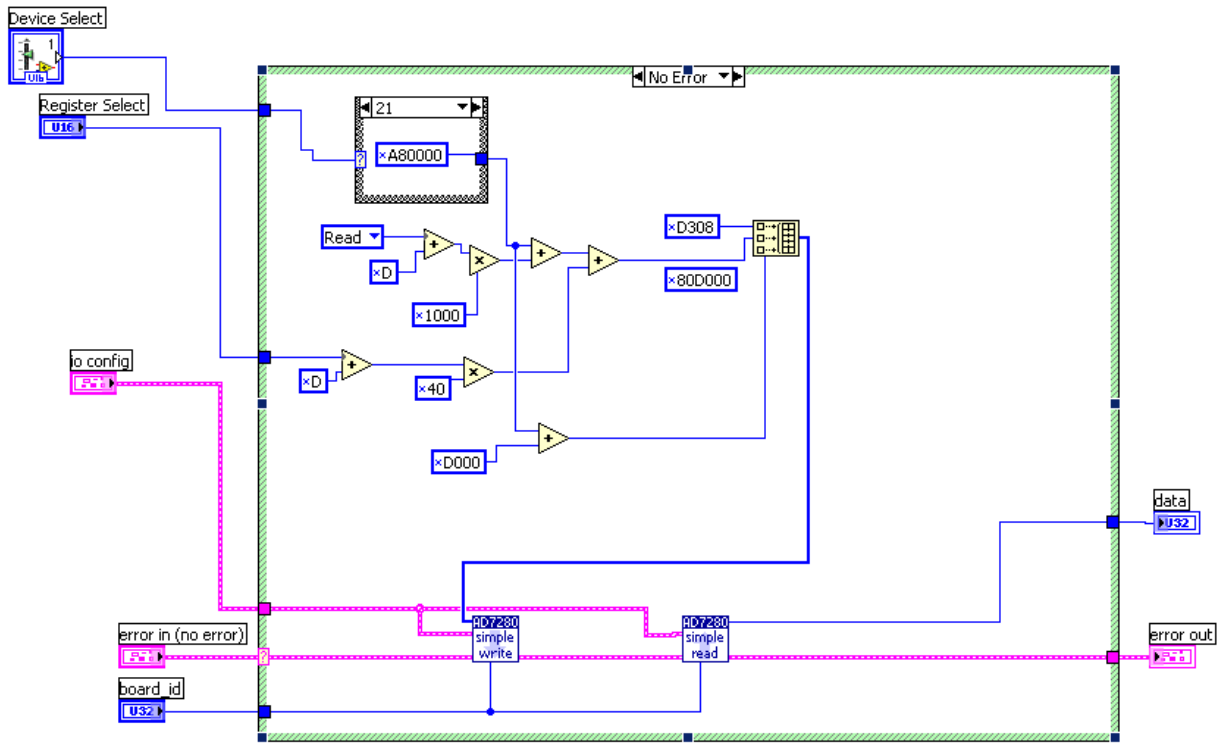


Figure 88 – **Read Reg**

Simple Read, shown in Figure 89, configures the serial I/O circuitry of the CED to read a single 24 bit data words the AD7280 by calling **I/O config**, and start read and then executes the read by calling the SUBVI, **upload**. The **I/O config** parameters are used except for num frames, continuous and num blocks which are over written with one, false and zero respectively.

Upload, shown on Figure 90, **upload**s the number of 24 bit words specified by **upload** size from the FIFO on the CED. Buffer used gives how many words are left in the FIFO after the **upload**. The FIFO size is 1048576 words. It calls the FPGA commands **Manual Send To** and **Manual Received From**. These two FPGA SUBVI performs similar functions as serial I/O with Master Send Slave Receive and Master Receive Slave Send.

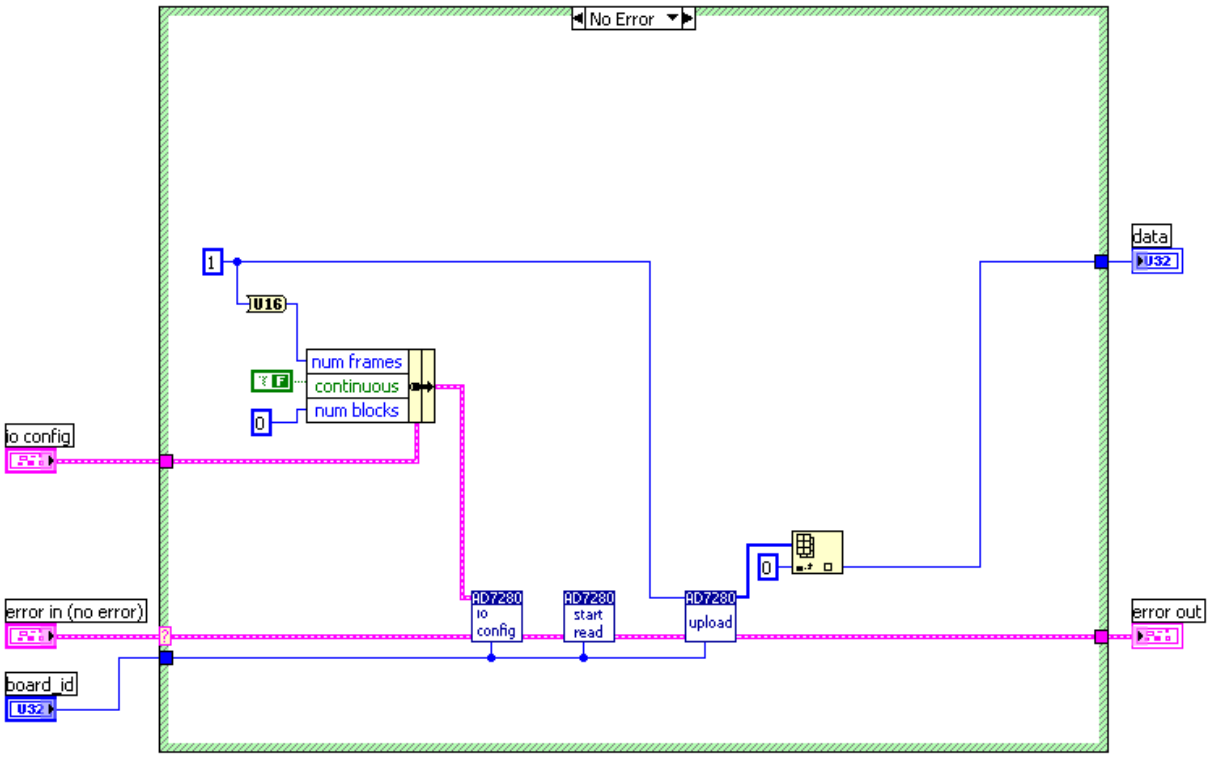


Figure 89 – **Simple Read**

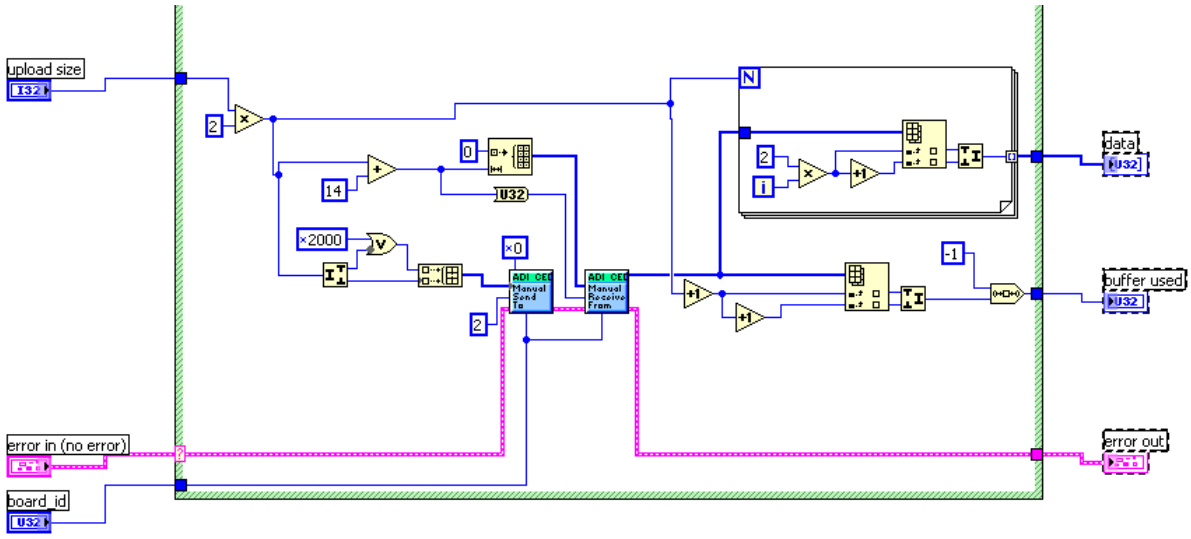


Figure 90 – **Upload**

It is recommended that **Write Reg** and **Read Reg** and all their SUBVIs are left unchanged.

After **Read Write Single** finishes executing, it sets a finished flag which sets num to 1 on figure 33 allowing the user to choose other things to do.

If the user clicks on Autoconfig Registers, num gets set to 6 and the sequence of codes on Figure 91 is executed.

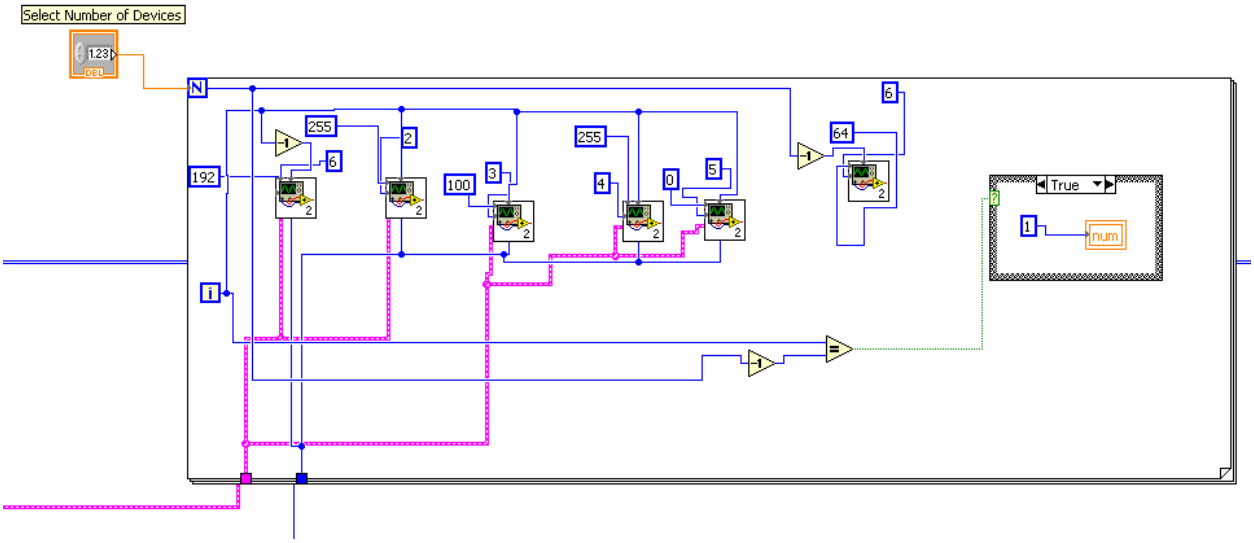


Figure 91 – Autoconfig loop

This sequence of codes is a for-loop that iterates device select from device 0 to device N where N is selected by the user stored in the Numeric Select Number of Devices. In each iteration, the registers under voltage, and alert are configured to be 2.6 volts and ON respectively. The proper way to configure alert is set 11 to the 7th and 6th bit respectively for all devices except the last slave device on the daisy chain. Set 01 to the 7th and 6th bit for the last slave device on the daisy chain. When the loop is finished 1 is set to num so that the user can do other things.

If the user clicks Autorun, the Autorun code activates and num is set to 2 periodically. As this happens, the subVI **upload** is called continuously shown in Figure 92. Thus, conversion data is uploaded continuously from the AD7280s.

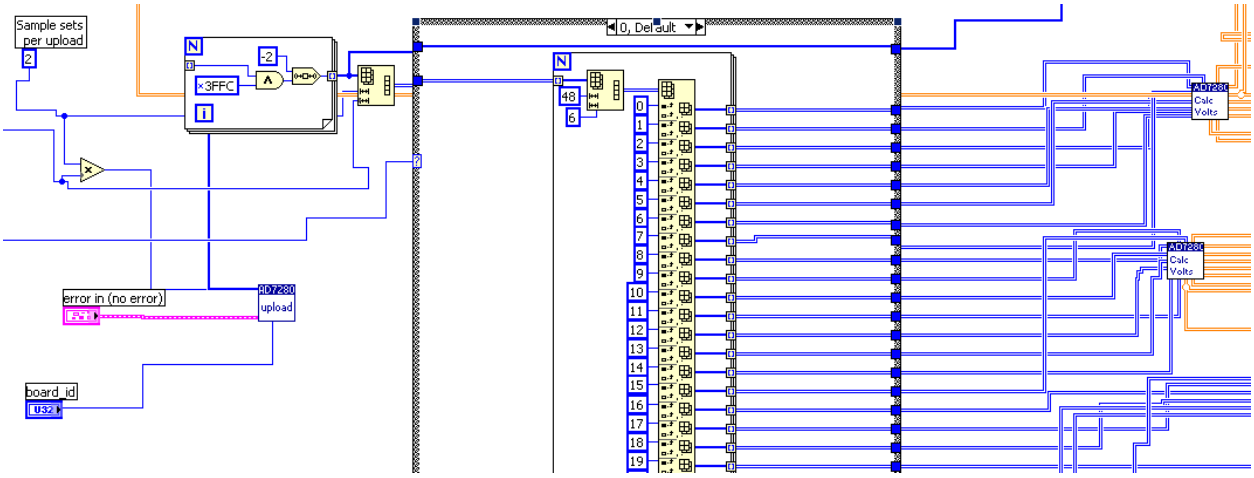


Figure 92 – **Upload** data and place data into array

The output of **upload** is parsed so that the codes from the AD7280s are stored in a 2 dimension array. This array is shown in the middle of Figure 92. The row index of this array has this pattern in codes: Row0-Device 0 Voltage Inputs, Row1- Device 0 Temperature Inputs, Row2- Device 1 Voltage Inputs, Row3- Device 1 Temperature Inputs, Row4- Device 2 Voltage Inputs, Row5- Device 2 Temperature Inputs, and so on. The column index of this array contains 6 elements, each element represent the data of one cell. Finally, this data gets passed onto the SUBVI **Calc Volts,** shown on the right side of Figure 92.

An important thing to note is the number 2 on the left hand side. This is the Sample sets per **upload**. Increasing this variable will allow for more samples being uploaded at each instance of the **upload**. This is only to be done when there are only a few devices (around 4) connected and consequently the number of frames is lowered to 48 (for 4 devices). Increasing this when having many devices in daisy chain will cause the chip to react slowly.

Stepping into **Calc Volts** in Figure 93, we see that simple algebra is used to convert the input codes and output voltage values and temperature values. Each **Calc Volts** can handle 4 voltage code inputs and 4 temperature code inputs.

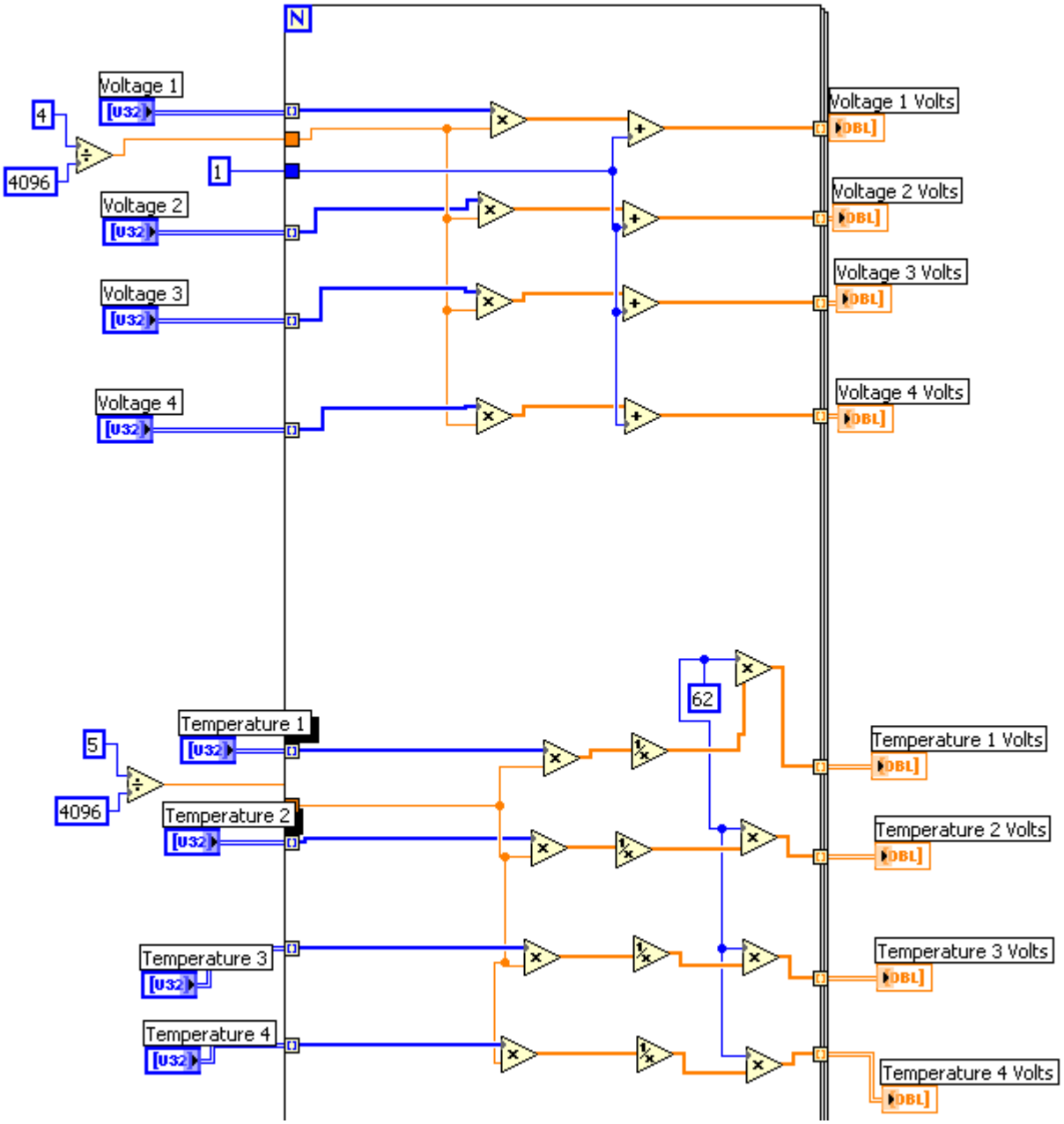


Figure 93 – Calculate voltages and temperatures from code

Lastly, if the user clicks the Save All Converted Data button, num will be set to 100. All conversion data is appended into a 2 dimension array and is then written to excel as shown in Figure 94.

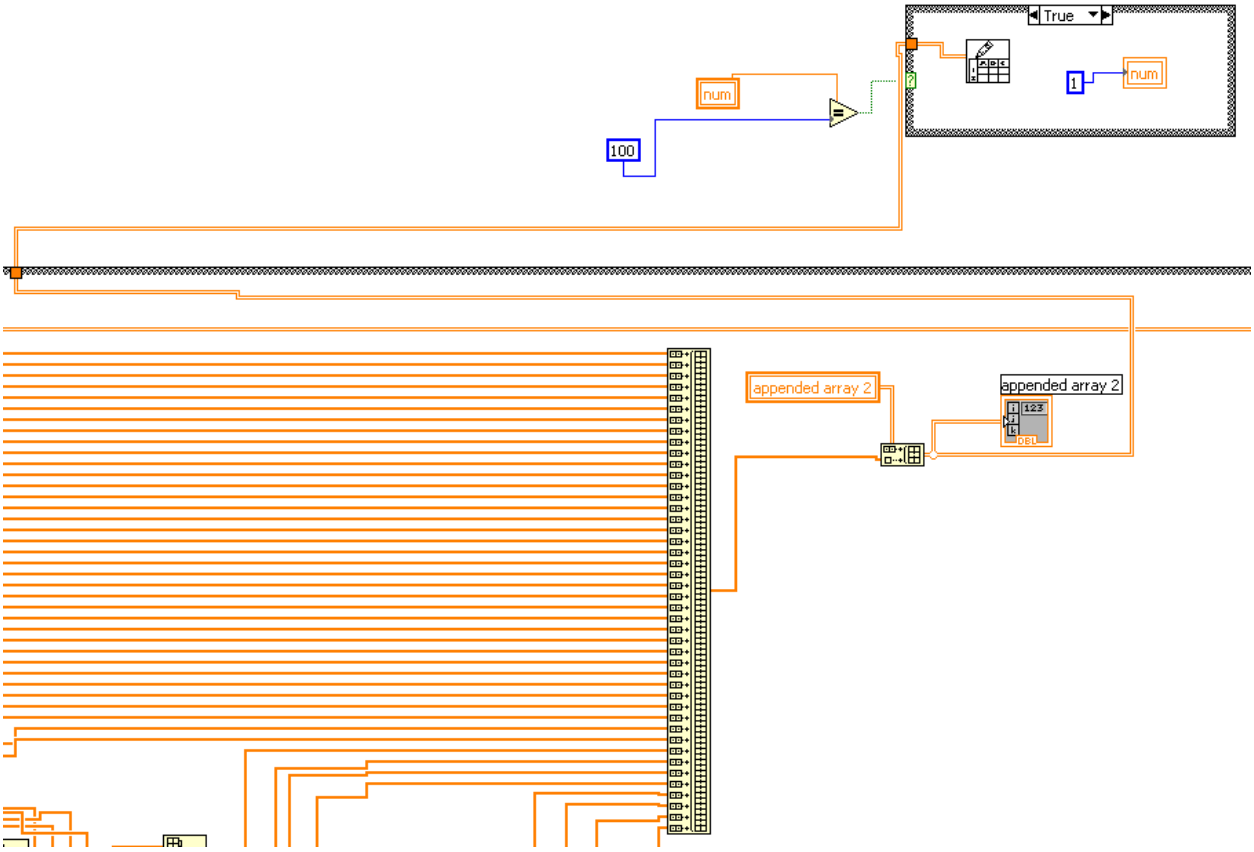


Figure 94 – Append all data and save

After the data is saved, num is set back to 1 again to allow the user to do other things.

6.3. DEMO Board PCB Design

Given that the DEMO board was an extension of the EVAL board, our DEMO board PCB layout was implemented by starting with the layout for the EVAL board. The digital logic portion and the first two AD7280s on the DEMO board are laid out exactly the same as they were on the EVAL board. Subsequent sets of two AD7280s copy that layout, and are placed in repeating patterns on the board.

The actual work for the layout was outsourced to Litho Circuits, because access to layout software licenses was unavailable from ADI. Consultations between our group members and the Litho employees took place frequently, however, to guarantee that certain components, particularly connectors, were in the correct places. Additionally, these consultations allowed us to update Litho about schematic changes, which could not be sent electronically due to incompatible software versions.

After the schematic and layout for the DEMO board were completed, the board was manufactured and assembled on a schedule of eight working days. During this time, a *temporary driver board* (TDB) was made from a connector to interface with the DEMO board, which had wires hanging off

of it, and plugging into a breadboard. Information about testing the DEMO board can be found in Section 9.6, which details the steps we undertook to guarantee correct functionality.

6.4. DEMO Board Troubleshooting

The demonstration board PCB was received in the afternoon of October fourteenth. When it arrived, there were 30 decoupling capacitors missing due to a shipping error. The value of the capacitors is ten microfarads. The capacitors were received the next morning and were manually soldered on. An image of the completed DEMO board can be seen in Figure 95. As the image shows, the AD7280s are not present. This is because they are not yet inserted, but are to be held down by customized clamps used for the AD7280 in previous applications.

The test procedure that was performed on the demonstration board can be seen in Section 9.6. The first step was to verify that the TDB was operational. The appropriate pins of the TDB were inserted into a bread board complete with a resistor string to mimic the same test that was done with the AD7280 Evaluation boards, detailed in Section 6.1.4.

A voltage of twenty volts was applied to the TDB. The voltage across each of the resistors was measured and the matched to the corresponding pins on the 64-pin connector to verify it was soldered correctly. This test was successful as each of the resistors yielded the same reading across them as the 64-pin connector.

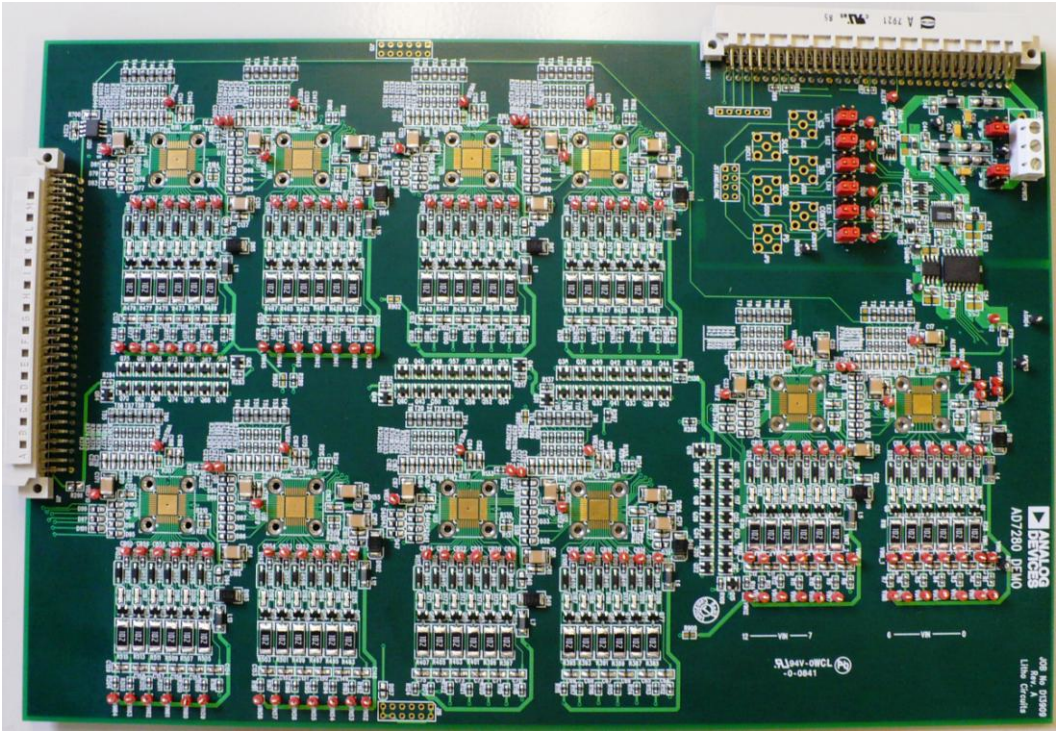


Figure 95 – A picture of the DEMO board without any chips inserted into the clamps.

The next step was to insert two of the AD7280s into the sockets of the demonstration board to simulate a single AD7280 Evaluation board with two AD7280s in series.

The procedure in Section 9.6, step three, was followed. The same voltage from the previous test of twenty volts was used to start. The voltages were successfully read. The voltage was increased in five-volt increments and at each increment the voltages were read correctly. This step was a success and a AD7280 Evaluation board had been successfully simulated.

Next, the demonstration board was to be reconfigured according to the test procedure in Section 9.6, step five. This would simulate two AD7280 Evaluations boards in series, as described in Section 6.1.1. The reason for this test was to verify multiple AD7280s could work in series as they are intended to which was proved at an earlier time. It was the next logical step in the test procedure due to the fact that when the current mirror circuit was first inserted in the system as described in Section 6.1.3, issues arose because the implications of their insertion was unknown. This test was designed to prevent that from happening again. Unfortunately, due to time constraints and supervisory issues, this test was not performed.

The next step that was taken in testing the demonstration board was inserting four AD7280s which simulates two AD7280 Evaluation boards in parallel, as detailed in Section 6.1.3. This is described in Section 9.6, step seven. At this point, it was discovered that a change which had occurred in our copy of the schematics had never been applied to the schematic that was sent for manufacture. There was a floating node on the DEMO board as a result, which was simple to fix by soldering a wire between two points on the board.

The power supplies were configured to apply twenty volts as the Vdd. This means ten volts across each chip. The complete quad-rail supply had to be configured as well to account for the current mirror circuit operating three volts outside of ground and Vdd. The rails were 0V, 3V, 10V, 20V, and 23V to represent GND-3, GND, Vdd, Vdd/2, Vdd, and Vdd+3, respectively. The power was applied and code was downloaded. When reading voltages, the first two chips read accurate voltages and the second two chips read nothing at all, as shown in Figure 96.

When this occurred, a digital multimeter was used to verify that the correct voltages were seen across known components. When the voltage across the current mirror circuit was probed, it was found that one of the biasing transistors had a voltage of 0.3 volts across it while the other had 0.6 volts across it. As explained in Section 6.1.2, these voltages need to be the same for the circuit to work. At those points our efforts went into addressing that problem but we were unsure if we were actually addressing the real problem or merely treating symptoms of a problem. The ground of the current mirrors are shifted by 0.3 volts when the code to the board.

We changed the zener diodes from 30V to 20V diodes in hopes of duplicating our prototype which we had working before. Unfortunately, the results remained the same. Then, after two days of testing, without making any substantive progress, the current mirrors suddenly seemed to behave normally. We believe the problem to was caused by loose connection issues, as we had inadvertently bumped the wires on the TDB just before the system started working. Figure 97 shows a screen capture of when we had four devices working in parallel.

Due to the time constraints we were under, we unfortunately were not able to test the system with a full ten chip setup. As such, we cannot absolutely guarantee that it works, but given that the schematic from that point forth is a direct copy, we feel very confident that the ten chips would work correctly if given the proper inputs.

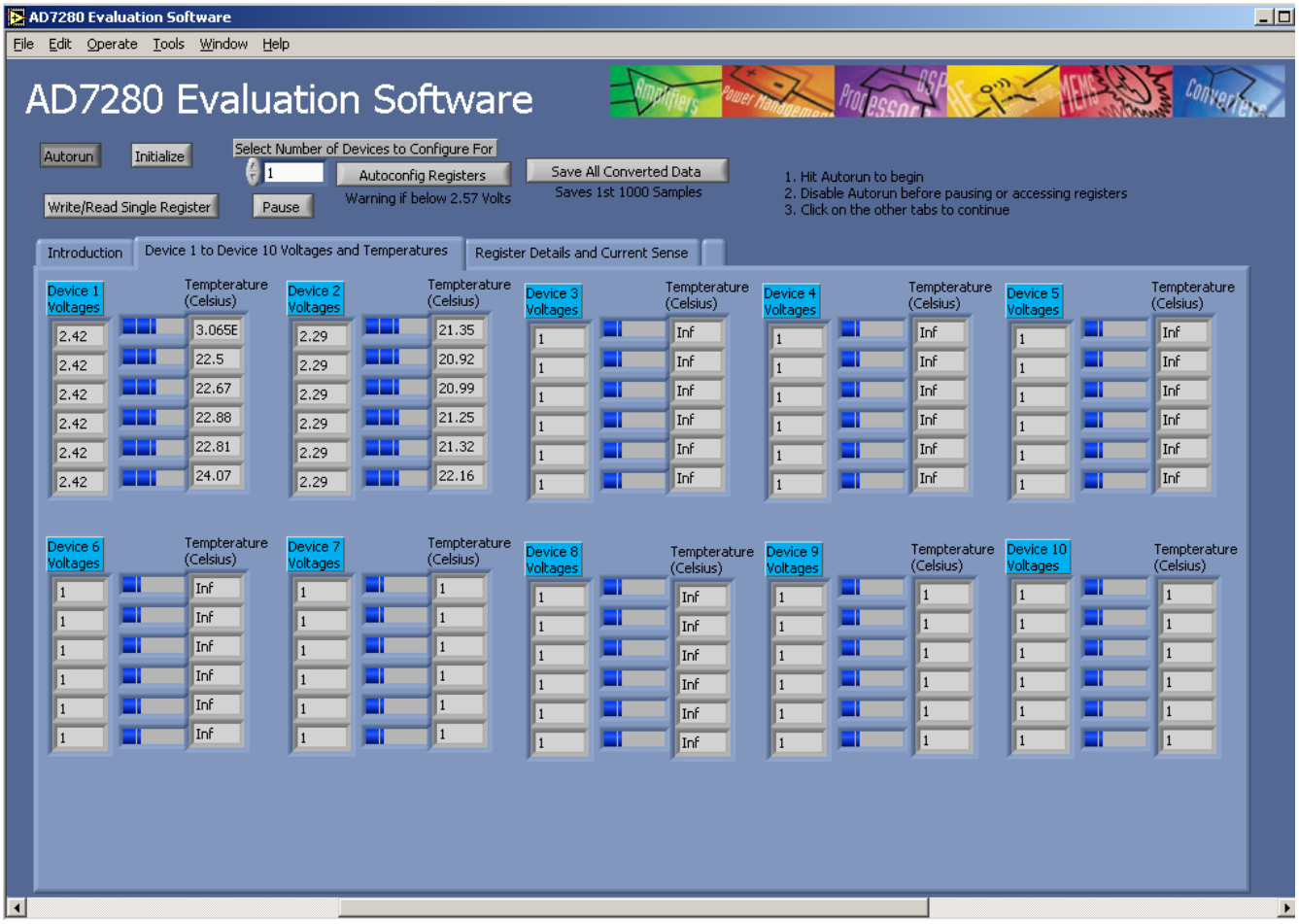


Figure 96 – Screenshot of two out of four boards working

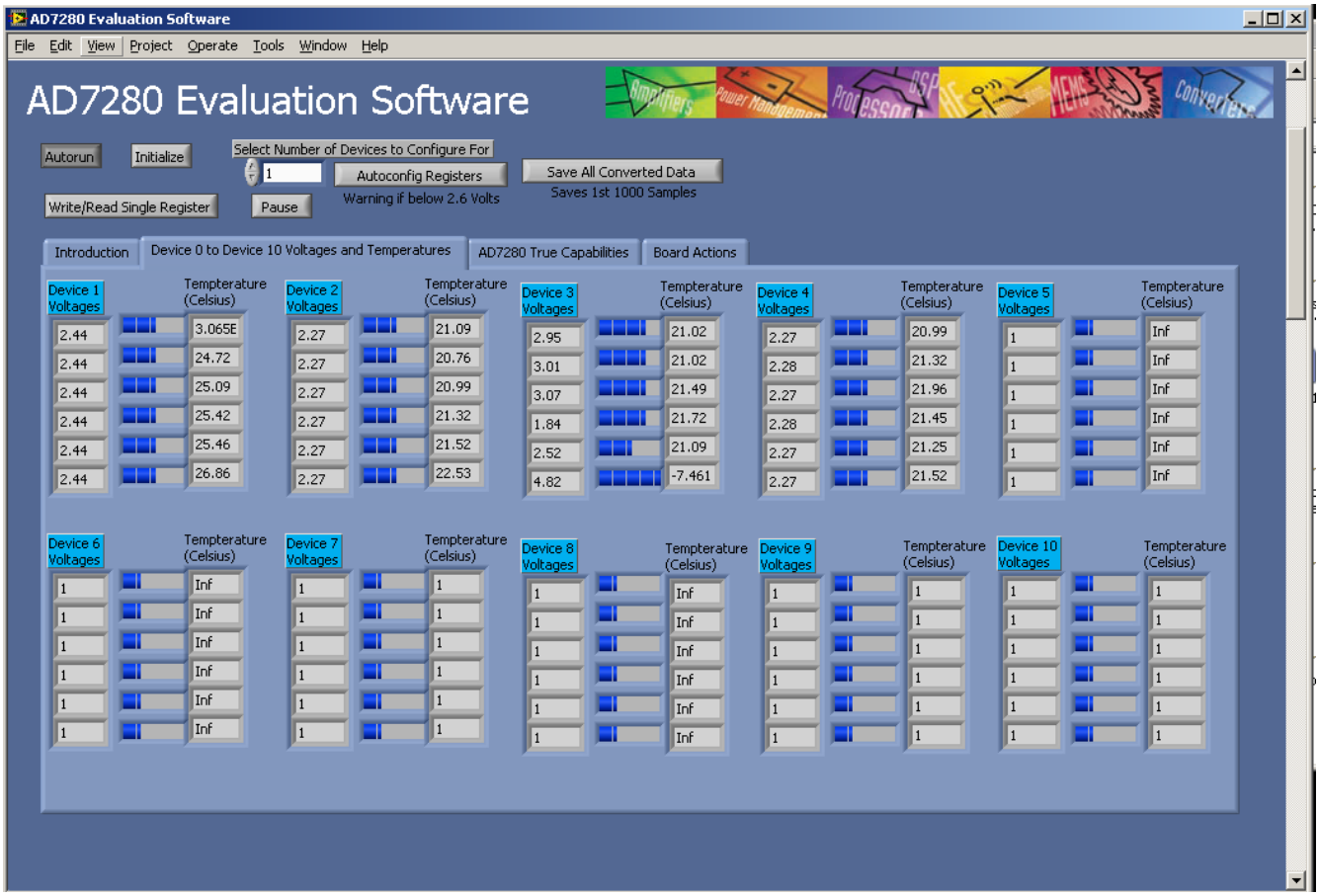


Figure 97 – Screenshot showing all four devices working properly

6.5. Driver Board Build

Building the driver board was not nearly as complicated as building the DEMO board. First of all, the sheer number of components necessary was significantly lower. Second, due to time constraints a PCB was never manufactured. Instead, a strip board was used to speed up development time.

Actually assembling the driver board took a significant amount of time due to the nature of strip board manufacturing. Each stage of the driver board was tested as it was completed, in accordance with our testing procedure which is listed in Section 9.7. We began by attaching the power supply connector to the board, followed by adding the voltage regulators, and finally adding the three resistor networks. The first resistor network was a simple series connection of twelve resistors, each in parallel with a capacitor to help regulate the outputs against any unexpected line fluctuations. The second resistor network was more complicated because it needed to be adjustable. Instead of twelve simple resistors in series, we replaced each of those twelve fixed resistors with a fixed resistor in series with a resistor in parallel with a potentiometer, as shown in Figure 98. The input to the network was a current on the order of a milliamp which we set up by using a current mirror, as shown in Figure 99. We used a constant

current source because we needed to guarantee that when we changed one of the outputs by turning the potentiometer, we would not be influencing the other output voltages.

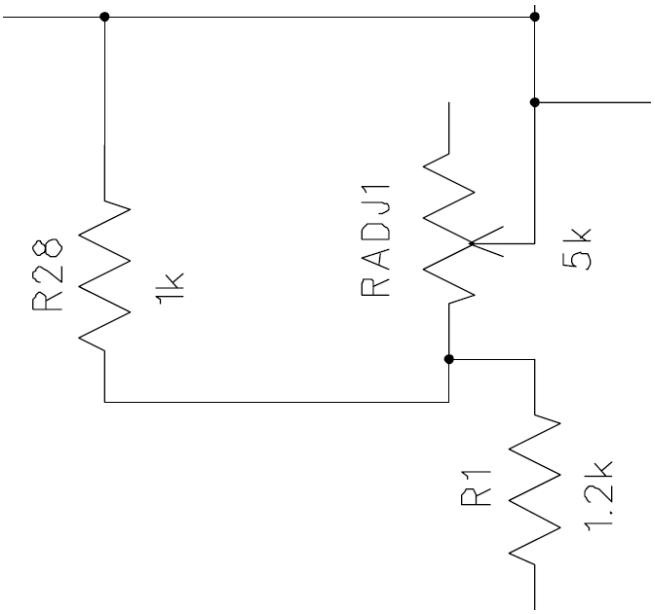


Figure 98 – A schematic representation of the resistor network we set up for the adjustable voltage outputs. As R3 increases, the total resistance increases, leading to a larger voltage drop across the combination of three resistors at constant current.

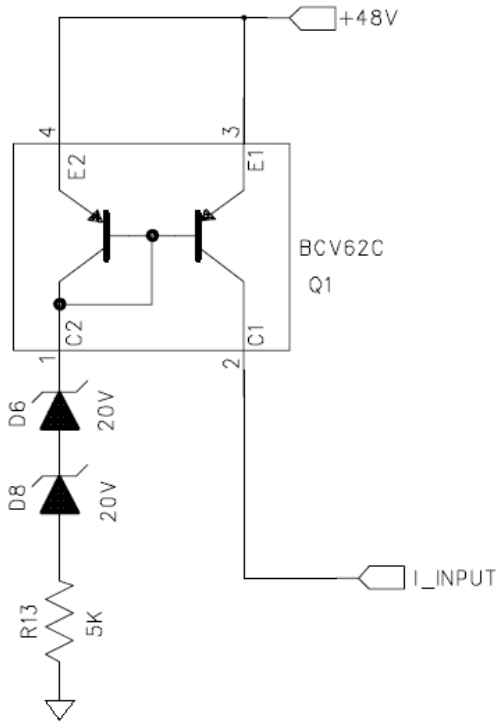


Figure 99 – Current mirror setup used to control the current going through the adjustable resistor network. A constant current was required in order to allow one output to vary without affecting the others.

The current sensing resistor network was the next block to be built. This was the easiest of the three resistor networks, and also the least critical to our project, which is why it was left for the end. As described in Section 5.3, we placed the three resistors in series between +3.3V and GND.

The final stage in assembling the driver board was to insert the buffer opamps and their associated connections and bypass capacitors. This was left for the end because, even though we were using sockets instead of soldering the opamps directly to the strip board, there was some fear that either the plastic socket would melt when the soldering iron came too close by accident, or some other connection would be more difficult to reach as a result of the bypass capacitors.

6.6. Driver Board Troubleshooting

The driver board was built as described in Section 6.5. As we went along, we tested each subsystem. The first block we tested, then, was the power supply and the voltage regulators. After successfully connecting the 48V power supply, we blew up one of the regulators because of a manufacturing error. We realized what we'd done after the fact, but it set us back by several hours.

After successfully rebuilding and testing the voltage regulator circuits, we moved on to the constant voltage output resistor network. This was a simple procedure, and was completed without incident.

Next, we moved on to the adjustable voltage output resistor network. Again, this was completed without incident, as was the current sensing network. When it came time to insert and test the buffers for the circuit, some project members were surprised to learn that the tantalum bypass capacitors we were using are polarized. The resulting puff of smoke was enough to convince the team that we should cut out all of the caps which were inserted improperly, and due to time constraints, just leave those who were already in correctly.

6.7. Interfacing the Driver Board with the EVAL Board

The final test of whether or not the driver board worked with the larger system was to attach the two using the 64-pin connectors. After the rework was performed on the DEMO board, though, the decision was made by our managers at ADI that the EVAL board would have to suffice for the upcoming trade show the Monday after our project finished. As such, we tested the driver board on a single EVAL board with two chips instead of a DEMO board with ten chips. We did this by attaching a second 64-pin connector to the one connected on the driver board, and soldering wires directly to the secondary connector. These wires were then screwed into the connectors on the EVAL board. When we applied power to the driver board, the EVAL board responded exactly as we had hoped. This validated the driver board to the extent that ADI required.

7. Recommendations/Future work

There are several recommendations we have regarding both engineering techniques that we learned and future work. There are some improvements that can be made to our system in both hardware and software that would benefit the demonstration for ADI. Additionally, there are some mistakes that were made during the course of the project that we would like to pass on to future groups in the hope that they do not make the same mistakes.

A very useful and important technique that we learned is to break down a system into smaller subsystems, or blocks, and verify their operation before inserting them into the larger system. It is strongly recommended to do so on as small a level as possible. We learned this lesson at more than one time during this project. The best example of this is when the current mirrors were initially built and inserted into the parallel system. When this was done the voltage across the system was too high and the current mirror circuit was destroyed, as described in Section 6.1.3. Some time was wasted in trying to determine what went wrong. Had the current mirror circuit been properly tested and built up on verified tests before being inserted into the system, the problem would have been avoided.

We also learned that when prototyping high frequency equipment using small signals, the environment needs to be noise free. This was a problem twice during our project. One occurrence was caused by an external hard drive that was connected through a USB to the computer running the evaluation software. It caused the current mirror circuit to propagate noisy signals and the software to read noisy voltages. It was determined that the reason for the noise was the external hard drive. The hard drive was unplugged from the USB and the noise on the oscilloscope vanished. When plugged back in, the noise returned. This phenomenon was verified several times. Two possible reasons for this were determined to be the long wires that were used in the preliminary system to connect different subsystems, and the fact that the USB hub was communicating with both the external hard drive and the CED board, so crosstalk was a possibility we had not thought of. Since we were using such small signals, the noise was enough to give bad readings. We recommend using wires that are as short as possible to reduce noise, and any unnecessary electronic devices or peripheral hardware should be removed from the area, particularly devices connected to the computer that is running the test.

Although the hardware performed as desired, there are still some improvements that can be made. First, the DEMO board has not yet been fully tested. It has been tested for up to four AD7280s but is capable of handling ten. It is recommended that the board be tested for full functionality. Connecting two DEMO boards together has also not been tested yet. Also, the change that was mentioned in Section 6.4 regarding fixing a floating node needs to be implemented. A second revision with these changes made would improve the DEMO board. Additionally, the second revision of the DEMO board should include additional test points for troubleshooting and jumpers instead of 0Ω links to isolate different blocks of the board. Next, while the driver board worked, it was not used for what was

intended. It was intended to drive the DEMO board but instead was used to drive the EVAL board due to time constraints. It is recommended to create a PCB from the driver board schematic and test it with the DEMO board. This would also eliminate much of the noise that can be picked up on the long wires, as was stated previously. One change that should be made to the driver board is the addition of a power switch on the back of the box. Currently, the only way to turn off the system is to remove the power cord. While that is usually fine, in the case of an electrical fire developing a switch would be faster to activate than pulling a cord out of the box.

If more time was available, a second revision of the DEMO board would be made and a PCB of the driver board would be made. The ultimate goal would be to have that system operational. Finally, it is recommended that a different thermistor be placed on the DEMO board's second revision. The current thermistor has a wide range of error, up to two degrees Celsius. A more accurate thermistor would improve the board's appeal.

There are also several improvements that can be made to the software to make it more user friendly. One improvement would be to create the ability to manipulate the voltage or temperature registers using decimal numbers as opposed binary numbers. Also, in the future, the alert output should be made available to be read in software as opposed to just outputting to an LED as it is now. Also, the software was never tested for more than four AD7280s. This must be done to be sure that it will work with the ten that are on the driver board. For the GUI, it is recommended that a total voltage reading be displayed. This would show that the voltage across the resistor chain remains the same regardless of variance. Additionally, an average temperature reading should be added. This would compensate for the thermistors having a high margin of error.

If what is mentioned in these recommendations is done, the system will be as close to the system we intended as possible. If time had not become a factor late in the project they would have been included in our project. Additionally, the engineering techniques described are very useful and a major part of what was taken away from this project.

8. Conclusions

We ended up creating two versions of the GUI software, one for the EVAL Board and the other for the DEMO Board. The DEMO Board had not been tested to work stably before we could leave so the presentation coming up will be done with the EVAL Board. The presentation in November, 2008 will be done with the DEMO Board once the DEMO Board has been tested fully and modified for errors.

The DEMO Board GUI was able to display temperature and voltage readings for ten AD7280s as well as allow user access to all the control registers. The GUI also showed the value of all the control registers, the current sense chip output and the alert condition.

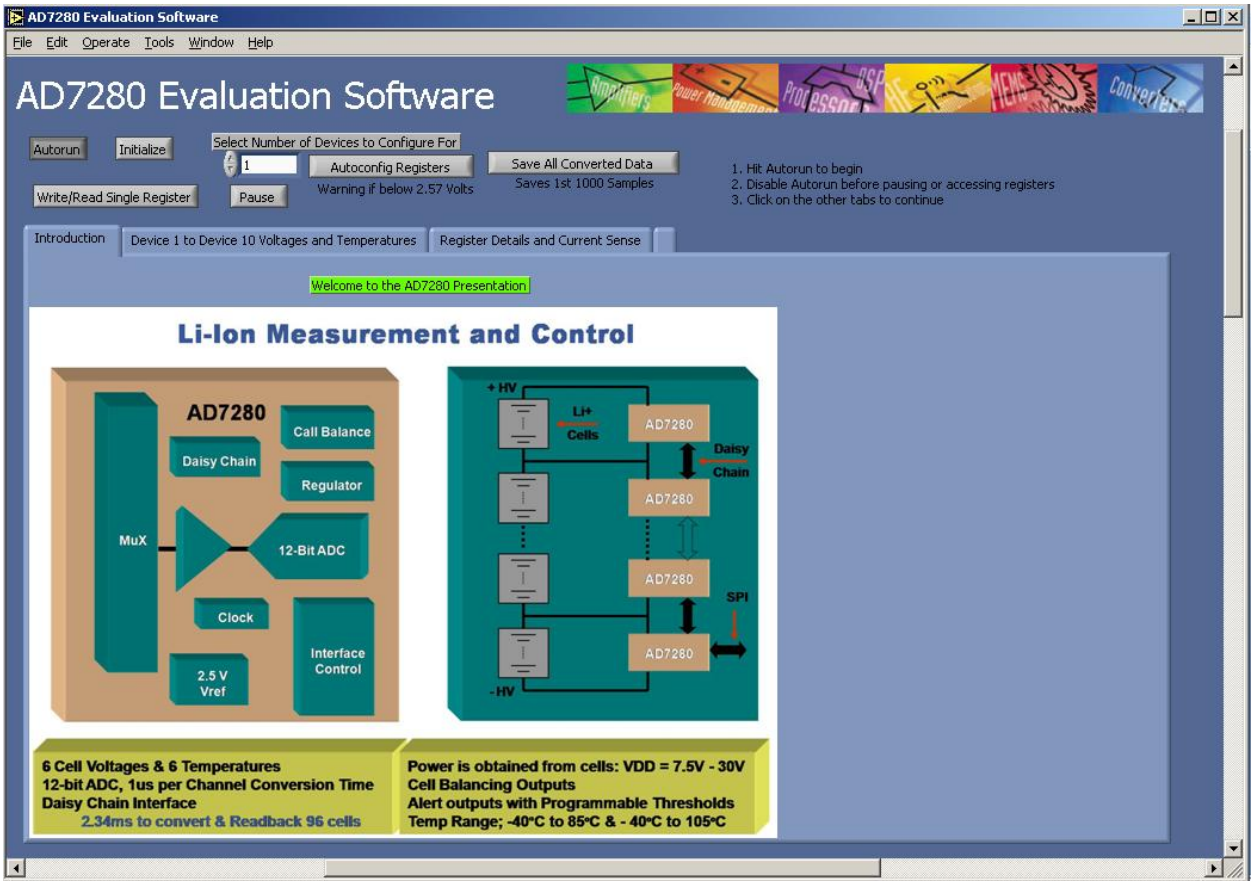


Figure 100 – Finalized Front Page

Figure 100 shows the front page of the GUI, which shows a captivating image. This is what the audience sees first.

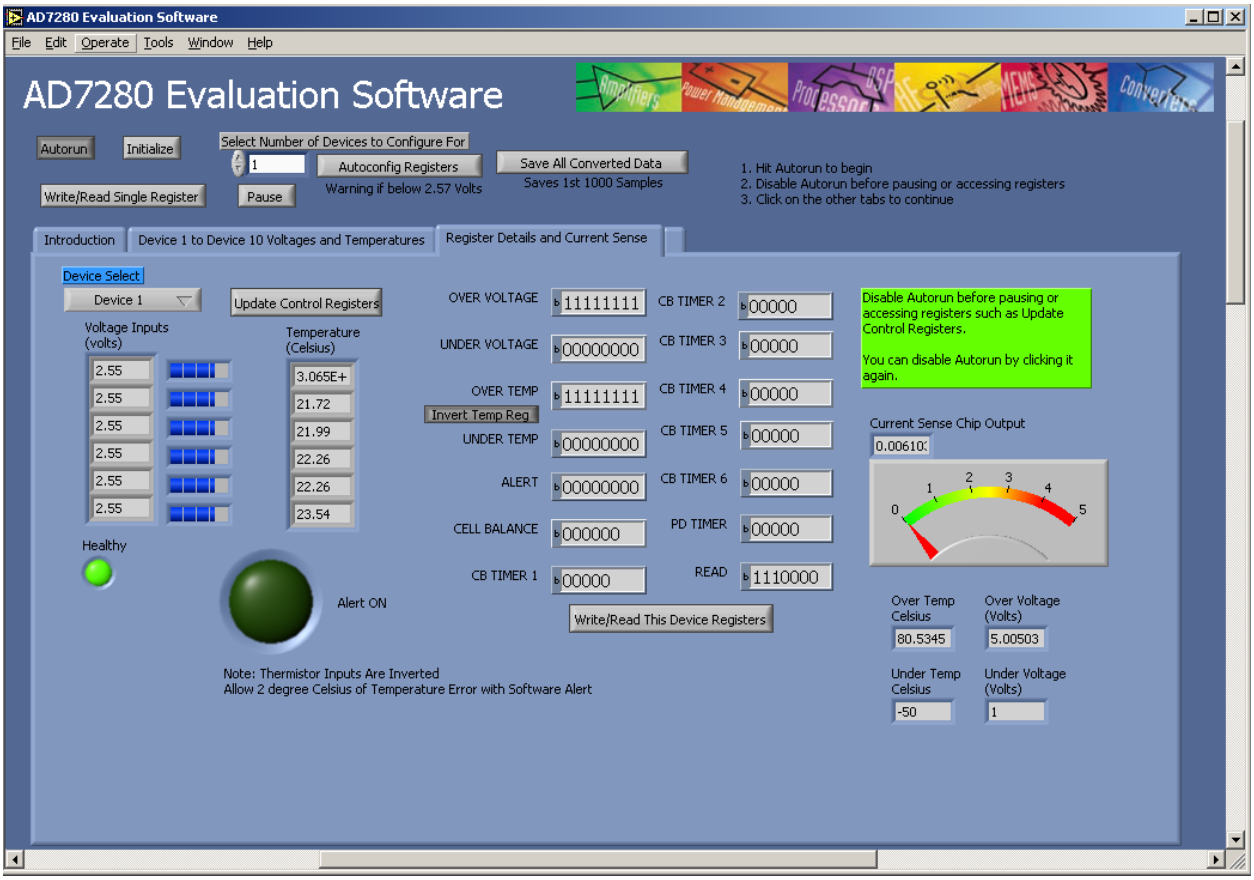


Figure 101 - DEMO Board Capabilities

Figure 101 shows the AD7280 device capabilities in detail. Shown on Figure 101 is a blue icon that says Device Select. The button below allows the presenter to select different devices on the DEMO Board and have the device data displayed on this screen. The two columns on the left show the voltage and temperature readings from the selected device. The center columns shows the control registers of the selected device and the presenter can toggle the Invert Temp Reg button to adjust the inverted thermistors. Figure 101 also shows two LEDs on the lower left corner indicating if the selected Device is healthy or on alert conditions. The right side of Figure 101 shows the output value of the current sense chip on the DEMO Board.

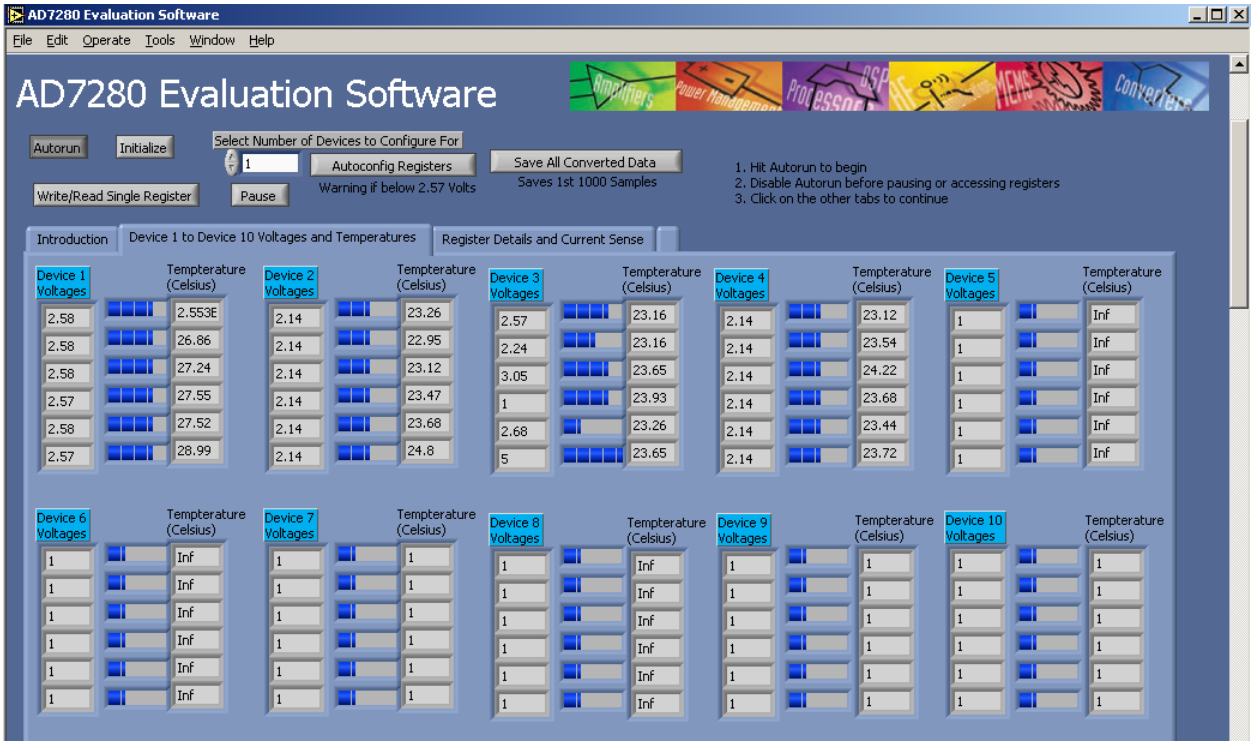


Figure 102 – Screen Showing All Ten Devices

Lastly, Figure 102 shows off the Daisy Chain capability by showing that ten devices on the DEMO Board can be connected together and communicates with each other.

The EVAL Board only has two devices on it so the EVAL Board GUI was program to display temperature and voltage readings for two AD7280s as well as allow user access to all the control registers. The GUI also showed the value of all the control registers, and the alert condition. The EVAL Board does not have not have a current sense chip so the capabilities screen would not show a current sense reading. The DEMO Board and the EVAL Board has the same front page GUI but the other two pages are slightly different.

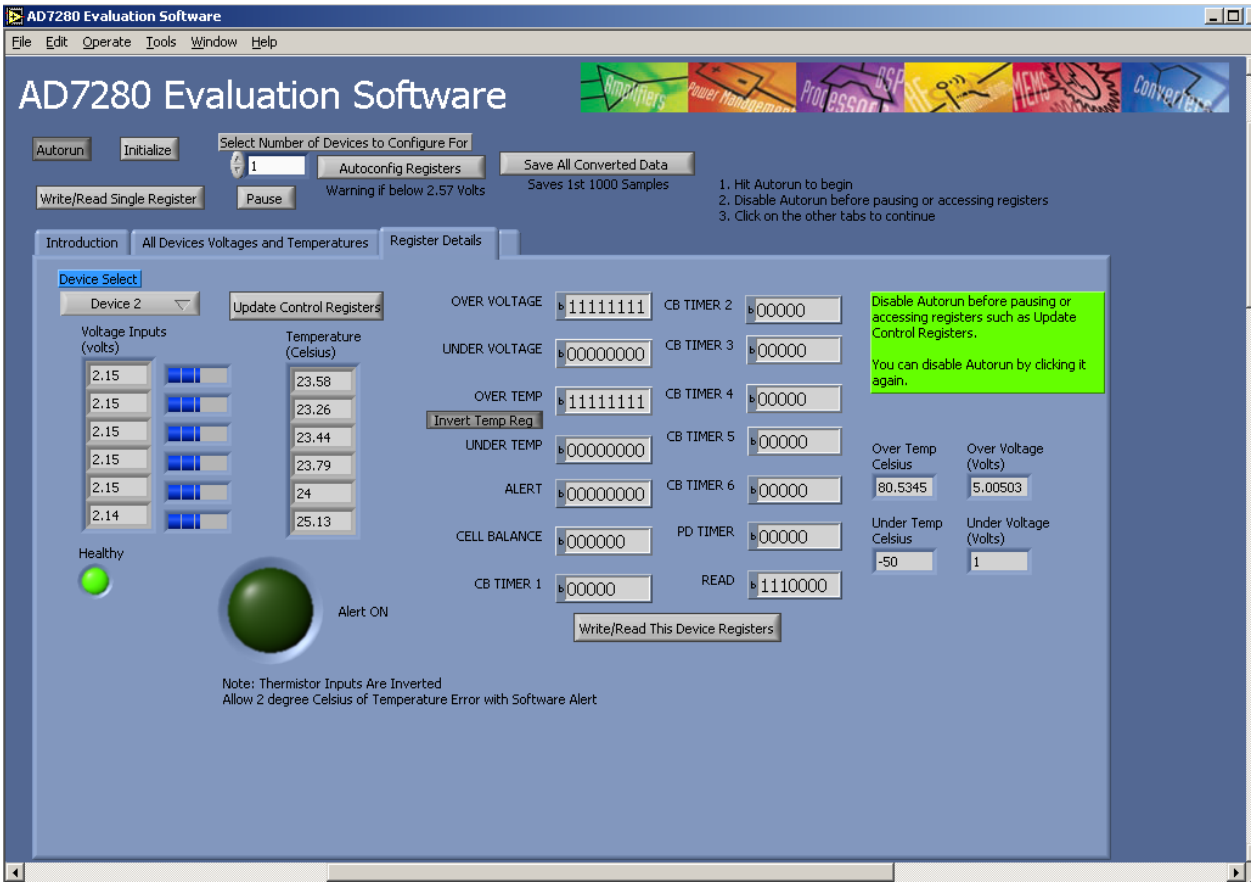


Figure 103 – EVAL Board Capabilities

Figure 103 shows EVAL Board GUI's device capabilities page and it shows everything from the the DEMO Board GUI can except for current sense chip output.

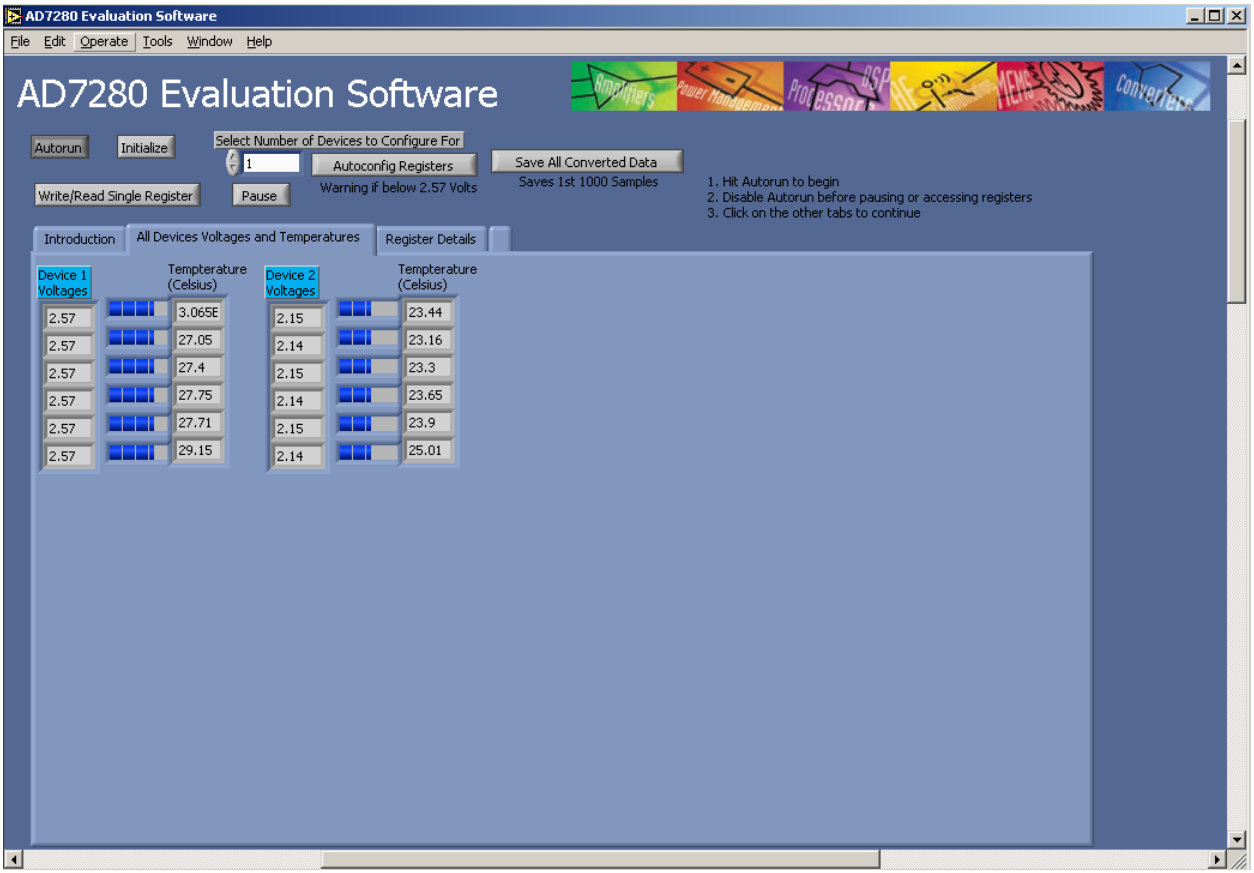


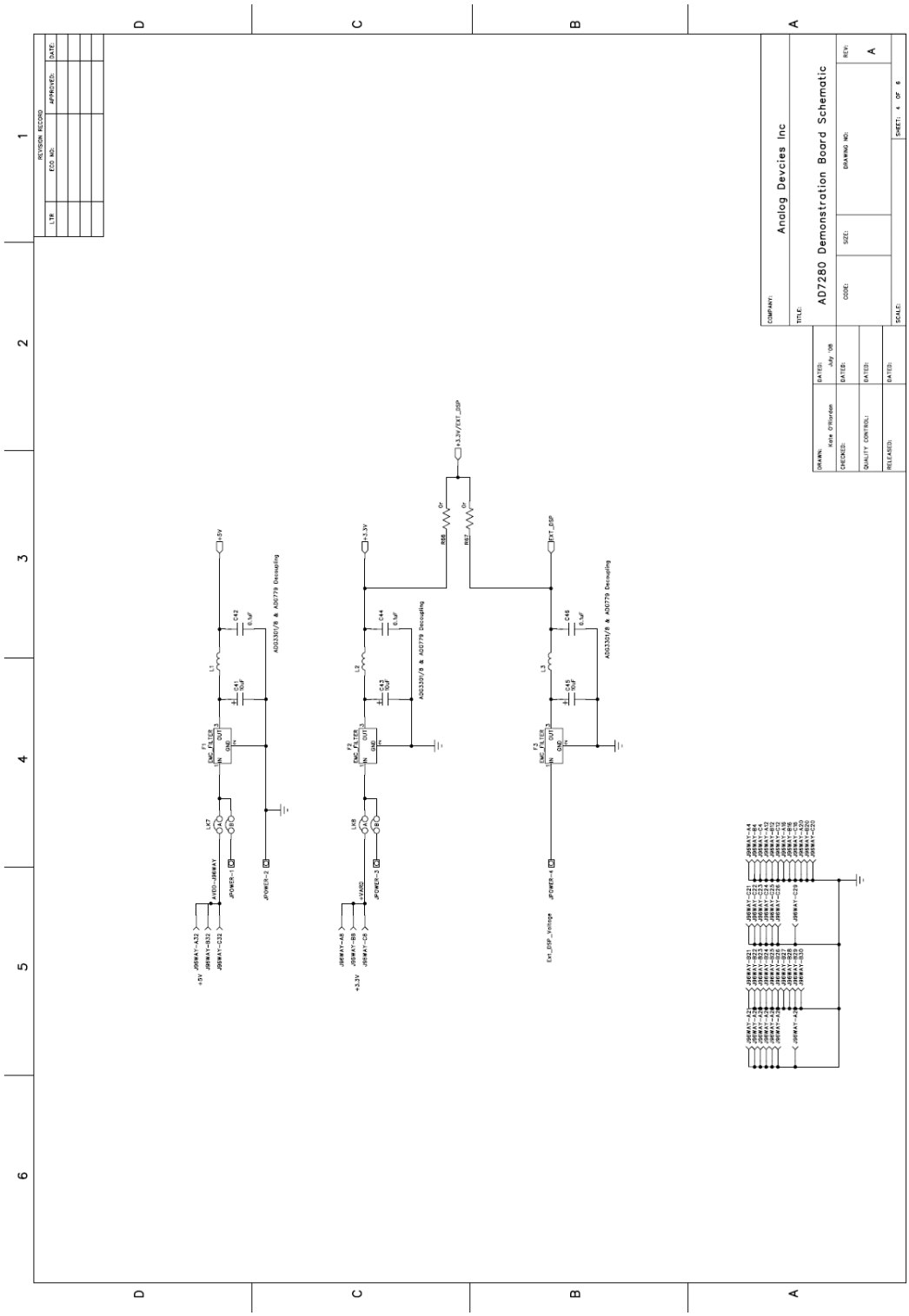
Figure 104 – GUI Showing Two Devices

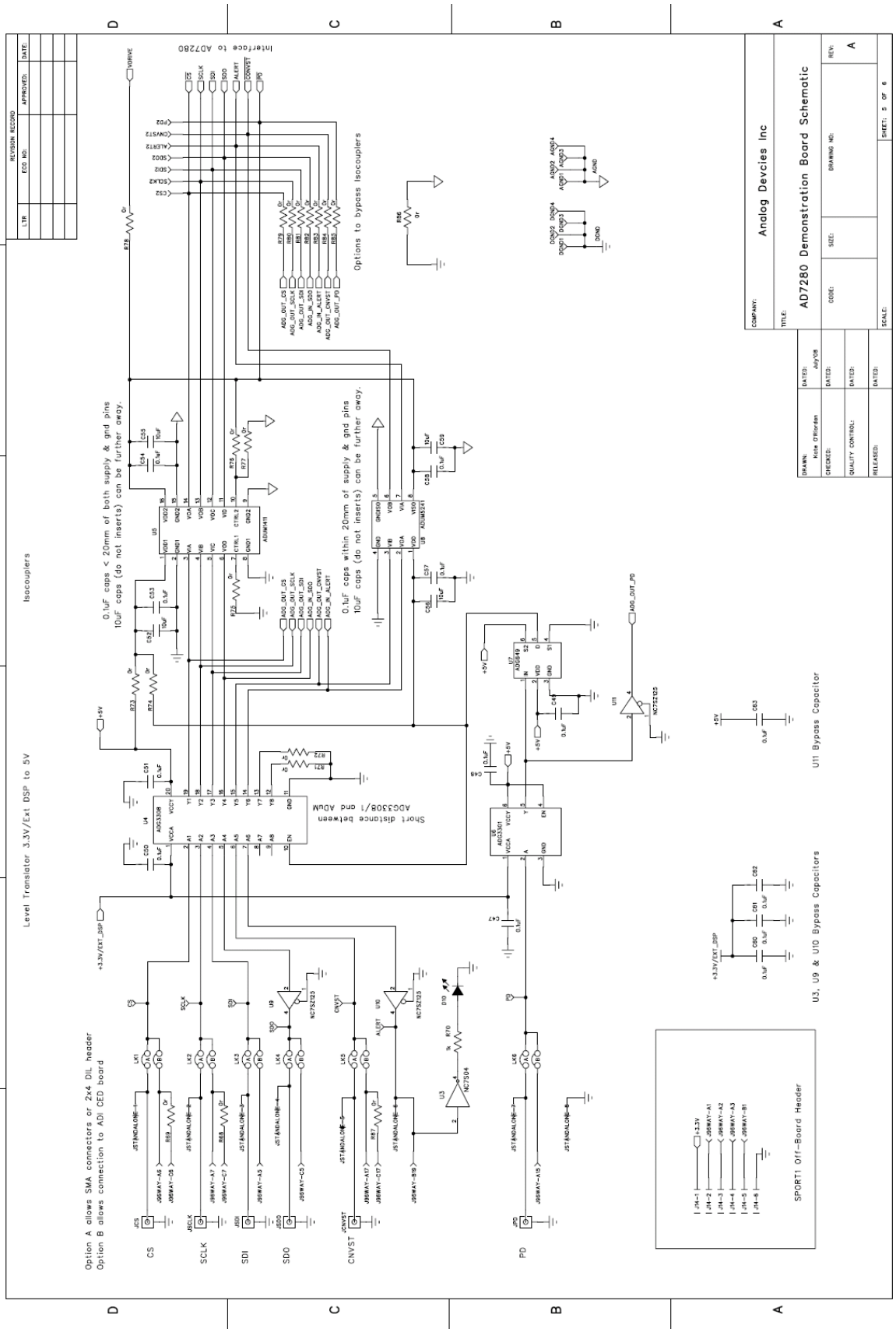
Figure 104 shows the EVAL Board's two devices' two device temperature and voltage readings.

Having written two different software, the user can easily switch between the DEMO Board and the EVAL Board and have the software to run them.

9. Appendix

9.1. DEMO Board Schematics




Level Translator 3.3V/Ext DSP to 5V
Isocouplers
Interface to AD7280
Options to bypass Isocouplers
0.1uF caps < 20mm of both supply & gnd pins
10uF caps (do not inserts) can be further away.
0.1uF caps within 20mm of supply & gnd pins
10uF caps (do not inserts) can be further away.
Short distance between
ADG3308/1 and ADuM
Option A allows SMA connectors or 2x4 DIL header
Option B allows connection to ADI CED board
U3, U9 & U10 Bypass Capacitors
U11 Bypass Capacitor
SPORT1 Off-Board Header
Analog Devcies Inc
AD7280 Demonstration Board Schematic

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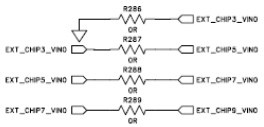
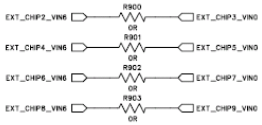


Only populate components above this note if it is being used as a demo

Only populate components below this note if it is being sent to the customer.



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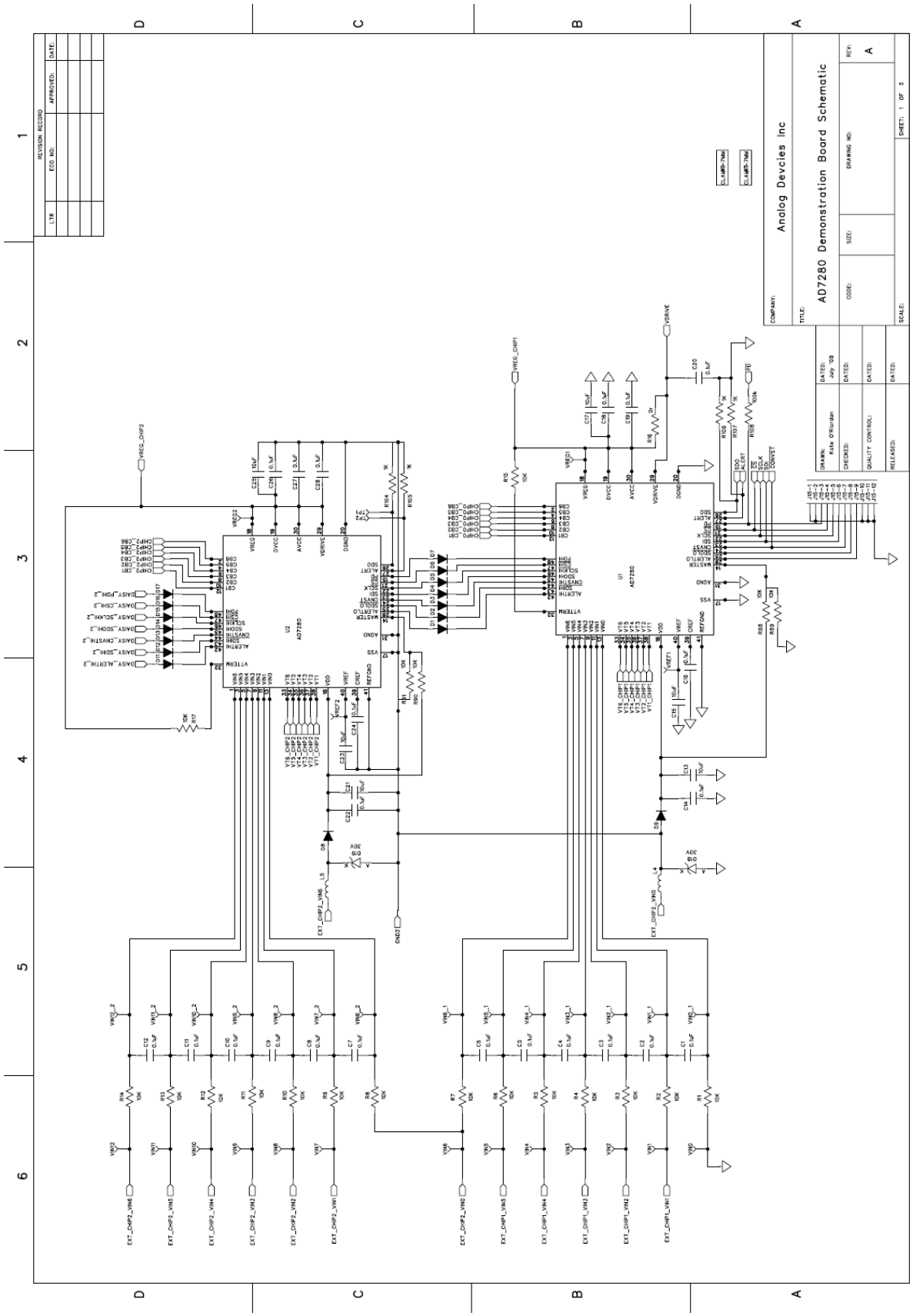
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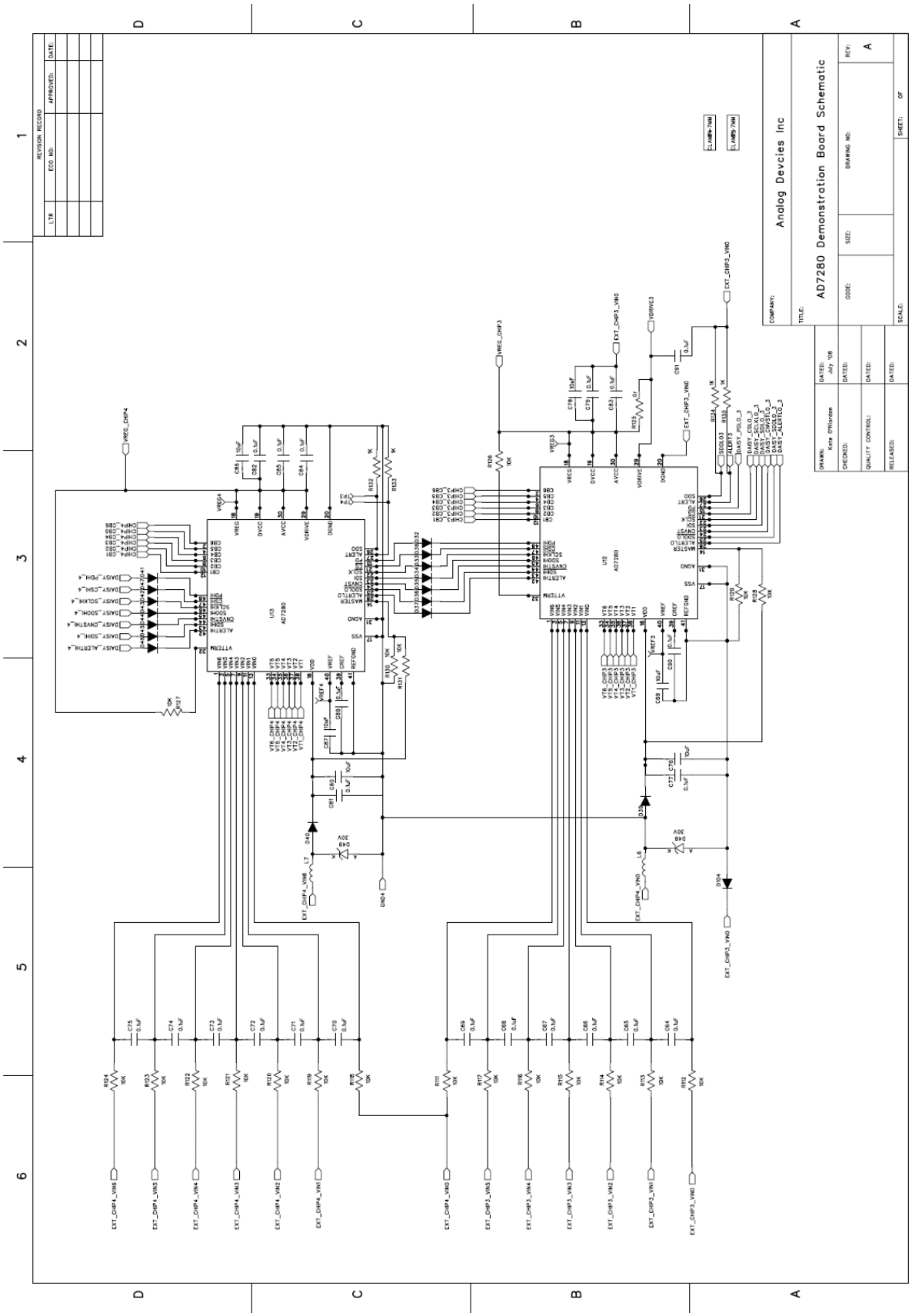
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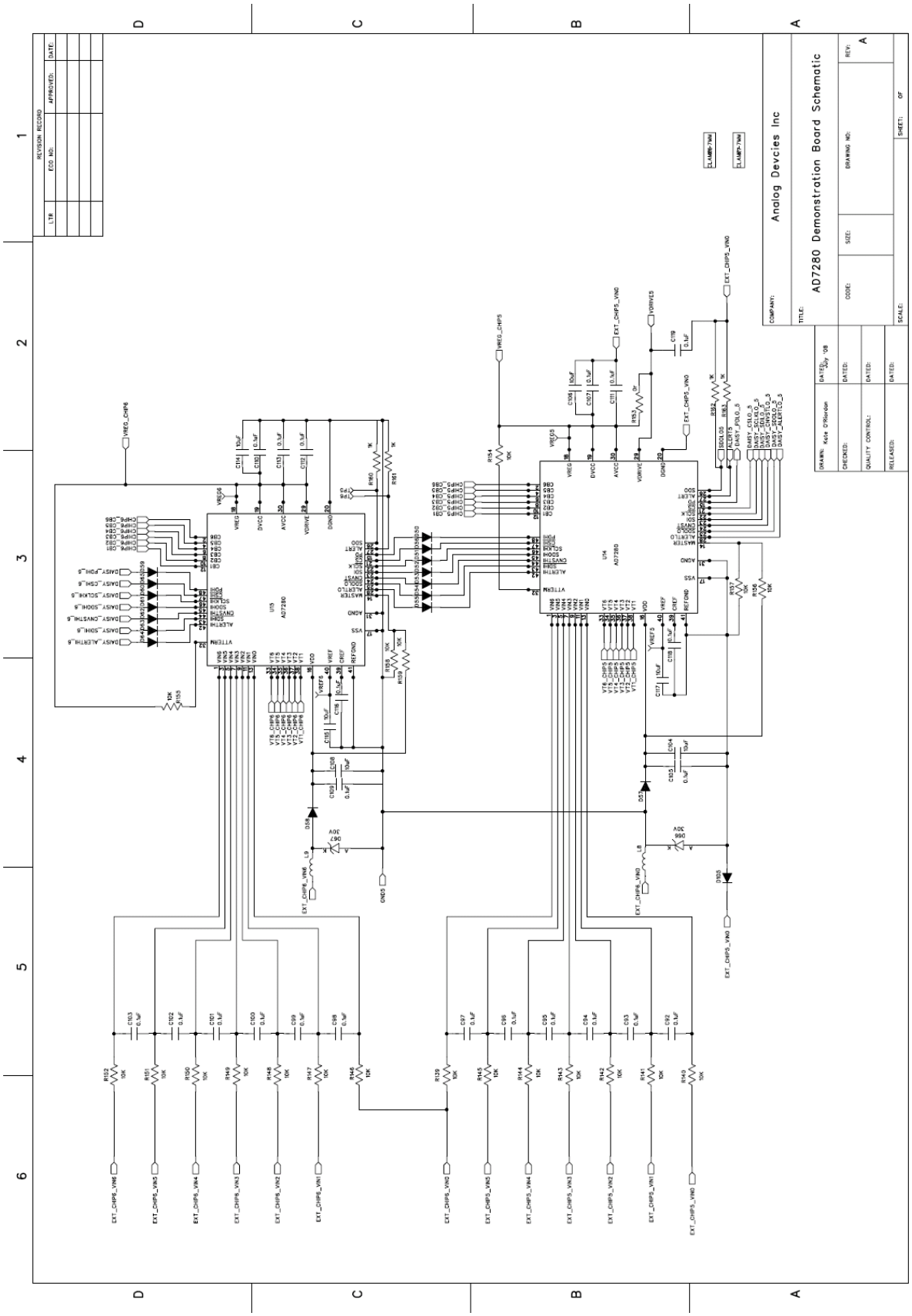
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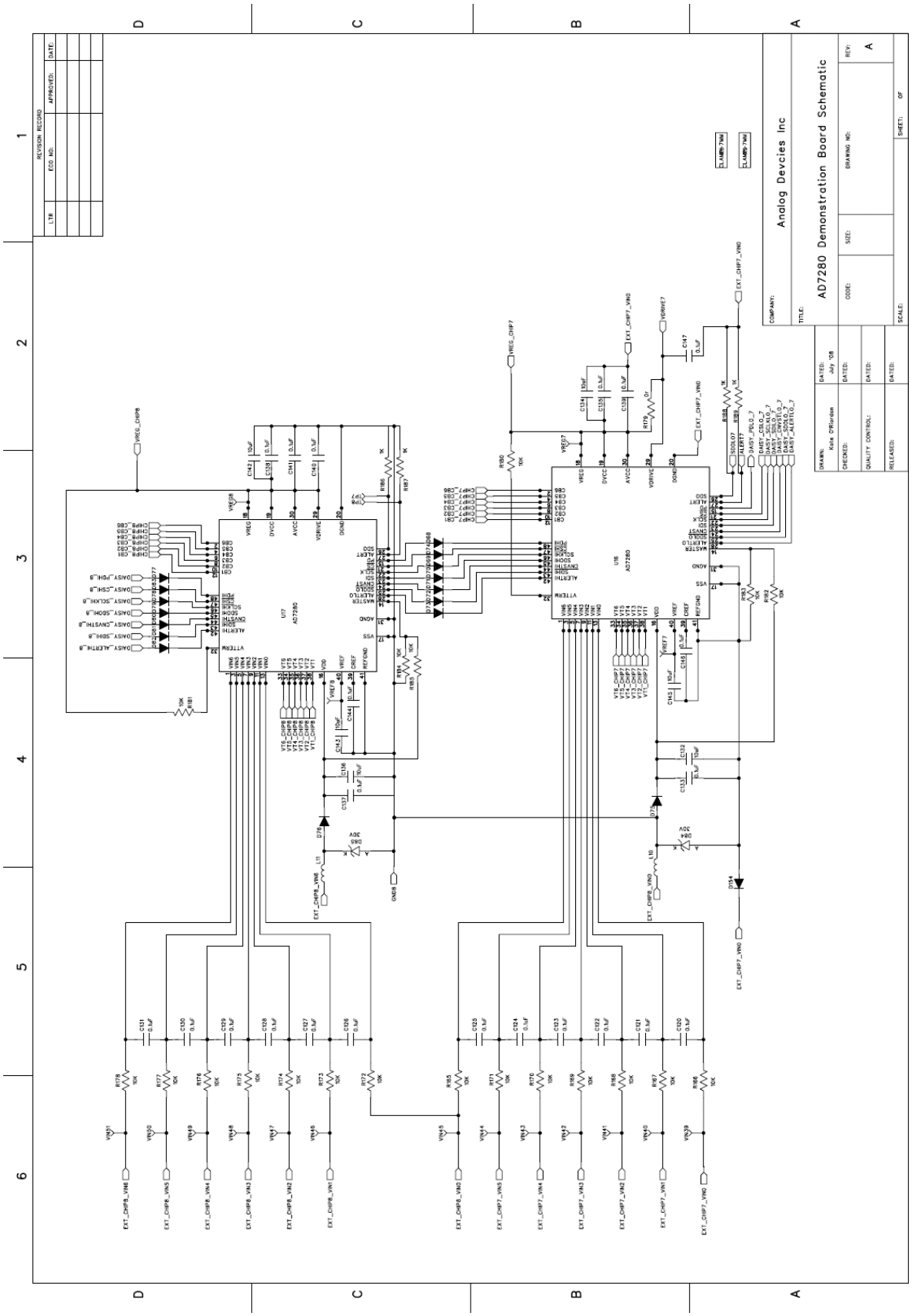
GND5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ECO NO:
APPROVED:
DATE:
COMPANY:
Analog Devcies Inc
TITLE:
AD7280 Demonstration Board Schematic
DRAWN:
Kate O'Riordan
DATED:
July '08
CHECKED:
QUALITY CONTROL:
RELEASED:
SIZE:
DRAWING NO:
REV:
A
SHEET:
OF
U7
AD7280
U8
AD7280
VREG_CHIP8
VREG_CHIP7
EXT_CHIP8_VN6
EXT_CHIP8_VN5
EXT_CHIP8_VN4
EXT_CHIP8_VN3
EXT_CHIP8_VN2
EXT_CHIP8_VN1
EXT_CHIP7_VN6
EXT_CHIP7_VN5
EXT_CHIP7_VN4
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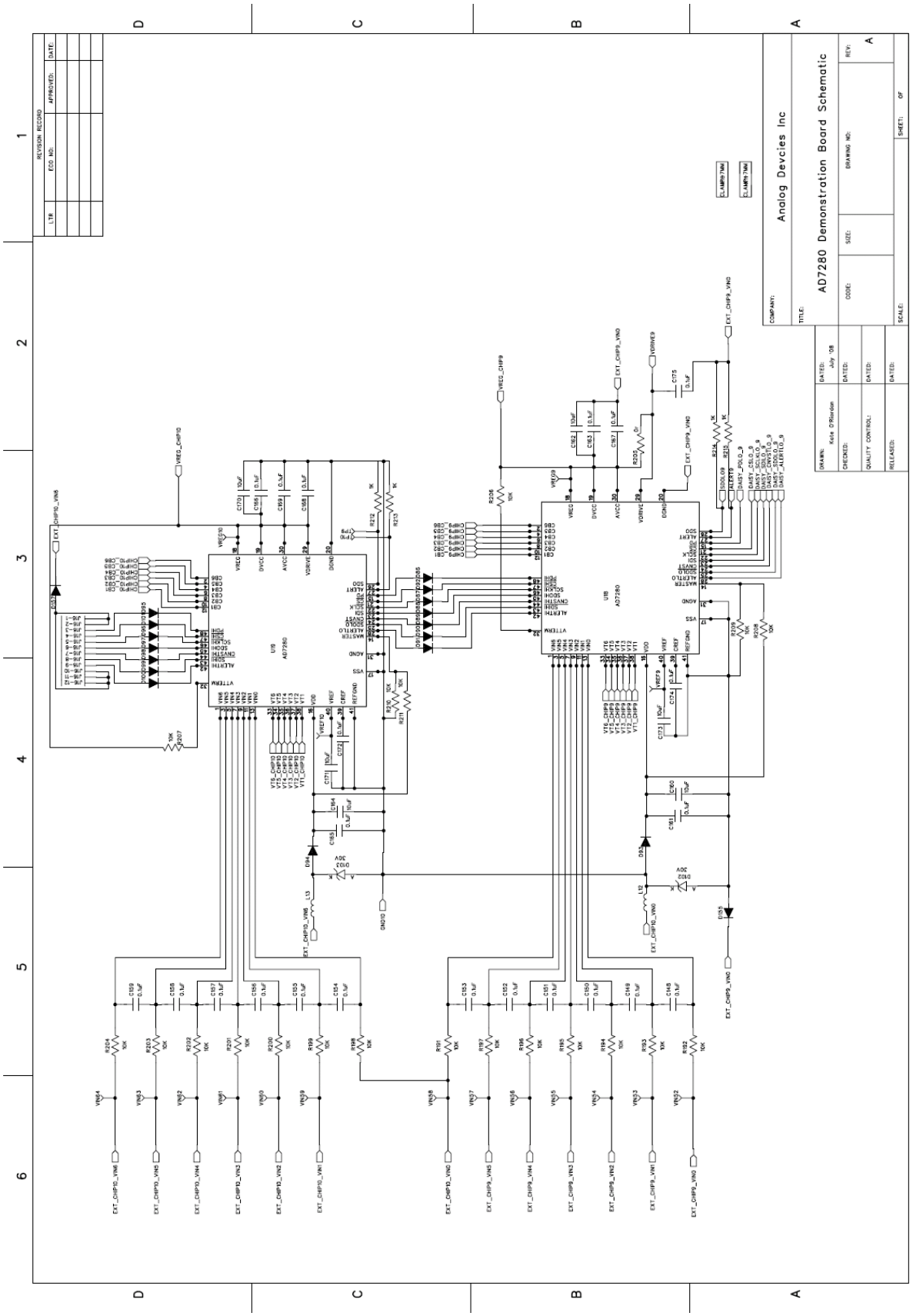
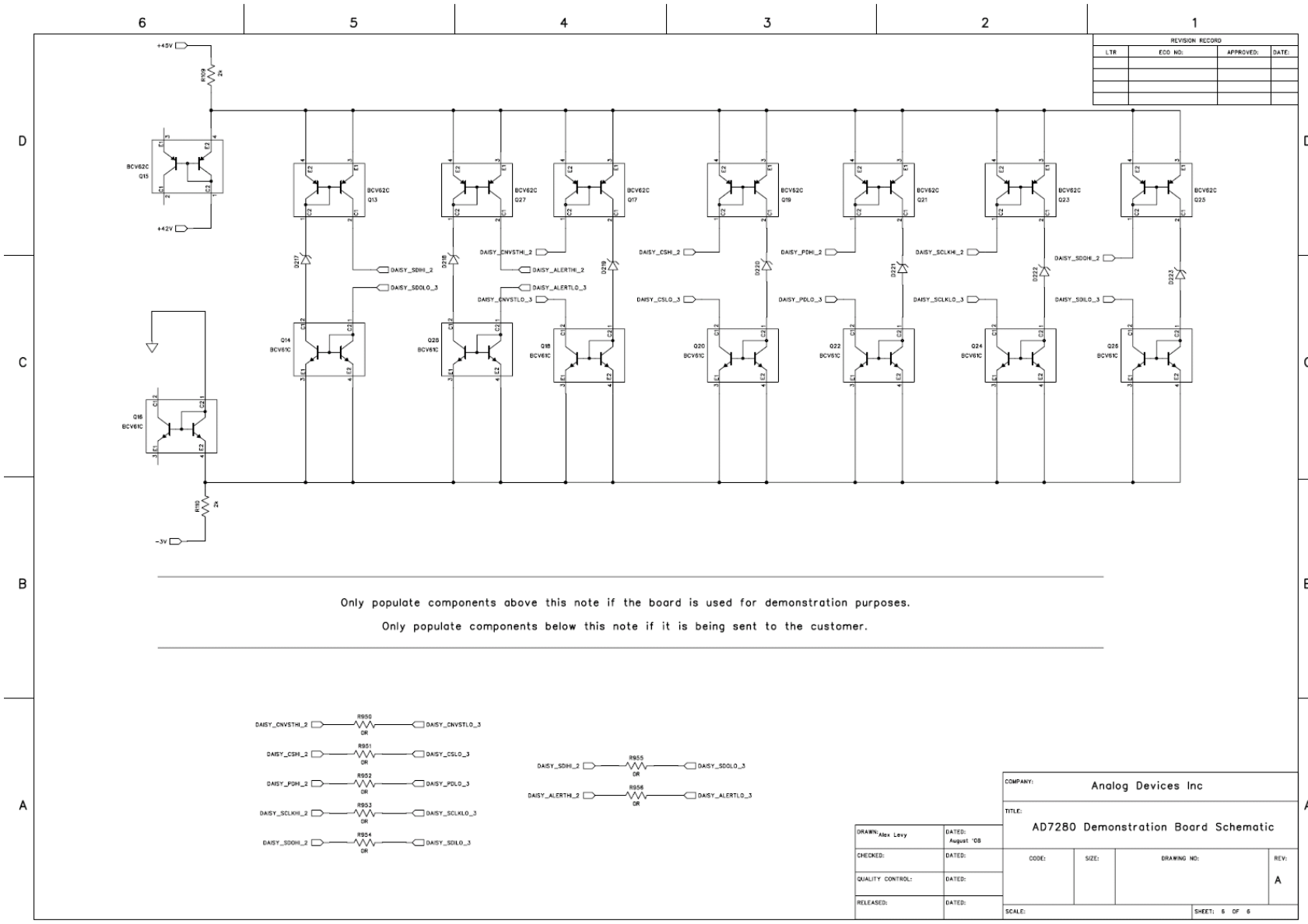
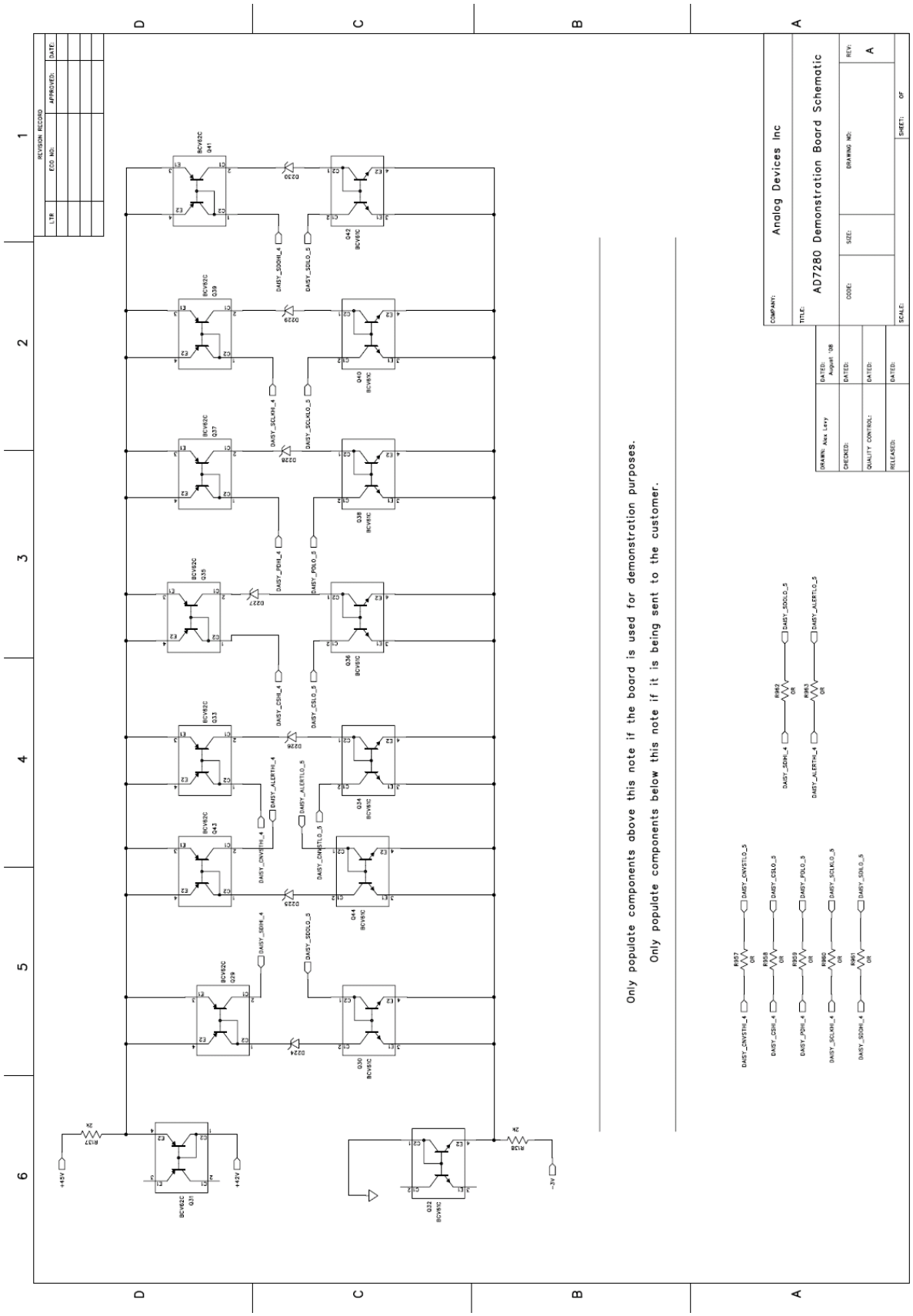
EXT_CHIP7_VN1
EXT_CHIP7_VN0
GND8
GND7


AD7280 Demonstration Board Schematic
Analog Devices Inc
REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
DRAWN:
Keia O'Riordan
July '08
CHECKED:
QUALITY CONTROL:
RELEASED:
SIZE:
DRAWING NO:
REV:
SCALE:
SHEET:
OF
U1B
AD7280
U1A
AD7280
VREG_CHIP10
VREG_CHIP9
EXT_CHIP10_VN6
EXT_CHIP9_VN0
DGND
AGND
CLAMP6.7kW


6
5
4
3
2
1
REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
+45V
+42V
-3V
R109
2k
R110
2k
BCV62C
Q15
Q13
Q27
Q17
Q19
Q21
Q23
Q25
Q14
BCV61C
Q25
Q18
Q20
Q22
Q24
Q26
Q16
D217
D218
D219
D220
D221
D222
D223
DAISY_SDIHI_2
DAISY_SDOLO_3
DAISY_CNVSTHI_2
DAISY_ALERTHI_2
DAISY_CNVSTLO_3
DAISY_ALERTLO_3
DAISY_CSHI_2
DAISY_CSLO_3
DAISY_PDHI_2
DAISY_PDLO_3
DAISY_SCLKHI_2
DAISY_SCLKLO_3
DAISY_SDOHI_2
DAISY_SDILO_3
Only populate components above this note if the board is used for demonstration purposes.
Only populate components below this note if it is being sent to the customer.
R950
R951
R952
R953
R954
R955
R956
0R
COMPANY:
Analog Devices Inc
TITLE:
AD7280 Demonstration Board Schematic
DRAWN: Alex Levy
DATED: August '08
CHECKED:
QUALITY CONTROL:
RELEASED:
CODE:
SIZE:
DRAWING NO:
REV:
A
SCALE:
SHEET: 5 OF 6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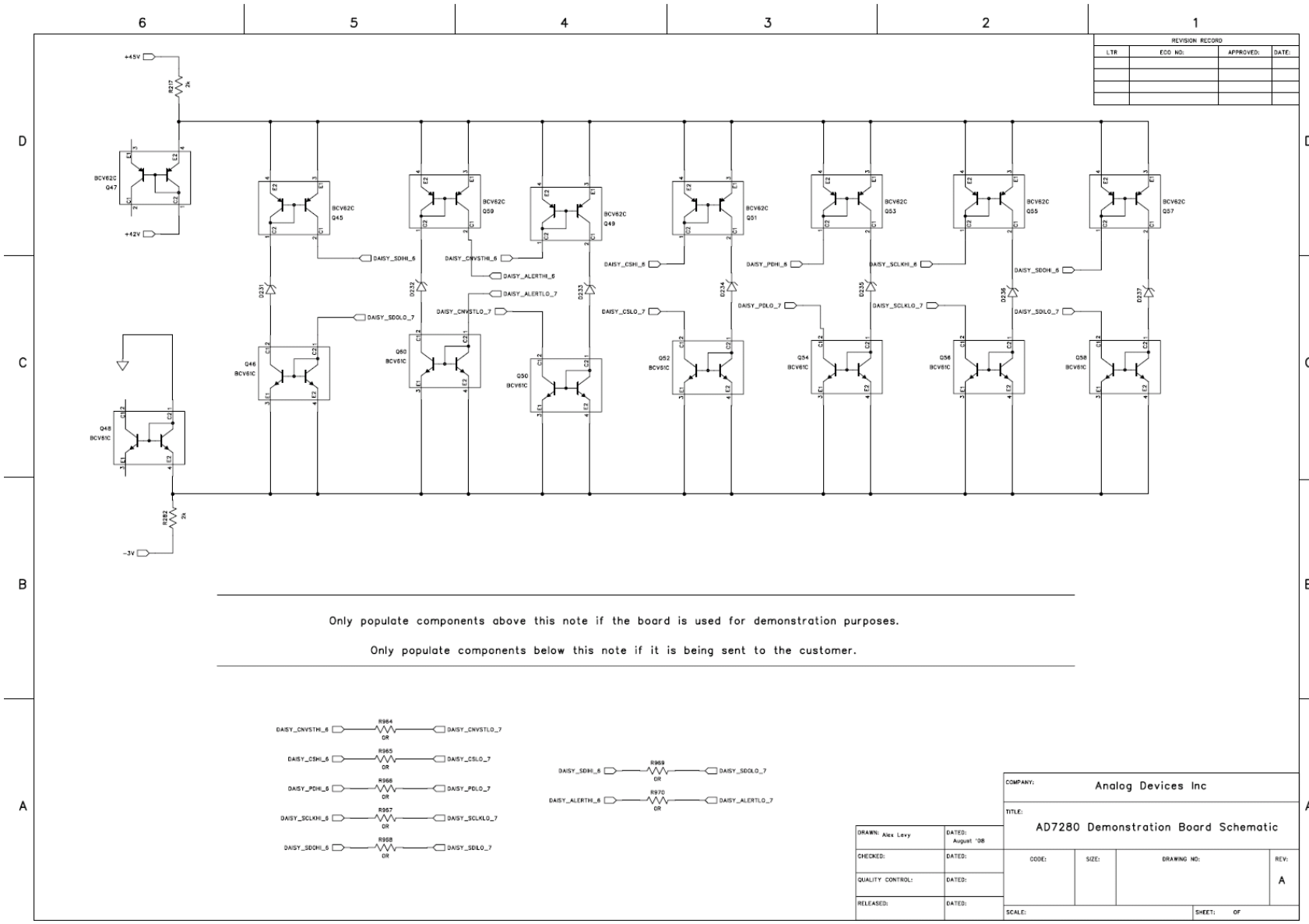
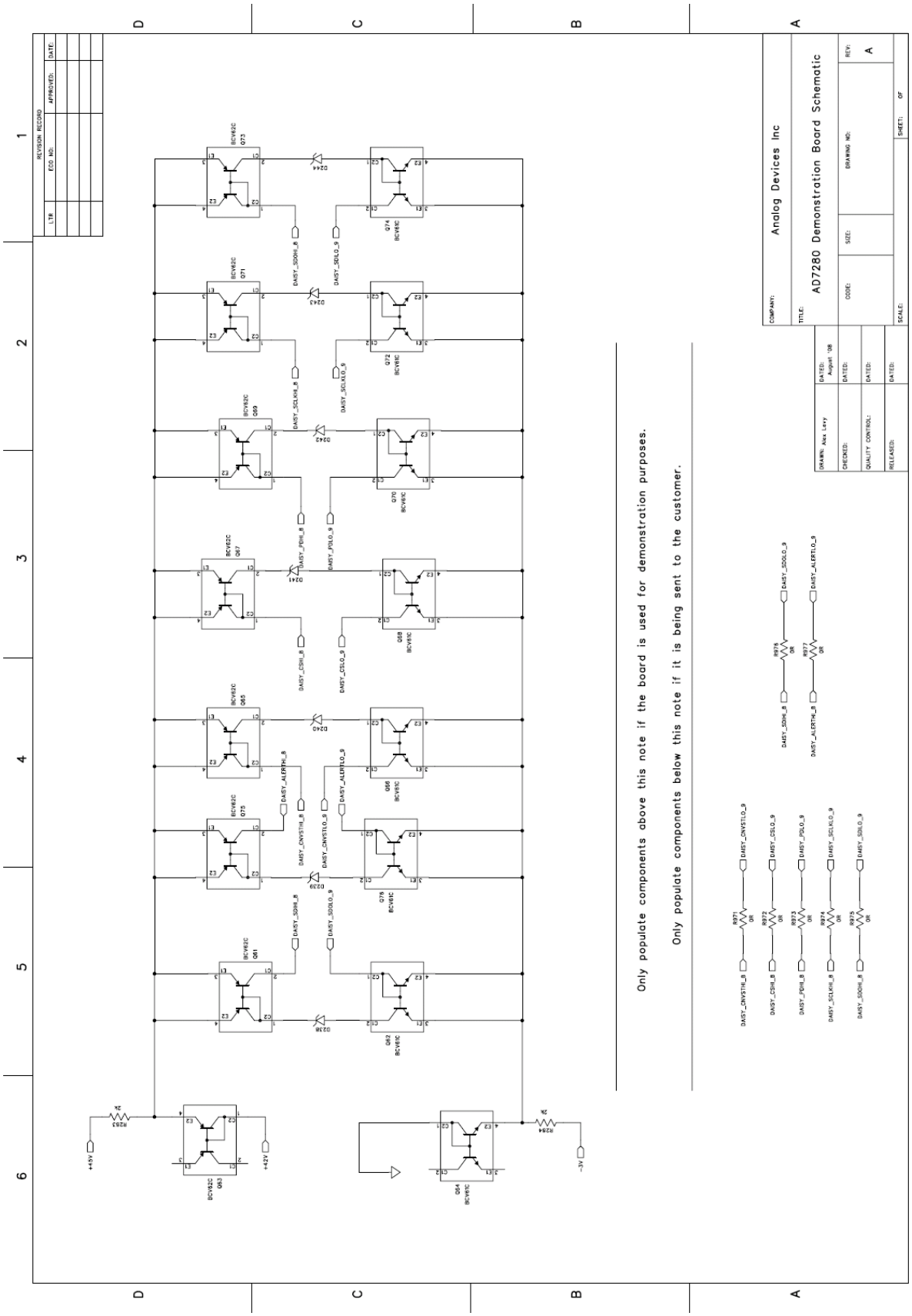
COMPANY:
Analog Devices Inc
TITLE:
AD7280 Demonstration Board Schematic
DRAWN: Alex Lavy
DATED: August '08
CHECKED:
QUALITY CONTROL:
RELEASED:
CODE:
SIZE:
DRAWING NO:
REV:
A
SCALE:
SHEET: OF
Only populate components above this note if the board is used for demonstration purposes.
Only populate components below this note if it is being sent to the customer.


6
5
4
3
2
1
REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
+45V
R227
2k
+42V
BCV62C
Q47
BCV62C
Q45
BCV62C
Q59
BCV62C
Q49
BCV62C
Q51
BCV62C
Q53
BCV62C
Q55
BCV62C
Q57
DAISY_SDIHI_6
DAISY_CNVSTHI_6
DAISY_ALERTHI_6
DAISY_CSHI_6
DAISY_PDHI_6
DAISY_SCLKHI_6
DAISY_SDOHI_6
D231
D232
D233
D234
D235
D236
D237
DAISY_SDOLO_7
DAISY_ALERTLO_7
DAISY_CNVSTLO_7
DAISY_CSLO_7
DAISY_PDLO_7
DAISY_SCLKLO_7
DAISY_SDILO_7
Q46
BCV61C
Q60
BCV61C
Q50
BCV61C
Q52
BCV61C
Q54
BCV61C
Q56
BCV61C
Q58
BCV61C
Q48
BCV61C
R282
2k
-3V
Only populate components above this note if the board is used for demonstration purposes.
Only populate components below this note if it is being sent to the customer.
DAISY_CNVSTHI_6
R964
0R
DAISY_CNVSTLO_7
DAISY_CSHI_6
R965
0R
DAISY_CSLO_7
DAISY_PDHI_6
R966
0R
DAISY_PDLO_7
DAISY_SCLKHI_6
R967
0R
DAISY_SCLKLO_7
DAISY_SDOHI_6
R968
0R
DAISY_SDILO_7
DAISY_SDIHI_6
R969
0R
DAISY_SDOLO_7
DAISY_ALERTHI_6
R970
0R
DAISY_ALERTLO_7
DRAWN: Alex Levy
DATED: August '08
CHECKED:
DATED:
QUALITY CONTROL:
DATED:
RELEASED:
DATED:
COMPANY: Analog Devices Inc
TITLE: AD7280 Demonstration Board Schematic
CODE:
SIZE:
DRAWING NO:
REV: A
SCALE:
SHEET: OF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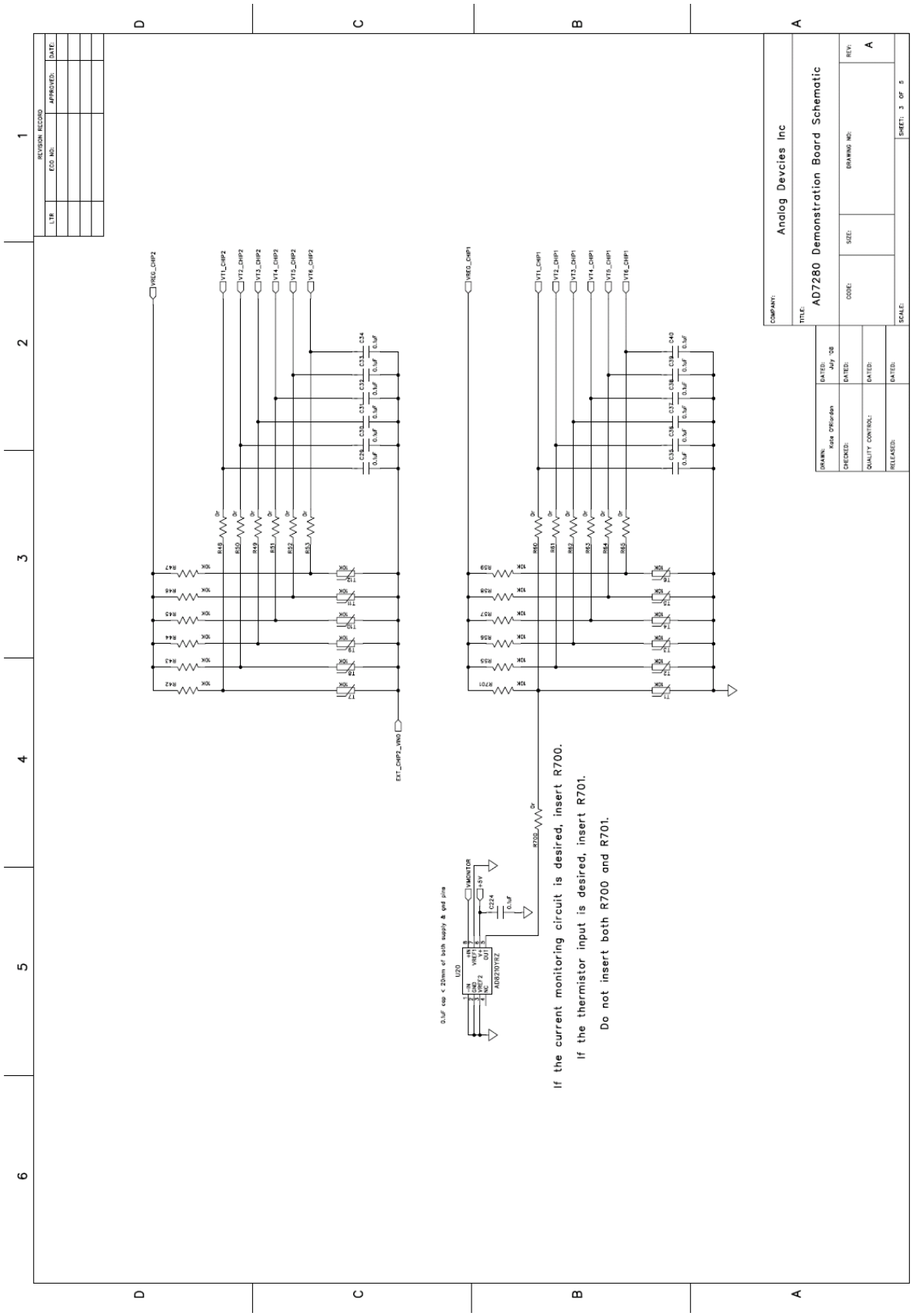
ECO NO:
APPROVED:
DATE:
COMPANY:
Analog Devices Inc
TITLE:
AD7280 Demonstration Board Schematic
DRAWN: Alex Lavy
DATED: August '08
CHECKED:
QUALITY CONTROL:
RELEASED:
SIZE:
DRAWING NO:
REV:
A
SHEET: OF
Only populate components above this note if the board is used for demonstration purposes.
Only populate components below this note if it is being sent to the customer.


REVISION RECORD
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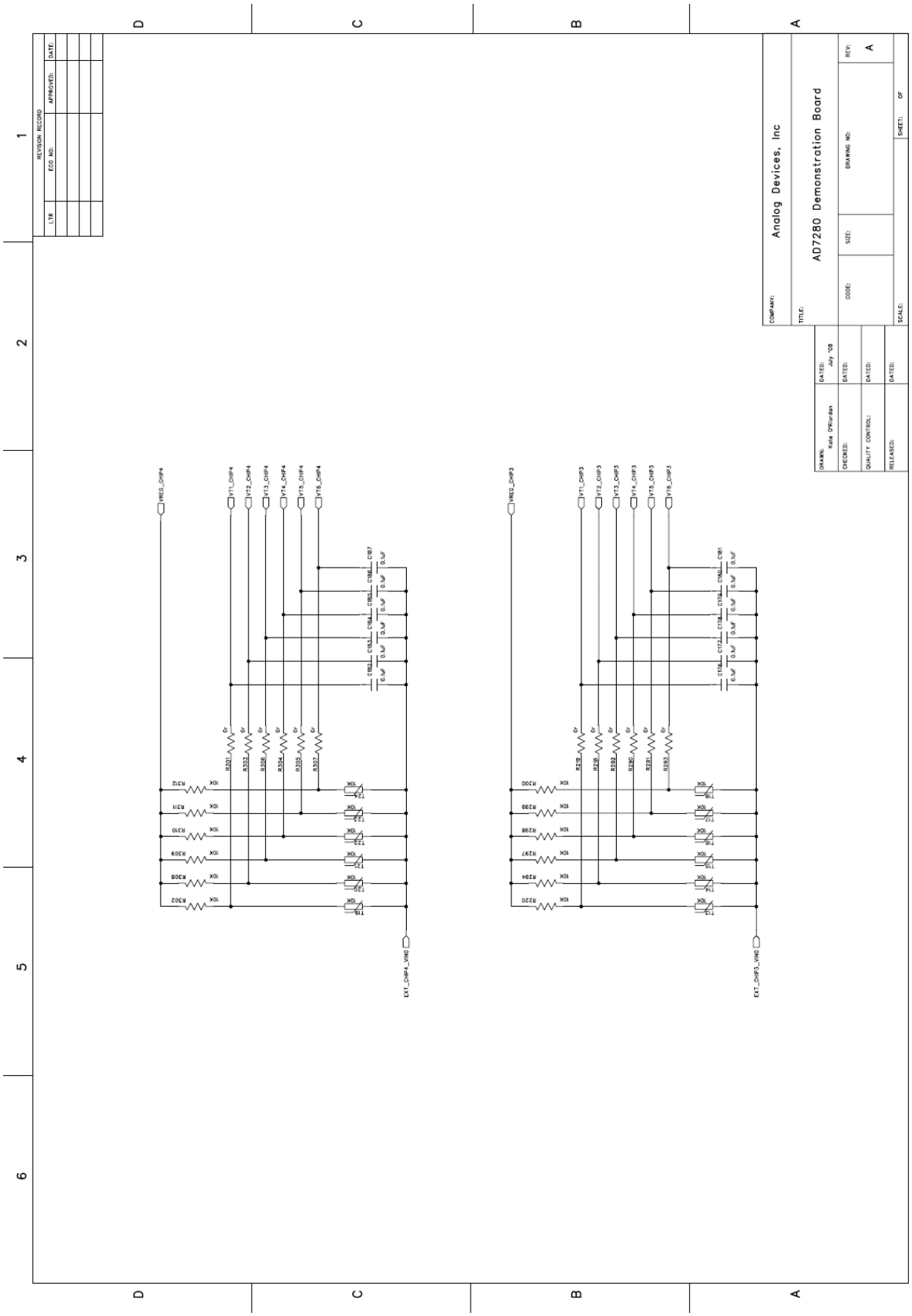
ECO NO:
APPROVED:
DATE:
COMPANY: Analog Devcies Inc
TITLE: AD7280 Demonstration Board Schematic
DRAWN: Kate O'Riordan
DATED: July '08
CHECKED:
QUALITY CONTROL:
RELEASED:
SIZE:
DRAWING NO:
REV: A
SHEET: 3 OF 6
VREG_CHIP2
VREG_CHIP1
EXT_CHIP2_VNO
If the current monitoring circuit is desired, insert R700.
If the thermistor input is desired, insert R701.
Do not insert both R700 and R701.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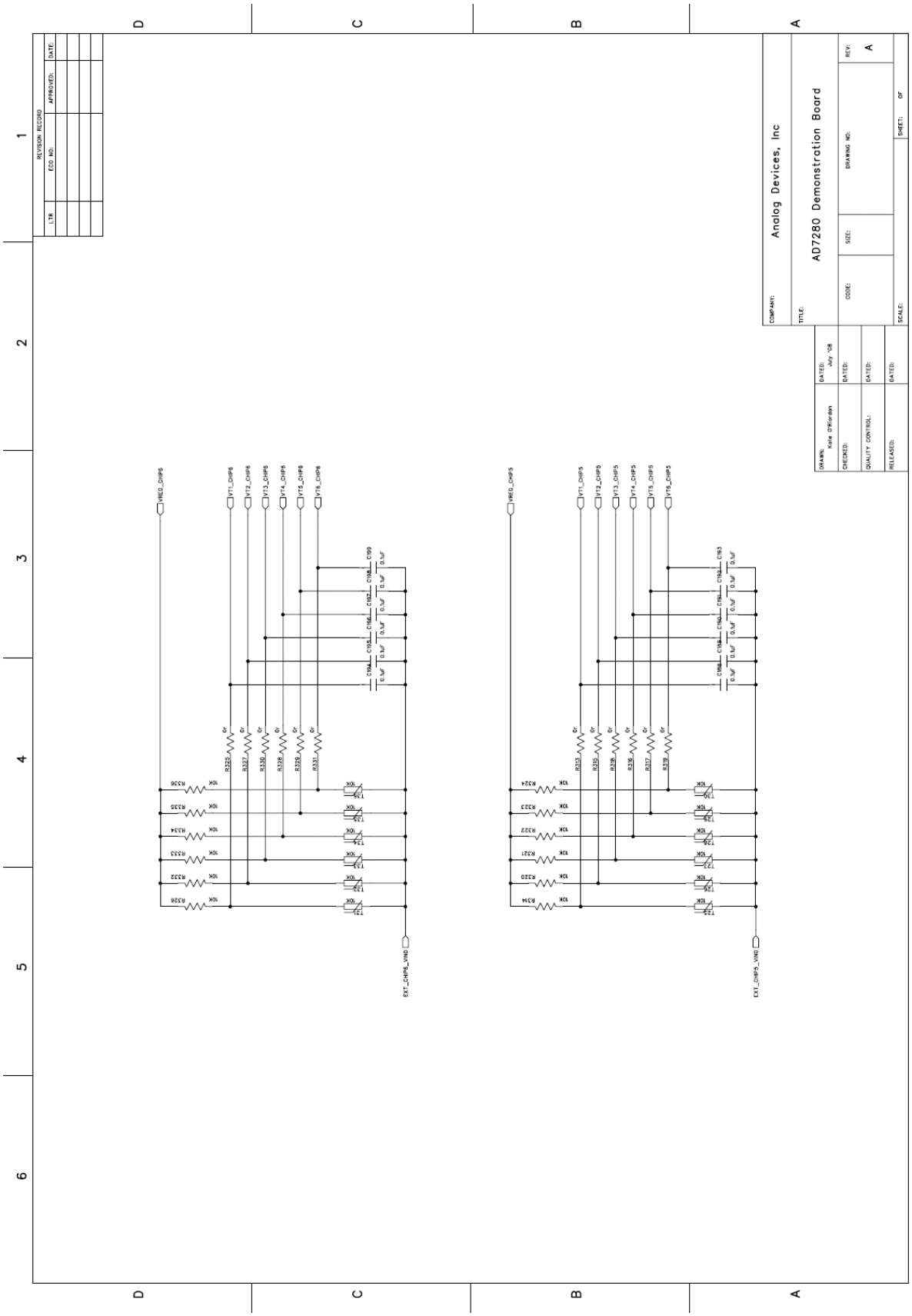
APPROVED:
DATE:
COMPANY:
Analog Devices, Inc
TITLE:
AD7280 Demonstration Board
DRAWN:
Kate O'Riordan
DATED:
July '08
CHECKED:
QUALITY CONTROL:
RELEASED:
CODE:
SIZE:
DRAWING NO:
REV:
A
SCALE:
SHEET:
OF
VREG_CHIP4
VREG_CHIP3
EXT_CHIP4_VNO
EXT_CHIP3_VNO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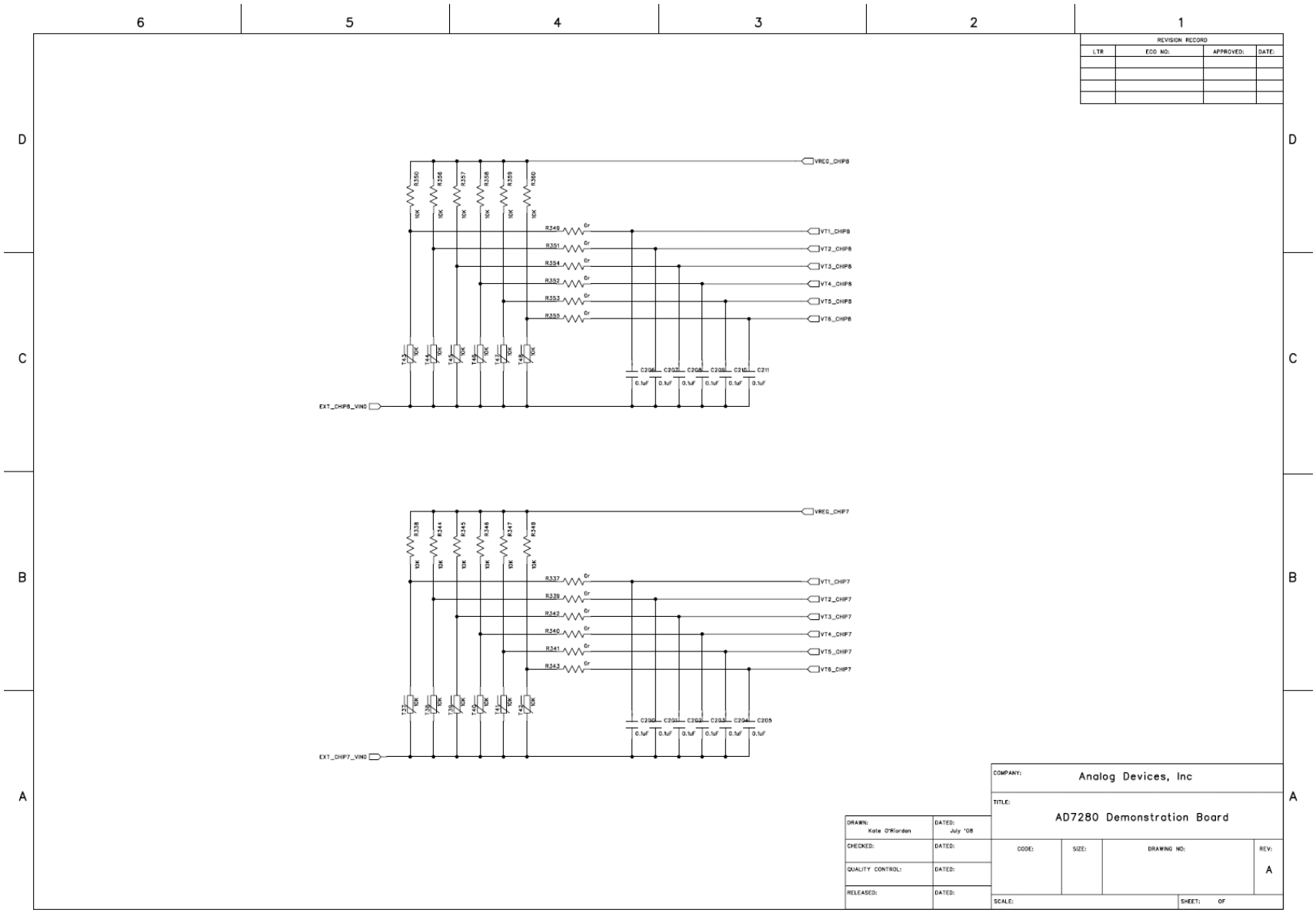
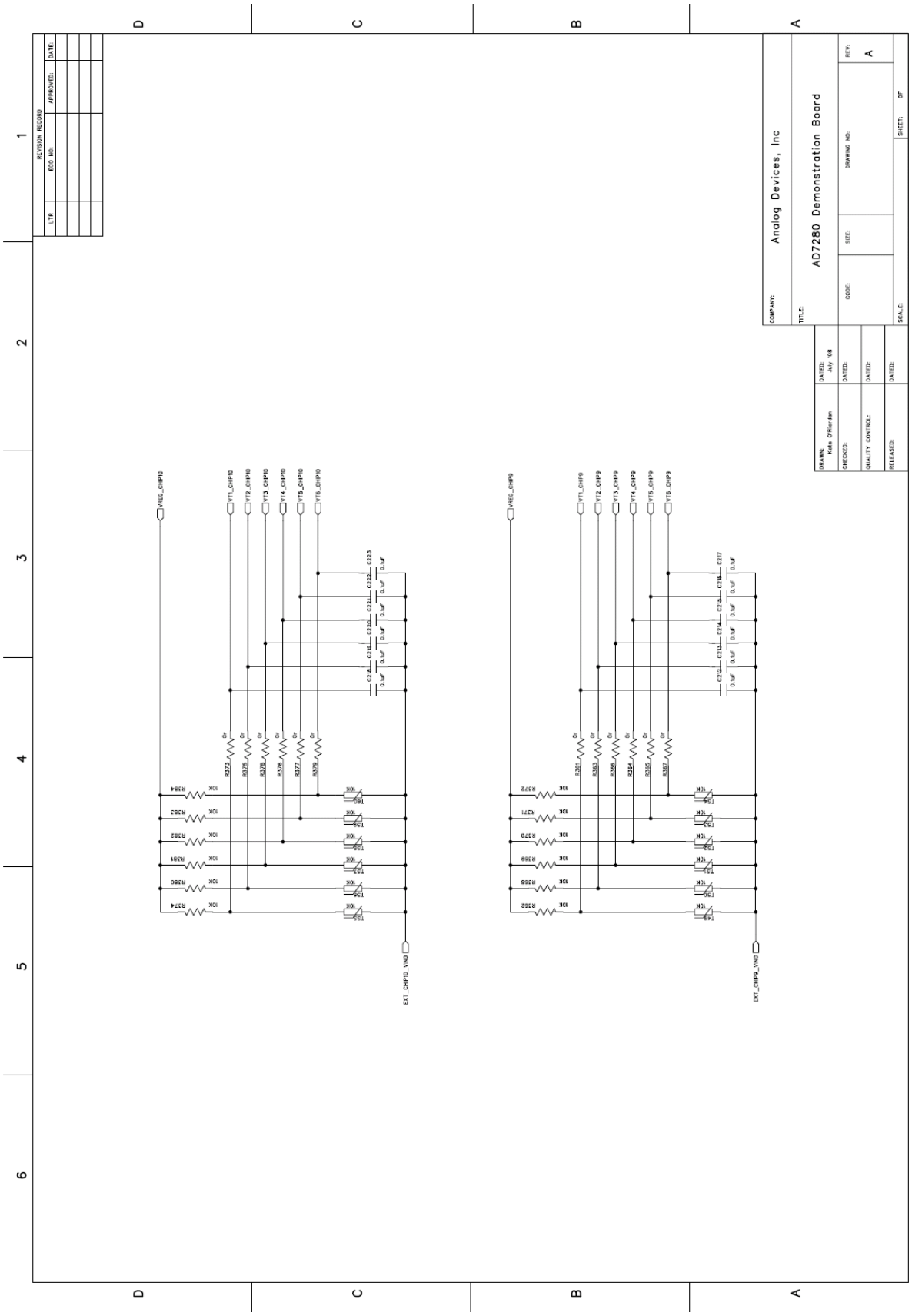
DATE:
Analog Devices, Inc
AD7280 Demonstration Board
COMPANY:
TITLE:
CODE:
SIZE:
DRAWING NO:
REV:
A
SHEET:
OF
SCALE:
DRAWN:
Kate O'Riordan
DATED:
July 108
CHECKED:
QUALITY CONTROL:
RELEASED:
VREG_CHIP6
VT1_CHIP6
VT2_CHIP6
VT3_CHIP6
VT4_CHIP6
VT5_CHIP6
VT6_CHIP6
EXT_CHIP6_VM0
VREG_CHIP5
VT1_CHIP5
VT2_CHIP5
VT3_CHIP5
VT4_CHIP5
VT5_CHIP5
VT6_CHIP5
EXT_CHIP5_VM0


6
5
4
3
2
1
REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
D
C
B
A
VREG_CHIP8
R350
R356
R357
R358
R359
R360
10K
R349
R351
R354
R352
R353
R355
0r
VT1_CHIP8
VT2_CHIP8
VT3_CHIP8
VT4_CHIP8
VT5_CHIP8
VT6_CHIP8
T13
T14
T15
T16
T17
T18
C206
C207
C208
C209
C210
C211
0.1uF
EXT_CHIP8_VIN
VREG_CHIP7
R338
R344
R345
R346
R347
R348
R337
R339
R342
R340
R341
R343
VT1_CHIP7
VT2_CHIP7
VT3_CHIP7
VT4_CHIP7
VT5_CHIP7
VT6_CHIP7
T12
T11
T10
T9
T8
T7
C200
C201
C202
C203
C204
C205
EXT_CHIP7_VIN
COMPANY:
Analog Devices, Inc
TITLE:
AD7280 Demonstration Board
DRAWN:
Kate O'Riordan
DATED:
July '08
CHECKED:
DATED:
QUALITY CONTROL:
DATED:
RELEASED:
DATED:
CODE:
SIZE:
DRAWING NO:
REV:
A
SCALE:
SHEET:
OF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COMPANY:
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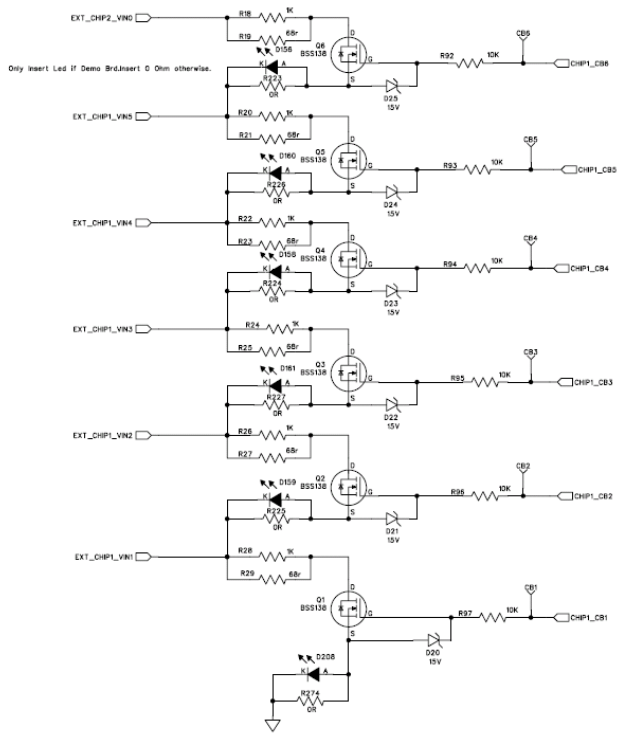
TITLE:
AD7280 Demonstration Board
DRAWN:
Kate O'Riordan
DATED:
July '08
CHECKED:
QUALITY CONTROL:
RELEASED:
CODE:
SIZE:
DRAWING NO:
REV:
A
SCALE:
SHEET:
OF
VREG_CHPB
VT1_CHPB
VT2_CHPB
VT3_CHPB
VT4_CHPB
VT5_CHPB
VT6_CHPB
EXT_CHPB_VND
VREG_CHPA
VT1_CHPA
VT2_CHPA
VT3_CHPA
VT4_CHPA
VT5_CHPA
VT6_CHPA
EXT_CHPA_VND

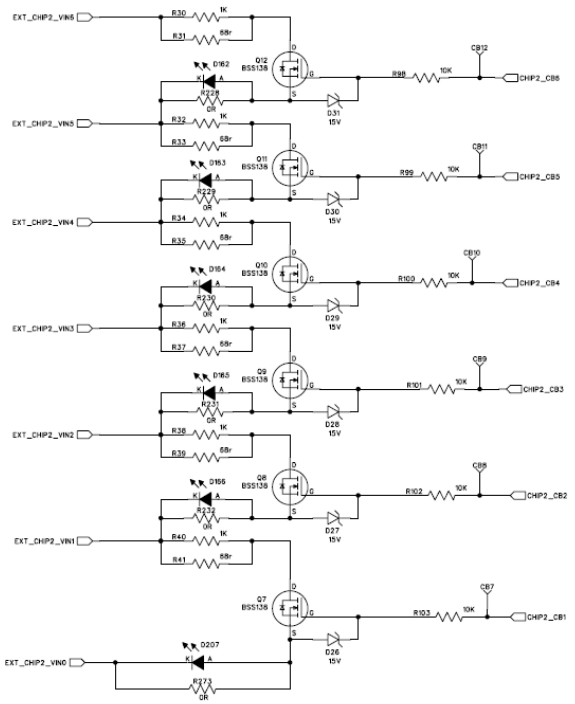
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

NOTE:LEDS MUST BE PLACED ON THE TOP SIDE OF THE BOARD.

NOTE:THE FOLLOWING PARTS ARE NOT TO BE INSERTED.
R19,R21,R23,R25,R27,R29

NOTE:THE FOLLOWING PARTS ARE NOT TO BE INSERTED.
R31,R33,R35,R37,R39,R41



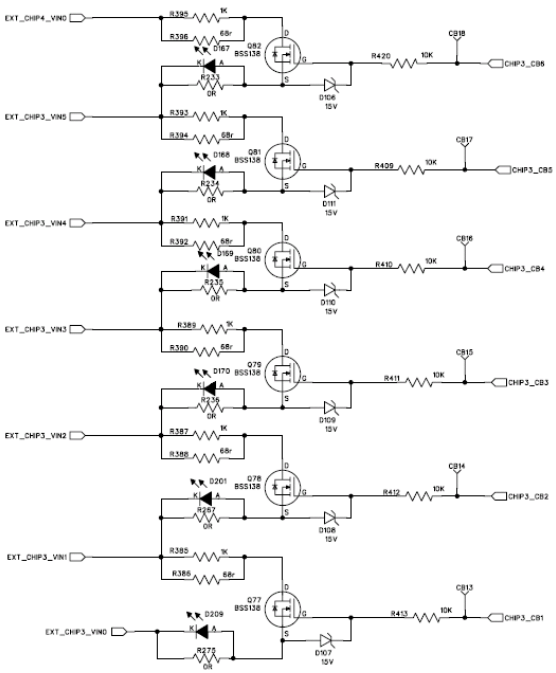


COMPANY:	Analog Devcies Inc
TITLE:	AD7280 Demonstration Board Schematic
DRAWN: Kate O'Riordan	DATED: July '08
CHECKED:	DATED:
QUALITY CONTROL:	DATED:
RELEASED:	DATED:
CODE:	SIZE:
DRAWING NO:	REV: A
SCALE:	SHEET: 2 OF 5

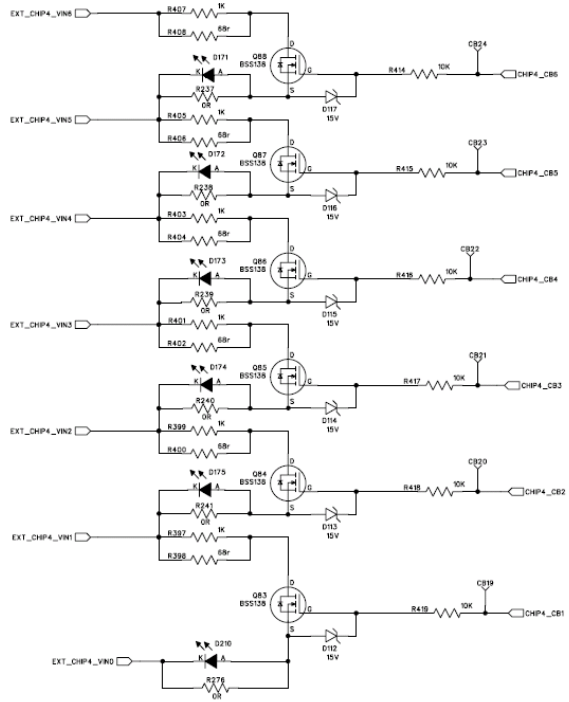
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

NOTE:LEDS MUST BE PLACED ON THE TOP SIDE OF THE BOARD.

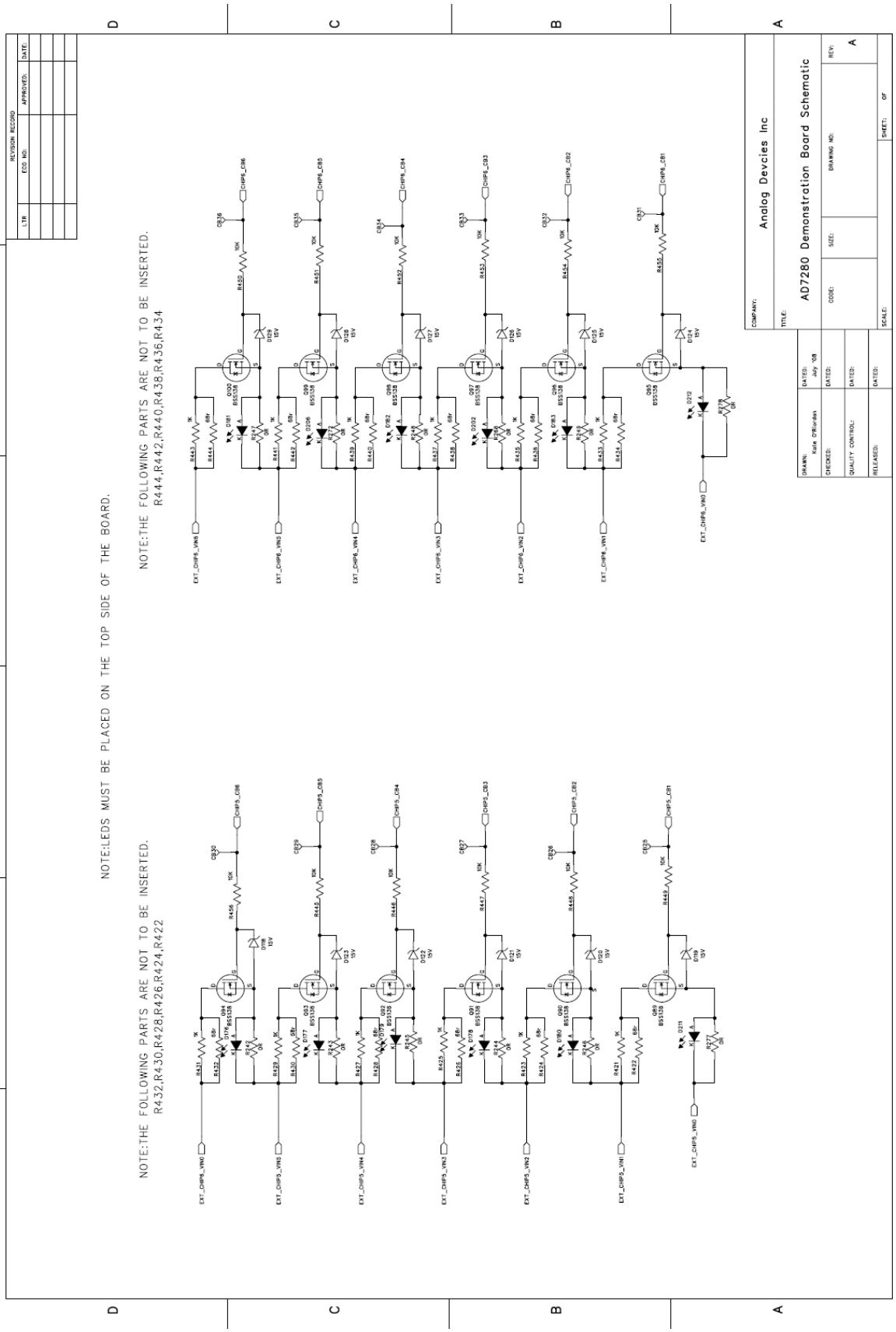
NOTE:THE FOLLOWING PARTS ARE NOT TO BE INSERTED.
R396,R394,R392,R390,R388,R386



NOTE:THE FOLLOWING PARTS ARE NOT TO BE INSERTED.
R408,R406,R404,R402,R400,R398



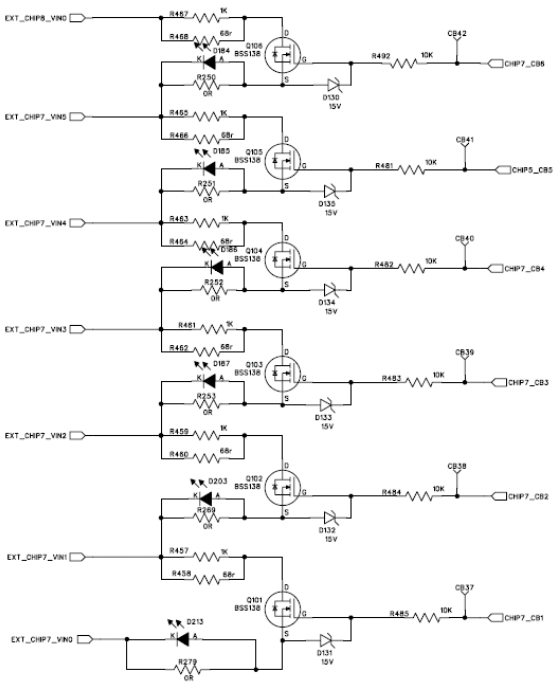
COMPANY:	Analog Devcies Inc		
TITLE:	AD7280 Demonstration Board Schematic		
DRAWN: Kate O'Riordan	DATED: July '08	CODE:	SIZE: DRAWING NO: REV: A
CHECKED:	DATED:		
QUALITY CONTROL:	DATED:		
RELEASED:	DATED:	SCALE:	SHEET: OF


NOTE:LEDS MUST BE PLACED ON THE TOP SIDE OF THE BOARD.
NOTE:THE FOLLOWING PARTS ARE NOT TO BE INSERTED.
R444,R442,R440,R438,R436,R434
NOTE:THE FOLLOWING PARTS ARE NOT TO BE INSERTED.
R432,R430,R428,R426,R424,R422
REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
COMPANY:
Analog Devcies Inc
TITLE:
AD7280 Demonstration Board Schematic
DRAWN:
Kate O'Riordan
DATED:
July '08
CHECKED:
QUALITY CONTROL:
RELEASED:
CODE:
SIZE:
DRAWING NO:
REV:
A
SCALE:
SHEET:
OF

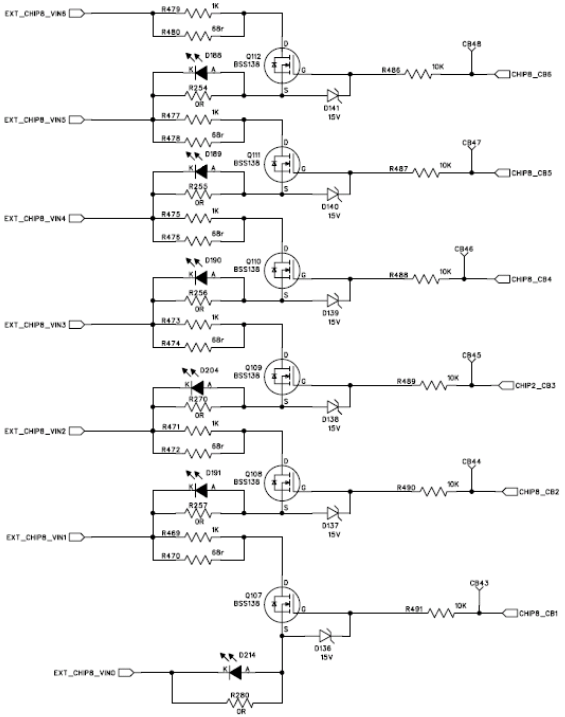
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

NOTE:LEDS MUST BE PLACED ON THE TOP SIDE OF THE BOARD.

NOTE:THE FOLLOWING PARTS ARE NOT TO BE INSERTED.
R468,R466,R464,R462,R460,R458



NOTE:THE FOLLOWING PARTS ARE NOT TO BE INSERTED.
R480,R478,R476,R474,R472,R470

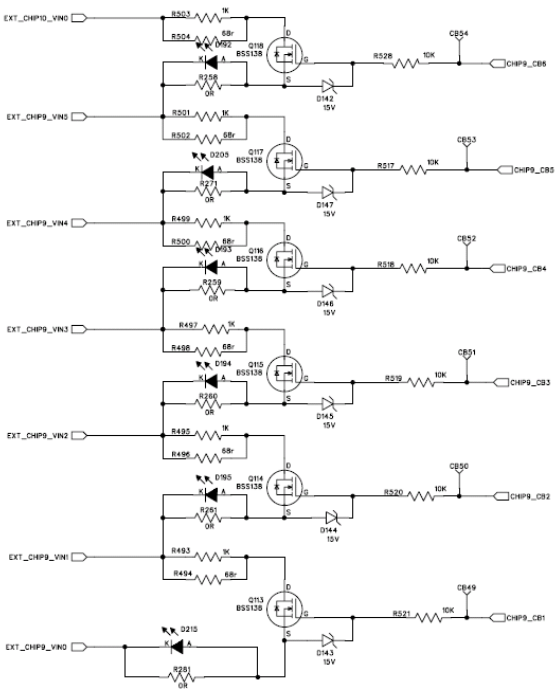


COMPANY: Analog Devcies Inc			
TITLE: AD7280 Demonstration Board Schematic			
DRAWN: Kate O'Riordan	DATED: July '08	CODE:	SIZE: DRAWING NO: REV: A
CHECKED:	DATED:		
QUALITY CONTROL:	DATED:		
RELEASED:	DATED:	SCALE:	SHEET: OF

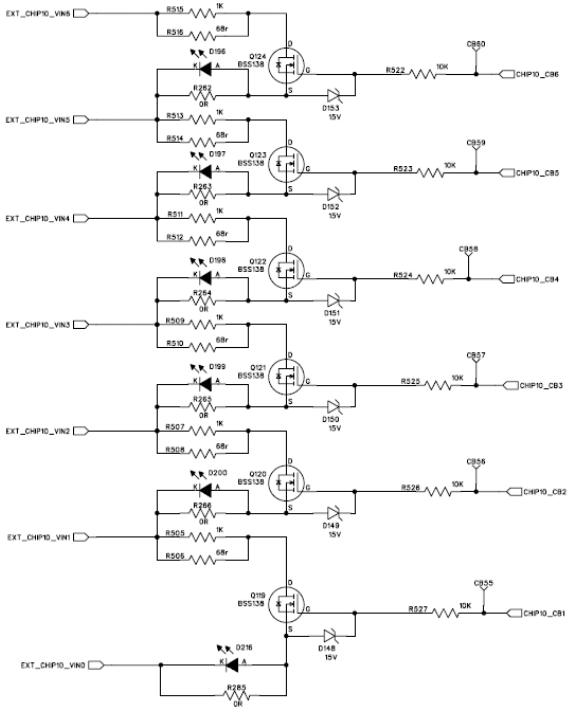
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

NOTE:LEDS MUST BE PLACED ON THE TOP SIDE OF THE BOARD.

NOTE:THE FOLLOWING PARTS ARE NOT TO BE INSERTED.
R504,R502,R500,R498,R496,R494



NOTE:THE FOLLOWING PARTS ARE NOT TO BE INSERTED.
R516,R514,R512,R510,R508,R506

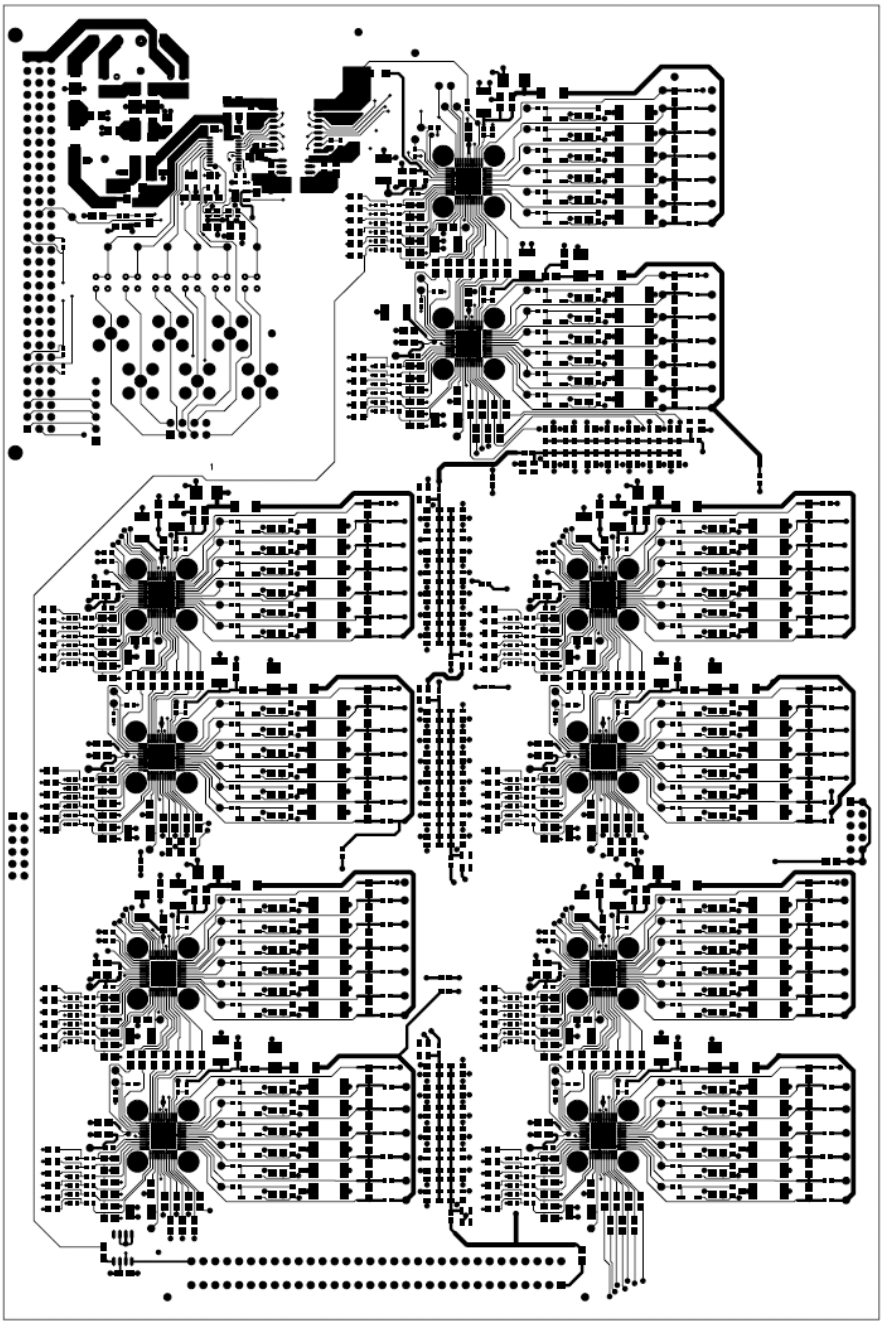


COMPANY:	Analog Devcies Inc		
TITLE:	AD7280 Demonstration Board Schematic		
DRAWN: Kate O'Riordan	DATED: July '08	CODE:	SIZE: DRAWING NO: REV: A
CHECKED:	DATED:		
QUALITY CONTROL:	DATED:		
RELEASED:	DATED:	SCALE:	SHEET: OF

9.2. DEMO Board PCB Layout

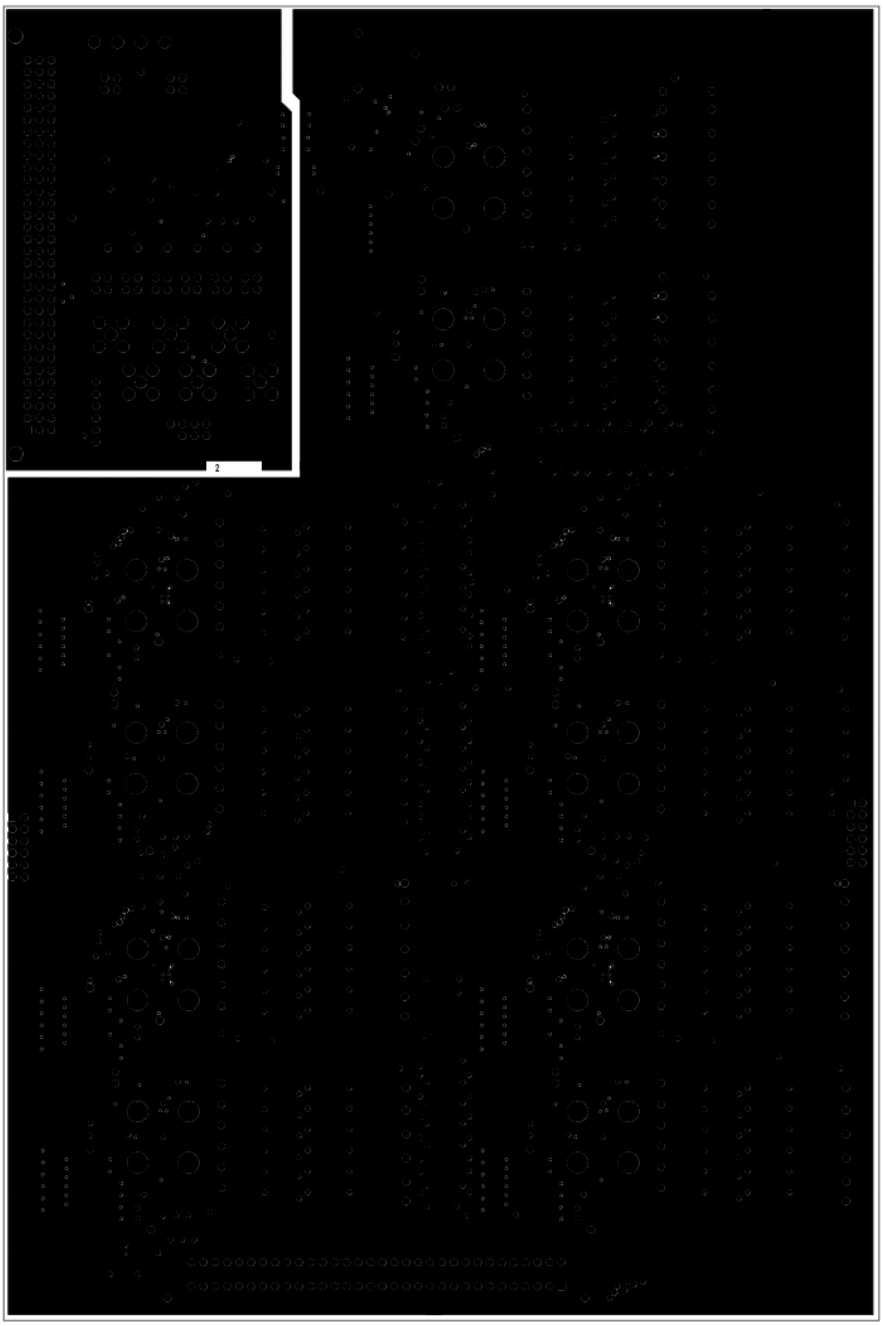
AD7280 DEMO (Rev. A) – Component Side View

Component Side – Layer 1



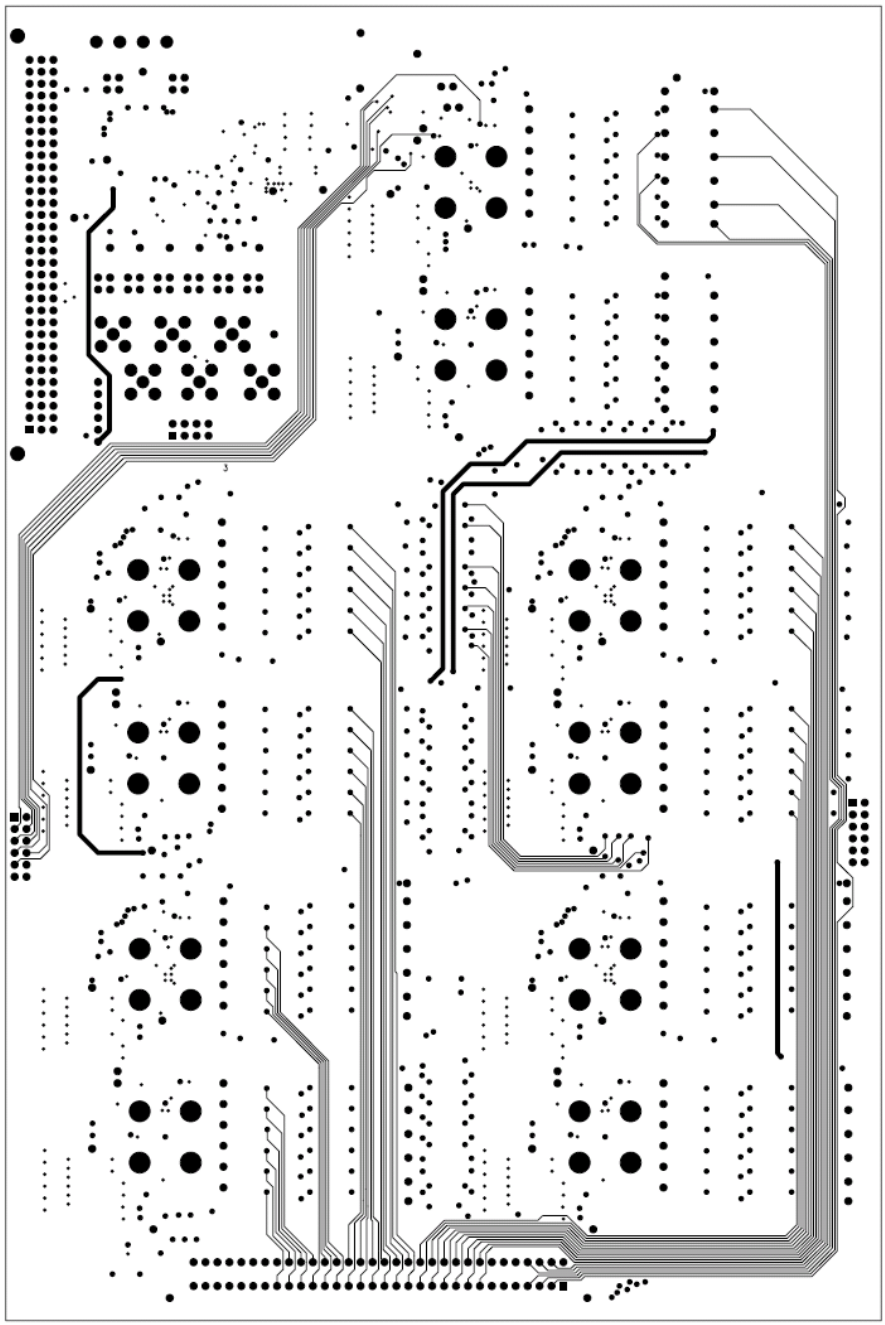
AD7280 DEMO (Rev. A) – Component Side View

Ground Plane – Layer 2



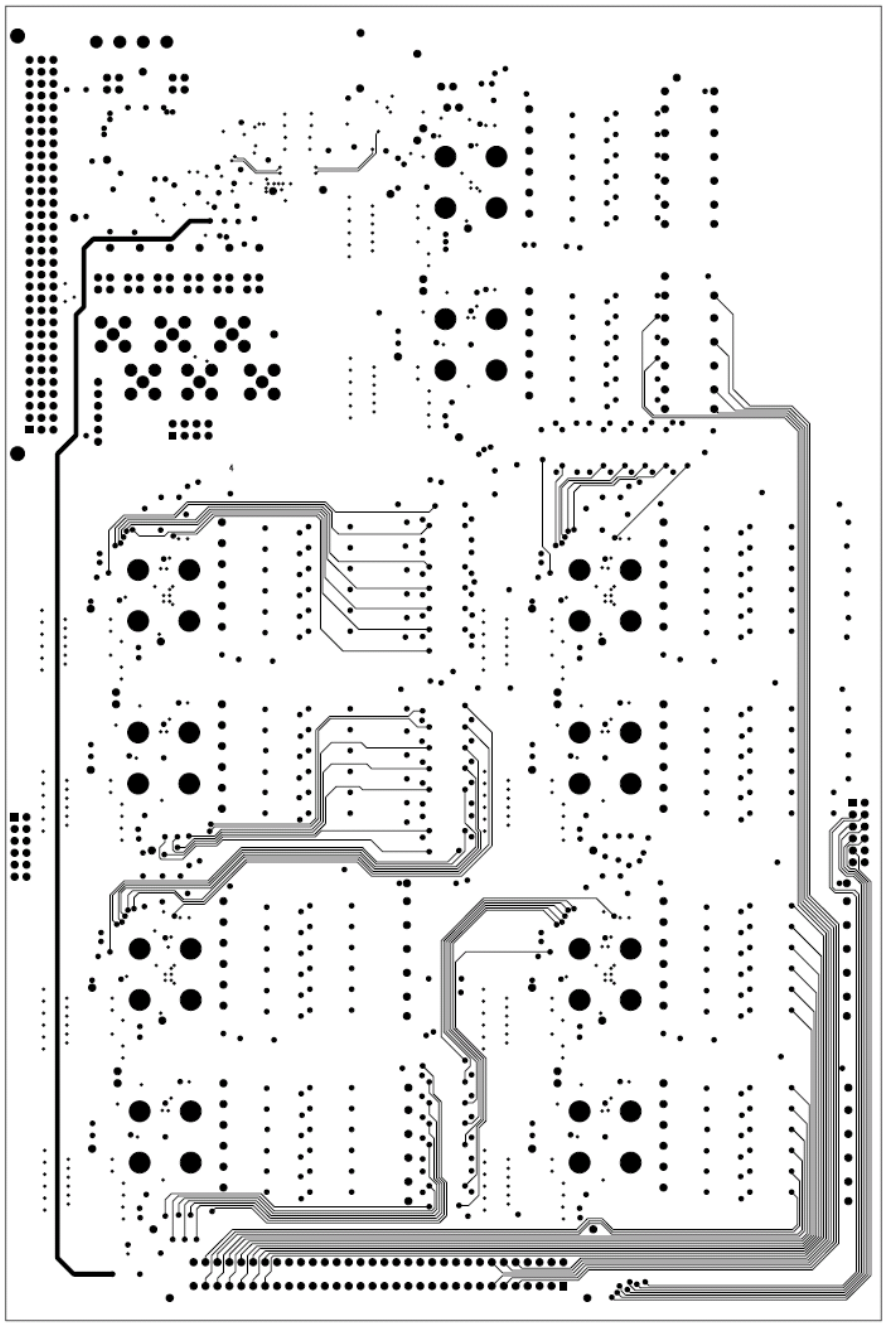
AD7280 DEMO (Rev. A) – Component Side View

Inner Layer 3



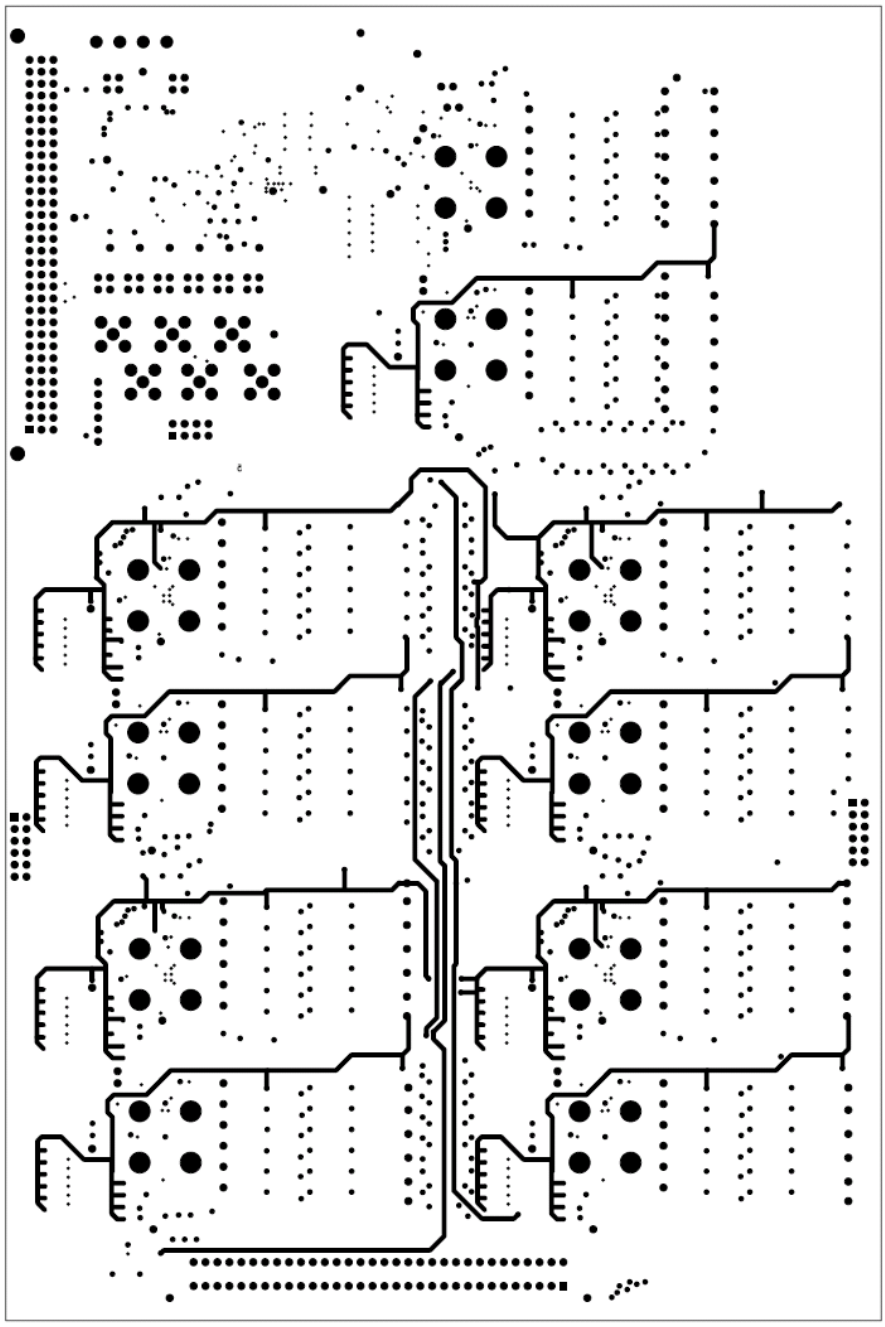
AD7280 DEMO (Rev. A) – Component Side View

Inner Layer 4



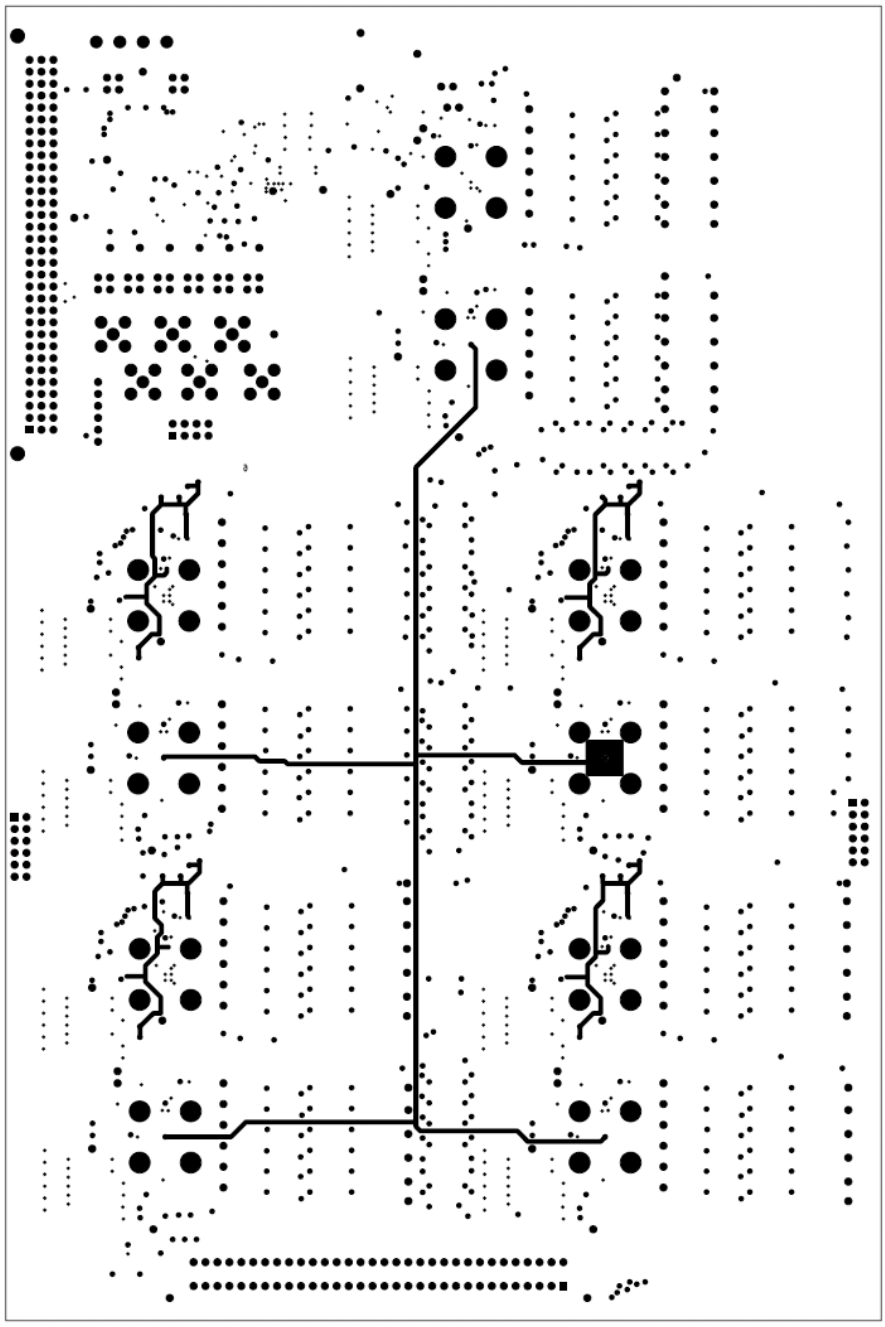
AD7280 DEMO (Rev. A) – Component Side View

Inner Layer 5



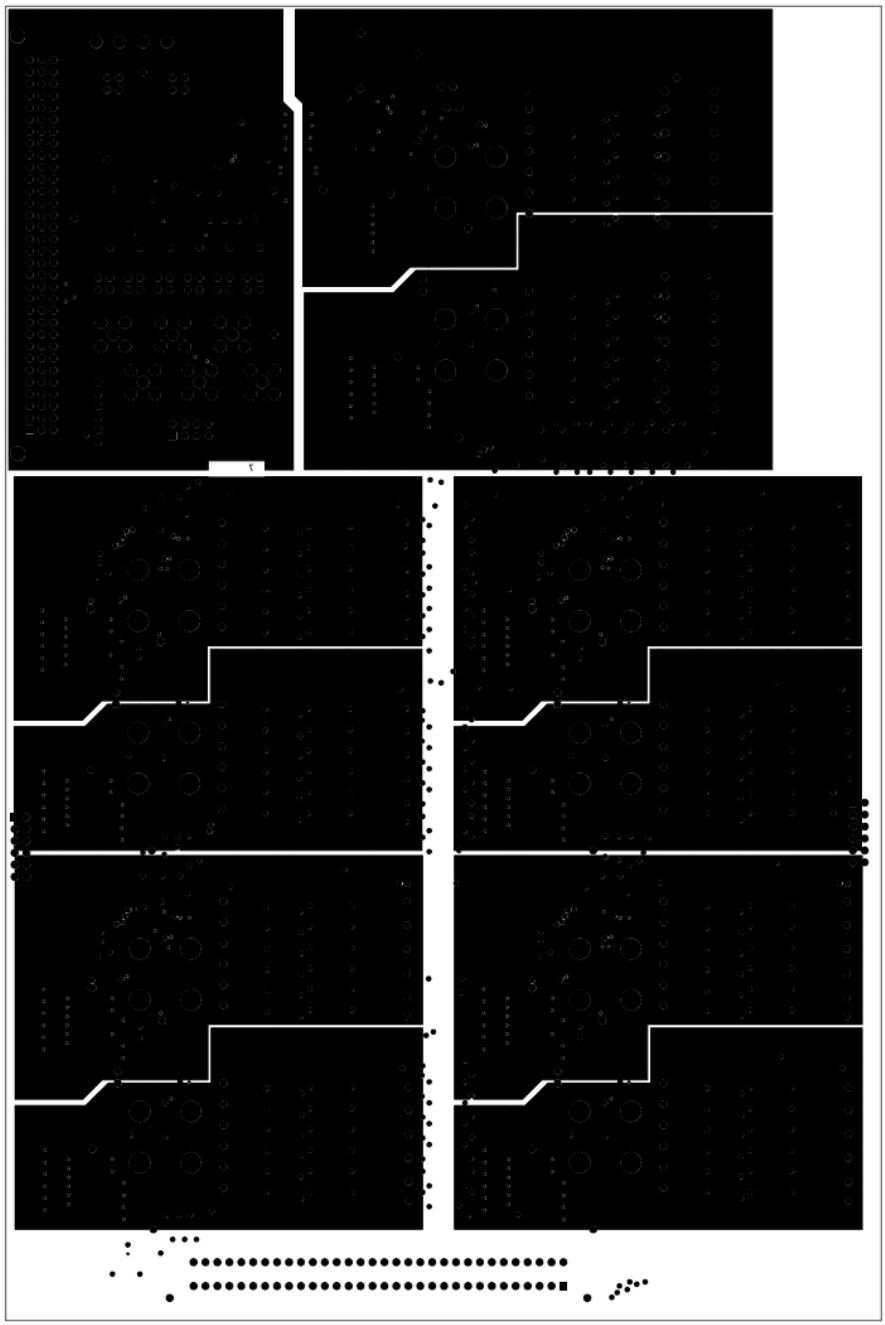
AD7280 DEMO (Rev. A) – Component Side View

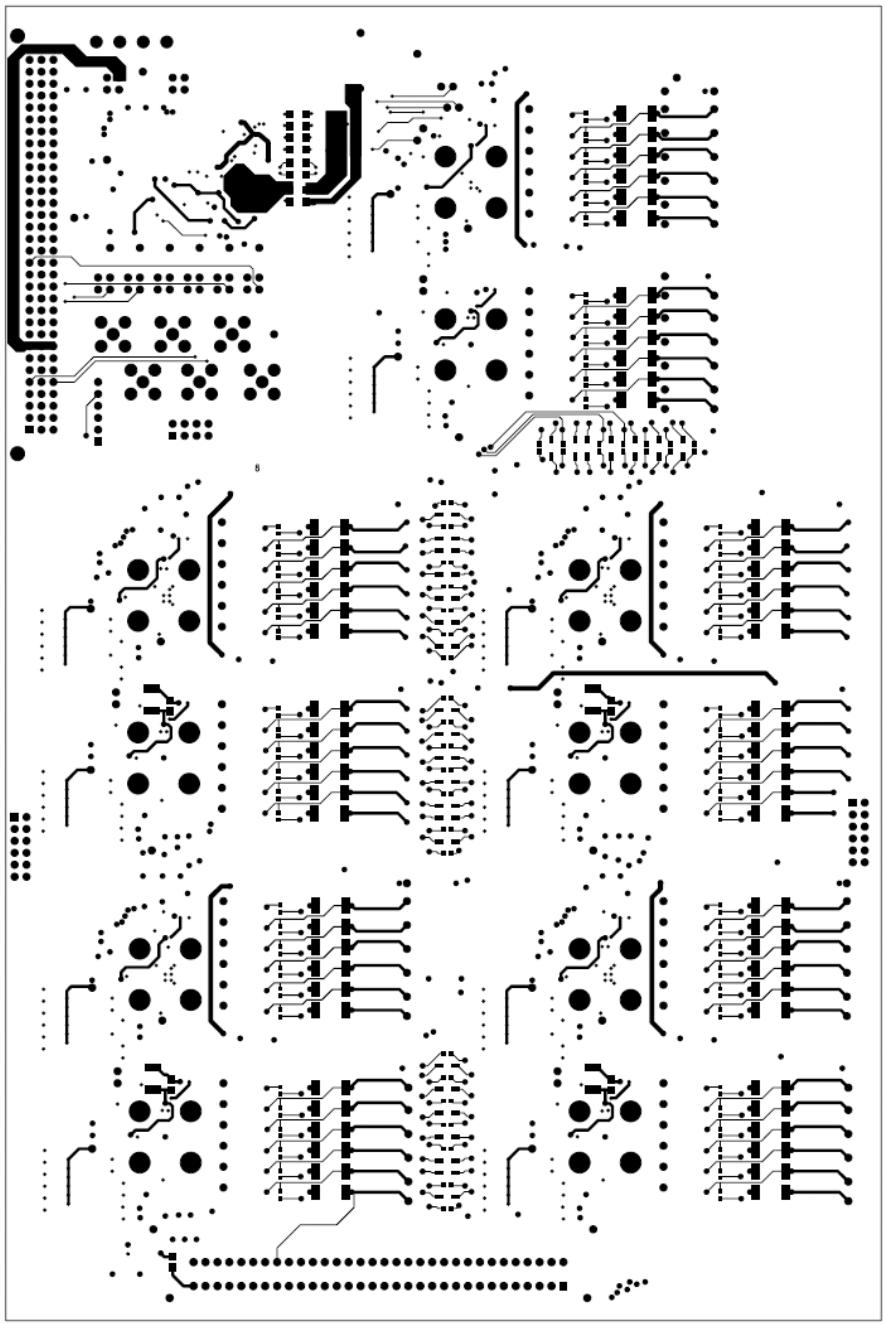
Inner Layer 6



AD7280 DEMO (Rev. A) – Component Side View

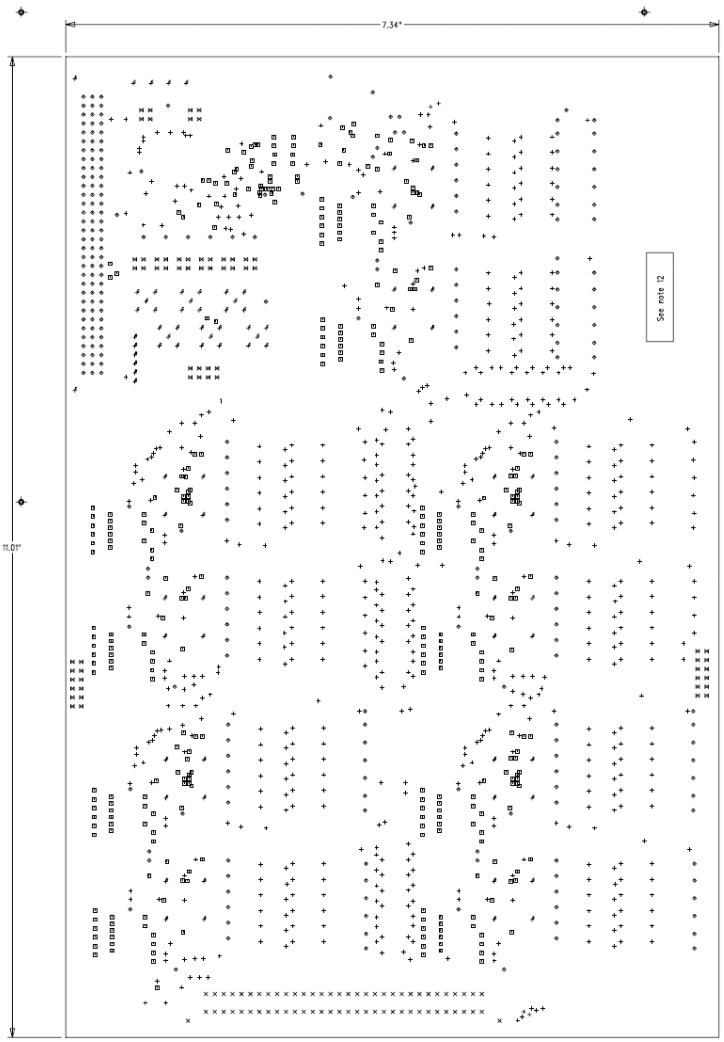
Ground Plane – Layer 7





AD7280 DEMO (Rev. A) – Component Side View

Solder Side – Layer 8



AD7280 DEMO (Rev. A) – Component Side View

Component Side – Layer 1

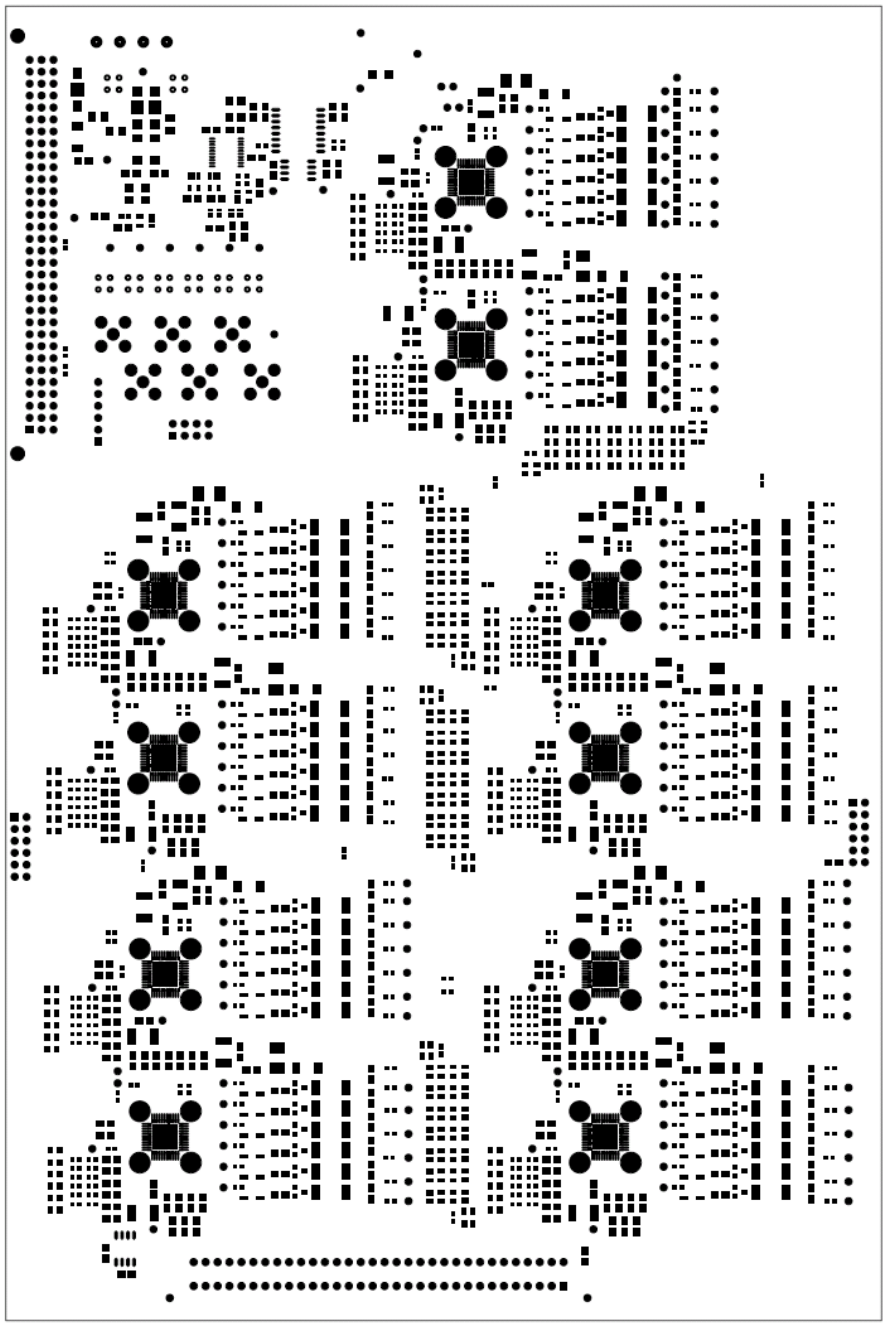
Drill Drawing

1. Material: Eight layer, FR4 glass epoxy laminate, 0.062" +/–.007" thick.
   1 oz. copper clad – external layers. 1 oz. copper clad – internal layers.
   Material to be RoHS compliant.
2. Plated thru holes and the conductive pattern electroplated with 0.001" min.
   thick copper. Terminal areas and plated thru holes to be ENIG plated.
   Soldermask over bare copper.
3. Finished Board ENIG
4. Datum for (x,y) co-ordinate drill files at this hole.
5. Processing tolerances:
   A. Conductive pattern front to back registration within .005" total.
   B. Minimum annular ring surrounding holes: 0.002"
   C. Finished conductive pattern within .002" of true size.
6. Warp and twist within .010 inch per inch
7. Dimensions are for the finished part.
8. Solder Mask: Liquid photo imagable solder mask over bare copper (smobc),
   colour green, both sides using the patterns provided. No mask is permitted
   on the terminal areas. Soldermask to etch registration within .003" total.
9. Screening: Screen component outlines and nomenclature using indelible white
   ink on the primary and secondary sides (as required). Nomenclature shall be
   legible. Screen to etch registration within .020" total.
10. Surfaces: Punched or machined surfaces 125 micro inches rms max.
11. Break all sharp edges .015" R max.
12. Manufacturer to add identification marks, UL Vendor ID Number, date code (YY/WW format)
    in this area on the component side silkscreen.
13. PCB Size = 11.01 Inches X 7.34 Inches. Tolerance +/– 10%

SIZE	QTY	SYM	PLATED	TOL
0.635	663	+	YES	–
1.0668	66	×	YES	–
0.3048	352	□	YES	–
1.0414	261	◇	YES	–
0.9398	64	⋈	YES	–
0.889	6	⊞	YES	–
1.524	34	⊞	YES	–
4.445	40	⊞	NO	–
2.9972	2	⊞	NO	–

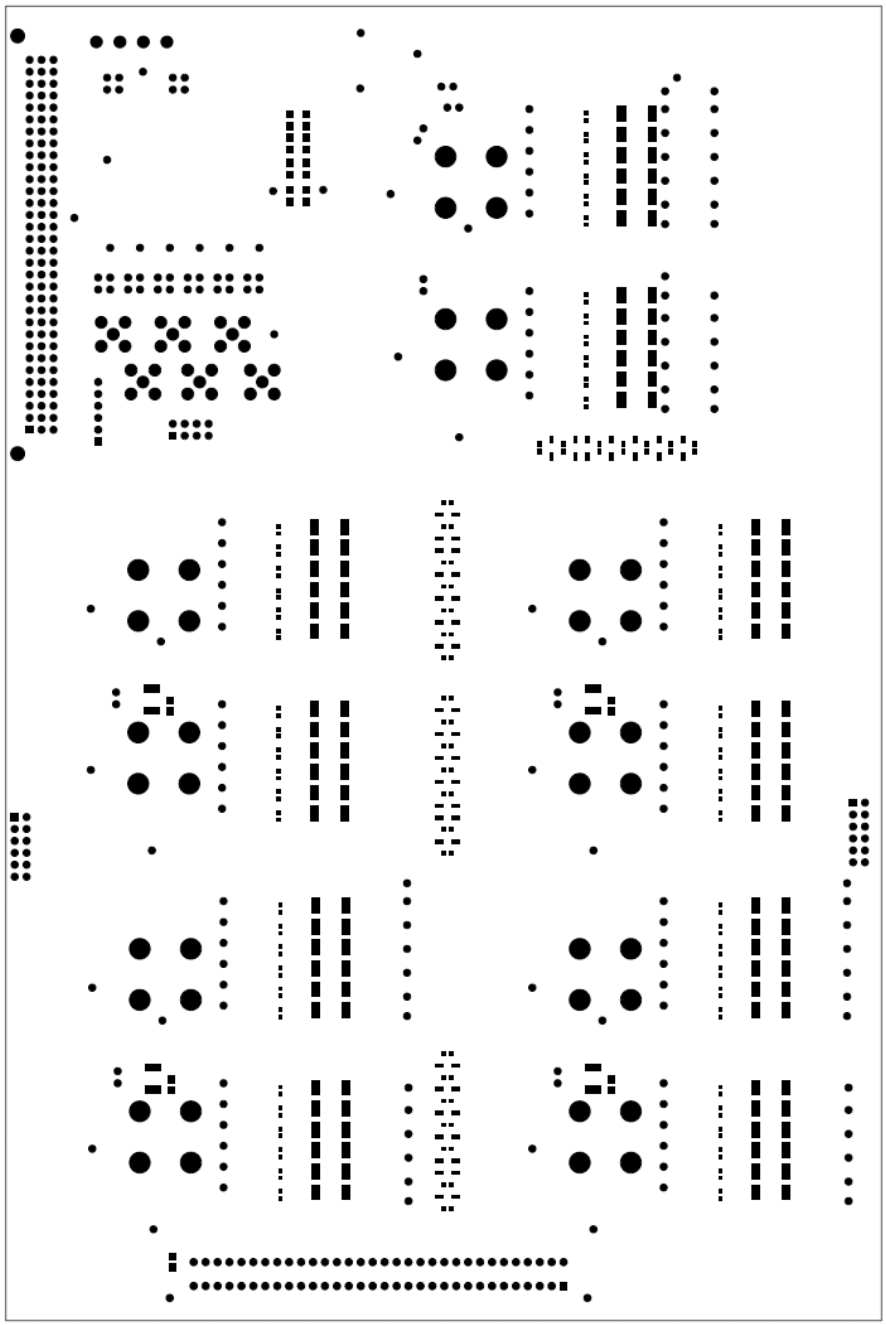
AD7280 DEMO (Rev. A) – Component Side View

Solder Mask – Comp side



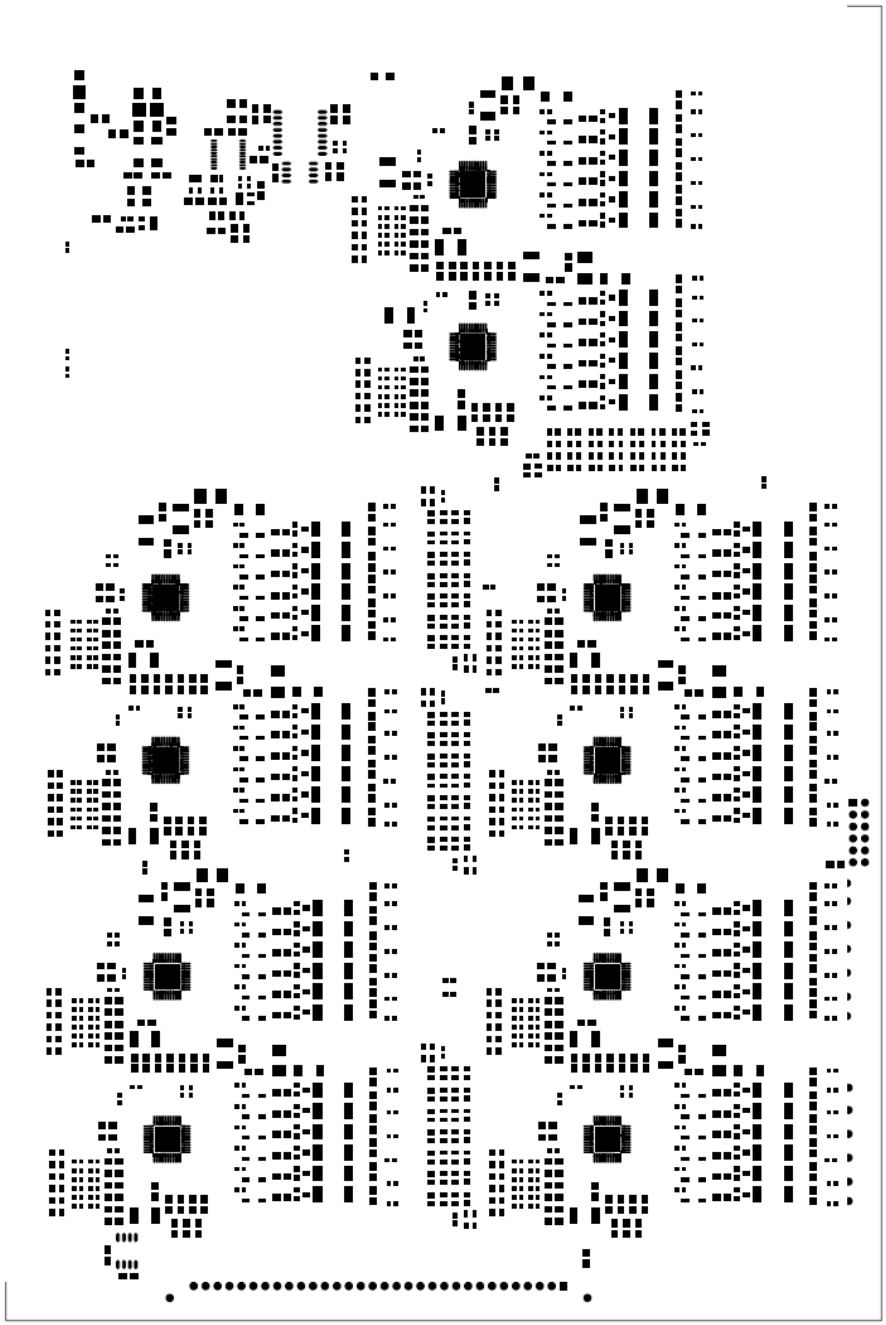
AD7280 DEMO (Rev. A) – Component Side View

Solder Mask – Solder side



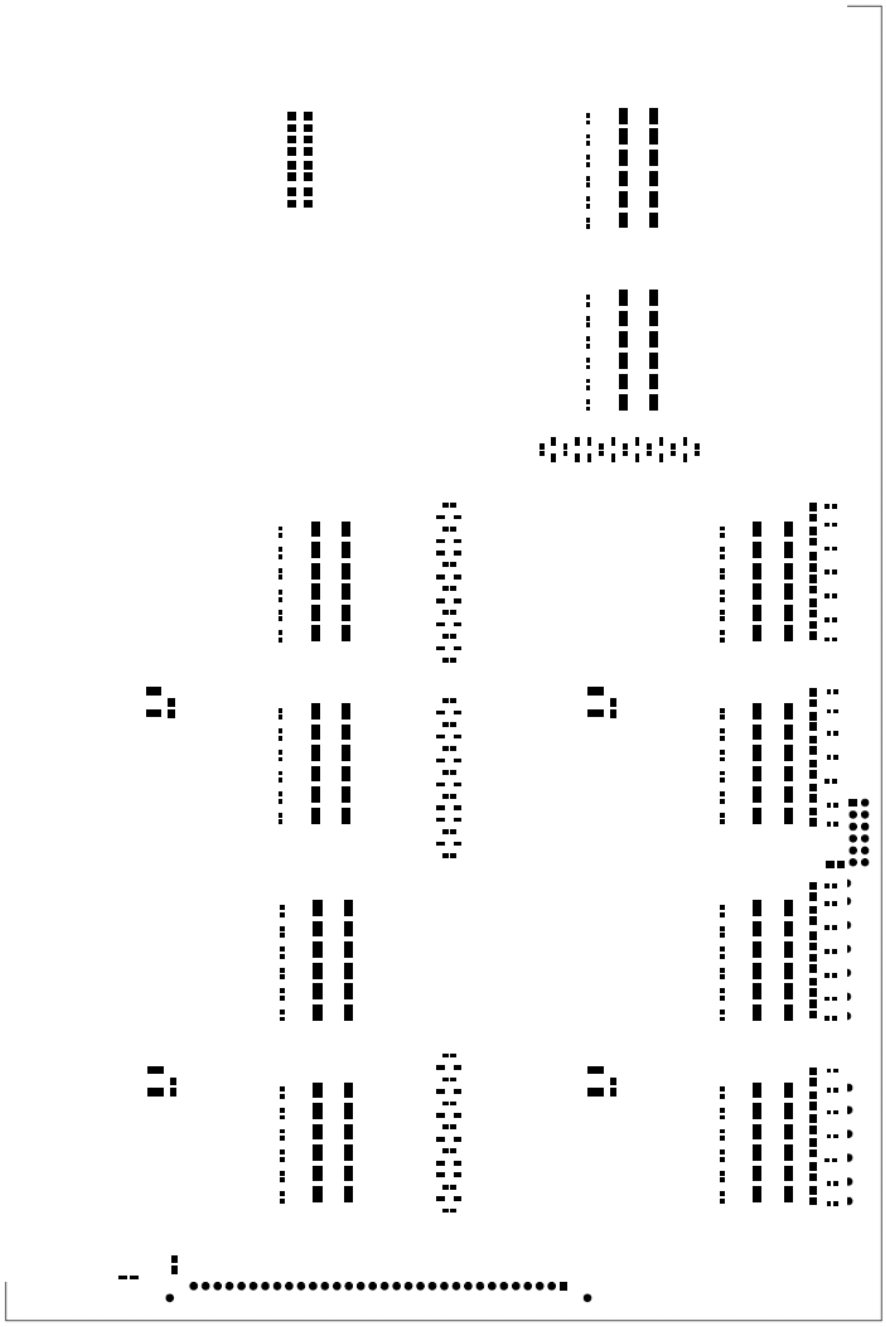
AD7280 DEMO (Rev. A) – Component Side View

Paste Mask – Comp side



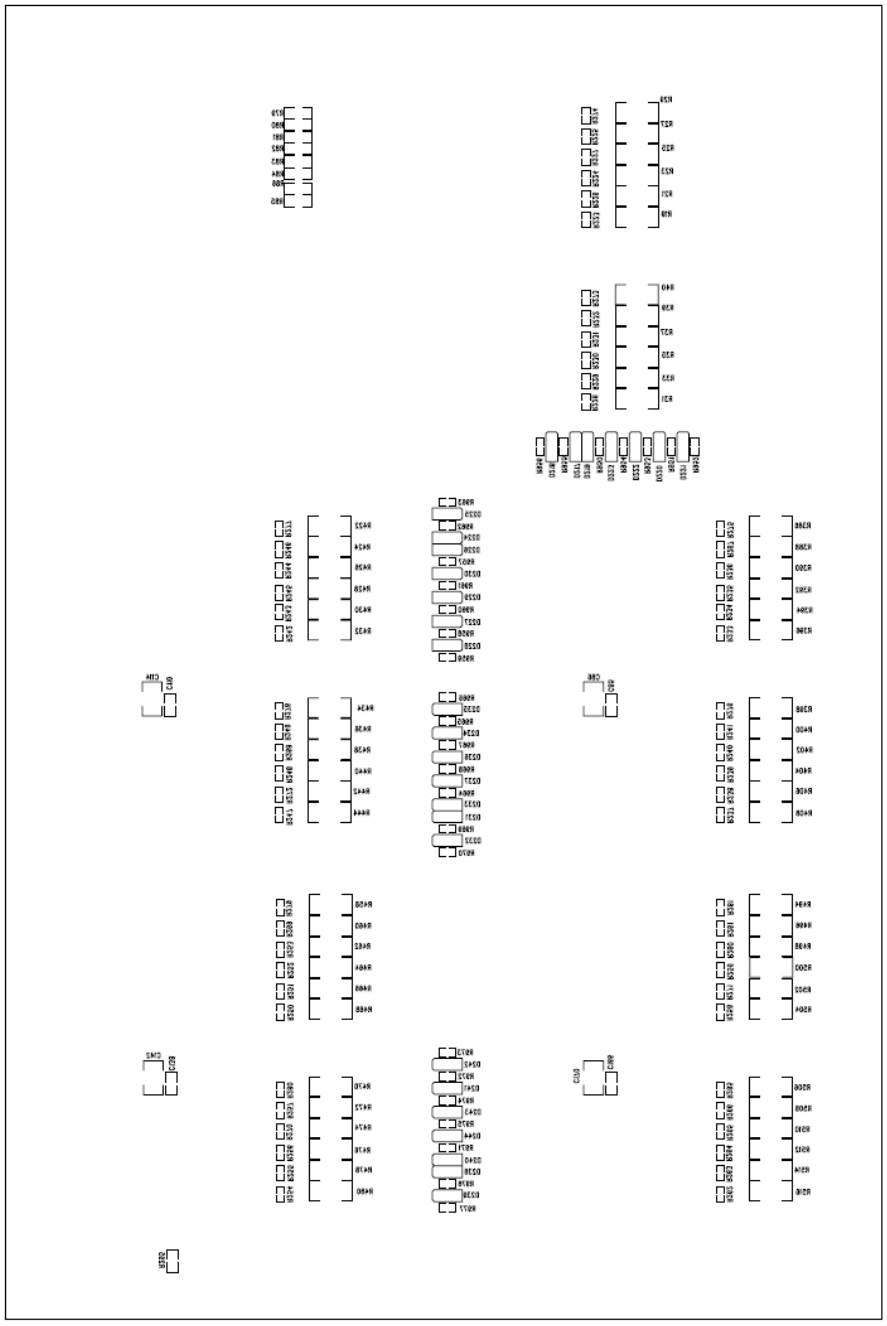
AD7280 DEMO (Rev. A) – Component Side View

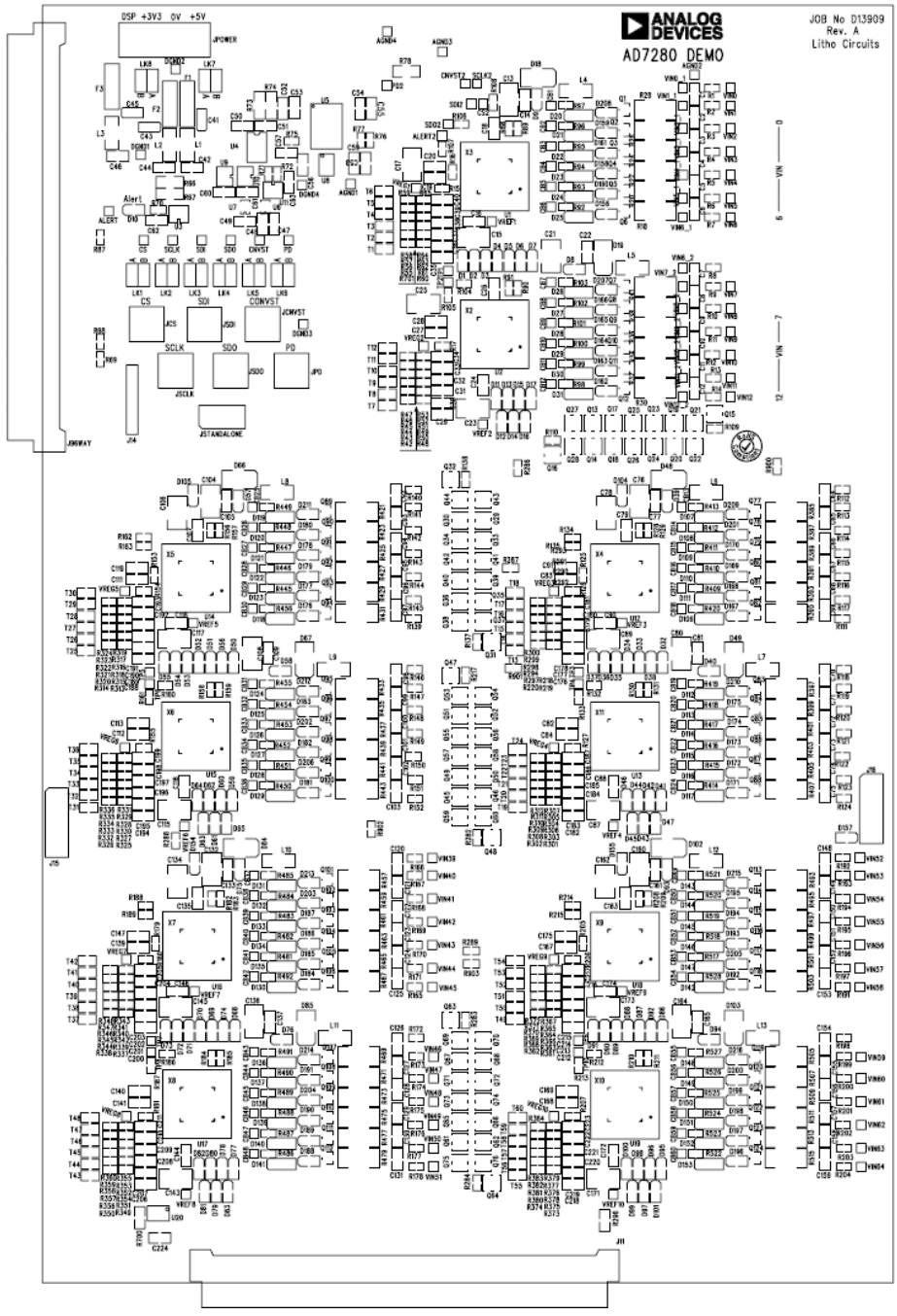
Paste Mask – Solder side



AD7280 DEMO (Rev. A) – Component Side View

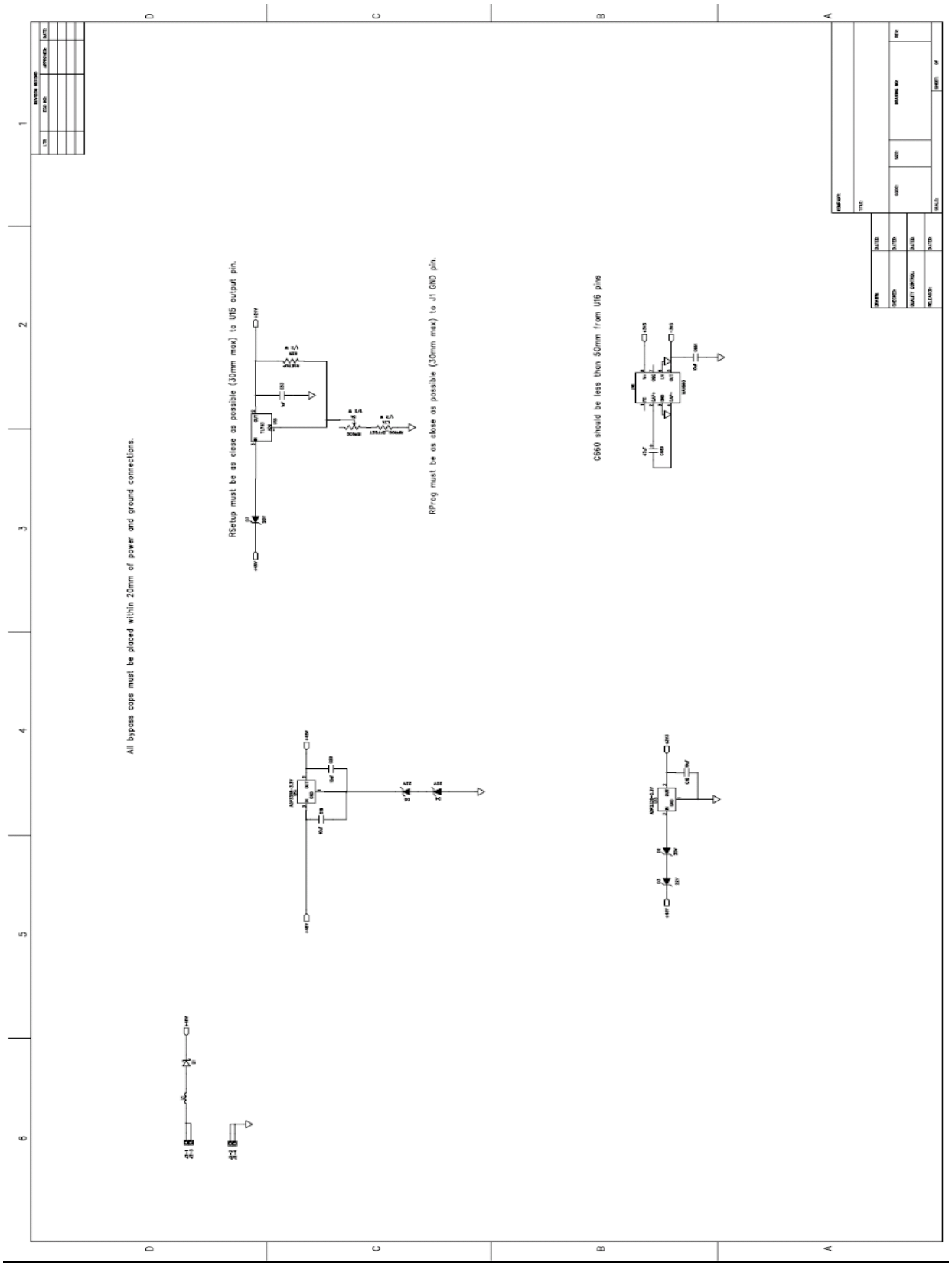
Silkscreen – Solder side

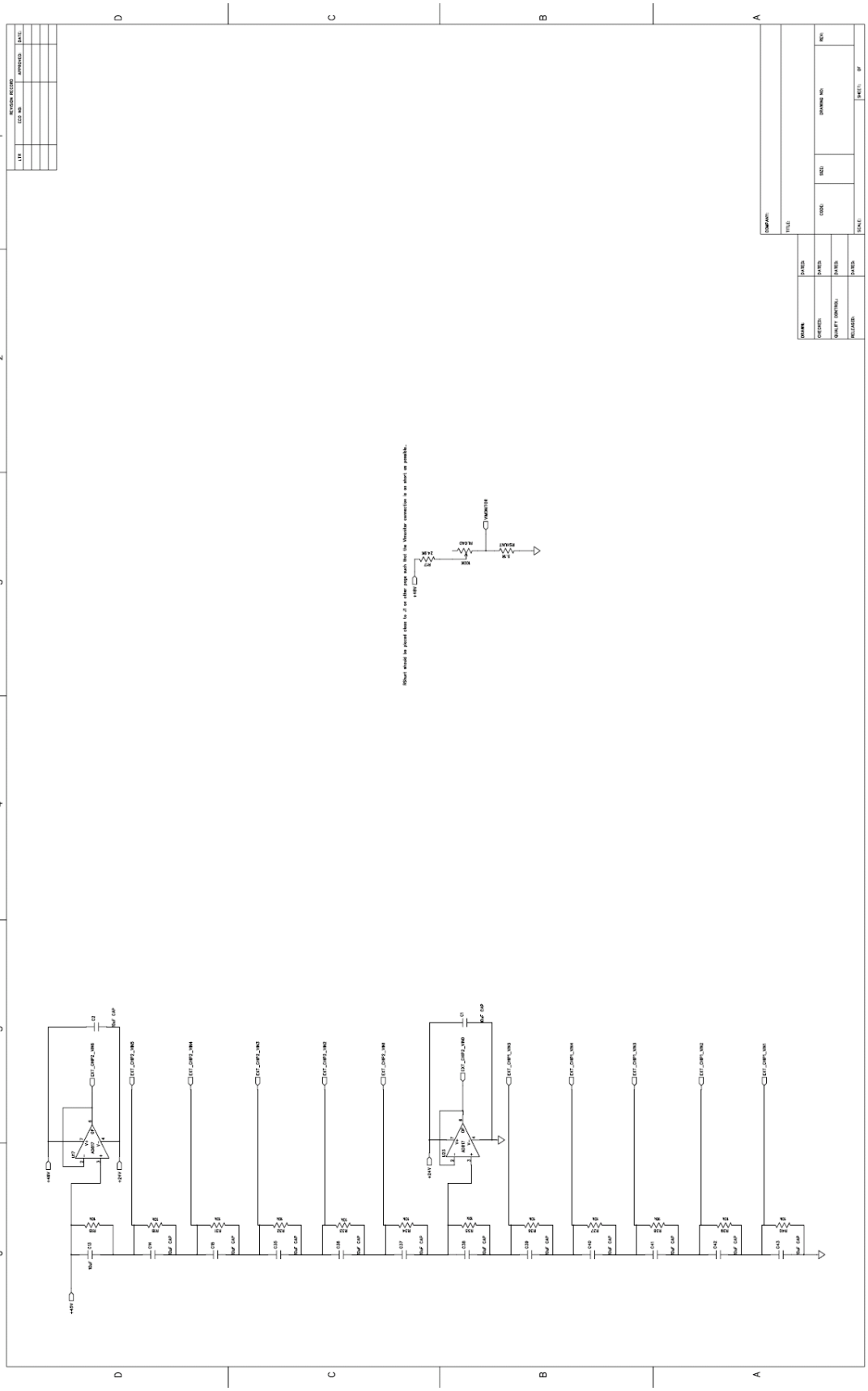


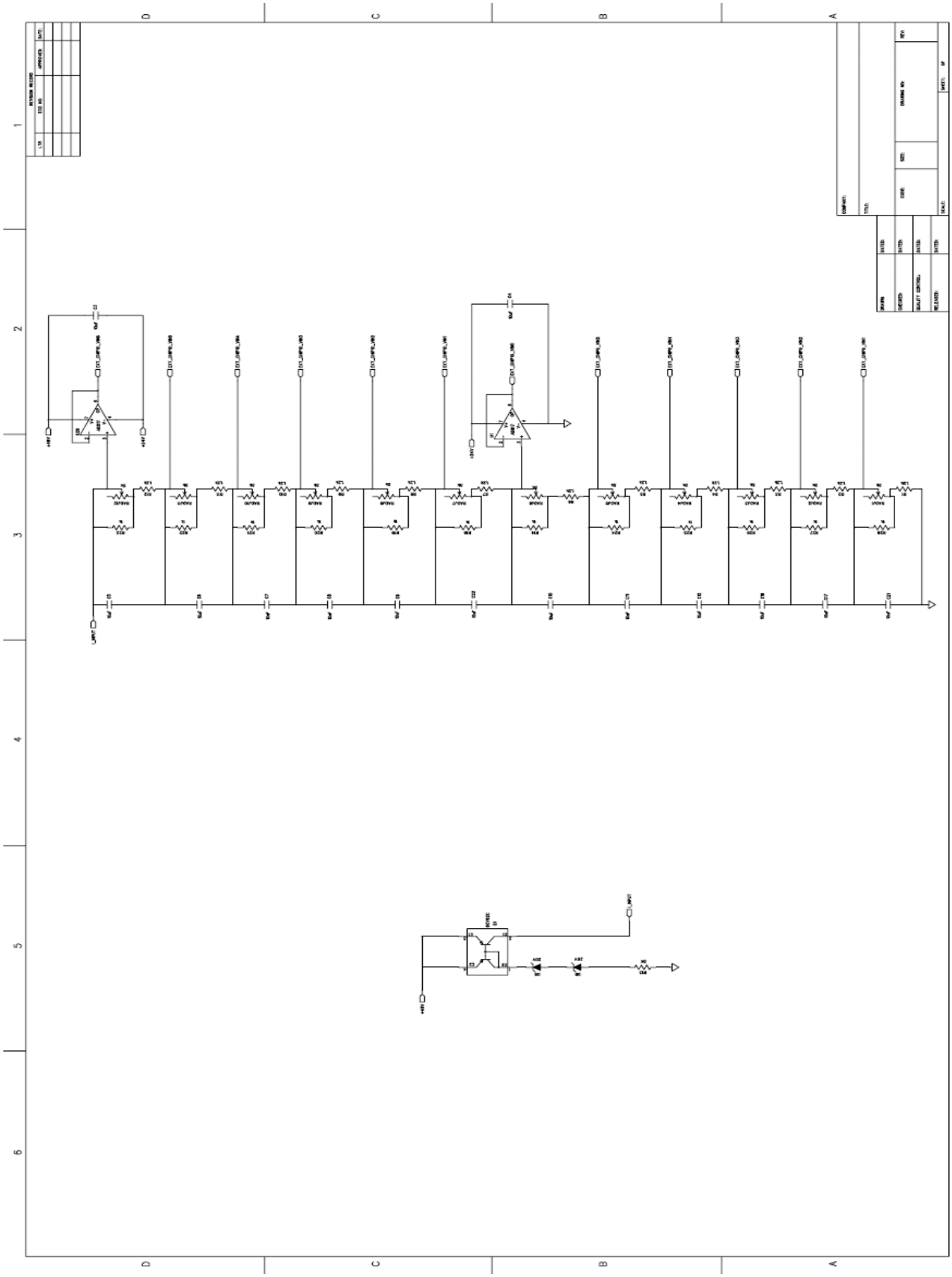


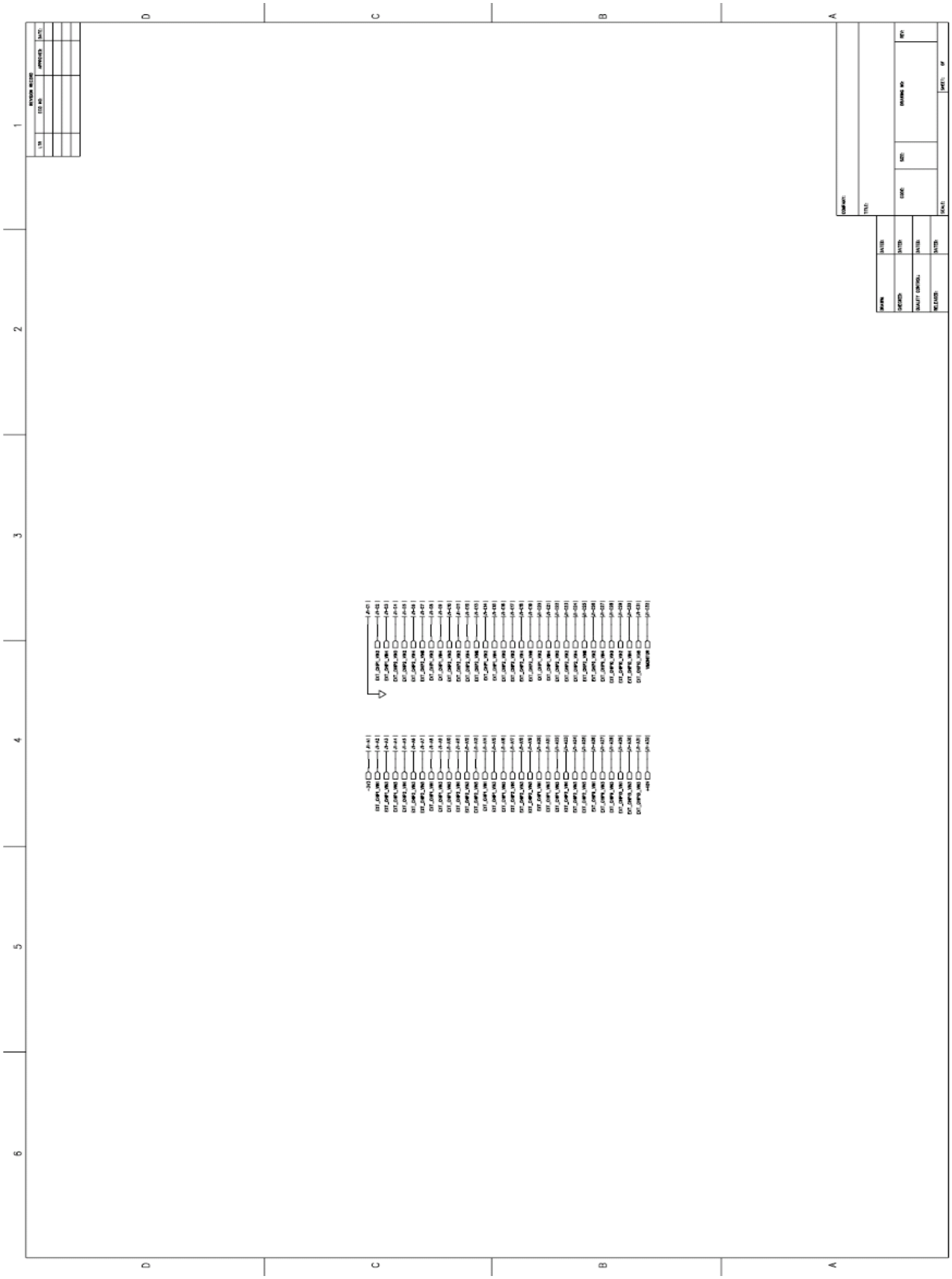
AD7280 DEMO (Rev. A) – Component Side View
Silkscreen – Comp side

9.3. Driver Board Schematics









9.4. Datasheets

9.4.1. AD7280 Lithium Ion Battery Monitoring System Datasheet

ANALOG DEVICES

Lithium Ion Battery Monitoring System

Preliminary Technical Data

AD7280

FEATURES

12-bit ADC, 1us per channel conversion time
6 Analog Input Channels, CM range 0.5V to 27.5V
6 Temperature Measurements Inputs.
On Chip Voltage Regulator
Cell Balancing Interface
Daisy Chain Interface
3 ppm Reference
Low Quiescent Current
High Input Impedance
Serial Interface with Alert Function
1 SPI interface for up to 300 channels
On Chip Registers for Channel Sequencing
V_{DD} Operating Range 7.5V to 30V
Temperature Range -40 °C to 105°C
48 lead LQFP and LFCSP Packages

APPLICATIONS

Lithium Ion Battery Monitoring
Nickel Metal Hydride Battery Monitoring

FUNCTIONAL BLOCK DIAGRAM

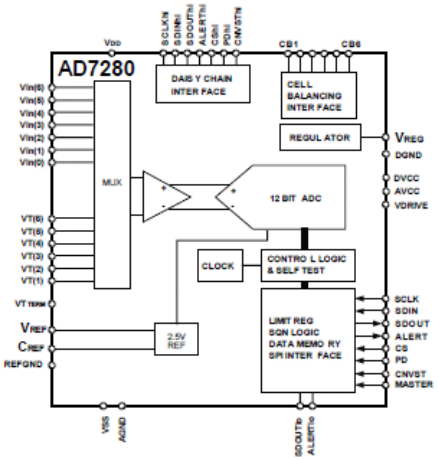


Figure 1

GENERAL DESCRIPTION

The AD7280[1] contains all the functions required for general purpose monitoring of stacked Lithium Ion batteries as used in Hybrid Electric Vehicles. The part has multiplexed analog input and temperature measurement channels for up to six cells of battery management. An internal 3-ppm reference is provided to drive the ADC. The ADC resolution is 12 bits with a 1 Msps throughput rate offering a 1µs conversion time.

The AD7280 operates from just one V_{DD} supply which has a range of 7.5V to 30V (with an absolute max rating of 33V). The part provides 6 pseudo differential analog input channels to accommodate large common mode signals across the full V_{DD} range. Each channel allows an input signal range, Vin(+) – Vin(-), of 0V to 5V. The input pins assume a series stack of 6 cells. In addition the part can accommodate 6 external sensors for temperature measurement.

The AD7280 includes on chip registers which allow a sequence of channel measurements to be programmed to suit the applications requirements.

The AD7280 also includes an Alert function which generates an interrupt output signal if the cell voltages exceed an upper or lower limit defined by the user. The AD7280 has balancing interface outputs designed to control external FET transistors to allow discharging of individual cells.

The AD7280 includes a Built In Self Test feature which internally applies a known voltage to the ADC inputs.

There is a daisy chain interface which allows up to 50 parts to be stacked without the need for individual device isolation.

The AD7280 requires only one supply pin which takes 7mA under normal operation, while converting at 1 Msps.

All this functionality is provided in a 48 pin LQFP or 48 pin LFCSP package operating over a temperature range of –40°C to +105°C.

[1] Patents Pending

Rev. PrD 0708

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

SPECIFICATIONS

V_{DD} = 7.5 V to 30 V, VSS = 0 V, D_{VCC} = A_{VCC} = V_{REG}, V_{DRIVE} = 2.7 V to 5.25 V, T_A = -40°C to 105°C, unless otherwise noted

Table 1.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
DC ACCURACY [Vin(0) to Vin(6)][2]					
Resolution	12			Bits	No Missing Codes
Integral Nonlinearity			±1	LSB	
Differential Nonlinearity			±1	LSB	
Offset Error		1		LSB	
Offset Error Drift		3		ppm/°C	
Offset Error Match		1		LSB	
Gain Error		1		LSB	
Gain Error Drift		2		ppm/°C	
Gain Error Match		1		LSB	
ADC Unadjusted Error[3]		0.05	0.1	%	-40°C to 85°C
		0.08	0.3	%	-40°C to 105°C
Total Unadjusted Error[4]		0.07	0.2	%	-40°C to 85°C
		0.1	0.5	%	-40°C to 105°C
ANALOG INPUTS [Vin(0) to Vin(6)]					
Pseudo Differential Input Voltage					
Vin(n) – Vin(n-1)	1V		$2V_{REF}$	V	
Absolute Input Voltage	V_{CM} - V_{REF}		V_{CM} + V_{REF}	V	
Common Mode Input Voltage	0.5		27.5	V	
DC Leakage Current		±70		nA	$\overline{CNVST}$ pulse every 100ms
Input Capacitance		15		pF	When in track
		3		pF	When in hold
DC ACCURACY [VT1 to VT6][2]					
Resolution	12			Bits	No Missing Codes
Integral Nonlinearity			±1	LSB	
Differential Nonlinearity			±1	LSB	
Offset Error		2		LSB	
Offset Error Drift		2		ppm/°C	
Offset Error Match		2		LSB	
Gain Error		2		LSB	
Gain Error Drift		1.2		ppm/°C	
Gain Error Match		2		LSB	
ADC Unadjusted Error[5]		0.1	0.2	%	-40°C to 85°C
		0.16	0.6	%	-40°C to 105°C
Total Unadjusted Error[6]		0.15	0.4	%	-40°C to 85°C
		0.2	1	%	-40°C to 105°C
ANALOG INPUTS (VT1 to VT6)					
Input Voltage Range	0		$2V_{REF}$	V	
Leakage Current		±70		nA	$\overline{CNVST}$ pulse every 100ms
Input Capacitance		15		pF	When in track
		3		pF	When in hold
DYNAMIC PERFORMANCE					
Common Mode Rejection Ratio [CMRR]		-75		dB	Up to 10kHz ripple frequency

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE					
Reference Voltage	2.495	2.5	2.505	V	V_{REF} @ 25°C
Reference Temperature Coefficient		±3	±15	ppm/°C	-40°C to +85°C
Output Voltage Hysteresis		50		ppm	-40°C to +85°C
Long Term Drift		100		ppm/1000 Hours	
Line Regulation		±15		ppm/V	AVDD =7.5V
Turn-On Settling Time		5		ms	V_{REF} = 10uF , C_{REF} = 100nF
REGULATOR OUTPUT					
Input Voltage Range	7.5		30	V	
Output Voltage V_{REG}	4.75	5	5.25	V	
Output Current[7]		1		mA	
Line Regulation		0.4		mV/V	
Load Regulation		2.5		mV/mA	
Output Noise Voltage		700		uV	
Internal Short Protection Limit		20		mA	For a 10 Ohm short
CELL BALANCING OUTPUTS[8]					
Output High Voltage, V_{OH}	4	5	5.25	V	For a 80pF load, I_{SOURCE} = 40 nA
Output Low Voltage, V_{OL}	0			V	
CB1 Output ramp up time[9]		5		us	For a 80pF load
CB1 Output ramp down time[10]		50		ns	For a 80pF load
CB2-CB6 Output ramp up time[11]		350		us	For a 80pF load
CB2-CB6 Output ramp down time[12]		330		us	For a 80pF load
LOGIC INPUTS					
Input High Voltage, V_{INH}	V_{DRIVE} – 0.2			V	
Input Low Voltage, V_{INL}			0.4	V	
Input Current, I_{IN}			±1	µA	
Input Capacitance, C_{IN}		10		pF	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	V_{DRIVE} – 0.2			V	I_{SOURCE} = 200 µA
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 200 µA
Floating-State Leakage Current			±1	µA	
Floating-State Output Capacitance		5		pF	
Output Coding	Straight natural binary				
POWER REQUIREMENTS					
V_{DD}	7.5		30	V	
During Conversion					
I_{DD}		7	10	mA	V_{DD} = 30 V
Data Readback					
I_{DD}		4	8	mA	V_{DD} = 30 V
Cell Balancing mode					
I_{DD}			2	mA	V_{DD} = 30 V
Software Powerdown Mode					
I_{DD}			1	mA	V_{DD} = 30 V
Full Powerdown Mode					
I_{DD}			4	µA	V_{DD} = 30 V

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
POWER DISSIPATION					
During Conversion			300	mW	V_{DD} = 30 V
Full Powerdown Mode			120	µW	V_{DD} = 30 V

[1] Temperature range is −40°C to +105°C.
[2] For dc accuracy specifications, the LSB size for cell voltage measurements is ($2V_{REF}$-1V)/4096, the LSB size for temperature measurements is $2V_{REF}$/4096.
[3] ADC Unadjusted Error includes the INL of the ADC and the Gain and Offset Errors of the Vin0 to Vin6 input channels.
[4] Total Unadjusted Error includes the INL of the ADC and the Gain and Offset Errors of the Vin0 to Vin6 input channels as well as the temperature coefficient of the 2.5V reference.
[5] ADC Unadjusted Error includes the INL of the ADC and the Gain and Offset Errors of the VT input channels.
[6] Total Unadjusted Error includes the INL of the ADC and the Gain and Offset Errors of the VT input channels as well as the temperature coefficient of the 2.5V reference.
[7] This spec outlines the regulator output current which is available for external use, that is, it does not include the regulator current already being used by the AD7280.
[8] CB output can be set to 0V or 5V with respect to negative terminal of cell being balanced.
[9] CB1 output ramp up time is defined from the rising edge of the CS command until the CB output exceeds 4V with respect to negative terminal of cell being balanced.
[10] CB1 output ramp down time is defined from the falling edge of the CS command until the CB output falls below 50mV with respect to negative terminal of cell being balanced. This specification is defined from the falling edge of CS as any CB outputs which on are switched off for the duration of a CS low pulse and will be switched back on following the rising edge of that CS pulse.
[11] CB2 to CB6 output ramp up time is defined from the rising edge of the CS command until the CB output exceeds 4V with respect to negative terminal of cell being balanced.
[12] CB2 to CB6 output ramp down time is defined from the falling edge of the CS command until the CB output falls below 50mV with respect to negative terminal of cell being balanced. This specification is defined from the falling edge of CS as any CB outputs which on are switched off for the duration of a CS low pulse and will be switched back on following the rising edge of that CS pulse.

TIMING SPECIFICATIONS

V_{DD} = 7.5 V to 30 V, VSS = 0 V, D_{VCC} = A_{VCC} = V_{REG}, V_{DRIVE} = 2.7 V to 5.25 V, T_A = -40°C to 105°C, unless otherwise noted.[1]

Table 2.

Parameter	Limit at T_{MIN}, T_{MAX}		Unit	Test Conditions/Comments
	2.7 V ≤ V_{DRIVE} < 4.75 V	**4.75 V ≤ V_{DRIVE} ≤ 5.25 V**		
t_{CONV}	610	610	ns max	ADC Conversion time
t_{DELAY}	50	50	ns max	Propogation delay between adjacent parts on the Daisy Chain
f_{SCLK}	10	10	kHz min	Frequency of serial read clock
	1	1	MHz max	
t_{QUIET}	200	200	ns min	Minimum quiet time required between the end of serial read and the start of the next conversion
t_1	10	10	ns min	Minimum $\overline{CONVST}$ low pulse
t_2	10	10	ns min	$\overline{CS}$ falling edge to SCLK rising edge
t_3	10	10	ns max	Delay from $\overline{CS}$ falling edge until SDO is three-state disabled
t_4	5	5	ns min	SDI setup time prior to SCLK falling edge
t_5	3	3	ns min	SDI hold time after SCLK falling edge
t_6[2]	20	14	ns max	Data access time after SCLK falling edge
t_7	7	7	ns min	SCLK to data valid hold time
t_8	0.3 × t_{SCLK}	0.3 × t_{SCLK}	ns min	SCLK high pulse width
t_9	0.3 × t_{SCLK}	0.3 × t_{SCLK}	ns min	SCLK low pulse width
t_{10}	10	10	ns min	$\overline{CS}$ rising edge to SCLK rising edge
t_{11}	10	10	ns max	$\overline{CS}$ rising edge to SDO high impedance

[1] Sample tested during initial release to ensure compliance. All input signals are specified with t_R = t_F = 5 ns (10% to 90% of V_{DRIVE}) and timed from a voltage level of 1.6 V. All timing specifications given are with a 25 pF load capacitance.
[2] The time required for the output to cross 0.4 V or 2.4 V.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted

Table 3.

Parameter	Rating
V_{DD} to AGND	−0.3 V to +33 V
V_{SS} to AGND	−0.3 V to +0.3 V
Vin0 to Vin5 Voltage to AGND	V_{SS} − 0.3 V to V_{DD} + 0.3 V
Vin6 Voltage to AGND	V_{DD} to V_{DD} + 1 V
CB1 Output to AGND	−0.3 V to DV_{CC} + 0.3 V
CB2 to CB6 Output to AGND	−0.3 V to V_{DD} + 0.3 V
VT1 to VT6 Voltage to AGND	−0.3 V to AV_{CC} + 0.3 V
AV_{CC} to AGND, DGND	−0.3 V to +7 V
DV_{CC} to AV_{CC}	−0.3 V to +0.3 V
DV_{CC} to DGND	−0.3 V to +7 V
V_{DRIVE} to AGND	−0.3 V to DV_{CC}
AGND to DGND	−0.3 V to +0.3 V
Digital Input Voltage to DGND	−0.3 V to V_{DRIVE} + 0.3V
Digital Output Voltage to GND	−0.3 V to V_{DRIVE} + 0.3V
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
LQFP Package	
θ_{JA} Thermal Impedance	76.2°C/W
θ_{JC} Thermal Impedance	17°C/W
LFCSP Package	
θ_{JA} Thermal Impedance	54°C/W
θ_{JC} Thermal Impedance	15°C/W
Pb-free Temperature, Soldering Reflow	260(+0)°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTIONAL DESCRIPTIONS

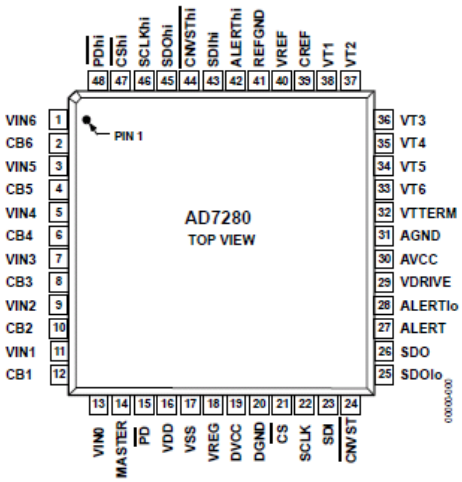


Figure 2.

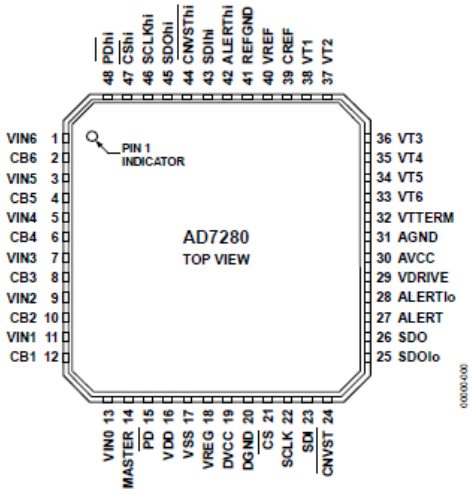


Figure 3.

Table 4.

Pin No.	Mnemonic	Description
1, 3, 5, 7, 9, 11, 13	Vin6 to Vin0	Analog Input 0 to Analog Input 6. Analog input 0 should be connected to the base of the series connected battery cells. Analog Input 1 should be connected to the top of cell 1, Analog Input 2 should be connected to the top of cell 2, etc. The Analog Inputs are multiplexed into the on-chip track-and-hold allowing the potential across each cell to be measured.
2, 4, 6, 8, 10, 12	CB6 to CB1	Cell Balance Outputs. These provide a voltage output which can be used to supply the gate drives of a cell balancing transistor network. Each CB(n) output provides a 5V voltage output referenced to the absolute voltage of Cell(n-1).
14	MASTER	Voltage Input. In an application with 2 or more AD7280s Daisy Chained the MASTER pin of the AD7280 connected directly to the DSP or uP should be connected to the V_{DD} supply pin through a 10kOhm resistor. The MASTER pin on the remaining AD7280s in the application should be tied to their respective V_{SS} supply pins through 10kOhm resistors.
15	$\overline{PD}$	Power down Input. This input is used to power down the AD7280. When acting as master the $\overline{PD}$ input is supplied from the DSP/uP. When acting as a slave on the Daisy Chain the $\overline{PD}$ input should be connected to the $\overline{PDhi}$ output of the AD7280 immediately below it in potential in the Daisy Chain. This input can also be tied to V_{CC} and the power down initiated through the serial interface.
16	V_{DD}	Positive Power Supply Voltage. This is the positive supply voltage for the high voltage analog input structure AD7280. The supply must be greater than a minimum voltage of 7.5 V. In an application monitoring the cell voltages of up to 6 series connected battery cells the supply voltage may be supplied directly from the cell with the highest potential. The maximum voltage which can be applied between V_{DD} and V_{SS} is 30V. Place 10 µF and 100 nF decoupling capacitors on the V_{DD} pin.
17	V_{SS}	Negative Power Supply Voltage. This is the negative supply voltage for the high voltage analog input structure of the AD7280. This input should be at the same potential as the AGND voltage.
18	V_{REG}	Analog Voltage output, 5V. The internally generated V_{REG} voltage, which provides the supply voltage for the ADC core, is available on this pin for use external to the AD7280. Place 10 µF and 100 nF decoupling capacitors on the V_{REG} pin.
19	DV_{CC}	Digital Supply Voltage, 4.75 V to 5.25 V. The DV_{CC} and AV_{CC} voltages should ideally be at the same potential. For best performance, it is recommended that the DV_{CC} and AV_{CC} pins be shorted together, to ensure that the voltage difference between them never exceeds 0.3 V even on a transient basis. This supply should be decoupled to DGND. Place 100 nF decoupling capacitors on the DV_{CC} pin. The DV_{CC} supply pin should be connected to the V_{REG} output

20	DGND	Digital Ground. Ground reference point for all digital circuitry on the AD7280. The DGND and AGND voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
21	$\overline{CS}$	Chip select Input. When acting as a master, that is the Master pin of the AD7280 is connected to V_{DD}, the $\overline{CS}$ input is used to frame the input and output data on the SPI. The $\overline{CS}$ input also frames the input and output data on the Daisy Chain Interface when the MASTER input of the AD7280 is connected to V_{SS}.
22	SCLK	Serial Clock Input. When acting as master the SCLK input is supplied from the DSP/uP. When acting as a slave on the Daisy Chain this input should be connected to the SCLKhi output of the AD7280 immediately below it in potential in the Daisy Chain.
23	SDI	Serial Data Input. Data to be written to the on-chip registers is provided on this input and is clocked into the AD7280 on the falling edge of SCLK. When acting as master this is the data input of the SPI interface. When acting as a slave on the Daisy Chain this input acepts data from the SDOhi output of the AD7280 immediately below it in potential in the Daisy Chain.
24	$\overline{CNVST}$	Convert Start Input. The conversion is initiated on the falling edge of CONVST. When acting as master the $\overline{CNVST}$ pulse is supplied from the DSP/uP. When acting as a slave on the Daisy Chain this input should be connected to the $\overline{CNVST}$hi output of the AD7280 immediately below it in potential in the Daisy Chain. This input can also be tied to V_{CC} and the conversion initiated through the serial interface.
25	SDOlo	Serial Data Output in Daisy Chain mode. This output should be connected to the SDIhi input of the AD7280 immediately below it in potential on the Daisy Chain. The data from each AD7280 in the Daisy Chain will be passed through the SDOlo outputs and SDIhi inputs of each AD7280 in the chain and supplied to the uP/DSP through the SDO output of the master AD7280.
26	SDO	Serial Data Output. The conversion output data or the register output data is supplied to this pin as a serial data stream. The bits are clocked out on the falling edge of the SCLK input, and 24 SCLKs are required to access the data. The data is provided MSB first. In a Daisy Chain application the SDO output of the master AD7280 should be connected to the uP/DSP. The SDO outputs of the remaining AD7280s in the chain should be terminated to V_{SS} through a 1kΩ resistor. The data from each AD7280 in the Daisy Chain will be passed through the SDOlo outputs and SDIhi inputs of each AD7280 in the chain and supplied to the uP/DSP through the SDO output of the master AD7280. 24 SCLKs are required for each AD7280 in the chain to access the data.
27	ALERT	Digital Output. Flag to indicate over voltage, under voltage, over temperature or under temperature. The ALERT output of the master AD7280 should be connected to the uP/DSP. The ALERT outputs of the remaining AD7280s in the chain should be be terminated to V_{SS} through a 1kΩ resistor..
28	ALERTlo	Alert Output in Daisy Chain mode. The alert signal from each AD7280 in the Daisy Chain will be passed through the ALERTlo outputs and ALERThi inputs of each AD7280 in the chain and supplied to the uP/DSP through the ALERT output of the master AD7280. This input should be connected to the ALERThi input of the AD7280 immediately below it in potential on the Daisy Chain.
29	V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin determines at what voltage the interface operates. This pin should be decoupled to DGND. The voltage range on this pin is 2.7 V to 5.25 V and may be different to the voltage at AV_{CC} and DV_{CC}, but should never exceed either by more than 0.3 V.
30	AV_{CC}	Analog Supply Voltage, 4.75 V to 5.25 V. This is the supply voltage for the ADC core. The AV_{CC} and DV_{CC} voltages should ideally be at the same potential. For best performance, it is recommended that the DV_{CC} and AV_{CC} pins be shorted together, to ensure that the voltage difference between them never exceeds 0.3 V even on a transient basis. This supply should be decoupled to AGND. Place 100 nF decoupling capacitors on the AV_{CC} pin. The AV_{CC} supply pin should be externally connected to the V_{REG} output.
31	AGND	Analog Ground. Ground reference point for all analog circuitry on the AD7280. This input should be at the same potential as the base of the series connected battery cells. The AGND and DGND voltages ideally should be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
32	VT_{TERM}	Thermistor termination resistor input.
33 to 38	VT6 to VT1	Voltage temperature input from potential divider with thermistor.
39	C_{REF}	A 100 nF decoupling capacitor to REFGND should be placed on this pin.
40	V_{REF}	Reference Output. The on-chip reference is availble on this pin for use external to the AD7280. The nominal internal reference voltage is 2.5V, which appears at the pin. A 10 µF decoupling capacitor to REFGND is recommended on this pin.
41	REFGND	Reference Ground. This is the ground reference point for the internal bandgap reference circuitry on the AD7280. The REFGND voltage should be at the same potential as the AGND voltage.
42	ALERThi	Alert Input in Daisy Chain mode. Flag to indicate over voltage, under voltage, over temperature or under temperature in Daisy Chain mode. The alert signal from each AD7280 in the Daisy Chain will be passed through the ALERTlo outputs and ALERThi inputs of each AD7280 in the chain and supplied to the uP/DSP through the ALERT output of the master AD7280. This input should be connected to the ALERTlo output of the AD7280 immediately above it in potential on the Daisy Chain.

43	SDIhi	Serial Data Input in Daisy Chain mode. The data from each AD7280 in the Daisy Chain will be passed through the SDOlo outputs and SDIhi inputs of each AD7280 in the chain and supplied to the uP/DSP through the SDO output of the master AD7280. This input should be connected to the SDOlo output of the AD7280 immediately above it in potential on the Daisy Chain.
44	$\overline{\text{CNVSThi}}$	Conversion Start Output in Daisy Chain mode. The convert start signal from the uP/DSP supplied to the $\overline{\text{CNVST}}$ input of the Master AD7280 is passed through each AD7280 by means of the $\overline{\text{CNVST}}$ input and the $\overline{\text{CNVSThi}}$ output. This output should be connected to the $\overline{\text{CNVST}}$ pin of the AD7280 immediately above it in potential on the Daisy Chain.
45	SDOhi	Serial Data Output in Daisy Chain mode. The Serial Data input from the uP/DSP supplied to the SDI input of the Master AD7280 is passed through each AD7280 by means of the SDI input and the SDOhi output. This output should be connected to the SDI input of the AD7280 immediately above it in potential on the Daisy Chain.
46	SCLKhi	Serial Clock Output in Daisy Chain mode. The clock signal from the uP/DSP supplied to the SCLK input of the Master AD7280 is passed through each AD7280 by means of the SCLK input and the SCLKhi output. This output should be connected to the SCLK input of the AD7280 immediately above it in potential in the Daisy Chain.
47	$\overline{\text{CShi}}$	Chip select Output in Daisy Chain mode. The chip select signal from the uP/DSP supplied to the $\overline{\text{CS}}$ input of the Master AD7280 is passed through each AD7280 by means of the $\overline{\text{CS}}$ input and the $\overline{\text{CShi}}$ output. This output should be connected to the $\overline{\text{CS}}$ input of the AD7280 immediately above it in potential on the Daisy Chain.
48	$\overline{\text{PDhi}}$	Power down Output in Daisy Chain mode. The power down signal from the uP/DSP supplied to the $\overline{\text{PD}}$ input of the Master AD7280 is passed through each AD7280 by means of the $\overline{\text{PD}}$ input and the $\overline{\text{PDhi}}$ output. This output should be connected to the $\overline{\text{PD}}$ pin of the AD7280 immediately above it in potential on the Daisy Chain.

TERMINOLOGY

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale (a point 1 LSB below the first code transition) and full scale (a point 1 LSB above the last code transition).

Offset Code Error
This applies to straight binary output coding. It is the deviation of the first code transition (00 ... 000) to (00 ... 001) from the ideal, that is, AGND + 1 LSB.

Gain Error
This applies to straight binary output coding. It is the deviation of the last code transition (111 ... 110) to (111 ... 111) from the ideal (that is, $4 \times V_{REF} - 1$ LSB, $2 \times V_{REF} - 1$ LSB, $V_{REF} - 1$ LSB) after adjusting for the offset error.

ADC Unadjusted Error
ADC Unadjusted Error includes integral nonlinearity errors, offset and gain errors of the ADC and measurement channel.

Total Unadjusted Error (TUE)
This is the maximum deviation of the output code from the ideal. Total Unadjusted Error includes integral nonlinearity errors, offset and gain errors and reference drift.

Offset Error Match
This is the difference in zero code error across all 6 channels.

Gain Error Match
The difference in gain error across all 6 channels.

Track-and-Hold Acquisition Time
The track-and-hold amplifier returns to track mode at the end of a conversion. Track-and-hold acquisition time is the time required for the output of the track-and-hold amplifier to reach its final value, within ±½ LSB, after the end of conversion.

Common Mode Rejection Ration (CMRR)
CMRR is defined as the ratio of the power in the ADC output at full-scale frequency, f, to the power of a 100 mV sine wave applied to the common-mode voltage of the Vin(n) and Vin(n-1) frequency, f_S, as

$$CMRR\ (\text{dB}) = 10 \log (Pf/Pf_S)$$

where Pf is the power at frequency f in the ADC output, and Pf_S is the power at frequency f_S in the ADC output.

Power Supply Rejection Ration (PSRR)
Variations in power supply affect the full-scale transition but not the converter's linearity. PSRR is the maximum change in the full-scale transition point due to a change in power supply voltage from the nominal value.

Reference Voltage Temperature Coefficient

Reference voltage temperature coefficient is derived from the maximum and minimum reference output voltage (V_{REF}) measured at T_{MIN}, T(25°C), and T_{MAX}. It is expressed in ppm/°C using the following equation:

$$TCV_{REF}(ppm/°C) = \frac{V_{REF}(Max) - V_{REF}(Min)}{V_{REF}(25°C) \times (T_{MAX} - T_{MIN})} \times 10^6$$

where:
$V_{REF}(Max)$ = Maximum V_{REF} at T_{MIN}, T(25°C), or T_{MAX}
$V_{REF}(Min)$ = Minimum V_{REF} at T_{MIN}, T(25°C), or T_{MAX}
$V_{REF}(25°C)$ = V_{REF} at +25°C
T_{MAX} = +85°C
T_{MIN} = –40°C

Output Voltage Hysteresis

Output voltage hysteresis, or thermal hysteresis, is defined as the absolute maximum change of reference output voltage after the device is cycled through temperature from either

T_HYS+ = +25°C to T_{MAX} to +25°C
$T\_HYS–$ = +25°C to T_{MIN} to +25°C

It is expressed in ppm using the following equation:

$$V_{HYS}(ppm) = \left| \frac{V_{REF}(25°C) - V_{REF}(T\_HYS)}{V_{REF}(25°C)} \right| \times 10^6$$

where:
$V_{REF}(25°C)$ = V_{REF} at 25°C
$V_{REF}(T\_HYS)$ = Maximum change of V_{REF} at T_HYS+ or T_HYS–.

THEORY OF OPERATION

CIRCUIT INFORMATION

The AD7280 is a Lithium Ion battery monitoring chip with the ability to monitor the voltage and temperature of 6 series connected battery cells. The AD7280 also provides an interface which can be used to control transistors for cell balancing.

The V_{DD} and V_{SS} supplies required by the AD7280 can be taken from the upper and lower voltages of the series connected battery cells. An internal V_{REG} rail is generated from the supply voltage which provides power for the ADC and the internal interface circuitry. This V_{REG} voltage is available on an output pin for use external to the AD7280.

The AD7280 consists of a high voltage input multiplexer, a low voltage input multiplexer and a 12 bit ADC. The high voltage multiplexer allows up to 6 series connected Lithium Ion battery cells to be measured. The low voltage multiplexer allows the temperature of each cell to be measured. A single $\overline{CNVST}$ signal is required to initiate conversions on all 12 channels, that is 6 voltage and 6 temperature channels. Alternatively the conversion can be initiated through the rising edge of $\overline{CS}$ on the SPI interface. Each conversion result is stored in a results register (See Register section). On power-up, the $\overline{CNVST}$ signal is the default option, this can be changed by writing to the CONTROL register. The default sequence of conversions completed following the $\overline{CNVST}$ signal, or software convert start, is all 6 voltage channels followed by all 6 temperature channels. Two further conversion sequences may be selected by the user, 6 voltage channels followed by 3 temperature channels or just 6 voltage channels. The conversion sequence may be selected by writing to the CONTROL register.

Each voltage and temperature measurement requires a minimum of 1us to acquire and complete a conversion. Depending on the external components connected to the analog inputs of the AD7280 additional acquisition time may be required. A higher acquisition time may be selected through the CONTROL register. The user may also select the averaging option through the CONTROL register. This option allows the user to complete 2, 4 or 8 averages on each cell voltage and cell temperature measurement. The averaged conversion results are stored in the results registers. On power-up the default combined acquisition and conversion time will be 1us, with the averaging register set to zero, that is a single conversion per channel.

The results of the voltage and temperature conversions are read back via the 4 wire Serial Peripheral Interface. The SPI interface is also used to write to and read data from the internal registers.

The AD7280 features an ALERT function which is triggered if the voltage conversion results or the temperature conversion results exceed the maximum and minimum voltage thresholds selected by the user. The threshold levels are selected by writing to the internal registers.

The AD7280 provides 6 analog output voltages which can be used to control external transistors as part of a cell balancing circuit. Each Cell Balance output provides a 0V or 5V voltage, with respect to the potential on base of each individual cell, which can be applied to the gate of the external cell balancing transistors.

The AD7280 features a daisy chain interface. Individual AD7280s can monitor the cell voltages and temperatures of 6 cells, a chain of AD7280s can be used to monitor the cell voltages and temperatures of a larger number of cells. The conversion data from each AD7280 in the chain passes to the system controller via a single standard serial interface. Control data can similarly be passed via the standard serial interface up the chain to each individual AD7280s

The AD7280 includes an on-chip 2.5V reference. The reference voltage is available for use external to the AD7280.

CONVERTER OPERATION

The AD7280 consists of a high voltage input multiplexer, a low voltage input multiplexer and a 12 bit ADC.

The high voltage multiplexer selects which pair of analog inputs, Vin0 to Vin6, are to be converted. The voltage of each individual cell is measured by converting the difference between adjacent analog inputs, that is, Vin1 – Vin0, Vin2 – Vin1, etc. This is illustrated in Figure 4 and Figure 5. The conversion results for each cell may be accessed after the programmed conversion sequence is complete.

The second multiplexer selects which voltage temperature input, VT1 to VT6, is to be converted. The conversion results for each cell may be accessed after the programmed conversion sequence is complete.

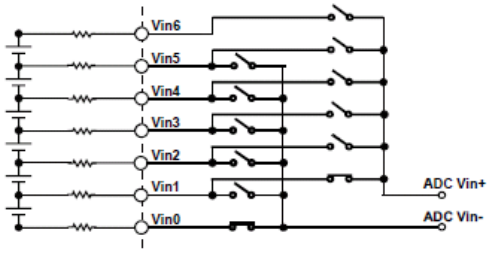


Figure 4. MUX Configuration During Vin1-Vin0 Sampling

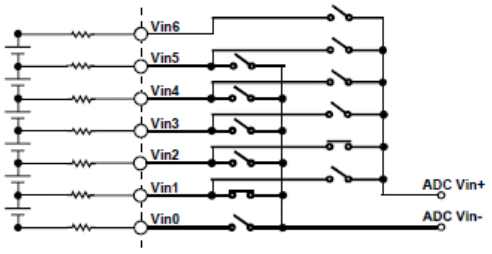


Figure 5. MUX Configuration During Vin2-Vin1 Sampling

The ADC is a 12-bit successive approximation analog-to-digital converter. The converter is composed of a comparator, SAR, some control logic and 2 capacitive DACs. Figure 6 shows a simplified schematic of the converter. During the acquisition phase switches SW1, SW2 and SW3 are closed. The sampling capacitor array acquires the signal on the input during this phase.

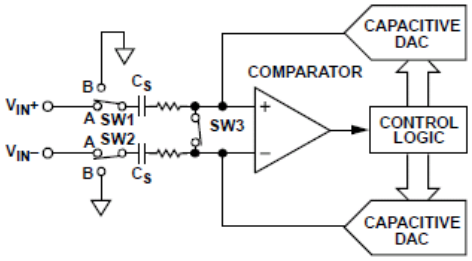


Figure 6. ADC Configuration During Acquisition Phase

When the ADC starts a conversion (Figure 7), SW3 opens and SW1 and SW2 move to position B, causing the comparator to become unbalanced. The control logic and capacitive DACs are used to add and subtract fixed amounts of charge to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. This output code is then stored in the appropriate register for the input that has been converted.

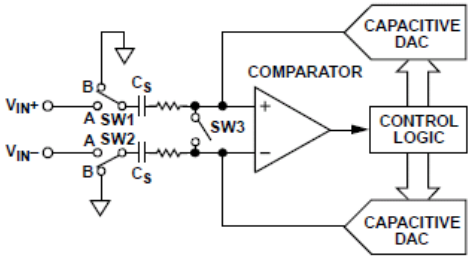


Figure 7. ADC Configuration During Conversion Phase

ANALOG INPUT STRUCTURE

Figure 8 shows the equivalent circuit of the analog input structure of the AD7280. The two diodes provide ESD protection. The resistors are lumped components made up of the on-resistance of the input multiplexer and the track-and-hold switch. The value of these resistors is typically about 300Ω. Capacitor C1 can primarily be attributed to pin capacitance while Capacitor C2 is the sampling capacitor of the ADC. The total lumped capacitance of C1 and C2 is approximately 13 pF.

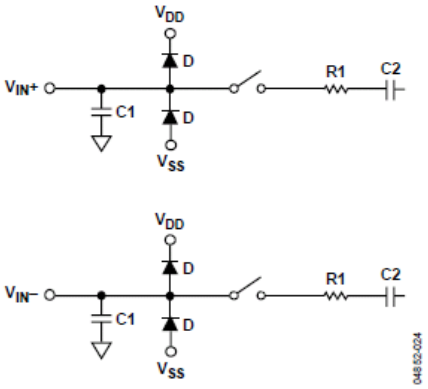


Figure 8. Equivalent Analog Input Circuit

TRANSFER FUNCTION

The output coding of the AD7280 is straight binary. The designed code transitions occur at successive integer LSB values (that is, 1 LSB, 2 LSB, and so on). The LSB size is dependent on whether the voltage or temperature inputs are being measured. The analog input range of the voltage inputs is 1V to 5V, the analog input range of the temperature inputs is 0V to 5V. The ideal transfer characteristic is shown in Figure 9.

Table 5. LSB Sizes for Each Analog Input Range

Selected inputs	Input Range	Full-Scale Range	LSB Size
Voltage	1 V to 5 V	4 V/4096	976 µV
Temperature	0 V to 5 V	5 V/4096	1.22 mV

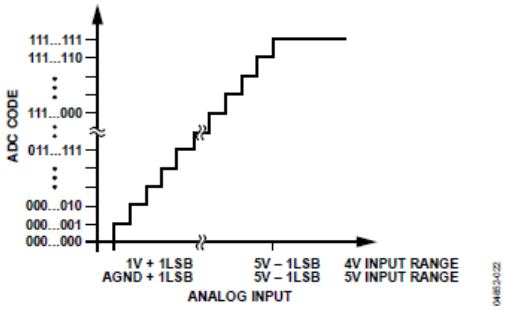


Figure 9. Transfer Characteristic

TYPICAL CONNECTION DIAGRAMS

The AD7280 can be used to monitor 6 battery cells connected in series. A typical configuration for a 6 cell battery monitoring application is shown in Figure 10.

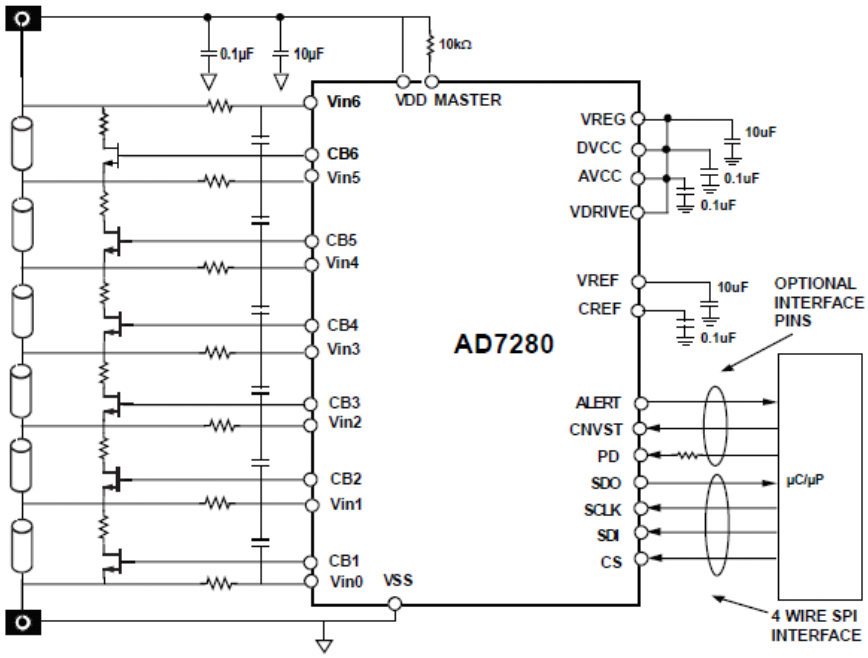


Figure 10. AD7280 Configuration Diagram for 6 Battery Cells

Lithium Ion Battery applications require a significant number of individual cells to provide the required output voltage. Individual AD7280s can monitor the cell voltages and temperatures of 6 series connected cells. The Daisy Chain Interface of the AD7280 allows each individual AD7280 to communicate with another AD7280 immediately above or below it. The daisy chain interface allows the AD7280s to be electrically connected to the battery management chip, as shown in Figure 11 without the need for individual isolation between each AD7280.

Daisy Chain Connection Diagram

As shown in Figure 11 external diodes have been included on the V_{DD} supply to each AD7280 and on each Daisy Chain signal between adjacent AD7280's. These diodes, in combination with the 10kΩ series resistors on the analog inputs, are recommended to prevent damage to the AD7280 in the event of an open circuit in the battery stack.

It is also recommended that a zener diode be placed across the supplies of each AD7280 as shown in Figure 11. This will prevent an over voltage across the supplies of each AD7280 during the initial connection of the daisychain of AD7280s to the battery stack. A voltage rating of 33V is suggested for this zener diode but lower values may also be used to suit the application.

When using a chain of AD7280s it is also recommended that a 100kOhm series resistor be placed on the PD input. This is recommended to limit current into the PD pin in the event that the uP/DSP or isolators are connected before the supplies of the master AD7280.

Please refer to the Daisy Chain Interface Section for a more detailed description of the Daisy Chain Interface.

In an application which includes a safety mechanism, designed to open circuit the Battery Stack, additional isolation will be required between the AD7280 above the break point and the battery management chip.

EMC Considerations

In addition to the standard decoupling capacitors, C2n and C3n, as shown in Figure 11, it is also recommended that an option for additional capacitors, C1n and C4n, be included in the circuit to increase immunity to Electomagnetic Interference. These capacitors, placed on either side of the V_{DD} protection diode, would be used to decouple the V_{DD} supply of each AD7280 with respect to system ground., that is the ground of the master AD7280 in the daisychain.

It is recommended that ferrite beads be included on the battery connections to the V_{DD} and V_{SS} supplies. It is also recommended that pull-down resistors should be used on the ALERT and SDO outputs on each of the slave parts in the AD7280 daisychain.

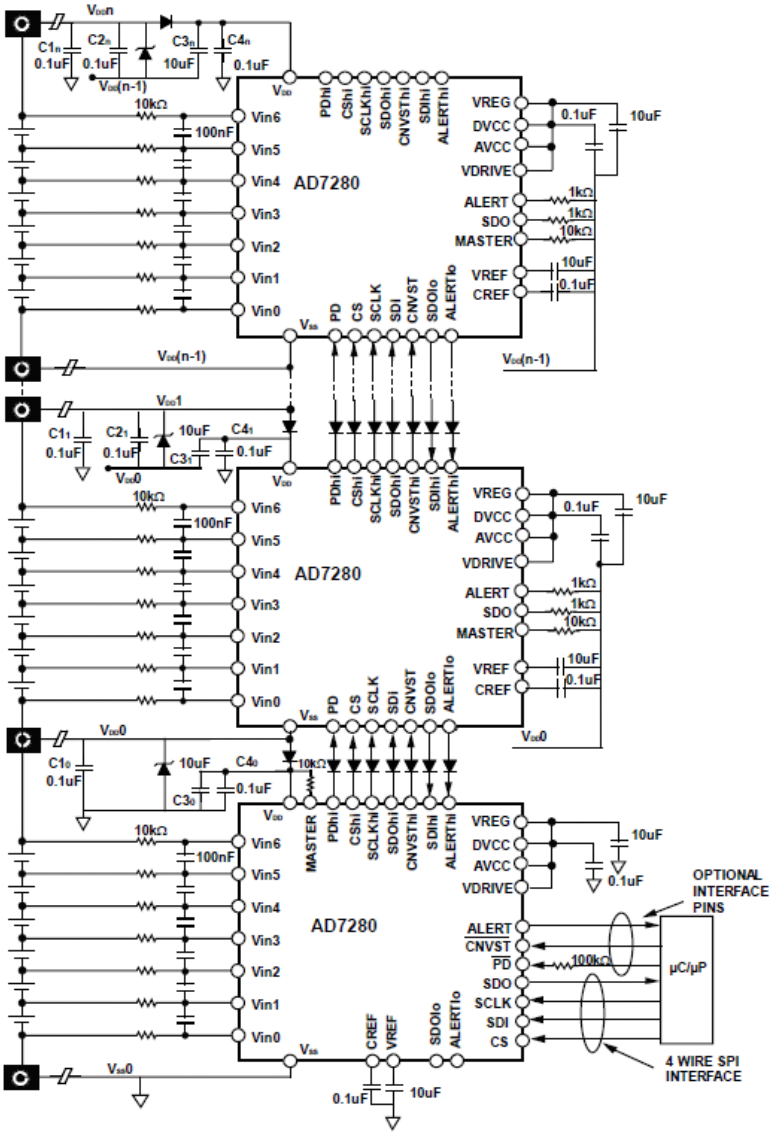


Figure 11. AD7280 Daisy Chain Configuration

*V*DRIVE

The AD7280 also has a V_{DRIVE} feature to control the voltage at which the serial interface operates. V_{DRIVE} allows the ADC to easily interface to both 3 V and 5 V processors. For example, in the recommended configuration the AD7280 is operated with a V_{CC} of 5 V, however the V_{DRIVE} pin could be powered from a 3 V supply, allowing a large dynamic range with low voltage digital processors.

REFERENCE

The internal reference is temperature compensated to 2.5 V ± 5 mV. The reference is trimmed to provide a typical drift of 3 ppm/°C . The internal reference circuitry consists of a 1.2 V band gap reference and a reference buffer. The AD7280 internal reference is available at the V_{REF} pin. The V_{REF} pin should be decoupled to AGND using a 10 µF, or greater, ceramic capacitor. The C_{REF} pin should be decoupled to AGND using a 0.1 µF, or greater, ceramic capacitor. The internal reference is capable of driving an external load of up to 10kOhms.

CONVERTING CELL VOLTAGES AND TEMPERATURES

A conversion may be initiated on the AD7280 using either the $\overline{CNVST}$ input or the serial interface. A single $\overline{CNVST}$ signal is required to initiate conversions on all 12 channels, that is 6 voltage and 6 temperature channels. Alternatively the conversion can be initiated through the rising edge of $\overline{CS}$ on the SPI interface.

When using the $\overline{CNVST}$ input the falling edge of $\overline{CNVST}$ places the track and hold on the voltage inputs Vin0 and Vin1, that is across Cell 1, into hold mode and initiates the conversion. At the end of the first conversion the AD7280 generates an internal End of Conversion signal. This internal EOC will select the next cell voltage inputs for measurement though the multiplexer, that is Vin1 and Vin2. The track-and-hold circuit will acquire the new input voltage and a second internal convert start signal is generated which places the track-and-hold into hold mode and initiates the conversion. This process is repeated until all the selected voltage and temperature cell inputs have been converted. Please refer to Figure 12 and Figure 13. Note, once all selected conversions have been completed voltage inputs Vin0 and Vin1 are again selected through the multiplexer and the voltage across Cell 1 is acquired in preparation for the next conversion request.

By setting bits D15 and D14 in the control register the voltage and temperature cells to be converted are selected. There are four options available.

Table 6. Voltage and Temperature Cell Selection

D15 to D14	Voltage inputs	Temperature Inputs
00	1 to 6	1 to 6
01	1 to 6	1, 3 & 5
10	1 to 6	None
11	ADC Self Test	None

Each voltage and temperature conversion requires a minimum of 1us to acquire and convert the cell voltage or temperature voltage input. For example. when D15 and D14 are set to zero the falling edge of $\overline{CNVST}$ will trigger a series of 12 conversions. This will require a minimum of 12µs to convert all selected measurements. If no temperature conversions are required then Bits D15 and D14 would be set to 10. In this case the conversion request will trigger a series of 6 conversions, requiring a minimum of 6µs.

Track-and-Hold

The track-and-hold on the analog input of the AD7280 allows the ADC to accurately convert an input sine wave of full-scale amplitude to 12-bit accuracy.

Following a completed conversion the AD7280 enters its tracking mode. The time required to acquire an input signal depends on how quickly the sampling capacitor is charged. This in turn will depend on the input impedance and any external components placed on the analog inputs. The default acquisition time of the AD7280 on initial power up is 400 ns. This can be increased in steps of 400ns to 1.6 us to provide flexibility in selecting external components on the analog inputs. The acquisition time is selected by writing to bits D6 and D5 in the CONTROL register.

Table 7.Analog Input Acquisition Time.

D6 to D5	Acquisition Time
00	400 ns
01	800 ns
10	1.2 µs
11	1.6 µs

The acquisition time required is calculated using the following formula:

$$t_{ACQ} = 10 \times ((R_{SOURCE} + R)\ C)$$

where:
C is the sampling capacitance, the value of the sampling capacitor, 18pF
R is the resistance seen by the track-and-hold amplifier looking at the input, 500Ω.
R_{SOURCE} should include any extra source impedance on the analog input.

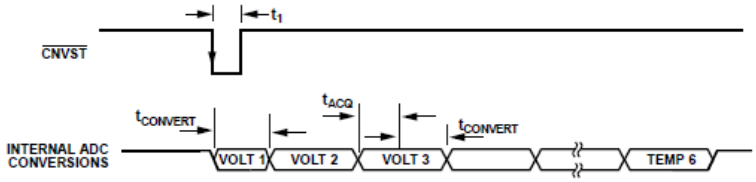


Figure 12. ADC conversions on the AD7280

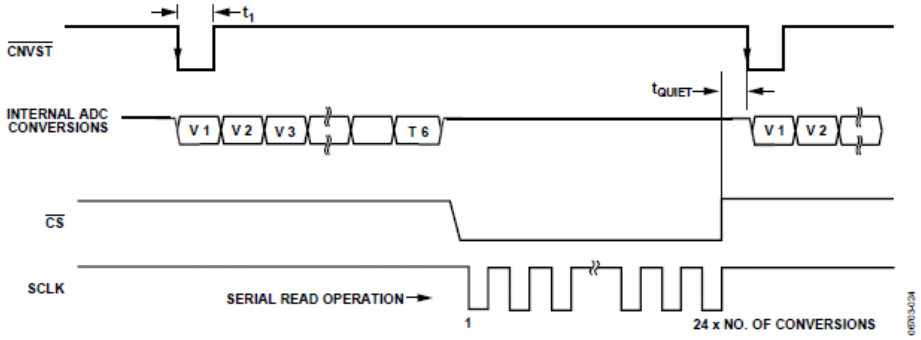


Figure 13. ADC conversions & Readback on the AD7280

Converting Cell Voltages and Temperatures with a chain of AD7280s

The AD7280 provides a daisy chain interface which allows up to 50 parts to be stacked without the need for individual isolation. One feature of this daisychain interface is the ability to initiate conversions on all parts in the daisychain stack with a single conversion start command. The conversion can be initiated through a single $\overline{\text{CNVST}}$ pulse or through the rising edge of $\overline{\text{CS}}$ on the SPI interface. The convert start command is transferred up the daisychain, from the master device, to each AD7280 in turn. The delay time between each AD7280 is t_{DELAY}, as outlined in Figure 14. The maximum delay between the start of conversions on the master AD7280 and the last AD7280 device in the chain can be determined by multiplying t_{DELAY} by the number ofAD7280s in the daisychain. The total conversion time for all cell voltage and temperature conversions can be calculated using the following equation:

$$\textit{Total Conversion time} = ((t_{ACQ} + t_{CONV}) \times (\#\text{conversions per part}) - t_{ACQ} + (\#\text{parts} \times t_{DELAY})$$

Where

t_{ACQ} is the analog input acquisition time of the AD7280 as outlined in Table 7

t_{CONV} is the conversion time of the AD7280 as outlined in Table 2

#conversions per part is 6, 9 or 12 as outlined in Table 6.

#parts is the number of AD7280s in the daisychain

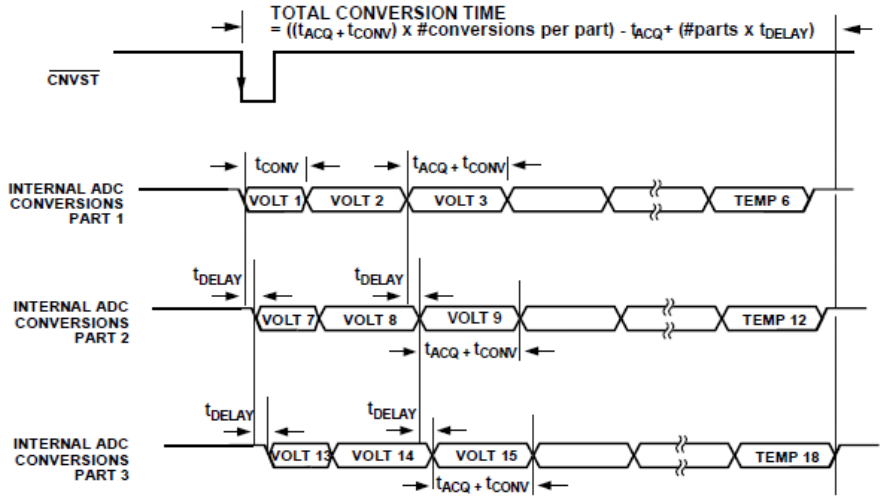


Figure 14. ADC conversions & Readback on a chain of 3 AD7280s

Suggested External Component Configurations on Analog Inputs

As outlined in the Track-and –Hold section the acquisition time of the AD7280 is selected by the status of bits D6 and D5 in the CONTROL register. This provides flexibility in selecting external components on the analog inputs. Included below are two suggested configurations for placing external components on the analog inputs to the AD7280.

Combined LP filter and Current Limiting Resistors

Please refer to Figure 15.

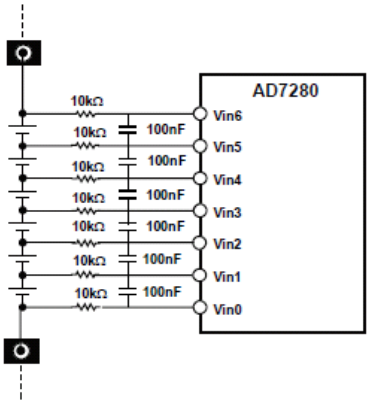


Figure 15. External Series Resistance & Shunt Capacitance

The 10kΩ resistor in series with the inputs provides protection to the analog inputs in the event of an over-voltage or under-voltage on those inputs. The 100nF capacitor across the pseudo differential inputs acts as a low pass filter in conjunction with the 10kΩ resistor. The cut off frequency of the low pass filter is 318Hz. Using these external components the default acquisition time of 400 ns may be used, which will allow a combined acquisition and conversion time of 1µs.

Current Limiting Resistors

Please refer to Figure 16.

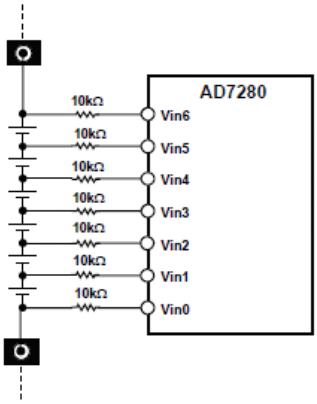


Figure 16. External Series Resistance

The 10kΩ resistor in series with the inputs provides protection to the analog inputs in the event of an over-voltage or under-voltage on those inputs. Using these external components an acquisition time of 1.6 µs should be used, which will allow a combined acquisition and conversion time of 2.2µs.

SELF TEST CONVERSION

A self-test conversion may be initiated on the AD7280 which allows the operation of the ADC to be verified. The self-test conversion is completed on the internal 1.2V bandgap reference voltage. The self-test conversion may be initiated on either a single AD7280 or on all AD7280s in the battery stack simultaneously. The conversion results may be read back though the read protocols defined in the Register map section.

The self-test conversion may also be used to verify the operation of the ALERT outputs as described in the ALERT Output section.

CONVERSION AVERAGING

The AD7280 includes an option where the ADC conversions completed on each cell input may be repeated with an averaged conversion result being stored in the individual register. The averaged conversion result may then be read back through the SPI interface in the same manner as a standard conversion result. The AD7280 may be programmed, through bits D10 and D9 of the CONTROL register, to complete 1, 2, 4 or 8 conversions. The default on power up is a single conversion.

CONVERSION OF LESS THEN 6 VOLTAGE CELLS

The AD7280 provides 6 input channels for Battery Cell voltage measurement. The AD7280 may also be used in applications which require less then 6 voltage measurements. In these applications care should be taken to ensure that the sum of the individual cell voltages will still exceed the minimum V_{DD} supply voltage. For this reason it is recommended that the minimum number of battery cells connected to each AD7280 is 4. Care should also be taken to ensure that the voltage on the Vin6 inputs is always greater than or equal to the voltage on the V_{DD} supply pin. This design requirement is in place to allow the use of a diode on the V_{DD} supply pin of the AD7280 which provides protection in the event of an open circuit in the battery stack. Even if a protection diode is not being used in the application the Vin6 input voltage must be greater than or equal to the V_{DD} supply voltage. An example of the battery connections to the AD7280 in a 4 cell battery monitoring application is shown in Figure 17.

Regardless of how many cell measurements are required in the user application the AD7280 will acquire and convert the voltages on all 6 voltage input channels. The conversion data on all 6 channels will be supplied to the DSP/uP using the SPI /Daisy Chain interfaces. The user should then ignore the conversion data which is not required in their application. If using the Alert function the user should program the Alert register to ensure that the shorted out channels do not incorrectly trigger an Alert output. Please refer to ALERT Output section.

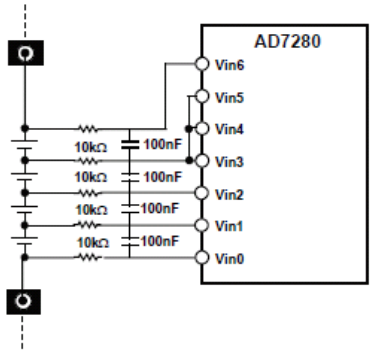


Figure 17. Typical connections for a 4 cell application

CELL TEMPERATURE INPUTS

The AD7280 provides 6 single ended analog inputs, VT1 to VT6, to the ADC which may be used to convert the voltage output of a thermistor temperature measurement circuit. In the event that no temperature measurements are required, or that individual cell temperature measurements are not required the VT inputs may be used to convert any other 0 V to 5 V input signal.

The AD7280 may be programmed to complete conversions on all 6 temperature channels, on 3 temperature channels (VT1, VT3 & VT5) or on none of the temperature input channels. The number of conversions is programmed through bits D15 and D14 of the CONTROL register. The number of conversions results supplied by the AD7280 for read back by the DSP/uP is programmed through bits D13 and D12 of the CONTROL register. In an application where the ALERT function is being used but only one or two temperature inputs are required the AD7280 should first be programmed to complete and readback only 3 temperature conversions, by setting bits D15 and D13 of the CONTROL register to 0, and bits D14 and D12 to 1. VT Channels VT5 and VT3 may be removed from the Alert detection by writing to bits D1 and D0 of the ALERT register. Please refer to ALERT Output section.

Thermistor Termination Input

In the event that thermistors circuits are being used to measure each individual cell temperature the Thermistors Termination pin, VT_{TERM}, may be used to the terminate the thermistor inputs for each cell temperature measurement. This reduces the termination resistor requirement from 6 resistors to 1. Bit D3 in the CONTROL register should be set to 1 when using the VT_{TERM} input.

It should be noted that, due to settling time requirements, the thermistor termination resistor option should only be used when the acquisition time of the AD7280 is set to its highest value, that is 1.6µs. The acquisition time is configured by setting bits D6 and D5 of the CONTROL register as outlined in Table 7.

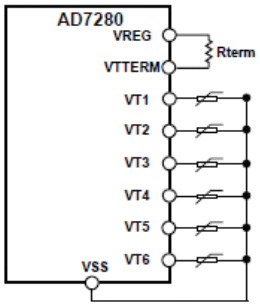


Figure 18. Typical Circuit using the Thermistor Termination Resistor

In the example shown the termination resistor is placed between the source voltage and the thermistor in the thermistor circuit. The VT_{TERM} input may be used to terminate the thermistor inputs to either high or low voltage of the Thermistor circuit.

POWER REQUIREMENTS

The current consumed by the AD7280 in normal operation, that is when not in powerdown mode, is dependant on the mode in which the part is being operated. In a typical Lithium Ion battery monitoring application there are 3 distinct modes of operation. These can be described as follows:

- Voltage and Temperature Conversion
- AD7280 Configuration & Data Readback
- Cell Balancing

The AD7280 consumes its highest level of current while converting voltage and/or temperature inputs to digital outputs. Depending on the configuration of the AD7280 the conversion time can be as little as 6us. As outlined in Table 1 the typical current required by the AD7280 during conversion is 7mA.

When configuring the chain of AD7280s or when reading back the voltage and/or temperature conversion results from a chain of AD7280s the current required for each AD7280 is typically 4mA, as outlined in Table 1. The time required to read back the voltage conversions results from 96 Lithium Ion cells will depend on the speed of the interface clock used, that is SCLK, but it can be as low as 2.5ms.

The typical current consumed by the AD7280 when the cell balancing outputs are switched on is 1mA. The duration of the Cell Balance outputs on time is defined by the user.

When the AD7280 is not being used in any of the above modes of operation it is recommended that the AD7280 be powered down, as outlined below. This will significantly reduce the current draw by each AD7280 on the chain which will avoid unnecessary draining of the Lithium Ion cells.

POWER DOWN

The AD7280 provides a number of power down options. These may be described as follows:

- Full, or Hardware, Powerdown
- Software Powerdown

The AD7280 may be placed into full powerdown mode, which requires only 4uA max current, by taking the $\overline{PD}$ pin low. The falling edge of the $\overline{PD}$ pin will power down all analog and digital circuitry.

The AD7280 may be placed into Software Power down mode, which requires only 1mA of current by setting bit D8 in the CONTROL register through the serial interface. When the AD7280 is powered down through the serial interface the regulator and the daisy chain circuitry stay powered up but the remaining analog and digital circuitry is powered down. This is necessary to ensure that the signal to power on the part, or series of parts, is correctly received.

The AD7280 offers a PD TIMER register which allows the user to program a set time after which the AD7280 will go into power down. This will act as a time delay between the falling edge of the $\overline{PD}$ input, or the setting of bit D8 in the CONTROL register, and the AD7280 powering down. The PD Timer can be set to a value between 0 and 31 minutes, with a resolution of 1 minute. The user should first write to the PD TIMER register, to define the desired delay. Any subsequent falling edge on the $\overline{PD}$ input or setting of bit D8 the CONTROL register, will start the PD timer and after the programmed time will place the AD7280 into powerdown. The default value of the PD TIMER register on power up is 0h.

POWER UP TIME

As outlined in the Power Down section a full power down of the AD7280, that is an active low on the $\overline{PD}$ input will power down all analog and digital circuitry. The recommended power up time for the internal reference, when decoupled with a 10µF capacitor, is 5ms. It is recommended that no conversions be completed until the 5ms power up time has elapsed as it may result in inaccurate data.

CELL BALANCING OUTPUTS

The AD7280 provides 6 CB outputs which can be used to drive the gate of external transistors as part of a cell balancing circuit. Each CB output may be set to provide either a 0V or 5V output with respect to the absolute amplitude of the negative terminal of the battery cell which is being balanced. For example, the CB6 output will provide a 0V or 5V output with respect to the voltage on the Vin5 analog input. The CB outputs are set by writing to the CELL BALANCE register. The default value of the CELL BALANCE register on power up is 0h.

In an application which daisychains a number of AD7280s

together it is recommended that series resistors be placed between the CB outputs of the AD7280 and the gates of the external Cell Balancing transistors. These are recommended to protect the AD7280s in the event that the external cell balancing transistors are damaged during the initial connection of the monitoring circuitry to the battery stack.

An example of how this could occur would be a connection sequence which first provides the system ground, that is the ground supply to the master AD7280 on the daisychain, followed by a connection from any of the battery cells at a potential high enough to exceed the V_{GS} of the cell balancing transistor, for example 40V. If these two connections are the only battery connections made in the system then this will result in 40V being applied to one of the Vin pins of the AD7280, which is also connected to the source input of one of the cell balancing transistors. However, because no power has been supplied to the V_{DD} pin of the AD7280 all the CB outputs will be 0V. This will result in a reverse voltage of 40V across the V_{GS} of the external transistor which may damage the device.

In the event that the external transistor is damaged, the AD7280 may be protected by the use of 10kOhm series resistors on each of the CB output pins. Consideration should also be given to the protection of these external transistors during the initial connection of the monitoring circuitry to the battery stack.

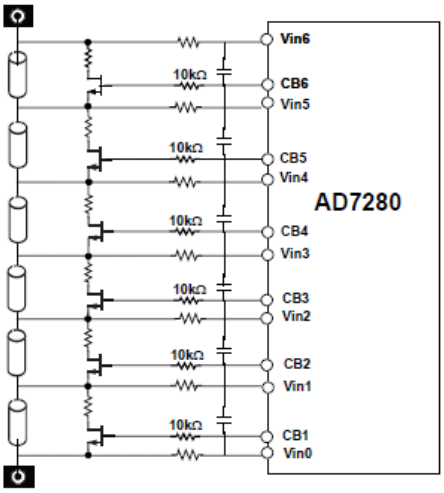


Figure 19. Cell Balancing Configuration

The AD7280 offers 6 Cell Balance timer registers which allow the on-time of each CB output to be programmed. These are referred to as the CB TIMER registers. The CB timers can be set to a value between 0 and 30 minutes. The resolution of the CB Timer is 1 minute. At the end of the programmed CB Time the 6 CB outputs will return to their default state of 0V. The default value of the CB TIMER registers on power up is 0h.

As noted in the Power Down section a power down timer may be programmed to allow cell balancing to occur for a set time before powering down the AD7280. If no power down timer has been set, that is if the PD TIMER register is at its default value of 0h, then a falling edge on the PD pin, or the setting of bit D8 in the CONTROL register to 1, will switch off the CB outputs and power down the AD7280. If a power down time has been set the CB outputs will be powered down when the programmed power down timer has elapsed and the AD7280 is powered down.

ALERT OUTPUT

The Alert output on the AD7280 may be used to indicate if any of the following faults have occurred:

- Over-Voltage
- Under-Voltage
- Over-Temperature
- Under-Temperature

Following each completed conversion the cell voltage and temperature measurement results are compared to the fault thresholds. The fault thresholds can be set by writing to the OVER VOLTAGE. UNDER VOLTAGE, OVER TEMP and UNDER TEMP registers. An ALERT output is generated if the cell voltage or temperature results are outside the programmed fault thresholds.

The Alert output can be defined as a static or a dynamic output, this is set by writing to the ALERT register. The static Alert output is a high signal which is pulled low in the event of a over or under voltage or temperature. The dynamic Alert is a square wave which can be programmed to a frequency of 100Hz or 1kHz. The Alert output may be used as part of a daisy chain in which case the AD7280 at the top of the chain, that is furthest away from the DSP/µP should be programmed to generate the initial Alert output and each AD7280 in the chain will either pass that output through or pull the Alert signal low to indicate that there is a fault with that particular device. At the end of the daisy chain the master AD7280, that is the AD7280 which is connected to the DSP/µP will take the Alert signal from the chain and pass it, in standard digital voltage format to the DSP/µP. The functionality of the fault detection circuit, which generates the Alert output may be programmed through bits D7 to D4 of the ALERT register.

As outlined previously (See Conversion of less then 6 Voltage cells) some applications may require less than 6 voltage measurements. As shown in Figure 17 it is recommended that the channels which are not being used on the AD7280 be shorted to the channel below them. To prevent the incorrect triggering of the Alert output in this application the AD7280 allows the user to select up to 2 voltage channels which may be taken out of the fault detection circuit. This may be

programmed through bits D3 and D2 of the ALERT register.

Table 8.ALERT Register settings

D7 to D6	D5 to D4	D3 to D0	AD7280 Action
00	XX	XXXX	No Alert signal generated or passed [Default]
01	XX	XXXX	Generates static [High] Alert signal to be passed down the Daisy Chain
10	00	XXXX	Generates 100Hz Square wave Alert signal to be passed down the Daisy Chain
10	01	XXXX	Generates 1kHz Square wave Alert signal to be passed down the Daisy Chain
10	10	XXXX	Reserved
10	11	XXXX	Reserved
11	XX	XXXX	Passes Alert signal from AD7280 at higher potential in Daisy Chain
D7 to D4	**D3 to D2**	**D1 to D0**	**AD7280 Action**
XXXX	00	XX	Includes all 6 Voltage channels in Alert detection [Default]
XXXX	01	XX	Removes Vin5 from Alert detection
XXXX	10	XX	Removes Vin5 & Vin4 from Alert detection
XXXX	11	XX	Reserved
XXXX	XX	00	Includes all 6 Temperature channels in Alert detection [Default]
XXXX	XX	01	Removes VT5 from Alert detection
XXXX	XX	10	Removes VT5 & VT3 from Alert detection

The operation of the ALERT output can be verified by initiating a Self-Test conversion. The self-test conversion will convert a known voltage, 1.2V, which will trigger an ALERT output if the under voltage fault threshold is higher than 1.25V. To test the ALERT output the self-test should be initiated on the AD7280 furthest away from the DSP/µP. This allows the ALERT path through each AD7280 to be verified. The remaining AD7280s in the battery stack should be placed into software powerdown to ensure that only the part which is converting the self-test voltage may generate an ALERT output.

REGISTER MAP

Table 9.

Register Name	Register Address	Register Data	Read/Write Register
CELL VOLTAGE 1	0h	D11 to D0	Read Only
CELL VOLTAGE 2	1h	D11 to D0	Read Only
CELL VOLTAGE 3	2h	D11 to D0	Read Only
CELL VOLTAGE 4	3h	D11 to D0	Read Only
CELL VOLTAGE 5	4h	D11 to D0	Read Only
CELL VOLTAGE 6	5h	D11 to D0	Read Only
CELL TEMP 1	6h	D11 to D0	Read Only
CELL TEMP 2	7h	D11 to D0	Read Only
CELL TEMP 3	8h	D11 to D0	Read Only
CELL TEMP 4	9h	D11 to D0	Read Only
CELL TEMP 5	Ah	D11 to D0	Read Only
CELL TEMP 6	Bh	D11 to D0	Read Only
SELF TEST	Ch	D11 to D0	Read Only
CONTROL	Dh	D15 to D8	Read/Write
	Eh	D7 to D0	Read/Write
OVER VOLTAGE	Fh	D7 to D0	Read/Write
UNDER VOLTAGE	10h	D7 to D0	Read/Write
OVER TEMP	11h	D7 to D0	Read/Write
UNDER TEMP	12h	D7 to D0	Read/Write
ALERT	13h	D7 to D0	Read/Write
CELL BALANCE	14h	D7 to D0	Read/Write
CB TIMER 1	15h	D7 to D0	Read/Write
CB TIMER 2	16h	D7 to D0	Read/Write
CB TIMER 3	17h	D7 to D0	Read/Write
CB TIMER 4	18h	D7 to D0	Read/Write
CB TIMER 5	19h	D7 to D0	Read/Write
CB TIMER 6	1Ah	D7 to D0	Read/Write
PD TIMER	1Bh	D7 to D0	Read/Write
READ	1Ch	D7 to D0	Read/Write

CELL VOLTAGE REGISTERS

Table 10. 12-Bit Registers

0h to 5h	D11 to D0	Read/Write

The CELL VOLTAGE registers store the conversion result from each cell input. The conversion result is in 12-bit natural binary format.

CELL TEMPERATURE REGISTERS

Table 11. 12-Bit Register

6h to Bh	D11 to D0	Read/Write

The CELL TEMP registers store the conversion result from each temperature input. The conversion result is in 12-bit natural binary format.

SELF-TEST REGISTER

Table 12. 12-Bit Register

Ch	D11 to D0	Read/Write

The SELF-TEST register stores the conversion result of the ADC self-test. A self-test conversion is initiated by setting bits D15 and D14 of the CONTROL register to 11. The user should then pulse the CNVST input or complete a software convert start through the $\overline{CS}$ input. The conversion result is in 12-bit natural binary format.

CONTROL REGISTER

Table 13. 16-Bit Register

Dh	D15 to D8	Read/Write
Eh	D7 to D0	Read/Write

The CONTROL register is an 16-bit register that sets the AD7280 Control modes.

Table 14. 16-Bit Register

D15 to D14	Select Conversion Inputs 00 = 6 Voltage & 6 Temp 01 = 6 Voltage & Temp 1,3 &5 10 = 6 Voltage only 11 = ADC Self Test
D13 to D12	Read Conversion Results 00 = 6 Voltage & 6 Temp 01 = 6 Voltage & Temp 1,3 &5 10 = 6 Voltage only 11 = No Read operation
D11	Conversion Start Format 0 = Falling edge of CNVST input 1 = Rising edge of CS
D10 to D9	Conversion Averaging 00 = Single Conversion only 01 = Average by 2 10 = Average by 4 11 = Average by 8
D8	Powerdown format 0 = Falling edge of $\overline{PD}$ input 1 = Software PD
D7	Software Reset 0 = Bring out of Reset 1= Reset AD7280
D6 to D5	Set Acquisition Tme 00 = Acquisition time 400ns 01 = Acquisition time 800ns 10 = Acquisition time 1.2us 11 = Acquisition time 1.6us
D4	Reserved; set to 1
D3	Thermistor Termination Resistor 0 = Function not in use 1 = Termination resistor connected
D2 to D0	Reserved; set to 1

Select Conversion Inputs

Bits D15 and D14 of the CONTROL register determine which cell voltages and temperatures are converted following a $\overline{CNVST}$ pulse or the setting of the CNVST bit, D11, in the CONTROL register. The default value of D15 and D14 on power up are 00.

Read Conversion Results

Bits D13 and D12 of the CONTROL register determine which cell voltages and temperatures conversion results are supplied to the serial or Daisychain data outputs pins for readback. The default value of D15 and D14 on power up are 00.

Conversion Start Format

The AD7280 offers two methods of initiating a conversion, the hardware $\overline{\text{CNVST}}$ pin or the software $\overline{\text{CS}}$ input. Bit D11 of the CONTROL register determines whether a conversion is initiated on the falling edge of the $\overline{\text{CNVST}}$ input or on the rising edge of the CS input. The default format on power up is the $\overline{\text{CNVST}}$ pin.

Conversion Averaging

Bits D10 and D9 of the CONTROL register determines the number of conversions completed on each input with the average result being stored in the Result registers. The default value of the Conversion Averaging bits is 00, that is no averaging.

Powerdown Format

Bit D8 of the CONTROL register allows the AD7280 be placed into a software powerdown. Pleas refer to the Power Down section of more details. The default format on power up is the $\overline{\text{PD}}$ pin.

Software Reset

Bit D7 of the CONTROL register allows the user to initiate a software Reset of the AD7280. Two write commands are required to complete the reset operation. Bit D7 must be set high to put the AD7280 into Reset. Bit D7 must then be set low to bring the AD7280 out of Reset.

Select Acquisition Time

Bits D6 and D5 of the CONTROL register determine the Acquisition time of the ADC. Please refer to the Track-and-Hold section for further detail. The default value of the Conversion time setting is 00.

Table 15.Analog Input Acquisition Time.

D6 to D5	Acquisition Time
00	400 ns
01	800 ns
10	1.2 µs
11	1.6 µs

Thermistor Termination Resistor

Bit D3 of the CONTROL register should be set if the user wishes to use a single thermistor termination resistor on the VT_{TERM} pin. It should be noted that, due to settling time requirements, the thermistor termination resistor option should only be used when the acquisition time of the AD7280 is set to its highest value, that is 1.6µs.

OVER VOLTAGE REGISTER

Table 16. 8-Bit Register

Fh	D7 to D0	Read/Write

The OVERVOLTAGE THRESHOLD register determines the high voltage threshold of the AD7280. Cell voltage conversions which exceed the Over Voltage threshold trigger the ALERT output. The AD7280 allows the user to set the Over Voltage threshold to a value between 1V and 5V. The resolution of the Over Voltage threshold is 8-bits, that is 16mV. The default value of the Over Voltage threshold on power up is TBD mV.

UNDER VOLTAGE REGISTER

Table 17. 8-Bit Register

10h	D7 to D0	Read/Write

The UNDER VOLTAGE THRESHOLD register determines the low voltage threshold of the AD7280. Cell voltage conversions lower than the Under Voltage threshold trigger the ALERT output. The AD7280 allows the user to set the Under Voltage threshold to a value between 1V and 5V. The resolution of the Under Voltage threshold is 8-bits, that is 16mV. The default value of the Under Voltage threshold on power up is TBD mV.

OVER TEMP REGISTER

Table 18. 8-Bit Register

11h	D7 to D0	Read/Write

The OVER TEMP THRESHOLD register determines the high temperature threshold of the AD7280. Cell temperature conversions which exceed the Over Temp threshold trigger the ALERT output. The AD7280 allows the user to set the Over Temperature threshold to a value between 0V and 5V. The resolution of the Over Temperature threshold is 8-bits, that is 19mV. The default value of the Over Voltage threshold on power up is TBD mV.

UNDER TEMP REGISTER

Table 19. 8-Bit Register

12h	D7 to D0	Read/Write

The UNDER TEMP THRESHOLD register determines the low temperature threshold of the AD7280. Cell temperature conversions lower than the Under Voltage threshold trigger the ALERT output. The AD7280 allows the user to set the Under Temperature threshold to a value between 0V and 5V. The resolution of the Under Voltage threshold is 8-bits, that is 19mV. The default value of the Under Voltage threshold on power up is TBD mV.

ALERT REGISTER

Table 20. 8-Bit Register

13h	D7 to D0	Read/Write

The ALERT register determines the configuration of the ALERT function. The ALERT can be configured to be a static signal or a square wave. The static signal can be programmed to be either high or low. The frequency of the square wave can be set to either 100Hz or 1kHz. When a number of AD7280s are

operating in daisy chain mode the ALERT configuration is set on the AD7280 furthest away from the uP or DSP only. The ALERT registers on the remaining AD7280s in the chain should be programmed to pass the ALERT signal through the chain. Each of these parts will pass the static or dynamic ALERT signal through the chain or pull the signal low to indicate that an over/under voltage or over/under temperature has occurred.

Table 21.ALERT Register settings

D7 to D6	D5 to D4	D3 to D0	AD7280 Action
00	XX	XXXX	No Alert signal generated or passed [Default]
01	XX	XXXX	Generates static [High] Alert signal to be passed down the Daisy Chain
10	00	XXXX	Generates 100Hz Square wave Alert signal to be passed down the Daisy Chain
10	01	XXXX	Generates 1kHz Square wave Alert signal to be passed down the Daisy Chain
10	10	XXXX	Reserved
10	11	XXXX	Reserved
11	XX	XXXX	Passes Alert signal from AD7280 at higher potential in Daisy Chain
D7 to D4	**D3 to D2**	**D1 to D0**	**AD7280 Action**
XXXX	00	XX	Includes all 6 Voltage channels in Alert detection [Default]
XXXX	01	XX	Removes Vin5 from Alert detection
XXXX	10	XX	Removes Vin5 & Vin4 from Alert detection
XXXX	11	XX	Reserved
XXXX	XX	00	Includes all 6 Temperature channels in Alert detection [Default]
XXXX	XX	01	Removes VT5 from Alert detection
XXXX	XX	10	Removes VT5 & VT3 from Alert detection

CELL BALANCE REGISTER

Table 22. 8-Bit Register

14h	D7 to D0	Read/Write

The CELL BALANCE register determines the status of the 6 Cell Balance outputs. The six CB outputs are set by writing to bits D7 to D2 of the Cell Balance register. The default value of the Cell Balance register on power up is 0h.

Table 23. Cell Balance register settings

D7	Set CB6 output 0 = output off 1 = output on
D6	Set CB5 output 0 = output off 1 = output on
D5	Set CB4 output 0 = output off 1 = output on
D4	Set CB3 output 0 = output off 1 = output on
D3	Set CB3 output 0 = output off 1 = output on
D2	Set CB1 output 0 = output off 1 = output on
D1-D0	Reserved, set to 0

CB TIMER REGISTERS

Table 24. 8-Bit Register

15h to 1Ah	D7 to D0	Read/Write

The CB TIMER registers allow the user to program individual ON times for each of the Cell Balance outputs. The AD7280 allows the user to set the CB Timer to a value between 0 and 30 minutes. The resolution of the CB Timer is 1 minute. The default value of the CB TIMER registers on power up is 0h.

Table 25. CB Timer register settings

D7-D3	5-bit binary code to set CB timer to value between 0 and 30 minutes
D2-D0	Reserved, set to 0

PD TIMER REGISTER

Table 26. 8-Bit Register

1Bh	D7 to D0	Read/Write

The PD TIMER register determines the elapsed time before the AD7280 is automatically powered down. The AD7280 allows the user to set the PD Timer to a value between 0 and 31 minutes. The resolution of the PD Timer is 1 minute. When using the PD timer in conjunction with the CB timers the value programmed to the PD Timer should exceed that programmed to the CB Timer by at least 1 minute. The default value of the PD TIMER registers on power up is 0h.

Table 27. PD Timer register settings

D7-D3	5-bit binary code to set PD timer to value between 0 and 31 minutes
D2-D0	Reserved, set to 0

READ REGISTER

Table 28. 8-Bit Register

1Ch	D7 to D0	Read/Write

The READ register, in conjunction with bits D13 and D12 of the CONTROL register and bit D3 of the write operation define the read operations of the AD7280. To read back a single register from the AD7280 the register address should be first written to the Read register. To read back a series of conversion results from the AD7280 an address of 0h should be written to the Read register. The default value of the READ register on power up is 0h.

Table 29. Read register settings

D7-D2	6-bit binary address for the register to be read
D1-D0	Reserved, set to 0

SERIAL INTERFACE

The AD7280's serial interface consists of four signals; $\overline{CS}$, SCLK, SDIN and SDOUT. The SDIN line is used for transferring data into the on chip registers while the SDOUT line is used for reading the conversion results from the ADCs. SCLK is the serial clock input for the device, and all data transfers, either on SDIN or on SDOUT, take place with respect to SCLK. Data is clocked into and out of the AD7280 on the SCLK falling edge. The $\overline{CS}$, input is used to frame the serial data being transferred to or from the device. $\overline{CS}$, can also be used to initiate the sequence of conversions.

In a Li-Ion Battery Monitoring application up to50 AD7280's may be daisy chained together to allow up to 300 individual Li-Ion cell voltages to be monitored. Each write operation must therefore include Device Address and Register Address in addition to the data to be written. An additional identifier bit is also required when addressing all AD7280s in the Daisy Chain. The AD7280 SPI Interface, in combination with the Daisy Chain Interface, allows any register in the 50 x AD7280 stack to be updated using one 24-bit write cycle.

Table 30. 24-Bit Write Cycle

Device Address[1]	Register Address	Data	Address All Parts	Additional Zero's
D23-D18	D17-D12	D11- D4	D3	D2-D0

There are two different types of read operation for the AD7280.

- Conversion Results Read
- Register Data Read

The data returned from a conversion result read operation includes the Device Address and Channel Address information in addition to the 12-bits of conversion data. The data returned from a Register Data read operation includes the Device Address and Register Address in addition to the 8-bits of register data. The AD7280 SPI Interface, in combination with the Daisy Chain Interface, allows the conversion results of any AD7280 in the 50 x AD7280 stack to be read back using an N x 24-bit read cycle, where N is defined by the number of conversions completed on that part, that is 12, 9 or 6 (Please refer to Table 6). The user has the option of taking CS low for the duration of the N x 24 bit read cycle, or may pulse CS low for each individual 24-bit read cycle, that is N 24-bit wide CS frames.

Table 31. 24-Bit Read Conversion result Cycle

Device Address[2]	Channel Address	Conversion Data	2bit CRC
D23-D18	D17-D14	D13-D2	D1-D0

Table 32. 24-Bit Read Register Data Cycle

Device Address[2]	Register Address	Register Data	Zero	2-bit CRC
D23-D18	D17-D12	D11-D4	D3-D2	D1-D0

Figure 20 shows the timing diagram for the serial interface of the AD7280. Please refer to the Daisy Chain Interface section for further information on the Daisy Chain Interface.

[1] Device Address should be written LSB first. For example, to address device #1 the sequence of bits input to the AD7280 should be 100000. The Register Address and Data bits are input MSB first.

[2] Device Address is read out LSB first. The Register Address, Channel Address and all Data bits are read out MSB first.

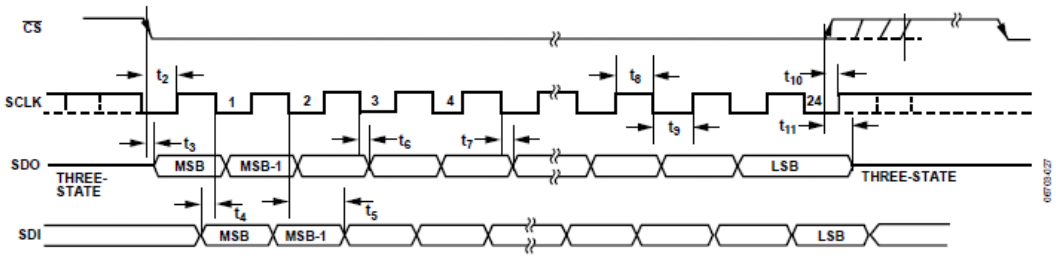


Figure 20. Serial Interface Timing Diagram

Cyclic Redundancy Check

The AD7280 SPI output includes a 2-bit Cyclic Redundancy Check (CRC) on the output data. This CRC may be used to detect any alteration in the data during transmission. The principle of a cyclic redundancy check is that the output data, to be transmitted, is divided by a fixed polynomial, the remainder of this mathematical operation is then attached to the output data and forms parts of the transmission. At the receiving end the user should complete the same mathematical operation on the data received. This will allow the user to confirm that the data which they have received is the same as the data which was originally transmitted. The 2-bit CRC, offered by the AD7280, will allow errors bursts of up to 2 bits to be detected. It will also detect up to 75% of errors bursts which are greater than 2 bits.

The polynomial used by the AD7280 to calculate the CRC bits is $x^2 + 1$. Data bits D17 to D2 of the 24-bit serial output are divided by this polynomial and the 2 bit remainder, following the division, becomes the CRC bits, D1 and D0, of the 24-bit serial output. On the AD7280 this division is implemented using the digital circuit outlined in Figure 21.

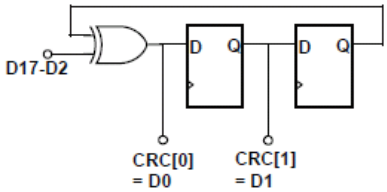


Figure 21. CRC Implementation

The following pseudo code may be used to calculate the CRC. First the following variables need to be declared:

1. *Data_D17toD2* – Data bits D17 to D2 of the 24-bit serial output. When reading a conversion result D17 to D2 includes the 4-bit channel address and the 12-bit conversion result. This data supplies one of the inputs to the XOR gate.

2. *xor_output* – integer variable. This will be the output of the XOR gate

3. *shift1* – integer variable. This will be the output of the first shift register

4. *shift2* – integer variable. This will be the output of the second shift register, which is in turn one of the inputs to the XOR gate

5. *i* – integer variable

With the exception of variable *Data_D17toD2* all variables should be initialised to zero. The following code will then implement the CRC calculation as outlined in Figure 21 above.

```
For (i = 0; I < 16; i++)
    {
    shift2 = shift1;
    shift1 = xor_output;
    if (shift2 == 1)
          {
          if (Data_D17toD2[i] == 1)
            {xor_output = 0;}
          else
            {xor_output = 1;}
            }
    else
        {
       xor_output = Data_D17toD2[i];
        }
    }
```

CRC Example 1

Reading a conversion result of A79h fromVin6 on device 0.

Device Address : 000000

Channel Address : 0101

Conversion Data : 101001111001

Only the channel address and the conversion data are used for the calculation of the CRC. The data inputs to the CRC algorithm would be 0101101001111001. Each step of the calculation, from i=0 to i=15, is outlined in Table 33. Following the completion of the calculation the values of CRC1[D1]and CRC0[D0] may be read from the table as follows:

CRC1 [D1] = Shift1 = 0

CRC0 [D0] = Xor_output = 1

CRC Example 2

Reading the OverVoltage register, Fh, of Device 1

Device Address : 000001

Register Address : 001111

Register Data : 11001010

The register address, the register data and 2 additional zero's are used for the calculation of the CRC. The data inputs to the CRC algorithm would be 0011111100101000. Each step of the calculation, from i=0 to i=15, is outlined in Table 34. Following the completion of the calculation the values of CRC1[D1]and CRC0[D0] may be read from the table as follows:

CRC1 [D1] = Shift1 = 1

CRC0 [D0] = Xor_output = 1

Table 33. CRC Example 1

CRC Calculation Steps	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
D17toD2	0	1	0	1	1	0	1	0	0	1	1	1	1	0	0	1
Xor_output	0	1	0	0	1	0	0	0	0	1	1	0	0	0	0	1
Shift1	0	0	1	0	0	1	0	0	0	0	1	1	0	0	0	0
Shift2	0	0	0	1	0	0	1	0	0	0	0	1	1	0	0	0

Table 34. CRC Example 2

CRC Calculation Steps	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
D17toD2	0	0	1	1	1	1	1	1	0	0	1	0	1	0	0	0
Xor_output	0	0	1	1	0	0	1	1	1	1	0	1	1	1	1	1
Shift1	0	0	0	1	1	0	0	1	1	1	1	0	1	1	1	1
Shift2	0	0	0	0	1	1	0	0	1	1	1	1	0	1	1	1

It should be noted that on receipt of a transmission which includes a cyclic redundancy check the user has 2 options. The CRC calculation may be completed on the received portion of the data which was used to generate the original CRC bits. This will allow the user to verify that the CRC bits received in the transmission are the same as those calculated based on the received data. Another option which is offered by the Cyclic Redundancy Check is that the user may complete the CRC calculation on the entire data set i.e. the transmitted data and the transmitted CRC. A feature of the redundancy check is that this operation will result in a remainder of zero if the data has been received correctly.

Table 35 shows a repeat of CRC Example 1 with 2 additional steps which allows the full transmission to be decoded. As can be seen this results in zero outputs on the *Shift1* and *Xor_output* variables.

Table 35. Repeat of CRC Example 1 with transmitted CRC bits included in calculation

CRC Calculation Steps	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
D17toD0	0	1	0	1	1	0	1	0	0	1	1	1	1	0	0	1	0	1
Xor_output	0	1	0	0	1	0	0	0	0	1	1	0	0	0	0	1	0	0
Shift1	0	0	1	0	0	1	0	0	0	0	1	1	0	0	0	0	1	0
Shift2	0	0	0	1	0	0	1	0	0	0	0	1	1	0	0	0	0	1

DAISY CHAIN INTERFACE

In a Li-Ion Battery Monitoring application up to 50 AD7280's may be daisy chained together to allow up to 300 individual Li-Ion cell voltages to be monitored. Each AD7280 is capable of monitoring up to 6 Li-Ion cells and is powered from the top and bottom voltage of the 6 Li-Ion cells. As a result the supply voltages of each AD7280 are offset by up to 30V from adjacent AD7280's in the chain. For this reason a standard Serial Interface Daisy Chain method cannot be used.

The AD7280 includes a Daisy Chain Interface separate to the standard SPI interface. This Daisy Chain interface allows each AD7280 in the chain to relay data to and from adjacent AD7280's. In addition to the standard wire SPI the AD7280 serial interface include 3 optional interface pins, ALERT, $\overline{\text{CNVST}}$ and $\overline{\text{PD}}$.

Each input and output pin on the 7 wire interface requires at least one additional I/O for the Daisy Chain Interface, that is to allow the information to passed to an AD7280 operating at a higher supply voltage. The SDO and ALERT outputs will also require a further daisy chain pin to allow the information to be passed to an AD7280 operating at a lower supply voltage. The remaining 5 interface pins, $\overline{\text{CS}}$, SCLK, SDI, $\overline{\text{CNVST}}$ and $\overline{\text{PD}}$ do not require additional pins to pass information to a AD7280 operating at a lower voltage as each of these input pins can operate as both SPI inputs or Daisy Chain inputs. Their functionality is defined by the state of the Master pin.

The MASTER pin on the AD7280 at the base of the Daisy Chain should be set high, tied to V_{DD} supply, to ensure that this device interfaces to the DSP or µProcessor using the standard Serial Interface. The MASTER pin on the remaining AD7280s in the Daisy Chain should each be connected to their respective V_{SS} pins which disables the serial interface pins on those devices. This allows the $\overline{\text{CS}}$, SCLK, SDI, $\overline{\text{CNVST}}$ and $\overline{\text{PD}}$ inputs, in addition to the SDOlo and ALERTlo outputs, to pass signals to and from an AD7280 operating at a lower potential.

As explained in the Serial Interface section only one 24-bit write cycle is required to write to any register in the 50 x AD7280 stack . To read back the conversion data from all channels monitoring the battery stack requires only a (24 x N)-bit read cycle where N is the number of channels in the battery stack. Note: this is the default read configuration on power up. If the settings of the Read or control registers have been changed then additional write cycles may be required. The recommended SCLK frequency to ensure correct operation of the Daisy Chain Interface is 1MHz. With a 1MHz SCLK it will take ~2.34 ms to read back the voltage conversions on 96 channels.

Addressing the AD7280

As explained in the previous section all write operations to the AD7280 must include the Device Address and Register Address in addition to the data to be written. In any application using a chain of AD7280's the Device Address corresponds to the position of the individual AD7280 in the chain with respect to the device acting as Daisy Chain Master, that is the device connected directly to the DSP/µP. For example, in an application which uses 16 AD7280's to monitor 96 channels the device acting as Daisy Chain Master should be addressed with a Device Address of 00000, the 16th AD7280 in the chain should be addressed with a Device Address of 001111.

Each individual AD7280 is preset with an address of zero, that is, 0h. When a write operation is initiated by the DSP or µProcessor the Daisy Chain Master compares the Device Address received with its own address. If the addresses do not match the AD7280 will decrement the Device Address by one, 1h, and the new Device Address will be passed to the next AD7280 in the chain with the remainder of the original 24-bit write. The second AD7280 will again compare the received Device Address with its own address, if the addresses do not match 1h will be subtracted from the Devices Address and again passed up the chain. This will continue until the received Device Address matches the preset address, 0h, and the write operation is completed.

The same principle will apply when transferring data down the stack to the DSP or µProcessor. The Device Address supplied from each individual AD7280 will be incremented by one for each AD7280 it passes through on the chain.

To write to the same register on all AD7280's in the stack bit D3 in the 24-bit write cycle should be set high. This will result in the 8-bit register data, bits D11-D4, are written to the same register address on all parts. The Device address, bits D23-D18, should be regarded as Don't Care bits when writing to all parts in the stack. For example when initiating a conversion on all AD7280s in the stack bit D3 should be set high, the Register address should be set to Dh, to address the CONTROL register and bit D11 of the 24-bit write cycle should be set high. This will initiate a conversion on the rising edge of $\overline{\text{CS}}$, on all AD7280s in the stack.

READING DATA FROM THE AD7280

There are a number of read options available on the AD7280. The user may read back the results from all the conversions completed on an individual part in the chain, from all the conversions completed on all parts in the chain or from individual registers on selected parts in the chain.

In each case the user is required to first write to the Read register on the selected parts to configure that part to supply the correct data on the outputs. When reading back an individual register result the address of that register should be written to the read register of the selected part. When reading back conversion results from any or all parts in the chain an address of 0h should be written to the read register of the selected parts. When the address written to the read register is 0h the conversion results selected for read back are controlled by setting bits D13 and D12 of the Control register. Please refer to Table 14. This allows the user to select 4 different read back options

- Read back 12 conversion results: 6 voltage and 6 temperature
- Read back 9 conversion results: 6 voltage and 3 temperature
- Read back 6 conversion results: 6 voltage results only
- Switch off read operation on this part

If the user wishes to read back the conversion results from a single AD7280 in the daisy chain bits D13 and D12 of the control register on that part should be set to select the correct conversion results. Bits D13 and D12 on all other AD7280s in the daisy chain should be set to switch off the read operation on those parts. It should be noted that it is more efficient in terms of 24-bit write cycles to first switch off the read operation on all AD7280s in the daisy chain. This can be achieved with a single write cycle, using bit D3 to address all parts in the chain. The user may then address the individual part and set bits D13 and D12 to select the required conversion results.

When reading back conversion data from any, or all, of the AD7280s in a daisy chain the conversion results returned from the AD7280 will be the last completed conversion on that part. It is recommended that the user also set bits D15 and D14 of the control register, to select the number of conversions to be completed on each part, and initiate the conversions through either the $\overline{\text{CNVST}}$ pin or the rising edge of $\overline{\text{CS}}$., as part of the read operation. This allows the user to implement a simple convert and read back routine with the most efficient number of 24-bit write and read operations. A general example of this routine, which would convert and read back from all parts in the AD7280 daisy chain would be:

- Write0h to the Read register on all of the parts in the daisychain. Note: 0h is the default value of this register on power up and following a reset operation.
- Write to the Control register on all parts. Set bits D15 and D14 to select the required conversions. Set bits D13 and D12 to select the required conversion results for read back.
- Initiate the conversions through either the falling edge of $\overline{\text{CNVST}}$ or the rising edge of $\overline{\text{CS}}$.
- Allow sufficient time for each conversion to be completed. Please refer to Converting Cell Voltages and Temperatures section.
- Either bring $\overline{\text{CS}}$ low and apply 24 SCLKs for each conversion result to be read back or apply an individual $\overline{\text{CS}}$ pulse, each framing 24 SCLKs, for each conversion result to be read back.

The following section outlines ten examples of Conversion and /or Readback routines which would be commonly used in an application using a chain of AD7280s to monitor the voltage and/or temperature of the a stack of Lithium Ion batteries.

Convert and Read all parts, all voltages and all temperatures

- Register address 0h should be written to the Read register on all parts
- Bits D15-D12 of the CONTROL register should be set to 0 on all parts.
- Initiate conversion through either the falling edge of $\overline{\text{CNVST}}$ or the rising edge of $\overline{\text{CS}}$.
- Following the completion of the conversion bring $\overline{\text{CS}}$ low and apply 24 SCLKs for each voltage and temperature result to be read back.

Convert and Read all parts, all voltages and three temperatures per part

- Register address 0h should be written to the Read register on all parts
- Bits D15 and D13 of the CONTROL register should be set to 0, bits D14 and D12 should be set to 1 on all parts.
- Initiate conversion through either the falling edge of $\overline{\text{CNVST}}$ or the rising edge of $\overline{\text{CS}}$.
- Following the completion of the conversion either bring $\overline{\text{CS}}$ low and apply 24 SCLKs for each conversion result to be read back or apply an individual $\overline{\text{CS}}$ pulse, each framing 24 SCLKs, for each conversion result to be read back.

Convert and Read all parts, all voltages

- Register address 0h should be written to the Read register on all parts
- Bits D15 and D13 of the CONTROL register should be set to 1, bits D14 and D12 should be set to 0 on all parts.
- Initiate conversion through either the falling edge of $\overline{CNVST}$ or the rising edge of $\overline{CS}$.
- Following the completion of the conversion either bring $\overline{CS}$ low and apply 24 SCLKs for each conversion result to be read back or apply an individual $\overline{CS}$ pulse, each framing 24 SCLKs, for each conversion result to be read back.

Convert and Read one part, all voltages and all temperatures

- Register address 000000 should be written to the Read register of the part that is to be read
- Bits D13-D12 of the CONTROL register should be set to 1 on all parts. This switches off the read operation on all parts.
- Bits D15-D12 of the CONTROL register of the part to be read from should be set to 0.
- Initiate conversion through either the falling edge of $\overline{CNVST}$ or the rising edge of $\overline{CS}$.
- Following the completion of the conversion either bring $\overline{CS}$ low and apply 24 SCLKs for each conversion result to be read back or apply an individual $\overline{CS}$ pulse, each framing 24 SCLKs, for each conversion result to be read back.

Convert and Read one part, all voltages and temperatures 1, 3 & 5

- Register address 000000 should be written to the Read register of the part that is to be read
- Bits D13-D12 of the CONTROL register should be set to 1 on all parts. This switches off the read operation on all parts.
- Bit D15 and D13 of the CONTROL register of the part to be read from should be set to 0 and bits D14 and D12 should be set to 1.
- Initiate conversion through either the falling edge of $\overline{CNVST}$ or the rising edge of $\overline{CS}$.
- Following the completion of the conversion either bring $\overline{CS}$ low and apply 24 SCLKs for each conversion result to be read back or apply an individual $\overline{CS}$ pulse, each framing 24 SCLKs, for each conversion result to be read back.

Convert and Read one part, all voltages, no temperatures

- Register address 000000 should be written to the Read register of the part that is to be read
- Bits D13-D12 of the CONTROL register should be set to 1 on all parts. This switches off the read operation on all parts.
- Bit D14 and D12 of the CONTROL register of the part to be read from should be set to 0 and bits D15 and D13 should be set to 1.
- Initiate conversion through either the falling edge of $\overline{CNVST}$ or the rising edge of $\overline{CS}$.
- Following the completion of the conversion either bring $\overline{CS}$ low and apply 24 SCLKs for each conversion result to be read back or apply an individual $\overline{CS}$ pulse, each framing 24 SCLKs, for each conversion result to be read back.

Convert and Read a single voltage or temperature result

- The register address corresponding to the voltage or temperature result to be read should be written to the Read register of the part that is to be read, see Table 9 for register addresses.
- Bits D13-D12 of the CONTROL register should be set to 1 on all parts. This switches off the read operation on all parts.
- Bits D13 and D12 of the CONTROL register of the part to be read from should be set such that a conversion will be completed on the required channel. Note: With the exception of a Self-Test conversion it is not possible to convert on a single channel, 6, 9 or 12 conversions must be completed.
- Initiate conversion through either the falling edge of $\overline{CNVST}$ or the rising edge of $\overline{CS}$.
- Following the completion of the conversion bring $\overline{CS}$ low and apply 24 SCLKs to be read back the desired voltage or temperature.

Read a single register

- The register address corresponding to the voltage or temperature result to be read should be written to the Read register of the part that is to be read, see Table 9 for register addresses.
- Bits D13-D12 of the CONTROL register should be set to 1 on all parts. This switches off the read operation on all parts.

- Bits D13 and D12 of the CONTROL register of the part to be read from should be set to 0.
- Bring $\overline{CS}$ low and apply 24 SCLKs to be read back the desired register.

Self-Test conversion, all parts

- The register address corresponding to the self-test conversion, should be written to the Read register of all parts, see Table 9 for register addresses.
- Bits D15-D14 of the CONTROL register should be set to 1 on all parts to select the self-test conversion.
- Bits D13-D12 of the CONTROL register should be set to 1 on all parts. This switches off the read operation on all parts.
- Initiate conversion through either the falling edge of $\overline{CNVST}$ or the rising edge of $\overline{CS}$.
- To read back the self-test conversion result from each individual part bits D13-D12 should be set to 0 for that part and the register data read back as outlined in Read a single register section. The self-test conversion results must be read back individually from each part.

Self-Test conversion, single part

- Bits D13-D12 of the CONTROL register should be set to 1 on all parts. This switches off the read operation on all parts.
- BitD8 in the CONTROL register of all parts should be set to 1 to put each part into a software power down. This prevents the ALERT function on the parts not undergoing a self-test conversion from being triggered.
- Bit D8 in the CONTROL register of the part for which a self-test conversion is requested should be set to 0. This bring this part out of powerdown.
- The register address corresponding to the self-test conversion, should be written to the Read register of the part under test, see Table 9 for register addresses.
- Bits D15-D14 of the CONTROL register should be set to 1 on the part under test to select the self-test conversion.
- Bits D13-D12 of the CONTROL register should be set to 0 the part under test.
- Initiate conversion through either the falling edge of $\overline{CNVST}$ or the rising edge of $\overline{CS}$.
- the register data should be read back as outlined in Read a single register section.

OUTLINE DIMENSIONS

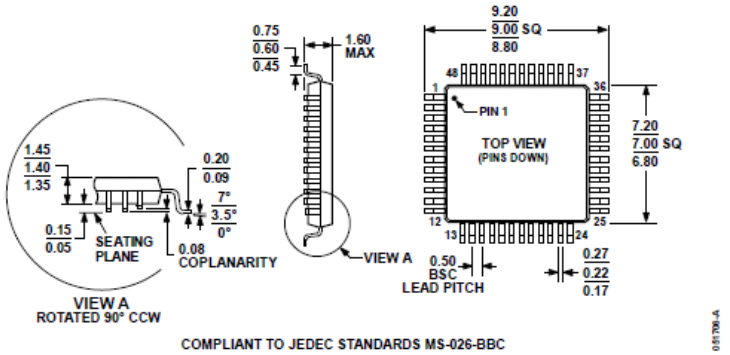


Figure 22. 48-Lead Low Profile Quad Flat Package [LQFP]

(ST-48)

Dimensions shown in millimeters

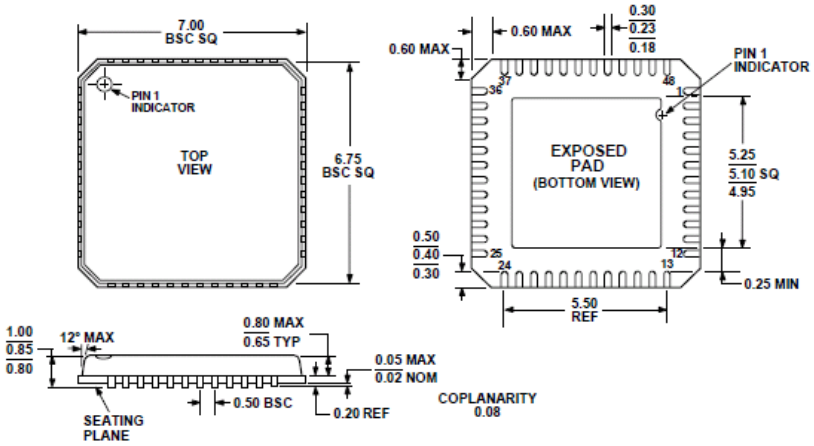


Figure 23. 48-Lead Frame Chip Scale Package [LFCSP]

(CP-48-1)

Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7280BSTZ[1]	–40°C to +85°C	48-Lead LQFP	ST-48
AD7280DSTZ[1]	–40°C to +105°C	48-Lead LQFP	ST-48
AD7280BCPZ[1]	–40°C to +85°C	48-Lead LFCSP	CP-48-1
AD7280DCPZ[1]	–40°C to +105°C	48-Lead LFCSP	CP-48-1

[1] Z = Pb-free part.

9.4.2. EVAL Board Datasheet

ANALOG DEVICES

Evaluation Board for AD7280 Lithium Ion Battery Monitoring System

EVAL-AD7280

FEATURES

Full-featured evaluation board for the AD7280
EVAL-CED1Z compatible
Standalone capability
Various linking options
DaisyChain capability
PC software for control and data analysis when used with EVAL-CED1Z

GENERAL DESCRIPTION

This data sheet describes the evaluation board for the AD7280, which is a complete, 12-bit resolution Lithium Ion Battery monitoring system, integrating multiple voltage and temperature input channels. Full details about the part are available in the AD7280 data sheet from Analog Devices, Inc., and should be consulted in conjunction with this data sheet when using the evaluation board.

On-board components include the ADG3308 and ADG3301 bidirectional logic level translators, the ADG779 switch as well as the ADuM1411 and the ADuM5241 digital isolators

Various link options and options for external connectors are explained in Table 1 , Table 5 and Table 6.

FUNCTIONAL BLOCK DIAGRAM

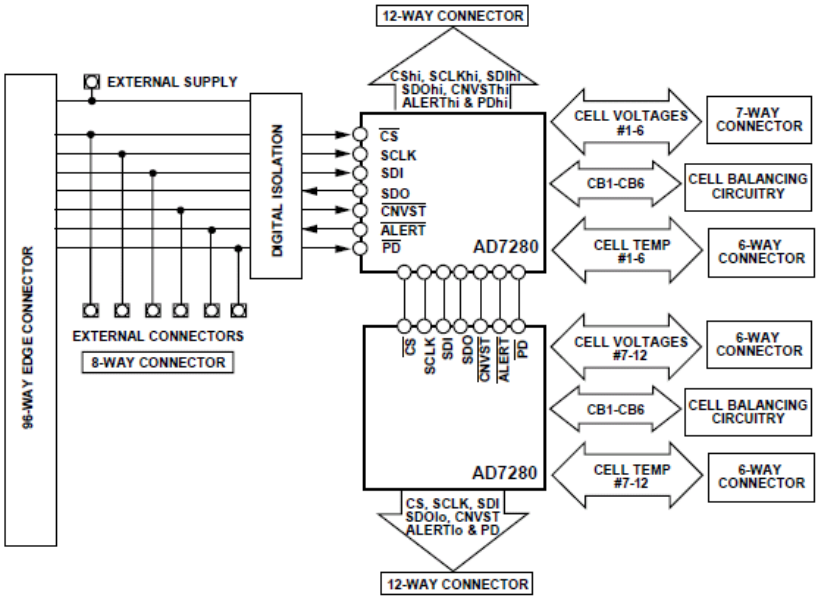


Figure 1

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

EVALUATION BOARD HARDWARE

POWER SUPPLIES

When using this evaluation board with the EVAL-CEDZ1, all supplies, with the exception of the battery connections, are provided from the EVAL-CED1Z through the 96-way connector. When using the EVAL-AD7280 board as a standalone unit, external supplies must be provided. This evaluation board has the following four power supply inputs:

- +5 V
- +3.3 V
- DSP/+3V3
- 0V (DGND)

If the evaluation board is used in standalone mode, 5 V must be connected to the 5V input to supply the ADG3308, the ADG3301, the ADG779, the ADuM1411 and the ADuM5241. In addition, a suitable voltage should be applied to either the +3.3V supply pin or the DSP/+3V3 supply pin. This voltage is dependant on the voltage levels of the users external DSP or uProcessor. The AD7280 Eval board default is to supply 3.3V to the +3.3V supply pin. However users with an external DSP/uP with voltage levels of either 1.8V or 5V should connect the required voltage to the DSP/+3V3 supply pin, remove resistor link R66 and install resistor link R67. Lastly, 0 V is connected to the 0V input.

The 5V, 3.3V and DSP/+3V3 supplies are decoupled to the relevant ground plane with 22 µF tantalum capacitors. The ADG3308, the ADG3301 and the ADG779, are decoupled to the relevant ground plane with 0.1 µF multilayer ceramic capacitors. The ADuM1411 and the ADuM5241 are decoupled to the relevant ground plane with 10 µF tantalum and 0.1 µF multilayer ceramic capacitors.

Power to supply the 2 AD7280s on the Evaluation board is taken from the battery inputs.

Extensive ground planes are used on this board to minimize the effect of high frequency noise interference. There are three ground planes on the AD7280 Evaluation board. One ground plane, DGND, is provided for the digital i/o's, the ADG3308, ADG3301, the ADG779 and the low side of the ADuM isolator parts. Separate ground planes, isolated from the DGND plane are provided for each of the AD7280 parts on the evaluation board.

LINK OPTIONS

There are 8 link options that must be positioned for the required operating setup before using the evaluation board. The functions of these options are outlined in Table 1.

Table 1. Link Option Functions

Link No.	Function
LK1	This link selects the source of the $\overline{CS}$ input signal for the AD7280. In Position A, the $\overline{CS}$ signal is taken from the externally applied $\overline{CS}$ signal via the J8 SMA socket or the J7 connector. In Position B, the $\overline{CS}$ signal is taken from the CED board via the 96-way connector.
LK2	This link selects the source of the SCLK input signal for the AD7280. In Position A, the SCLK signal is taken from the externally applied $\overline{CS}$ signal via the J9 SMA socket or the J7 connector. In Position B, the SCLK signal is taken from the CED board via the 96-way connector.
LK3	This link selects the source of the SDI input signal for the AD7280. In Position A, the SDI signal is taken from the externally applied $\overline{CS}$ signal via the J10 SMA socket or the J7 connector. In Position B, the SDI signal is taken from the CED board via the 96-way connector.
LK4	This link selects the output path of the SDO output signal from the AD7280. In Position A, the SDO signal is supplied to the J11 SMA socket or and to the J7 connector. In Position B, the SDO signal is supplied to the CED board via the 96-way connector.
LK5	This link selects the source of the $\overline{CNVST}$ input signal for the AD7280. In Position A, the $\overline{CNVST}$ signal is taken from the externally applied $\overline{CNVST}$ signal via the J12 SMA socket or the J7 connector. In Position B, the $\overline{CNVST}$ signal is taken from the CED board via the 96-way connector.
LK6	This link selects the source of the $\overline{PD}$ input signal for the AD7280. In Position A, the $\overline{PD}$ signal is taken from the externally applied $\overline{PD}$ signal via the J13 SMA socket or the J7 connector. In Position B, the $\overline{PD}$ signal is taken from the CED board via the 96-way connector.
LK7	This link is used to select the source of the +5V supply for the EVAL-AD7280. In Position A, the +5V supply is sourced from the evaluation board controller via the 96-way connector. In Position B, the +5V supply is sourced externally via the J6 connector.
LK8	This link is used to select the source of the +3.3 V supply for the EVAL-AD7280. In Position A, the +3.3 V supply is sourced from the evaluation board controller via the 96-way connector. In Position B, the +3.3 V supply is sourced externally via the J6 connector.

SETUP CONDITIONS

Care should be taken before applying power and signals to the evaluation board to ensure that all link positions are as per the required operating mode. There are a few different modes in which to operate the evaluation board. Either the user can operate the board with the EVAL-CED1Z or it can be used as a standalone board.

Table 2 shows the position in which all the links are set when the evaluation board is packaged. When the board is shipped, the assumption is that the user will be operating with the EVAL-CED1Z board. The links are set so that all power supplies and control signals are supplied by the EVAL-CEDZ1.

Table 2. Link Positions on the Packaged EVAL- AD7280EDZ

Link No.	Position	Function
LK1	B	The logic input to the $\overline{CS}$ pin of the AD7280 is supplied from the EVAL-CED1Z board.
Lk2	B	The logic input to the SCLK pin of the AD7280 is supplied from the EVAL-CED1Z board.
LK3	B	The logic input to the SDI pin of the AD7280 is supplied from the EVAL-CED1Z board.
LK4	B	The logic output from the SDO pin of the AD7280 is supplied to the EVAL-CED1Z board.
LK5	B	The logic input to the $\overline{CNVST}$ pin of the AD7280 is supplied from the EVAL-CED1Z board.
LK6	B	The logic input to the $\overline{PD}$ pin of the AD7280 is supplied from the EVAL-CED1Z board.
LK7	A	+5 V is supplied from the EVAL-CED1Z board.
LK8	A	+3.3 V is supplied from the EVAL-CED1Z board.

INTERFACING THE EVALUATION BOARD TO THE EVAL-CEDZ1

Interfacing the EVAL-CED1Z board to the evaluation board is via a 96-way connector, J1. The pinout for the J1 connector is shown in Figure 2. Table 3 gives a description of the pins on the 96-way connector used to interface between the EVAL-CED1Z board and the EVAL-AD7280. Table 4 gives the pin designations for the 96-way connector.

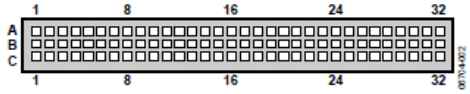


Figure 2. Pin Configuration for the 96-Way Connector, J1

Table 3. The 96-Way Connector Pin Description

Signal	Description
TFS	Transmit Frame Sync. This output is connected to the $\overline{CS}$ pin of the AD7280, via level shift and isolation, to frame the serial data transfer.
RFS	Receive Frame Sync. This input is connected to the TFS pin on the AD7280 Evaluation board to frame the serial data read.
TSCLK	Transmit Serial Clock. This output is connected to the SCLK pin of the AD7280, via level shift and isolation, to clock the serial data transfer.
RSCLK	Receive Serial Clock. This input is connected to the TSCLK pin on the AD7280 Evaluation board to frame the serial data read.
DT0PRI	Data Transmit 0 Primary. This output is connected to the SDI pin of the AD7280 via level shift and isolation.
DR0PRI	Data Receive 0 Primary. This input is connected to the SDO pin of the AD7280 via level shift and isolation.
RXINT	Interrupt. This output is connected to the $\overline{CNVST}$ pin of the AD7280, via level shift and isolation. The $\overline{CNVST}$ signal is used to initiate conversions on the AD7280.
GPIO 0	General Purpose Input Output. This output is used to disable the level shift circuitry and to supply the PD signal to the AD7280.
GPIO 1	General Purpose Input Output. This output is connected to the ALERT pin of the AD7280 via level shift and isolation.
AV_{CC}	Analog +5 V Supply. This is used to supply the ADuM1411, ADuM5241, ADG3308, ADG3301 and ADG779.
DV_{DD}	Digital +3.3 V supply. This is used to supply the ADG3308 and ADG3301.
DGND	Digital Ground. These lines are connected to the ground plane on the low side of the evaluation board.
AGND	Analog Ground. These lines are connected to the ground plane on the low side of the evaluation board.

Table 4. 96-Way Connector Pin Functions[1]

Pin	ROW A	ROW B	ROW C
1	DTPRI	GPIO3	DR1PRI
2	TFS1		RFS1
3	TSCLK1		RSCLK1
4	DGND	DGND	DGND
5	DT0PRI		DR0PRI
6	TFS0		RFS0
7	TSCLK0		RSCLK0
8	DV_{DD} (+3.3V)	DV_{DD} (+3.3V)	DV_{DD} (+3.3V)
9			
10			
11	DTOSEC		GPIO6
12	DGND	DGND	DGND
13			DROSEC
14	GPIO5		GPIO7
15	GPIO0		GPIO4
16	DGND	DGND	DGND
17			RXINT
18			
19		GPIO1	
20	DGND	DGND	DGND
21	AGND	AGND	AGND
22	AGND	AGND	AGND
23	AGND	AGND	AGND
24	AGND	AGND	AGND
25	AGND	AGND	AGND
26	AGND	AGND	AGND
27		AGND	
28		AGND	
29	AGND	AGND	AGND
30	−12 V	AGND	+12 V
31	AV_{SS} (−5V)	AV_{SS} (−5V)	AV_{SS}(−5V)
32	AV_{CC} (+5V)	AV_{CC} (+5V)	AV_{CC} (+5V)

[1] The unused pins of the 96-way connector are not shown.

OPERATING WITH THE EVAL-CED1Z BOARD

The evaluation board can be operated in a standalone mode or operated in conjunction with the EVAL-CED1Z board. This Evaluation Board Controller is available from Analog Devices under the order entry "EVAL-CEDZ1".

When interfacing the EVAL-AD7280 directly to the EVAL-CED1Z board, all supplies, with the exception of the battery connections, and control signals to operate the AD7280 board are provided by the EVAL-CED1Z board. The SCLK frequency supplied by the EVAL-CED1Z is fixed at 1MHz for the AD7280.

Software to communicate with the EVAL-CED1Z and AD7280 is provided with the AD7280 evaluation board package.

The 96-way connector on the EVAL-AD7280 plugs directly into the 96-way connector on the EVAL-CED1Z board. The EVAL-CED1Z board provides all the supplies for the evaluation board. It is powered from a +7V, 15W power supply which accepts input voltages from 100V to 240V AC and contains the relevant adaptors for worldwide use. The power supply is provided with the EVAL-CEDZ1.

Connection between the EVAL-CED1Z and the USB port of a PC is via a standard USB 2.0 connection cable that is provided as part of the EVAL-CED1Z package.

INTERFACING TO THE EVALUATION BOARD IN STANDALONE OPERATION

Options for interfacing with the evaluation board are via J1, the 96-way connector to the EVAL-CED1Z board or via J7, an 8-way connector. The J7 connector is provided to allow the evaluation board to be interfaced with systems other than Analog Devices EVAL-CED1Z board. The pin designations for the J7 connector is shown in Table 5. It should be noted that, when the AD7280 Evaluation board is shipped, the assumption is that the user will be operating with the EVAL-CED1Z board. For this reason the J7 connector is not inserted.

Table 5. Pin Designations for 8-Way Connector J7

Pin No.	Function
1	$\overline{CS}$
2	SCLK
3	SDI
4	SDO
5	$\overline{CNVST}$
6	ALERT
7	$\overline{PD}$
8	GND

SOCKETS

There are five input sockets relevant to the operation of the AD7280 on the evaluation board. The functions of these sockets are outlined in Table 6. All of these sockets are used to apply externally generated digital i/o signals to the evaluation board. When operating the board with the EVAL-CED1Z board, these external connections are not required. It should be noted that, when the AD7280 Evaluation board is shipped, the assumption is that the user will be operating with the EVAL-CED1Z board. For this reason the sockets J8-J12 are not inserted.

Table 6.

Socket	Function
J8	SMA socket for external $\overline{CS}$ input.
J9	SMA socket for external SCLK input.
J10	SMA socket for external SDI input.
J11	SMA socket for external SDO output
J12	SMA socket for external $\overline{CNVST}$ input.
J13	SMA socket for external $\overline{PD}$ input.

CONNECTORS

There are ten connectors on the AD7280 evaluation board .The functions of these sockets are outlined in Table 7. ConnectorsJ1 is used to interface with the EVAL-CED1Z board. Connectors J2 and J3 are used to connect the AD7280s to the battery cells. Connectors J1, J2 and J3 are inserted on the AD7280 Evaluation board when the board is packaged. The remaining connectors, J4-J7 and J14 to J16 are not inserted.

Table 7.

Connector	Function
J1	96-way connector for CED interface connections.
J2	7-way connector for 6 Li-Ion Battery cells
J3	6-way connector for additional 6 Li-Ion Battery cells
J4	8-way connector for 6 thermistor inputs
J5	8-way connector for 6 additional thermistor inputs
J6	External 5V, 3.3V, DSP/3V3 and GND power connector.
J7	8-way connector External DSP/uP operation.
J14	6-way connector, Reserved for ADI Test requirements
J15	External 12-way connector to allow Daisy-chaining of Evaluation boards
J16	External 12-way connector to allow Daisy-chaining of Evaluation boards

DAISY CHAINING TWO OR MORE AD7280 EVALUATION BOARDS

The AD7280 Evaluation board includes two connectors, J15 and J16, which allow two or more AD7280 Evaluation boards to be daisy chained together. A connection should be made between J16 on the Evaluation board connected to the DSP/µP, measuring voltage on battery cells 1 through 12, and connector J15 on the Evaluation board connected to the battery cells 13 through 24. The default setting of each AD7280 Evaluation board is for the master pin on Device0 to be tied to V_{DD} through resistor, R88. Each board also includes an option to solder a resistor, R89, from the Master pin to V_{SS}. When daisy-chaining two or more evaluation boards the R88 resistor on Slave boards should be removed and a zero-ohm resistor should be included in the R89 footprint. The pin designations for the J15 and J16 connectors are shown in Table 8 and Table 9.

Table 8. Pin Designations for 12-Way Connector J15

Pin No.	Function
1	GND
2	GND
3	$\overline{PD}$
4	$\overline{CS}$
5	SCLK
6	SDI
7	$\overline{CNVST}$
8	SDO
9	ALERT
10	GND
11	GND
12	GND

Table 9. Pin Designations for 12-Way Connector J16

Pin No.	Function
1	V_{DD}
2	V_{DD}
3	$\overline{PDhi}$
4	$\overline{CShi}$
5	SCLKhi
6	SDOhi
7	$\overline{CNVSThi}$
8	SDIhi
9	ALERThi
10	V_{DD}
11	V_{DD}
12	V_{DD}

TEST POINTS

There are numerous test points on the AD7280 evaluation board. These enable the user to have easy access to these signals for probing, evaluation, and debugging.

EVALUATION BOARD SOFTWARE

INSTALLING THE SOFTWARE

The EVAL-AD7280EDZ evaluation kit includes self-installing software on CD ROM, for controlling and evaluating the performance of the AD7280 when it is operated with the EVAL-CED1Z board. The software is compatible with Windows* 2000/XP*. If the setup file does not run automatically, setup.exe can be run from the CD-ROM.

When the CD is inserted into the PC, an installation program automatically begins. This program installs the evaluation software. The user interface on the PC is a dedicated program written especially for the AD7280 when operating with the EVAL-CED1Z board.

The software should be installed before the USB cable is connected between the EVAL-CED1Z and the PC. This ensures that the appropriate USB driver files have been properly installed before the EVAL-CED1Z is connected to the PC.

When the software is run for the first time with the EVAL-CED1Z board connected to the PC, the PC will automatically find the new device and will identify it. Follow the onscreen instructions that appear automatically. This installs the drivers for the CED on the PC. If an error appears on screen when the software is first opened, then the PC is not recognizing the USB device. This error is corrected by

1. Opening the PC's Device Manager. The Device Manager is accessed by right clicking on the My Computer Icon, and selecting Properties. When the System Properties Window opens, select the Hardware tab.
2. Click on Device Manager in the Hardware Tab of the System Properties window.
3. Examine the devices listed under the Universal Serial Bus Controller heading.
4. If an unknown device is listed, right click on this option and select, Update Driver.
5. The New Hardware Wizard will run twice, and under the ADI Development Tools the following hardware is listed:

ADI Converter Evaluation and Development Board (WF)

6. Reboot the PC.

SETTING UP THE EVAL-CEDZ1

This section describes how the evaluation board, the EVAL-CED1Z board and the software should be setup to begin using the complete system.

- Install the AD7280 evaluation board software.
- Connect the AD7280 Evaluation board to the battery via connectors J2 and J3
- Connect the EVAL-CED1Z board and the evaluation board together via the 96-way connector. Apply power to the EVAL-CED1Z via +7V, 15W power supply provided. At this stage, the green LED labeled Power, on the EVAL-CED1Z should be lighting, which indicates that the EVAL-CED1Z is receiving power
- The USB cable can then be connected between the PC and the EVAL-CEDZ1. A green LED positioned beside the USB connector on the EVAL-CED1Z board will light indicating that the USB connection has been established.
- The EVAL-AD7280 will be detected - proceed through any dialog boxes that may appear(use the recommended options), to finalize the installation.
- Start the EVAL-AD7280 software. The FPGA code will be automatically downloaded to the EVAL-CEDZ1. The red LED, D14, on the EVAL-CED1Z will now light. This indicates that the EVAL-CED1Z is functional and ready to receive instructions.
- The software may now be operated as described in the following sections.
- It should also be noted that when completing conversions on the AD7280 Evaluation board, using the EVAL-CED1Z board, the red LED, D14, on the EVAL-CED1Z will light to indicate that the conversions are occurring.

SOFTWARE OPERATION

With the hardware set up, you can now use the software to control the EVAL-CED1Z and the AD7280 evaluation board. To launch the software, from the **Analog Devices** menu click on the **AD7280** submenu, then click on **AD7280 icon.** Figure 3 displays the main window that is opened. If an Error message appears, click OK and restart the application after checking the connection between the adapter board and the USB port on the PC. Also check that the USB device is identified by the Device Manager as detailed in the Installing the Software Section.

The software that controls the EVAL-CED1Z and, therefore, the AD7280 evaluation board, has one main window. Figure 3 shows the window that appears when the software is run. The main function of this window is to allow you to read samples from the evaluation board and display them. The screen can be divided into three main sections. The top portion of the screen contains the menu bar. The **Control Buttons**, below the menu bar and a **Data Capture** display below these which consists of a number of sub-tabs;

- Voltage (Codes)
- Voltage (Volts)
- VT Output (Codes)
- VT Output (Volts)

USING THE SOFTWARE

Menu Bar

The menu bar consists of the following menus:

Save (Conversion Data). Saves the conversion data to a spreadsheet file.

Print Front Panel Picture. Prints the software screen displayed.

Save as Picture. Saves the displayed screen plot, i.e. Voltage or VT waveforms.

Exit. Closes the AD7280 Evaluation software.

Control Buttons

The AD7280 software includes the follows user controlled buttons on the front panel.

Init. Resends the AD7280 FPGA code to the EVAL-CEDZ1

Real Time. Initiates continuous conversions on the AD7280 Evaluation board. The default conversion loop interval is 2ms and can be changed by accessing the **Configure AD7280** button.

Read/Write Registers. Allows the user to read from and write to the registers on both AD7280s on the Evaluation board.

Configure AD7280. Allows the user to configure the number of voltage and temperature channels converted and read back on each AD7280 on the Evaluation board.

Reset. Executes a software reset on both AD7280s on the Evaluation board.

STOP. Closes the AD7280 Evaluation software.

The section below the menu items also includes a **CED buffer** indicator. The AD7280 Evaluation board allows conversions on all or selected channels to be initiated at periodic intervals. The default conversion loop interval is 2ms but can be increased to 5ms, 10ms or 30ms through the **Configure AD7280** button. conversion data from the AD7280 . The AD7280 Evaluation software and hardware is designed such that all conversion results are written to external memory, on the EVAL-CED1Z and blocks of samples are then uploaded through the USB port to the PC. The CED Buffer indicator provides an indication as to the available memory remaining. If there is a lot of activity on the USB port the transfer of data may be slowed down which may cause the external memory to fill before the data can be uploaded to the PC. In this case the **CED buffer** indicator will show that the buffer is full. The user should either disconnect other external devices which may be using the USB port or may increase the conversion loop interval to decrease the number of samples to upload which will ease the requirement on the USB port. It should also be noted that the transfer of data from the EVAL-CED1Z to the PC will be slower when connecting to a USB 1.1 port then it would be when connecting to a USB2.0 port.

Data Capture Display

In the **Data Capture** display, the user may select the format in which they would like to view the cell voltage or cell temperature conversion results. For both cell voltage and temperature conversions the data may be displayed either in digital output code format or as an equivalent voltage. The desired display options are selected by clicking on the **Voltage(Codes)**, **Voltage(Volts)**, **VT (Codes)** or **VT (Volts)** tab buttons.

Voltage(Codes) Tab

The **Voltage(Codes)** tab displays the conversion results of the Vin inputs of the two AD7280 devices on the AD7280 Evaluation board. The conversion results are displayed, on the running chart, as integer code values. The upper chart refers to the conversion results from Device0 (U2) on the AD7280 Evaluation board. The lower chart refers to the conversion results from Device1 (U1). The instantaneous value of each conversion result is displayed, in hex format, on the individual indicators to the right of each chart. If the user would like to focus on the results of one channel, or selected channels, in particular the conversion results input to the chart from the remaining channels may be individually removed from the plot using the **Plot EN** buttons to the right of each chart.

At the bottom left of the graph are the zoom options. These allow you to zoom in and out to get a closer look at a sample, if required.

Voltage(Volts) Tab

The **Voltage(Volts)** tab displays the conversion results of the Vin inputs of the two AD7280 devices on the AD7280 Evaluation board. The conversion results are displayed, on the running chart in units of voltage. It should be noted that the voltage output is calculated using an LSB size of 977µV, that is 4V/4096 and offset by 1V to allow for the 1V to 5V input range specified on the AD7280 cell voltage measurement channels. The upper chart refers to the conversion results from Device0 (U2) on the AD7280 Evaluation board. The lower chart refers to the conversion results from Device1 (U1). The instantaneous value of each conversion result is displayed, in voltage format, on the individual indicators to the right of each chart. If the user would like to focus on the results of one channel, or selected channels, in particular the conversion results input to the chart from the remaining channels may be individually removed from the plot using the **Plot EN** buttons to the right of each chart.

At the bottom left of the graph are the zoom options. These allow you to zoom in and out to get a closer look at a sample, if required.

VT(Codes) Tab

The **VT(Codes)** tab displays the conversion results of the VT inputs of the two AD7280 devices on the AD7280 Evaluation board. The conversion results are displayed, on the running chart as integer code values. The upper chart refers to the conversion results from Device0 (U2) on the AD7280 Evaluation board. The lower chart refers to the conversion results from Device1 (U1). The instantaneous value of each conversion result is displayed, in hex format, on the individual indicators to the right of each chart. If the user would like to focus on the results of one channel, or selected channels, in particular the conversion results input to the chart from the remaining channels may be individually removed from the plot using the **Plot EN** buttons to the right of each chart.

At the bottom left of the graph are the zoom options. These allow you to zoom in and out to get a closer look at a sample, if required.

VT(Volts) Tab

The **VT(Volts)** tab displays the conversion results of the Vin inputs of the two AD7280 devices on the AD7280 Evaluation board. The conversion results are displayed, on the running chart in units of voltage. It should be noted that the voltage output is calculated using an LSB size of 1.22mV, that is 5V/4096. The upper chart refers to the conversion results from Device0 (U2) on the AD7280 Evaluation board. The lower chart refers to the conversion results from Device1 (U1). The instantaneous value of each conversion result is displayed, in hex format, on the individual indicators to the right of each chart. If the user would like to focus on the results of one channel, or selected channels, in particular the conversion results input to the chart from the remaining channels may be individually removed from the plot using the **Plot EN** buttons to the right of each chart.

At the bottom left of the graph are the zoom options. These allow you to zoom in and out to get a closer look at a sample, if required.

TAKING SAMPLES

Initiating Conversions on the AD7280 Evaluation board

To initiate conversions and capture the sample data you must click on the **Real Time** button. When you click the **Real Time** button, the software instructs the EVAL-CED1Z board to continuously initiate conversions and read back the conversion data from the AD7280 Evaluation board. The AD7280 Evaluation board allows conversions on all or selected channels to be initiated at periodic intervals. The default conversion loop interval is 2ms but can be increased to 5ms, 10ms or 30ms through the **Configure AD7280** button. conversion data from the AD7280. The samples taken are then uploaded and displayed on the Data Capture Tabs. To stop conversions you must click on the **Real Time** button again

Reading from and Writing to Registers on the AD7280 Evaluation board

To read from and write to the registers on the two AD7280 devices on the AD7280 Evaluation board you must click on the **Read/Write Register** button. When you click the **Read/Write Register** button, the software instructs the EVAL-CED1Z board to read the data in each of the AD7280 registers and displays this information on the screen, please refer to Figure 4. The register data for Device0 (U2) is on the left of the screen and the register data for Device1 (U1) is on the right. The register data is presented in binary format.

To change the settings of any of the displayed registers you must overwrite the displayed binary value with the new value and then click on the **Update** button. It should be noted that one or all of the registers may be written to with a single update.

Configuring the AD7280 Evaluation board

The default configuration of the AD7280 on power up is to convert on all Voltage and VT channels following a Convert Start request. The AD7280 allows the option of converting, and reading back, conversion data from:

- 6 Voltage and 6 VT channels
- 6 Voltage and 3 VT channels
- 6 Voltage channels only

The user may select which configuration they would like by clicking on the **Configure AD7280** button. When you click this button the a new window will open, please refer to Figure 5, which allows the numbers of channels to convert and read back to be selected using the pull down menus. This window also

provides a pull down menu to allow you to select the conversion loop interval of the AD7280 Evaluation board.

As mentioned previously, please refer to Using the Software, increasing the conversion loop interval is recommended in the event that activity on the USB port is slowing down the transfer of data from the EVAL-CED1Z board to the PC.

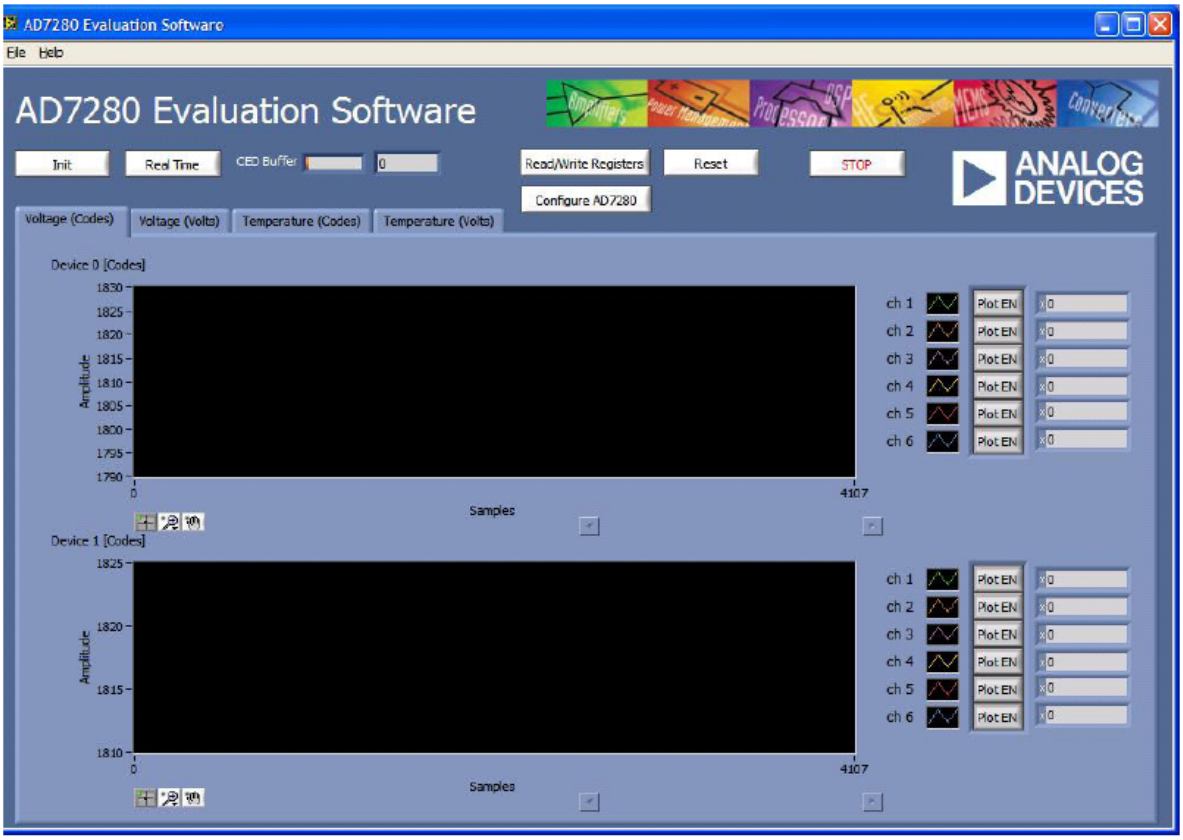


Figure 3. AD7280 Main Window

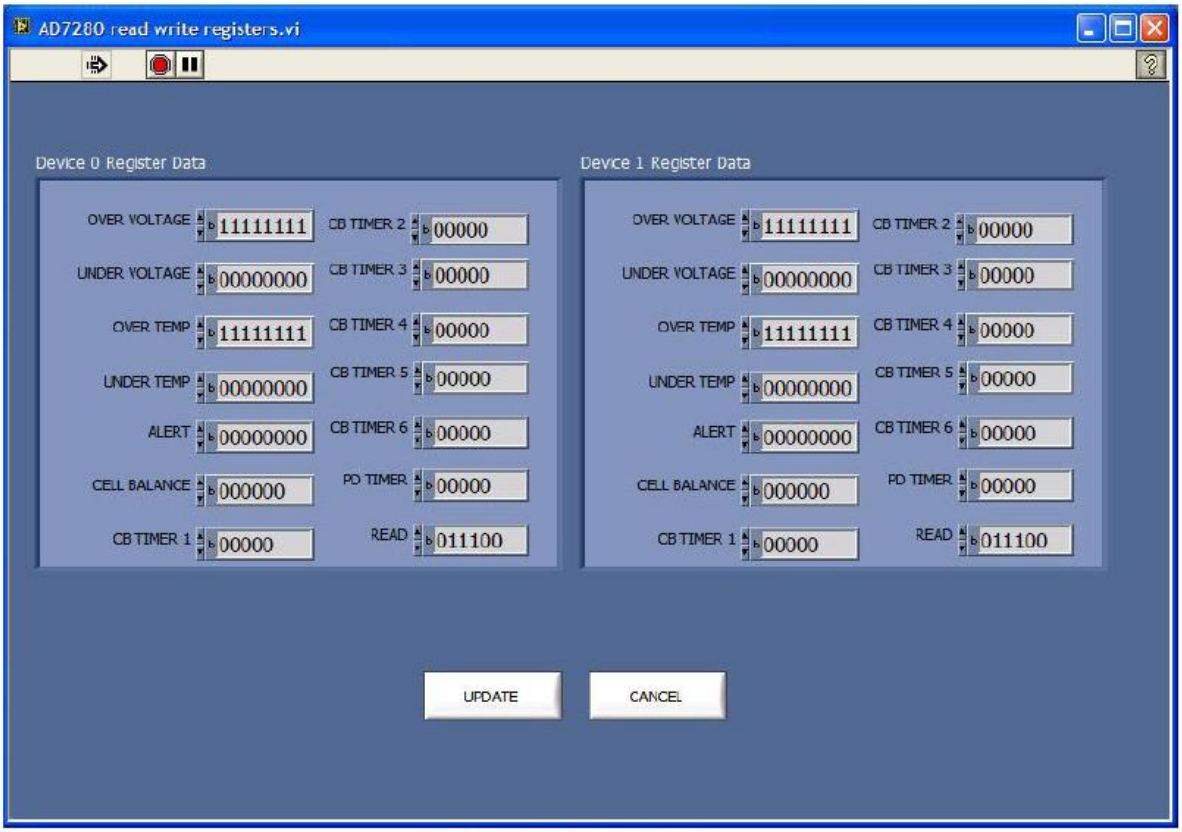


Figure 4. AD7280 Read/Write Register Window

Figure 5.Configure AD7280 Window

EVALUATION BOARD SCHEMATICS AND ARTWORK

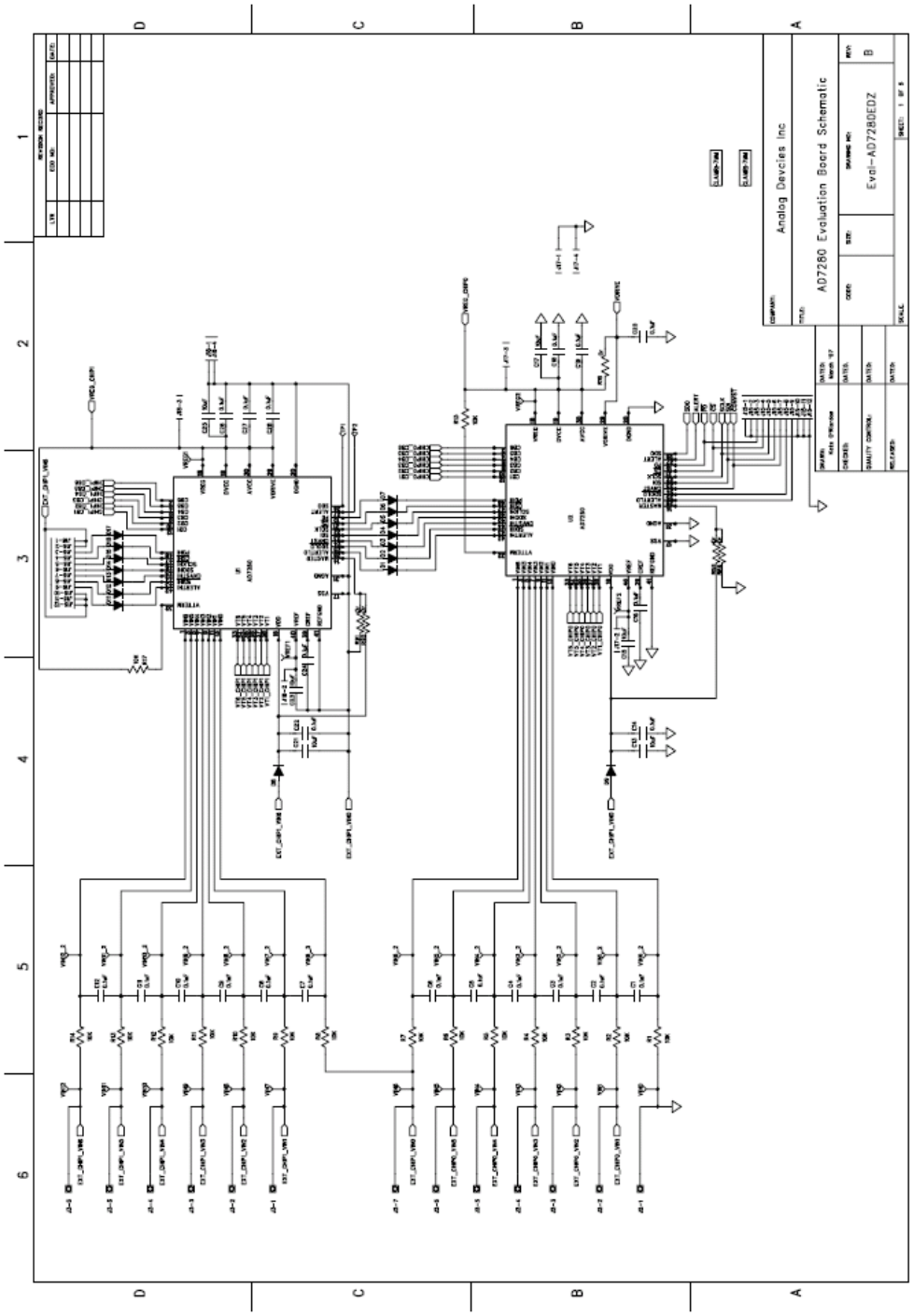


Figure 6. EVAL-AD7280 Schematic—Page 1

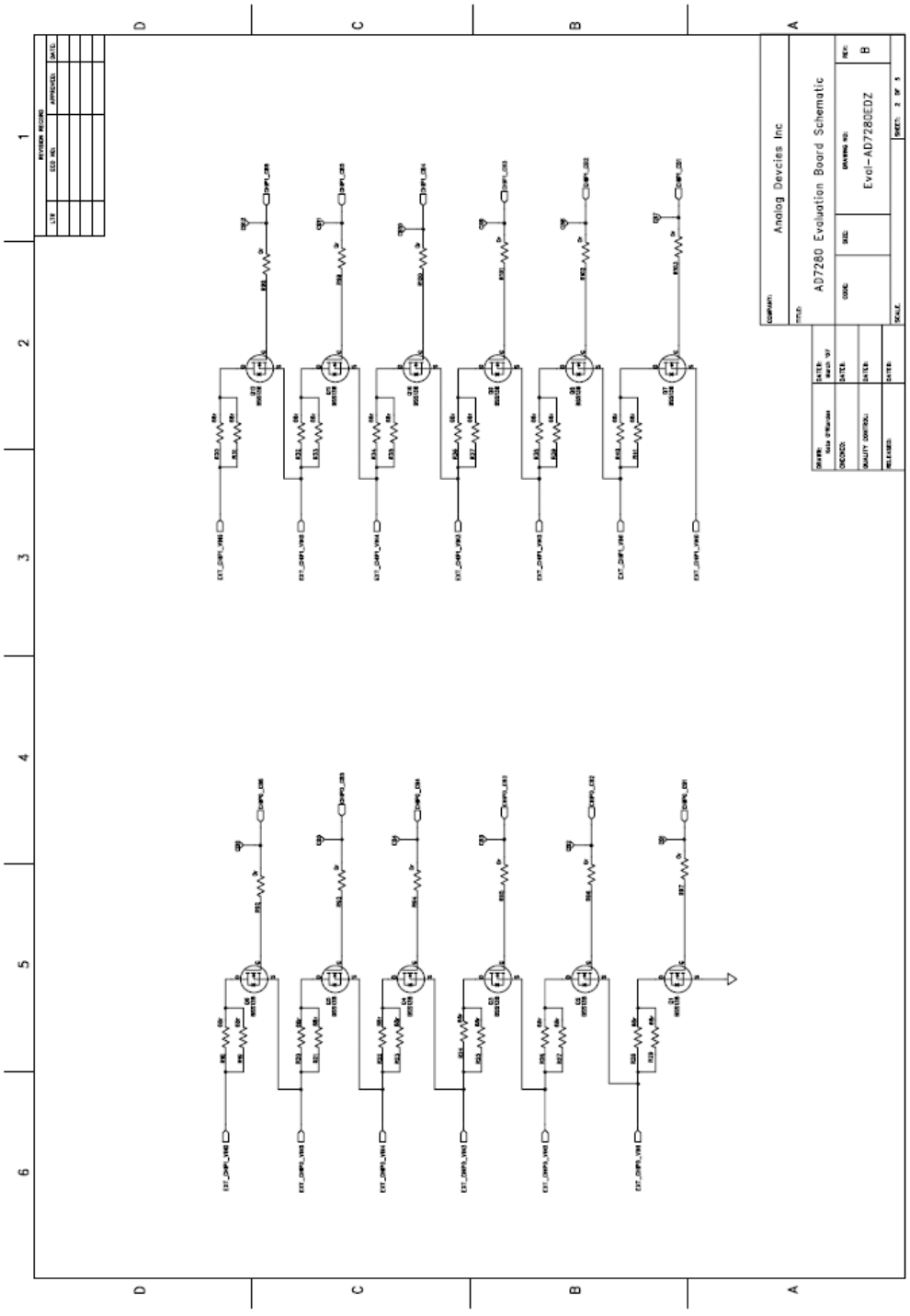


Figure 7. EVAL-AD7280 Schematic—Page 2

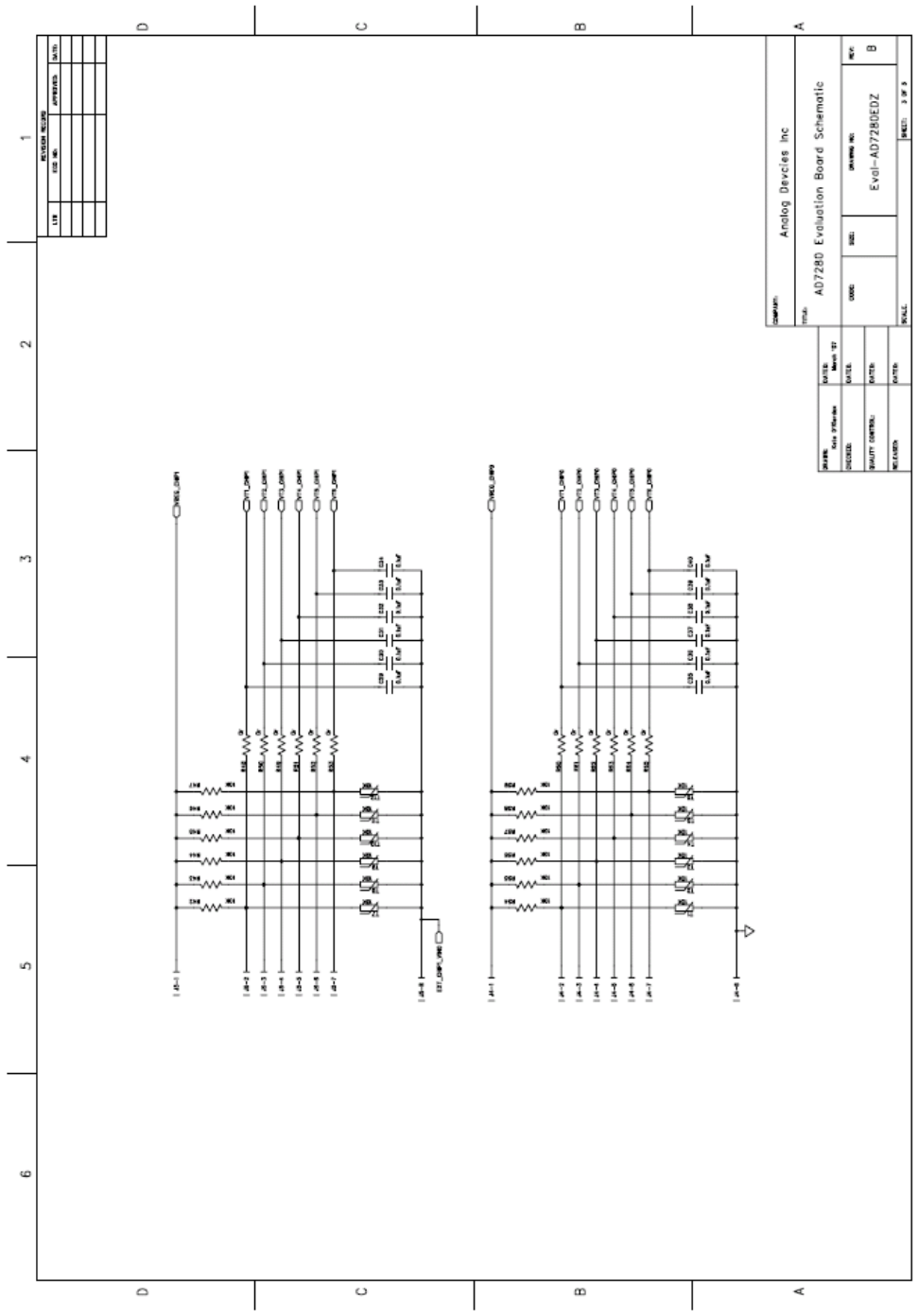


Figure 8. EVAL-AD7280 Schematic —Page 3

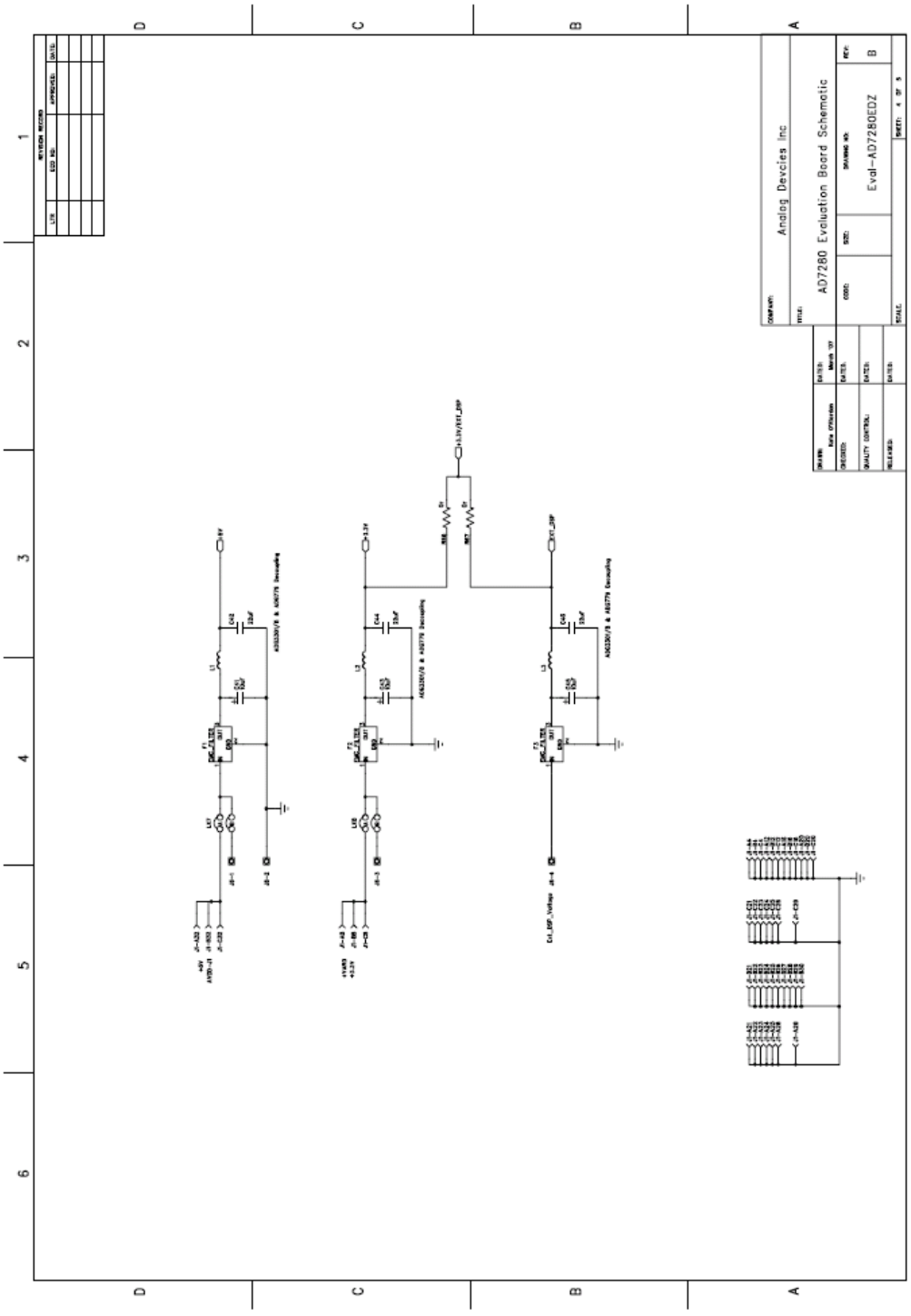


Figure 9. EVAL-AD7280 Schematic —Page 4

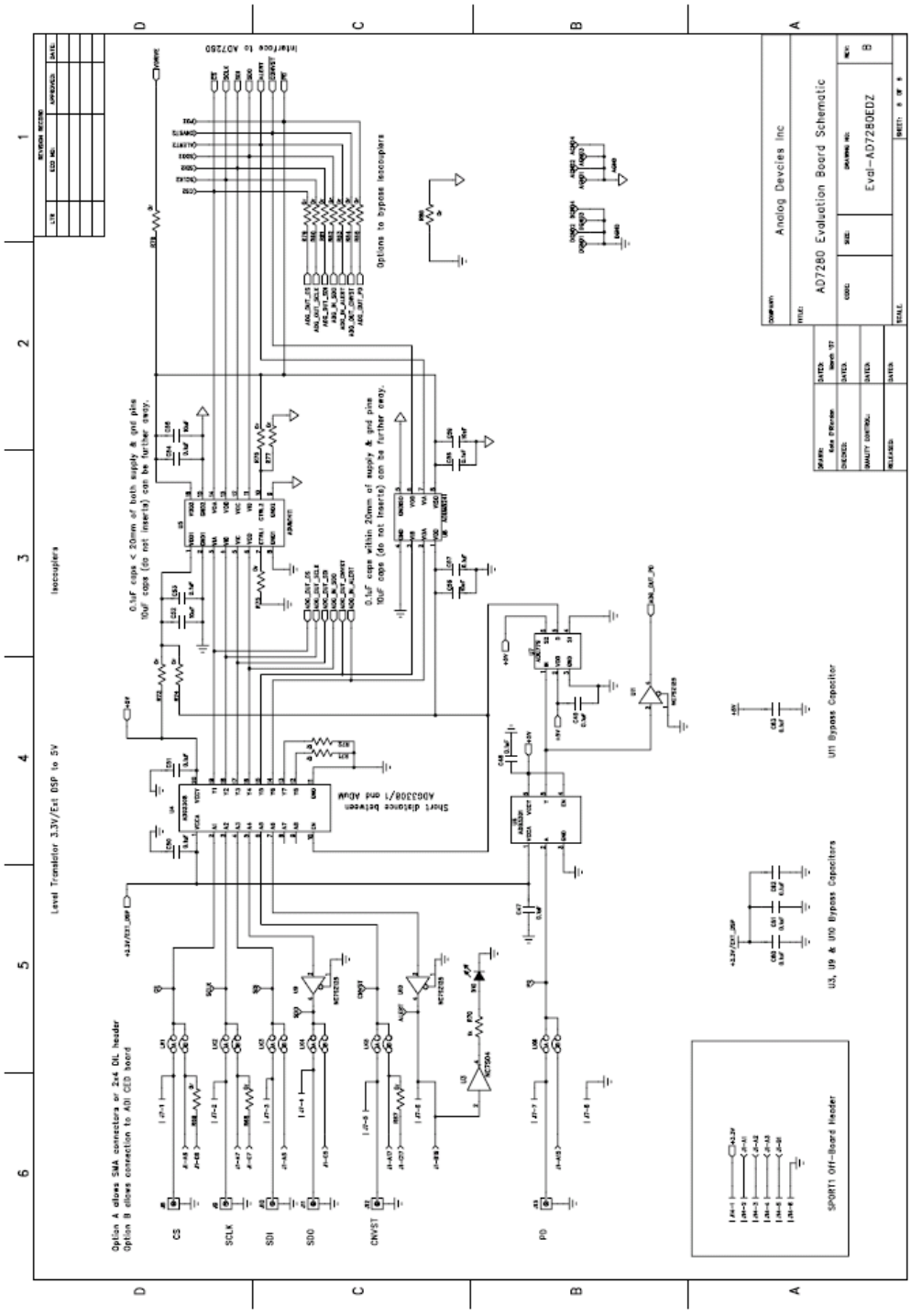


Figure 10. EVAL-AD7280 Schematic—Page 5

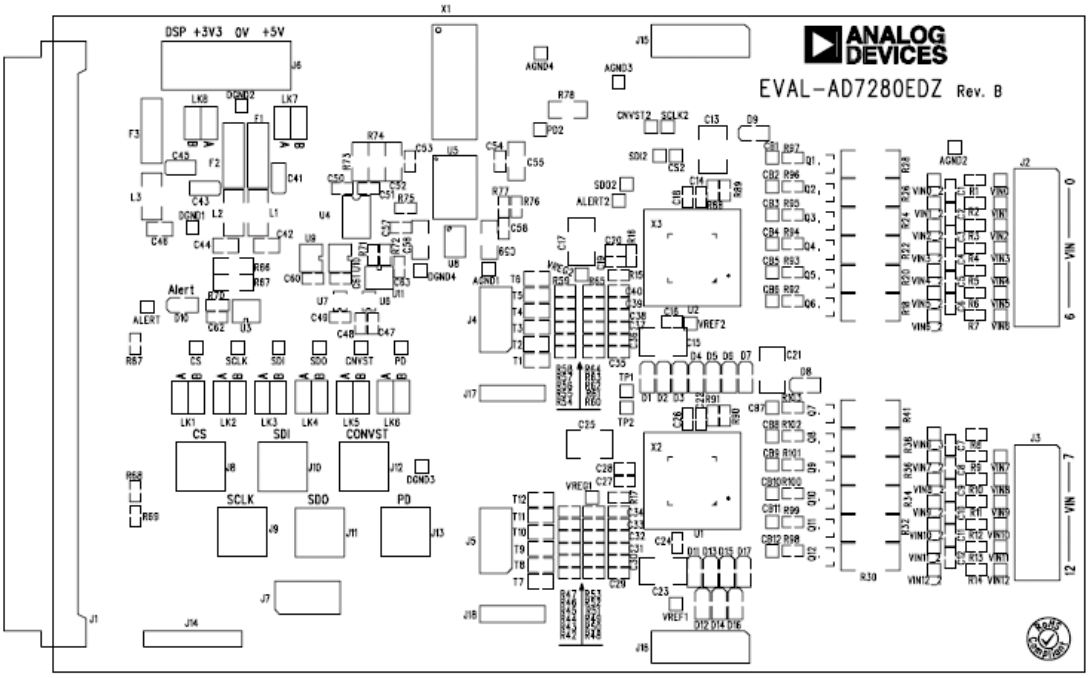


Figure 11. Silkscreen-Top Image

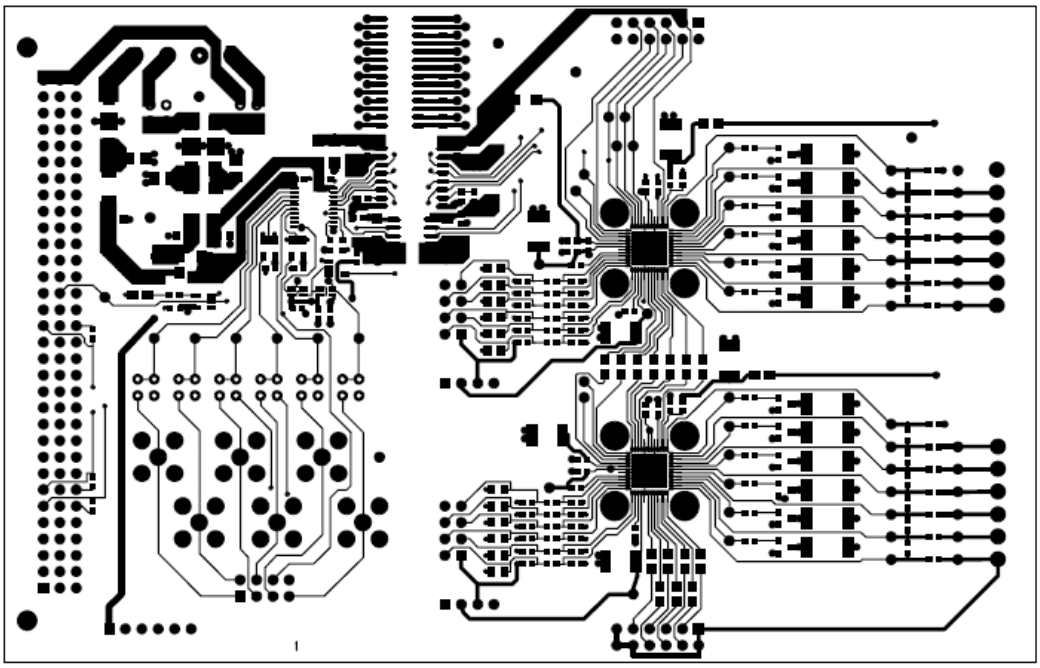


Figure 12. Layer1

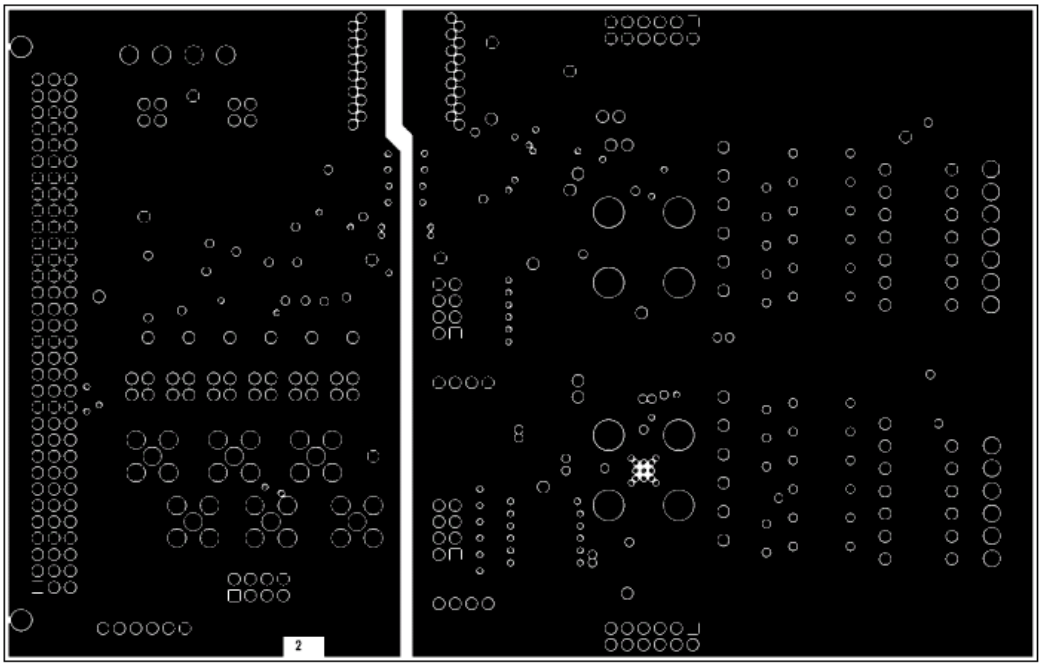


Figure 13. Layer 2

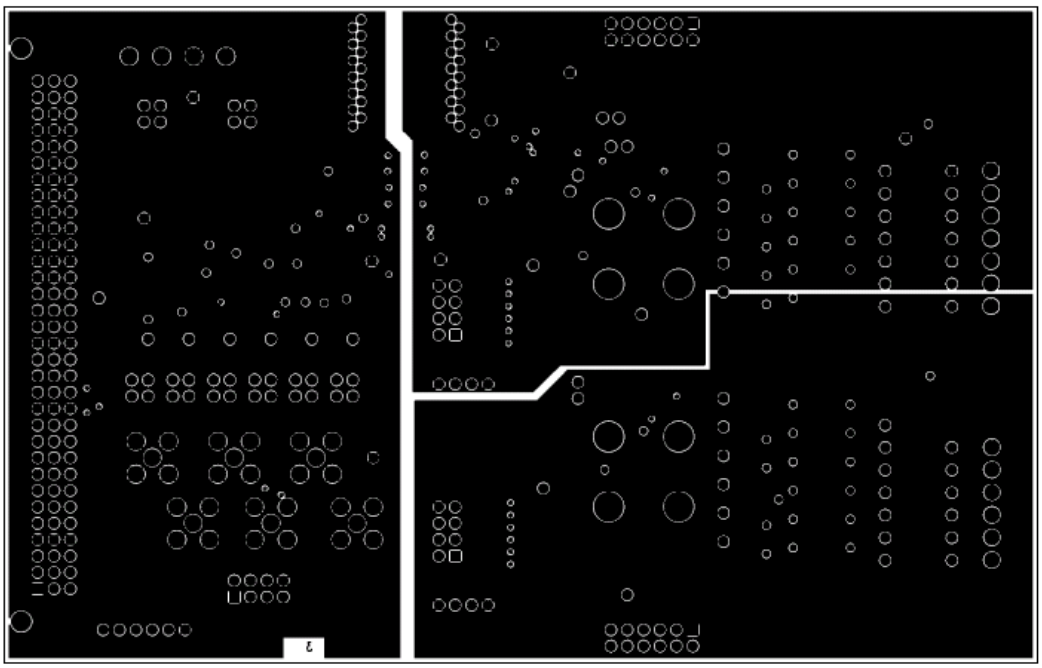


Figure 14. Layer 3

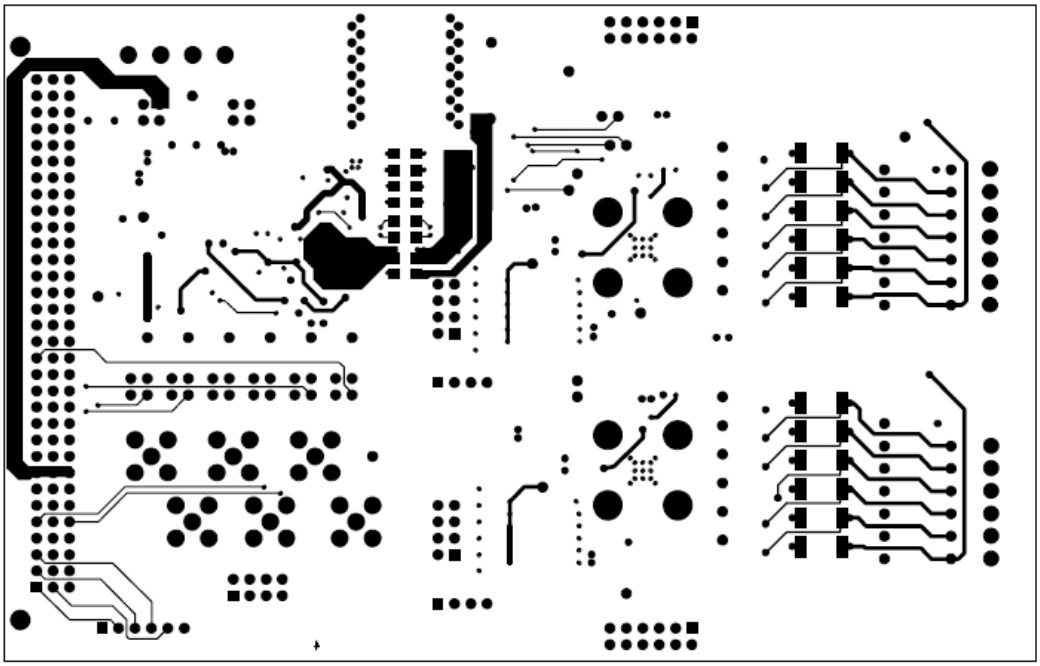


Figure 15. Layer 4

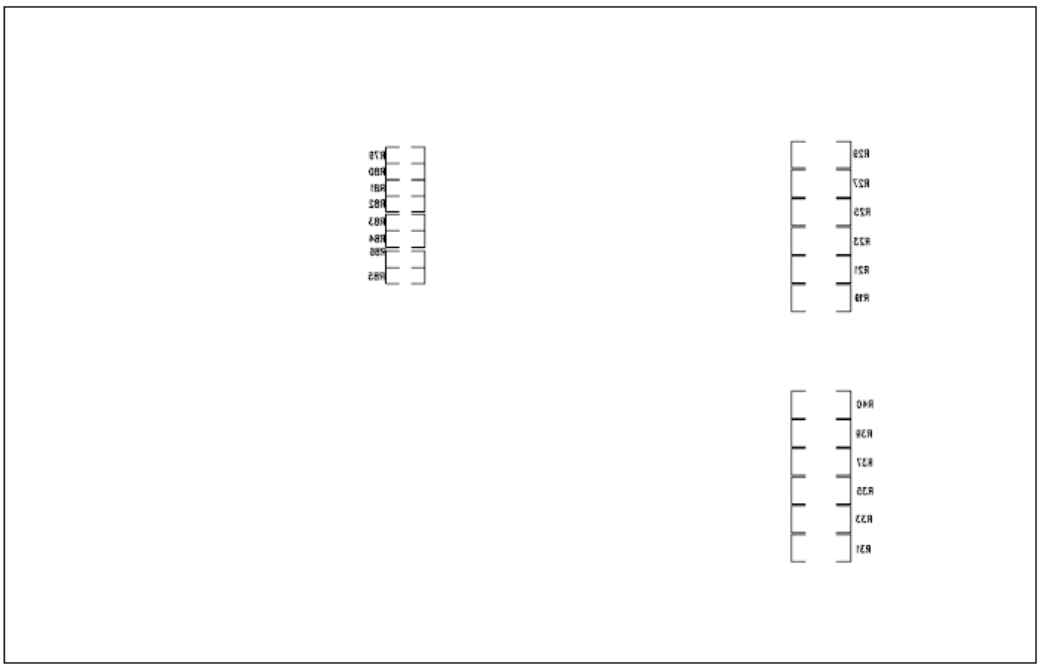


Figure 16. Silkscreen-Bottom Image

ORDERING INFORMATION

BILL OF MATERIALS

Table 10.

Quantity	Part Description	Reference Designator	Stock Code[1, 2]
2	12-Bit A/D Converter	U1, U2	AD7280BSTZ
1	NC7SZ04	U3	FEC 101-4133
1	ADG3308	U4	ADG3308BRUZ
1	ADuM1411	U5	ADuM1411BRWZ
1	ADG3301	U6	ADG3301BKSZ
1	ADG779	U7	ADG779BKSZ
1	ADuM5241	U8	ADuM5241ARZ
2	NC7SZ125	U9, U10	FEC 101-3811
33	0.1 µF Ceramic Capacitor, 50V, SMD0603	C1-C12, C14, C18-C20, C22, C24, C26 - C40	FEC 8820023
6	10 µF Ceramic Capacitor, 35V, SMD1812	C13, C15, C17, C21, C23 & C25	Digikey PCC2183CT-ND
3	10 µF Tantalum Capacitor, 10 V	C41, C43 & C45	FEC 197-130
3	22 µF Tantalum Capacitor, 6.3 V, SMD0805	C42, C44 & C46	Digikey 490-1719-1-ND
17	0.1 µF Ceramic Capacitor, 16V, SMD0603	C47-C51, C53, C54, C57 & C58	FEC 432210
4	10 µF Ceramic Capacitor,, 10V SMD1206	C52, C55, C56, C59	Digikey PCC1894CT-ND
9	TS4148 Small signal diode, SMD0805	D1 – D9, D11 – D17	FEC 815-0206
1	Red SMD 0805 Chip LED	D10	FEC 105-8373
3	Surface-Mount EMC Filters	F1 to F3	FEC 952-8202
1	96 – way connector	J1	FEC 1096832
1	7-Pin Terminal Block	J2	FEC 388-2615 (x2) & FEC 388-2627
1	6-Pin Terminal Block	J3	FEC 388-2627 (x2)
3	8 – way connector	J4, J5, J7	FEC 1022233 [Do not insert]
1	3-Pin Terminal Block	J6	FEC 151-790
6	Gold 50 SMA Jack	J8 - J13	FEC 1169631 [Do not insert]
1	6 – way connector	J14	FEC 1022255 [Do not insert]
2	12 – way connector	J15 – J16	FEC 1022238 [Do not insert]
2	4 – way connector	J17 – J18	FEC 1022251 [Do not insert]
3	Ferrite Beads	L1 to L3	FEC 952-6900
6	1-Way Jumper (1 × 2)	LK1 – LK8	FEC 1022244 (36-Pin Strip) & FEC 150411
12	BSS138	Q1 – Q12	FEC 984-5330
26	10 kΩ SMD0603 Resistor	R1 - R14, R42 - R47, R54 - R59	FEC 933-0399
35	0 Ω SMD0603 Resistor	R16, R76, R89, R90	FEC 933-1662 [Do not insert]
24	68 Ω SMD2512 Resistor	R18 - R41	FEC 128-3154
2	10 kΩ SMD0603 Resistor	R15, R17	FEC 933-0399 [Do not insert]
3	0 Ω SMD1206 Resistor	R66, R73, R78	FEC 933-6974
19	0 Ω SMD1206 Resistor	R67, R79 - R86	FEC 933-6974 [Do not insert]
33	0 Ω SMD0603 Resistor	R48 - R53, R60 - R65, R68, R69, R71, R72, R75, R77, R87, R88, R91, R92-R103	FEC 933-1662
1	1 kΩ SMD0603 Resistor	R70	FEC 933-0380
12	10 kΩ SMD0603 Thermistor	T1 – T12	FEC 118-7088
67	Testpoints		FEC 873-1144 (Pack)

[1] FEC = Farnell.
[2] P = Pericom Semiconductor Corporation.

ORDERING GUIDE

Model	Description
EVAL-AD7280EDZ[1]	AD7280 Evaluation Board

[1] Z = RoHS Compliant Part.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

)411

ANALOG DEVICES

www.analog.com

9.4.3. CED Datasheet

Converter Evaluation and Development (CED) Board

Preliminary Technical Data

EVAL-CED1Z

FEATURES

Interfaces to multiple serial and parallel precision converter evaluation boards
Supports high-speed LVDS interface
32MB SDRAM
4MB SRAM
USB 2.0 connection to PC
User reprogrammable Altera Cyclone FPGA
Provides 8 separate power supplies
Connects directly to Blackfin Ez-Kit

APPLICATIONS

Evaluating Precision Converters
Creation of demonstration systems
Prototyping of end-user systems

GENERAL DESCRIPTION

The CED1 board is part of a next generation platform from Analog Devices Inc., intended for use in evaluation, demonstration and development of systems using Analog Devices precision converters. It provides the necessary communications between the converter and the PC, programming or controlling the device, transmitting or receiving data over a USB link.

PACKAGE CONTENTS

- CED Board
- USB A to Mini-B cable
- 7 Volt 15W Power Supply

.

FUNCTIONAL BLOCK DIAGRAM

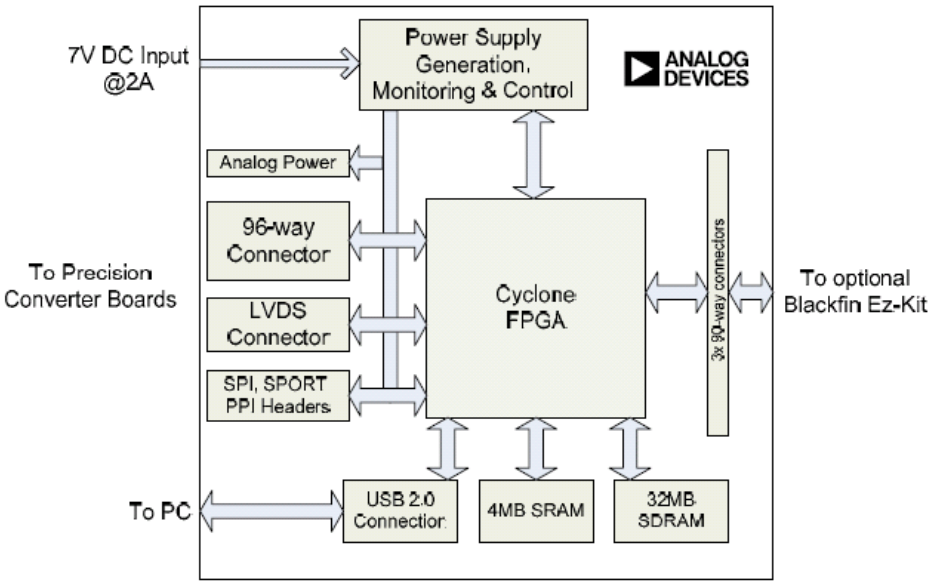


Figure 1.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

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REVISION HISTORY

7/07—Revision 0: Initial Revision

GENERAL DESCRIPTION

The Converter Evaluation and Development board is intended to assist system designers evaluate and prototype systems utilizing precision converter components from Analog Devices. It provides a means to read and write data, control and program devices from a PC via a high-speed USB 2.0 connection.

Due to its design, the CED1 can handle interfacing to multiple devices simultaneously for users who may wish to prototype their system utilizing proven hardware components from Analog Devices.

The reconfigurable FPGA-based architecture of the board allows the FPGA to be reprogrammed at any time via the USB connection. This allows the user to develop and run their own code to accomplish their desired task.

The many interfacing options accommodate connection to a wide range of precision converter evaluation boards in different form factors. Three standard 0.1-inch pitch headers are available, supporting SPI, SPORT and parallel functionality. A 96-way connector provides links to multiple interfaces and power supplies simultaneously. LVDS is supported through a dedicated connector designed for data pairs with individual grounds.

For developments that require a processor as well as an FPGA, the CED1 board provides the means to connect directly to a Blackfin EZ-Kit. Three 90-way connectors present on the board mate directly with the Blackfin Ez-Kit allowing the development of very powerful systems and demonstrations.

To help minimize the amount of external equipment needed to run a system successfully, the CED board provides eight separate power supplies made available for external connection. The details of these supplies and their current ratings are contained in the Power Supply section of this document.

The CED board requires a single 7V, 15W supply which ships with the board. The user may also connect a bench-top supply providing it can source a minimum current of 2A.

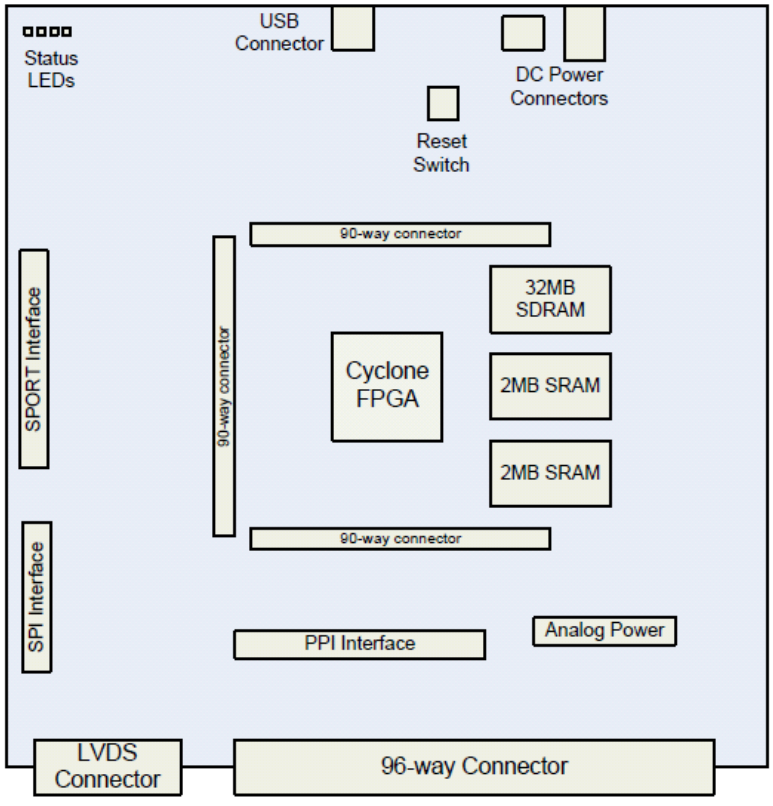


Figure 2. Major Component Locations

CONNECTORS

Many connectors are provided on the CED board to facilitate design and attachment of a range of different form factor converter boards. Due to the number of connections available on the FPGA, certain signals on different connectors are shared and replicated across different connectors.

All signals have been named to assist the user in identifying the shared signals and to which group they belong. SPI signals begin with SPI_xxx, SPORT signals begin with SPORT_xxx and parallel/PPI signals begin with PAR_xxx/PPI_xxx. More details of these signals are given in the relevant connector sections.

J5 – LVDS CONNECTOR

If connecting the CED1 to a high-speed LVDS converter evaluation board, this connector should be used. The connector provides for four differential receive and four differential transmit data pairs in addition to separate differential receive and transmit clocks. Control of any high-speed device is normally achieved over an interface separate to the data. For this purpose, the SPI and some parallel control signals are also routed over this connector. With the inclusion of three power supplies, this connector provides the flexibility to interface to many LVDS converters. Details of the pin-out of this connector are given in Table 1.

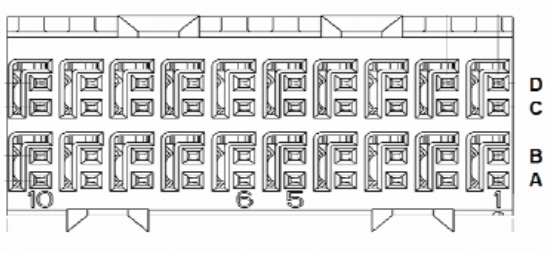


Figure 3. LVDS Connector pin locations

Table 1. LVDS Connector pin out

Pin Num	Pin Name	Description
1A, 1B	+VarA	Variable voltage analog power supply. See power supply section for more details.
1C, 1D	CLKOUT+/-	Differential Clock Output
2A	$\overline{\text{PAR\_CS0}}$	Parallel Chip Select 0
2B	$\overline{\text{PAR\_RD}}$	Parallel Read Strobe
C2-9, D2-7	Dx+/-	Differential Data Receive or Transmit Pair. By default the CED board is configured for 4 receive pairs (D0-3) and 4 transmit pairs (D4-7). These can be reconfigured by changing the termination resistors on the CED board. See schematics for more details.
A3-6	SPI_SELx	SPI Peripheral Chip Select
B3	$\overline{\text{PAR\_WR}}$	Parallel Write Strobe
B4	SPI_MISO	SPI Master In, Slave Out Data line
B5	SPI_MOSI	SPI Master Out, Slave In Data line
B6	SPI_CLK	SPI Clock
A7	TMR0/PPI_FS2	Timer 0 or Frame Sync 2 for PPI usage
B7	GPIO3/TMR1/PPI_FS1	General Purpose I/O, Timer 1 or Frame Sync 2 for PPI usage
A8	RXINT/GPIO2/PPI_FS3	Receive Interrupt, General Purpose I/O or Frame Sync 3 for PPI usage
B8	GPIO4/PAR_A0	General Purpose I/0 or parallel address LSb
A9, B9	+3.3VD_Edge	+3.3V Digital power supply
A10, B10	+VarD	Variable voltage digital power supply. See power supply section for more details.
C10, D10	CLKIN+/-	Differential Clock Input pair

J1 – MINI USB 'B' CONNECTOR

This is used to connect the CED1 to the PC for control and data transfer

J2 – 2-PIN SCREW TERMINAL POWER CONNECTOR

This connector is used when powering the CED board with a lab supply. Care must be taken to ensure the external supply is connected with the correct polarity.

J4 – DC POWER CONNECTOR

When using the CED1 with the supplied power supply, the DC plug should be connected here. The polarity for this connector is centre positive.

J6 – FPGA JTAG CONNECTOR

This can be used with Altera SignalTap Logic Analyzer and appropriate hardware to assist with FPGA development and debug.

J8, 9, 10 – 3× 90-WAY BLACKFIN EZ-KIT CONNECTORS

These three connectors bring across most of the peripheral signals from the Blackfin Ez-Kit directly into the FPGA where they can be used directly or rerouted to the other connectors. Additional processor or microcontroller boards could be designed and connected here if the user wished to add a processor to the design. See the Blackfin Ez-Kit manual for details of these connectors.

J3 – 96-WAY DIN41612 CONNECTOR

This connector has traditionally appeared on most precision ADC evaluation boards. It contains SPI, SPORT and Parallel signals as well as programmable digital and 5 separate analog power supplies. Pin out for this connector is shown in Table 2.

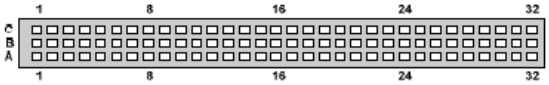


Figure 4. 96-way connector pin locations

Table 2. 96-way connector pin-out

Pin Num	Pin Name	Description
A1	SPORT_DT1PRI/ SPI_MOSI/PAR_D16	Sport1 Data Transmit Primary. SPI Master Out, Slave In data line. Parallel Data bit 16.
B1	GPIO3/TMR1/ PPI_FS1	General Purpose I/O bit 3. Timer 1. Parallel Peripheral Interface Frame Sync 1.
C1	SPORT_DR1PRI/ SPI_MISO/PAR_D19	Sport 1 Data Receive Primary. SPI Master In, Slave Out data line. Parallel Data bit 19.
A2	SPORT_TFS1/ SPI_SEL0/PAR_D17	Sport 1 Transmit Frame Sync. SPI Peripheral Chip Select 0. Parallel Data bit 17.
B2	PAR_D0	Parallel Data bit 0 (LSb)
C2	SPORT_RFS1/ SPI_SEL1/PAR_D20	Sport 1 Receive Frame Sync. SPI Peripheral Chip Select 1. Parallel Data bit 20.
A3	SPORT_TSCLK1/ SPI_CLK/PAR_D18	Sport 1 Transmit Serial Clock. SPI Clock. Parallel Data bit 18.
B3	PAR_D1	Parallel Data bit 1.
C3	SPORT_RSCLK1/ SPI_CLK/PAR_D21	Sport 1 Receive Clock. SPI Clock. Parallel Data bit 21.
A4, B4, C4	DGND	Digital Ground
A5	SPORT_DT0PRI/ SPI_SEL7	Sport 0 Data Transmit Primary. SPI Peripheral Chip Select 7
B5	PAR_D2	Parallel Data bit 2

C5	SPORT_DR0PRI/ SPI_SEL4	Sport 0 Data Receive Primary. SPI Peripheral Chip Select 4
A6	SPORT_TFS0/ SPI_SEL6	Sport 0 Transmit Frame Sync. SPI Peripheral Chip Select 6
B6	PAR_D3	Parallel Data bit 3
C6	SPORT_RFS0/ SPI_SEL3	Sport 0 Receive Frame Sync. SPI Peripheral Chip Select 3
A7	SPORT_TSCLK0/ SPI_SEL5	Sport 0 Transmit Serial Clock. SPI Peripheral Chip Select 5
B7	PAR_D4	Parallel Data bit 4
C7	SPORT_RSCLK0/ SPI_SEL2	SPORT 0 Receive Serial Clock. SPI Peripheral Chip Select 2
A8, B8, C8	+VarD (DV_{DD})	Variable Digital Power Supply. See Power Supply section for further details.
A9	PAR_RD	Parallel Read Strobe
B9	PAR_D5	Parallel Data bit 5
C9	PAR_WR	Parallel Write Strobe
A10	PAR_D22/PAR_A7	Parallel Data bit 22. Parallel Address bit 7 (MSb)
B10	PAR_D6	Parallel Data bit 5
C10	PAR_CS0	Parallel Chip Select 0
A11	SPORT_DT0SEC/ PAR_CS1/PAR_A5	Sport 0 Data Transmit Secondary. Parallel Chip Select 1. Parallel Address bit 5
B11	PAR_D7	Parallel Data bit 7
C11	GPIO6/PAR_D23/ PAR_A6	General Purpose I/O bit 6. Parallel Data bit 23. Parallel Address bit 6
A12, B12, C12	DGND	Digital Ground
A13	TWI_SDA/PAR_CS3/ PAR_A3	Two Wire Interface Serial Data. Parallel Chip Select 3. Parallel Address bit 3
B13	PAR_D8	Parallel Data bit 8
C13	SPORT_DR0SEC/ PAR_CS2/PAR_A4	Sport 0 Data Receive Secondary. Parallel Chip Select 2. Parallel Address bit 4
A14	GPIO5/PAR_A1	General Purpose I/O bit 5. Parallel Address bit 1
B14	PAR_D9	Parallel Data bit 9
C14	TWI_SCL/GPIO7/ PAR_A2	Two Wire Interface Serial Clock. General Purpose I/O bit 7 (MSb). Parallel Address bit 2
A15	GPIO0	General Purpose I/O bit 0 (LSb)
B15	PAR_D10	Parallel Data bit 10
C15	GPIO4/PAR_A0	General Purpose I/O bit 4. Parallel Address bit 0 (LSb)
A16, B16, C16	DGND	Digital Ground

A17	TMR0/PPI_FS2	Timer 0. Parallel Peripheral Interface Frame Sync 2
B17	PAR_D11	Parallel Data bit 11
C17	RXINT/GPIO2/ PPI_FS3	Receive Data Interrupt. General Purpose I/O bit 2. Parallel Peripheral Interface Frame Sync 3
A18	PAR_D12	Parallel Data bit 12
B18	PAR_D13	Parallel Data bit 13
C18	PAR_D14	Parallel Data bit 14
A19	CLKOUT	Clock Output
B19	GPIO1	General Purpose I/O bit 1
C19	PAR_D15	Parallel Data bit 15
A20, B20, C20	DGND	Digital Ground
A21-26, B21-26, C21-26	AGND	Analog Ground
A27, C27	+VarA	Variable Analog Power Supply. See Power Supply section for further details.
B27	AGND	Analog Ground
A28	N/C	No Connect. Do not use this pin.
B28	AGND	Analog Ground
C28	N/C	No Connect. Do not use this pin.
A29, B29, C29	AGND	Analog Ground
A30	-12VA	-12V Analog Power Supply. See Power Supply section for further details.
B30	AGND	Analog Ground
C30	+12VA	+12V Analog Power Supply. See Power Supply section for further details.
A31, B31, C31	-5VA (AV_{SS})	-5V Analog Power Supply. See Power Supply section for further details.
A32, B32, C32	+5VA (AV_{DD})	+5V Analog Power Supply. See Power Supply section for further details.

J7 – ANALOG POWER CONNECTOR

If any analog power supplies are required on boards connected to the CED1 via any connector other than the J3 (96-way), they can be taken from this pin header. Pin-out details of this connector are given in Table 3. Further details of the power supplies are given in the following section.

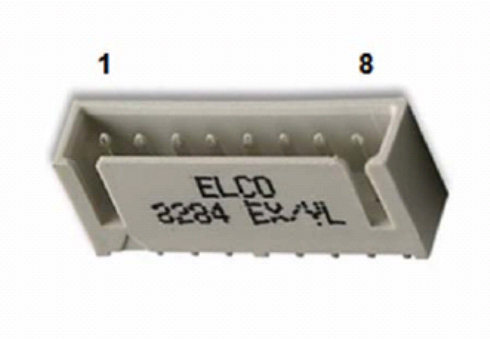


Figure 5. Analog Power Connector Pin Locations

Table 3. Analog Power Connector pin-out

Pin No	Function	Description
1	+12VA_Edge	+12V Analog Supply
2	-12VA_Edge	-12V Analog Supply
3, 6, 8	AGND	Analog Ground
4	+5VA_Edge	+5V Analog Supply
5	-5VA_Edge	-5V Analog Supply
7	+VarA	Variable Voltage Analog Supply. See Power Supply Section for more details.

J12 – SPORT INTERFACE

This standard two row, 0.1-inch connector can be used to connect any daughter board that utilizes the SPORT interface. This connector also contains all the SPI and Two Wire Interface (TWI) signals as well as 5V, 3.3V and the +7V CED board supply. See Table 4 for details. The pin-out of this connector is compatible with the Blackfin Stamp and Ez-Kit SPORT connector. More information on the pin names is given in the section detailing the 96-way connector.

Table 4. SPORT Connector Pin out

+5VD_Edge	1	2	+7V
DGND	3	4	N/C (Keying Pin)
$\overline{\text{RESET}}$	5	6	SPORT_TSCLK0/SPI_SEL5
SPORT_RFS0/SPI_SEL3	7	8	SPORT_DR0PRI/SPI_SEL4
DGND	9	10	SPORT_DR0SEC
SPORT_TFS0/SPI_SEL6	11	12	SPORT_DT0SEC
+3.3VD_Edge	13	14	SPORT_DT0PRI/SPI_SEL7
+3.3VD_Edge	15	16	SPORT_RSCLK0/SPI_SEL2
$\overline{\text{SPI\_SS}}$	17	18	SPI_MOSI
SPI_SEL1	19	20	SPI_MISO
SPI_SEL2	21	22	SPI_CLK
SPI_SEL3	23	24	TWI_SDA
SPI_SEL4	25	26	TWI_SCK
SPI_SEL5	27	28	RXINT/GPIO2/PPI_FS3
SPI_SEL6	29	30	GPIO3/TMR1/PPI_FS1
SPI_SEL7	31	32	TMR0/PPI_FS2
DGND	33	34	DGND

J13 – SPI INTERFACE

Using the SPI connector instead of the SPORT should only be considered when the user is satisfied that the device being connected is completely compatible with the SPI specification. This implies that only 8- or 16-bit active low framing is required. See Table 5 for pin-out details of this connector. This connector is compatible with the SPI connector on the Blackfin Stamp and Ez-Kits. More information on the pin names is given in the section detailing the 96-way connector.

Table 5. SPI Connector Pin out

+5VD_Edge	1	2	+3.3VD_Edge
+5VD_Edge	3	4	+3.3VD_Edge
SPI_MOSI	5	6	SPI_MISO
$\overline{\text{RESET}}$	7	8	SPI_CLK
SPI_SEL1	9	10	$\overline{\text{SPI\_SS}}$
SPI_SEL3	11	12	SPI_SEL2
SPI_SEL5	13	14	SPI_SEL4
SPI_SEL7	15	16	SPI_SEL6
N/C (Keying Pin)	17	18	DGND
+7V	19	20	DGND

J14 – PPI INTERFACE

This connector is intended to allow attachment of daughter boards designed to connect to the PPI Connector on the Blackfin Stamp and Ez-Kit. However, with the signals provided, it should be possible to connect to most parallel interface devices needing up to 16 data bits and multiple control signals.

The inclusion of the SPI signals on this connector allows for separate data and configuration interfaces if required. See Table 6 for details of this connector. More information on the pin names is given in the section detailing the 96-way connector.

Table 6. PPI Connector Pin out

+5VD_Edge	1	2	+7V
+5VD_Edge	3	4	N/C (Keying Pin)
+3.3VD_Edge	5	6	CLKOUTP_EXT
+3.3VD_Edge	7	8	PAR_D0
PAR_D1	9	10	PAR_D2
PAR_D3	11	12	PAR_D4
PAR_D5	13	14	PAR_D6
PAR_D7	15	16	PAR_D8
PAR_D9	17	18	PAR_D10
PAR_D11	19	20	PAR_D12
PAR_D13	21	22	PAR_D14
PAR_D15	23	24	SPI_SEL3
SPI_SEL2	25	26	SPI_SEL1
$\overline{\text{SPI\_SS}}$	27	28	$\overline{\text{RESET}}$
RxInt/GPIO2/PPI_FS3	29	30	SPI_MOSI
GPIO3/TMR1/PPI_FS1	31	32	SPI_MISO
TMR0/PPI_FS2	33	34	SPI_CLK
DGND	35	36	TWI_SDA
DGND	37	38	TWI_SCK
DGND	39	40	DGND

CONNECTOR PART NUMBERS

Table 7. Connector Part Numbers

Ref. Des.	Description	Manufacturer	Part Number	Mating Connector
J1	USB Mini-B connector	Molex	565790576	Standard Mini-B USB Cable
J2	2-pin screw terminal	Camden Electronics	CTB5000/2	Cables inserted directly
J3	96-Way 90° DIN41612 socket	Harting	0973 296 6801	0903 196 6921
J4	DC Barrel connector, 2mm centre	Kycon	KLDX-SMT2-0202-A	Cliff - DCPP1 (FC68147)
J5	LVDS connector	Tyco Electronics	1469028-1	1469169-1
J6	10-Pin, 2 row standard 0.1" pitch header	Harwin	M20-8760542	M20-7830546
J8-10	90-way Micro-strip Terminal	Samtec	TFC-145-X2-FD-A	SFC-145-T2-FD-A
J12	34-Pin, 2 row standard 0.1" pitch header	Harwin	M20-8761742	M20-7831746
J13	20-Pin, 2 row standard 0.1" pitch header	Harwin	M20-8761042	M20-7831046
J14	40-Pin, 2 row standard 0.1" pitch header	Harwin	M20-8762042	M20-7832046

POWER SUPPLIES

The CED board provides multiple power supplies that are made available for use with connected boards. A single 7V supply is required for the CED board and this is used to power the board itself and the supplies for boards connected to it. A resettable 2A fuse limits the current that can be drawn from the supply thus limiting the power consumption of the CED and any attached boards.

On it's own without any converter boards attached, the idle current of the CED is approximately 220 mA. When accessing SRAM for example, the current drawn by the CED board itself can increase significantly. Users designing boards to operate with the CED that wish to use the supplies provided must bear in mind the total available power when calculating their power requirements.

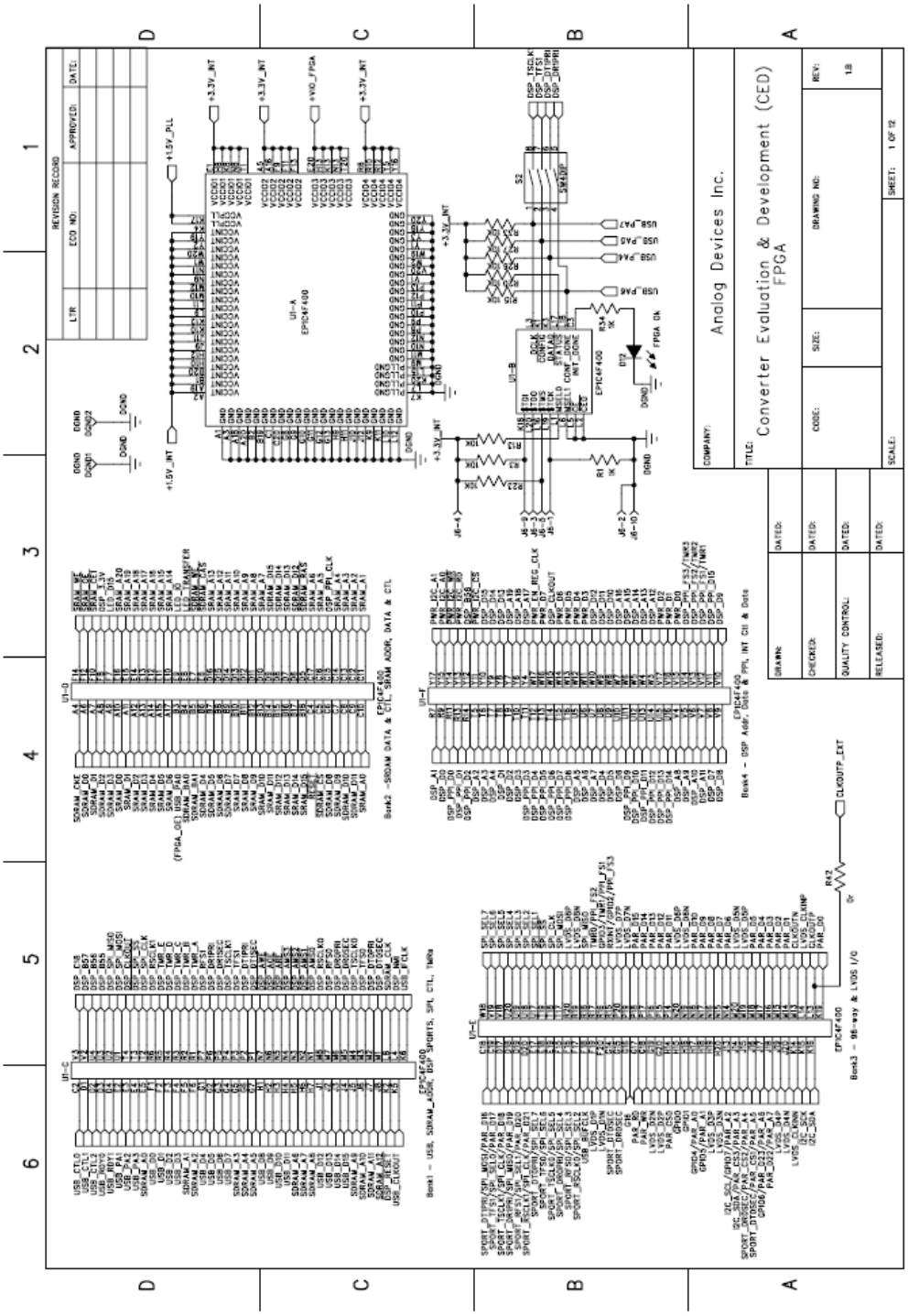
While the supplies generated on the CED are kept as clean as possible, designers of boards connected to the CED must ensure that all devices and supplies are adequately decoupled. This will prevent noise being fed back onto the power supplies of the CED. Excessive noise introduced on to the power supplies may cause the CED or attached boards to malfunction.

The voltage and current ratings of the supplies listed in Table 8 are defined to be absolute maximum limits. While fuses and thermal overload protection have been provided in the power supply circuitry, attempting to draw more current from a particular supply or exceeding the total power available from a combination of supplies may cause damage to the CED board.

Table 8. Power Supplies

Name	Voltage	Max. Current	Test Conditions / Comments
+VarA	+1.5V to +5.5V	300mA	Regulation may suffer at lower voltages.
-12VA	-12V ±5%	100mA	Fuse limited at 100mA.
+12VA	+12V ±5%	100mA	Fuse limited at 100mA.
-5VA	-5V ±5%	100mA	Fuse limited at 100mA.
+5VA	+5V ±5%	500mA	Regulator rated for 500mA but thermally limited.
+5VD	+5V ±5%	500mA	Regulator rated for 500mA but thermally limited.
+3.3VD	+3.3V ±5%	300mA	Thermally limited.
+VarD	+1.5V to +5.5V	300mA	Regulation may suffer at lower voltages.
+7V	+7V ±5%	2A	Total current that can be drawn through board including all other supplies. Fuse limited.

SCHEMATICS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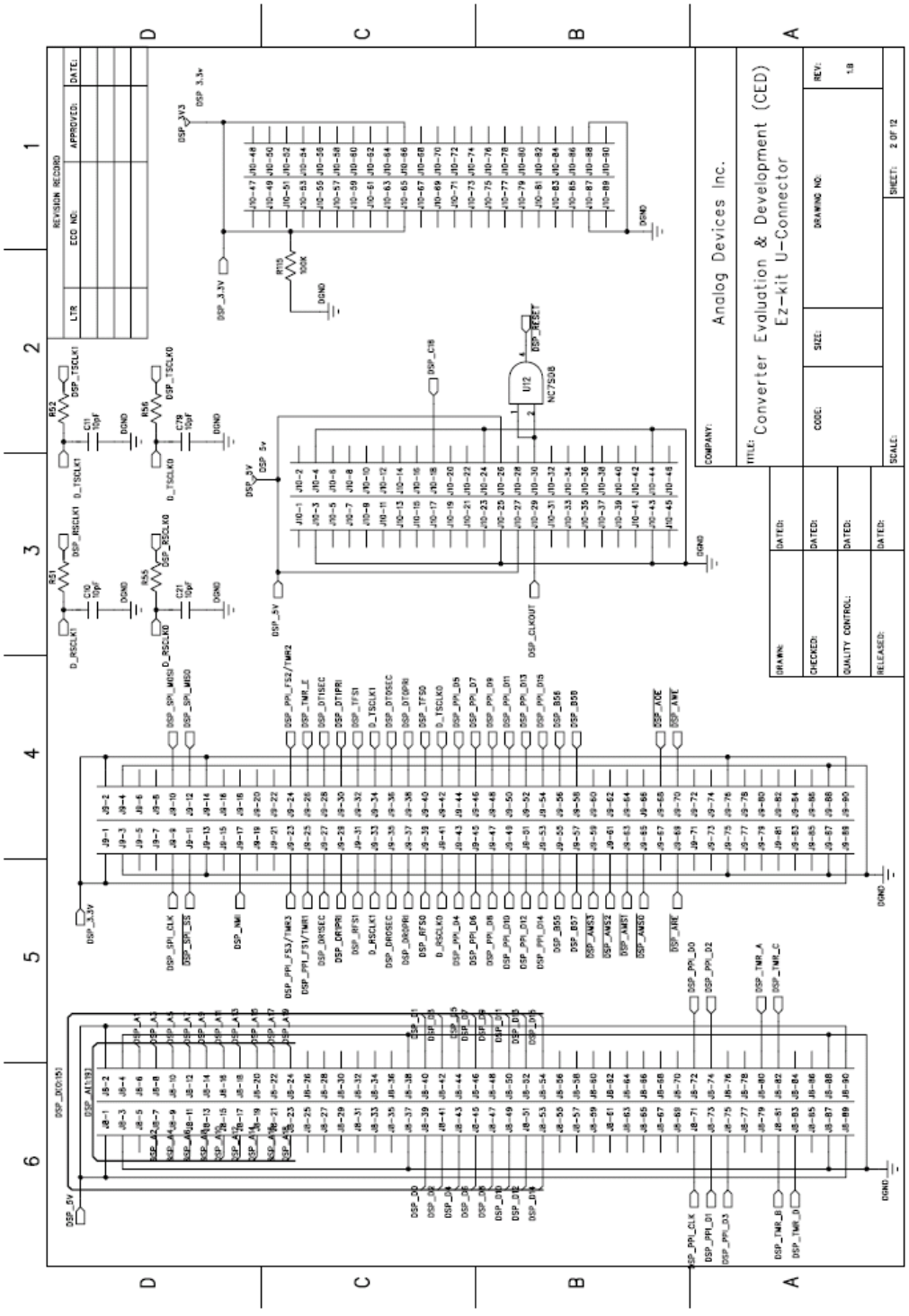
Converter Evaluation & Development (CED)
FPGA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Converter Evaluation & Development (CED)
Ez-kit U-Connector
REVISION RECORD
DSP_3V3
DSP_5V
DSP_A3.3V
DGND
DSP_RESET
DSP_CLKOUT
DSP_TSCLK1
DSP_TSCLK0
DSP_RSCLK1
DSP_RSCLK0
DSP_SPI_MOSI
DSP_SPI_MISO
DSP_SPI_CLK
DSP_SPI_SS
DSP_NMI
DSP_PPI_FS3/TMR3
DSP_PPI_FS1/TMR1
DSP_TMR_A
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DSP_TMR_C
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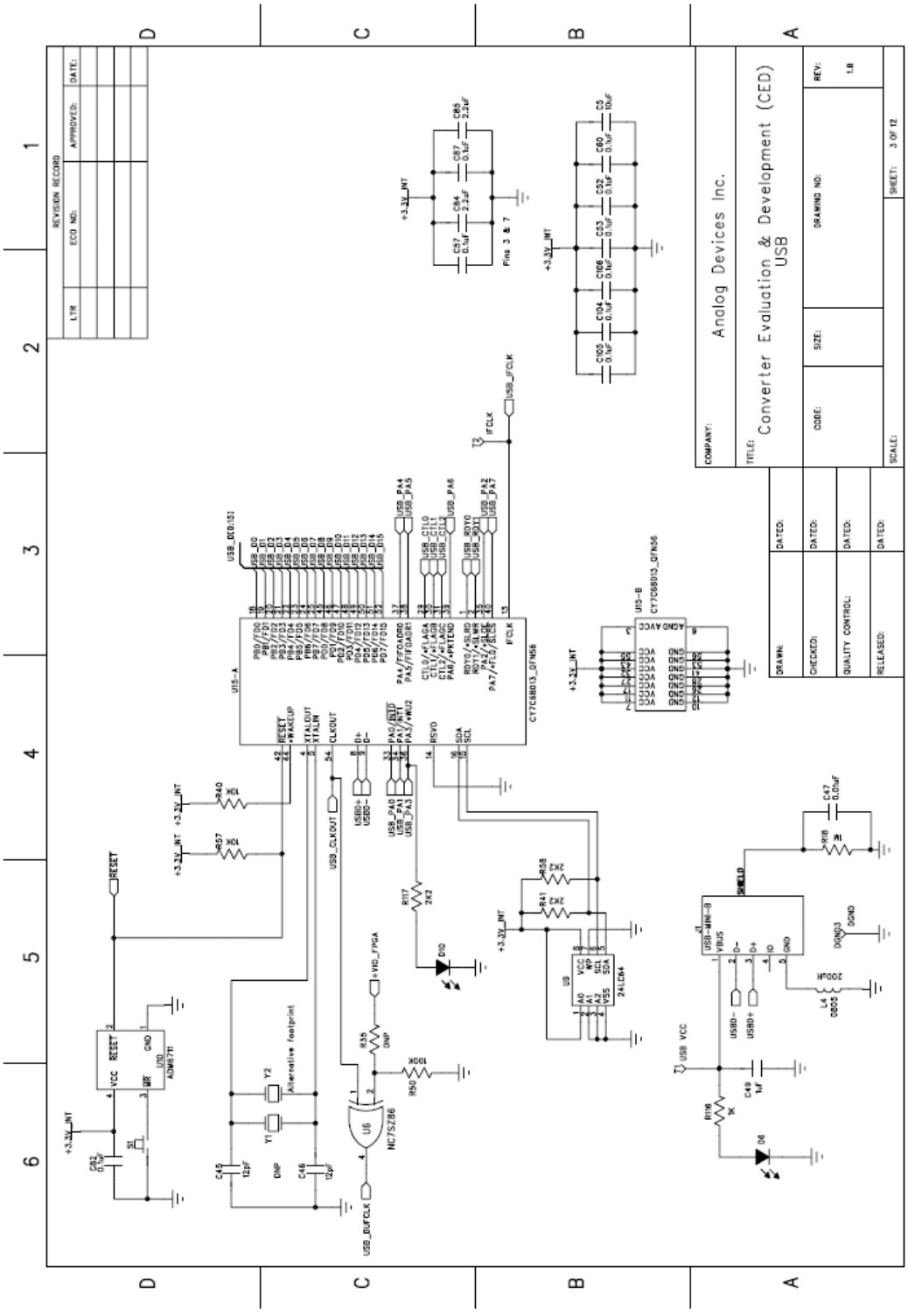
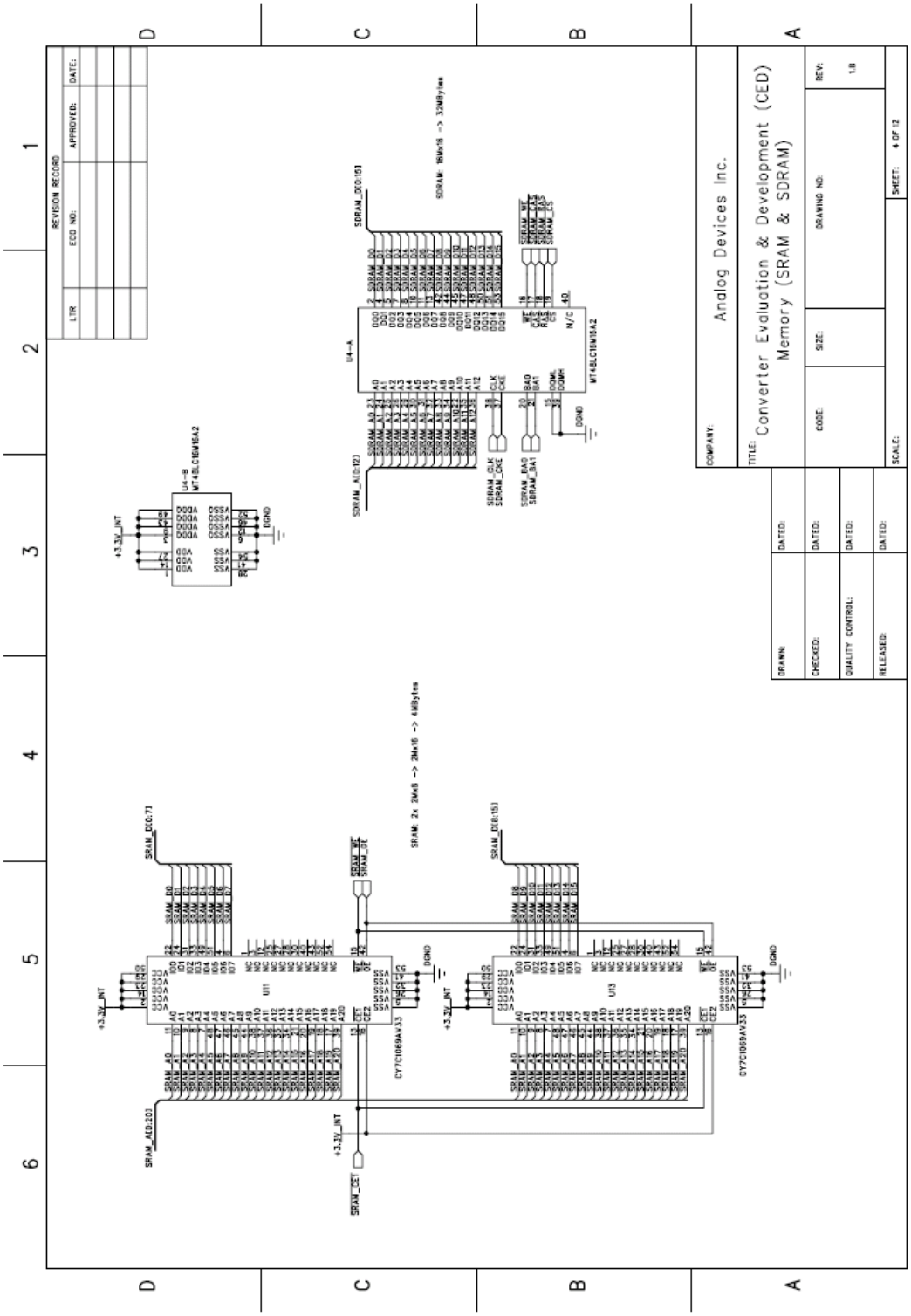
DSP_PPI_D1
DSP_PPI_D3


Analog Devices Inc.
Converter Evaluation & Development (CED)
USB
COMPANY:
TITLE:
SIZE:
CODE:
DRAWING NO:
REV:
SHEET:
SCALE:
DRAWN:
CHECKED:
QUALITY CONTROL:
RELEASED:
DATED:
REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
U15-A
CY7C68013_QFN56
U15-B
U10
ADM6711
U5
NC7SZ86
U9
24LC64
J1
USB-MINI-B
Y1
Y2
Alternative footprint
D10
D6
RESET
+3.3V_INT
+VID_FPGA
USB_CLKOUT
USB_BUFCLK
USB_IFCLK
USB_D[0:15]
DGND
SHIELD
USB VCC
Pins 3 & 7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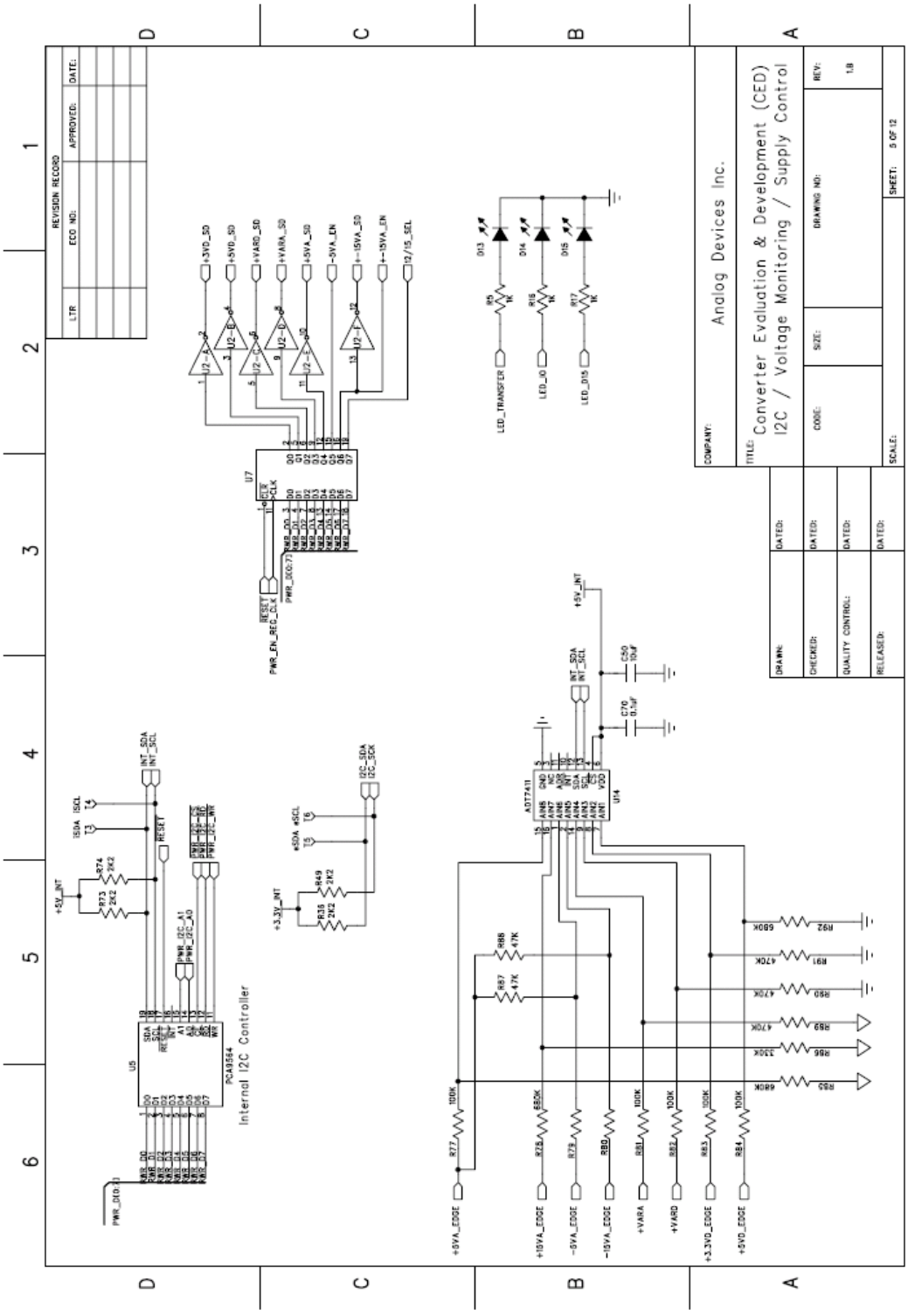
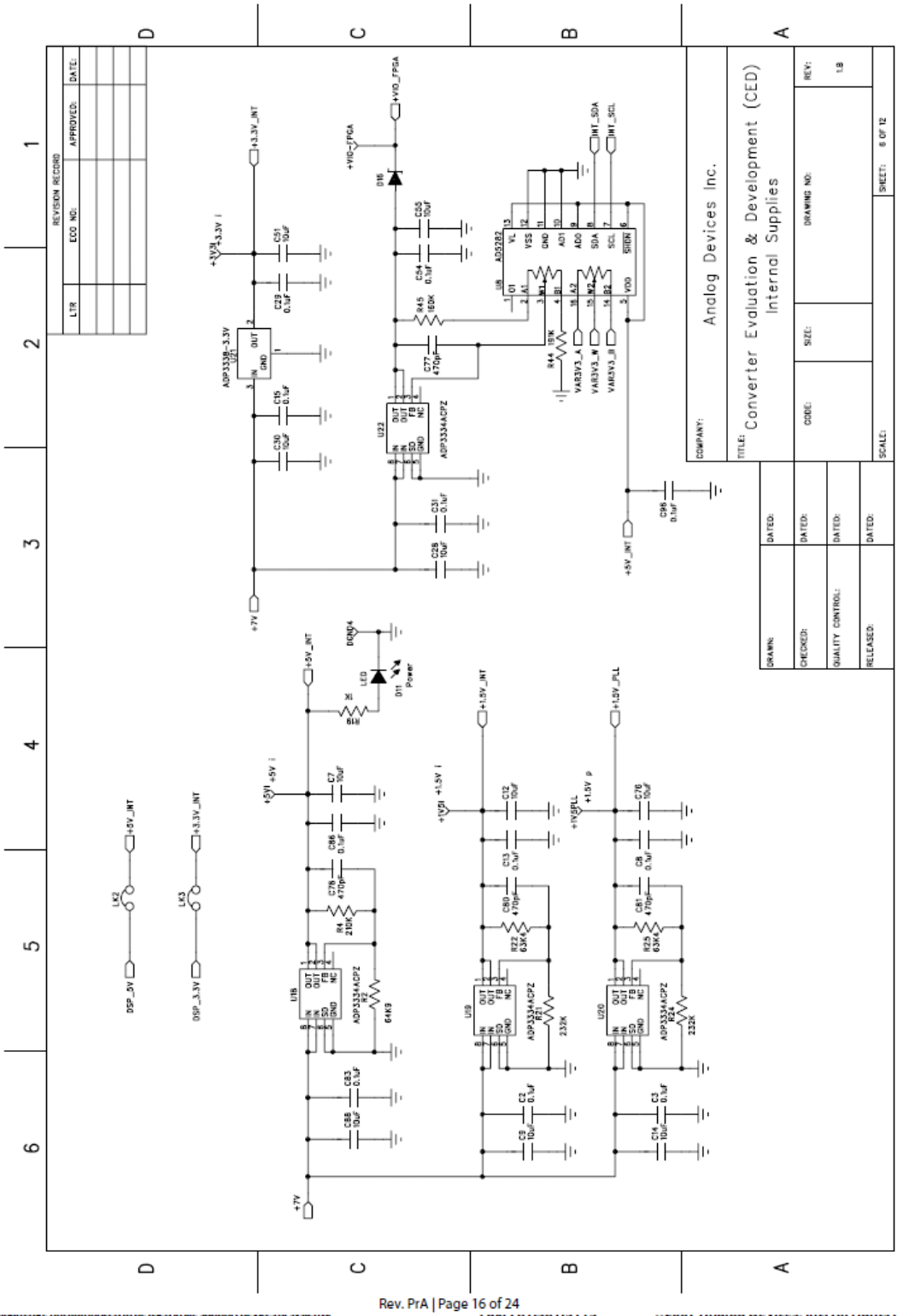
LTR
ECO NO:
APPROVED:
DATE:
COMPANY:
Analog Devices Inc.
TITLE:
Converter Evaluation & Development (CED)
Memory (SRAM & SDRAM)
CODE:
SIZE:
DRAWING NO:
REV:
1.B
SHEET:
4 OF 12
SCALE:
DRAWN:
CHECKED:
QUALITY CONTROL:
RELEASED:
DATED:
SDRAM: 16Mx16 -> 32MBytes
SRAM: 2x 2Mx8 -> 2Mx16 -> 4MBytes
SDRAM_D[0:15]
SDRAM_A[0:12]
SRAM_D[0:15]
SRAM_A[0:20]
WT48LC16M16A2
CY7C1069AV33
+3.3V_INT
DGND


Analog Devices Inc.
Converter Evaluation & Development (CED)
I2C / Voltage Monitoring / Supply Control
Internal I2C Controller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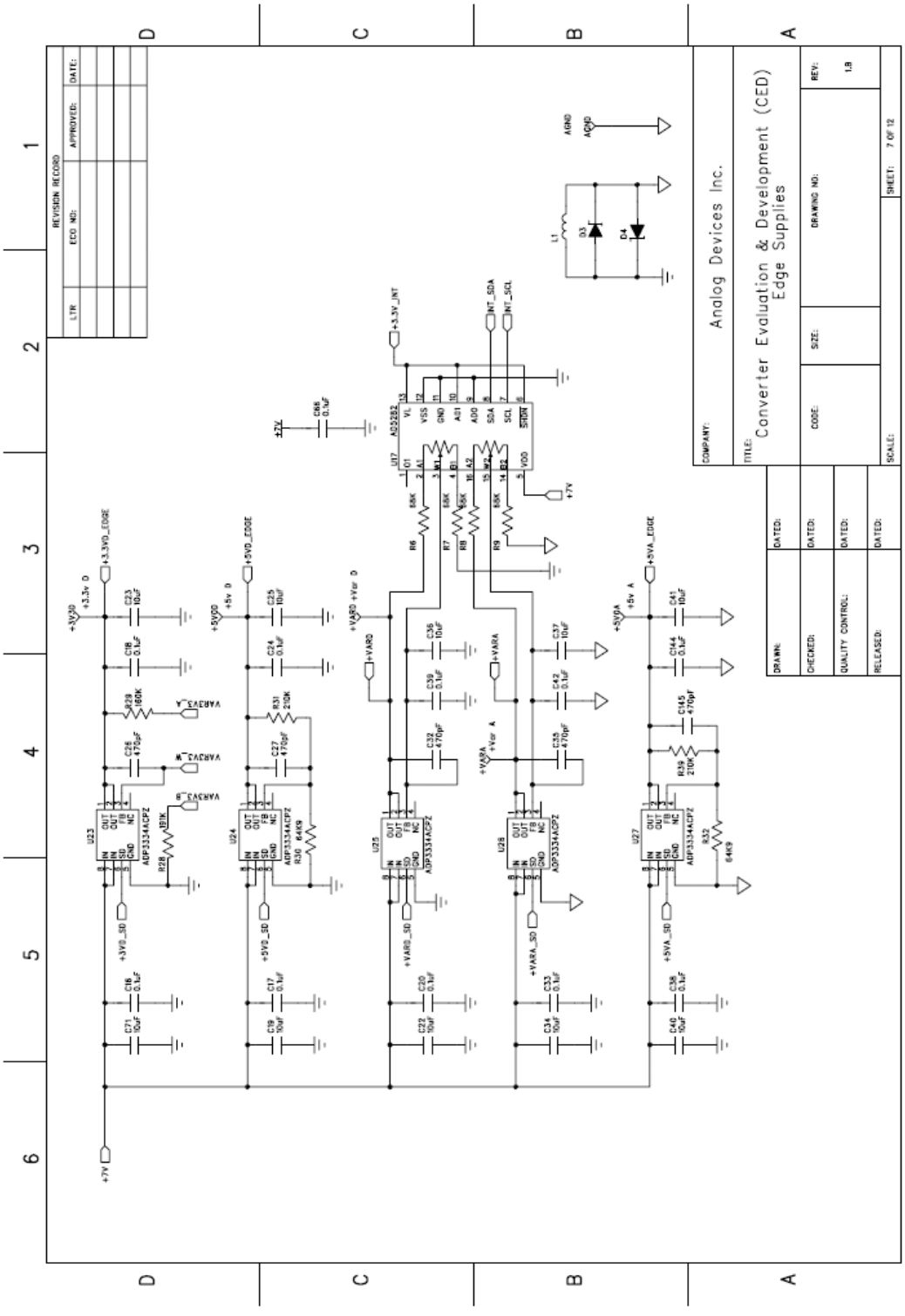
Internal Supplies
COMPANY:
TITLE:
DRAWING NO:
REV:
1.B
SIZE:
CODE:
SCALE:
SHEET: 6 OF 12
DRAWN:
CHECKED:
QUALITY CONTROL:
RELEASED:
DATED:
REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
+3.3V_INT
+VIO_FPGA
+5V_INT
+1.5V_INT
+1.5V_PLL
+7V
INT_SDA
INT_SCL
VAR3V3_A
VAR3V3_W
VAR3V3_B
DSP_5V
DSP_3.3V
ADP3338-3.3V
ADP3334ACP2
AD5282
LED
Power


Analog Devices Inc.
Converter Evaluation & Development (CED) Edge Supplies
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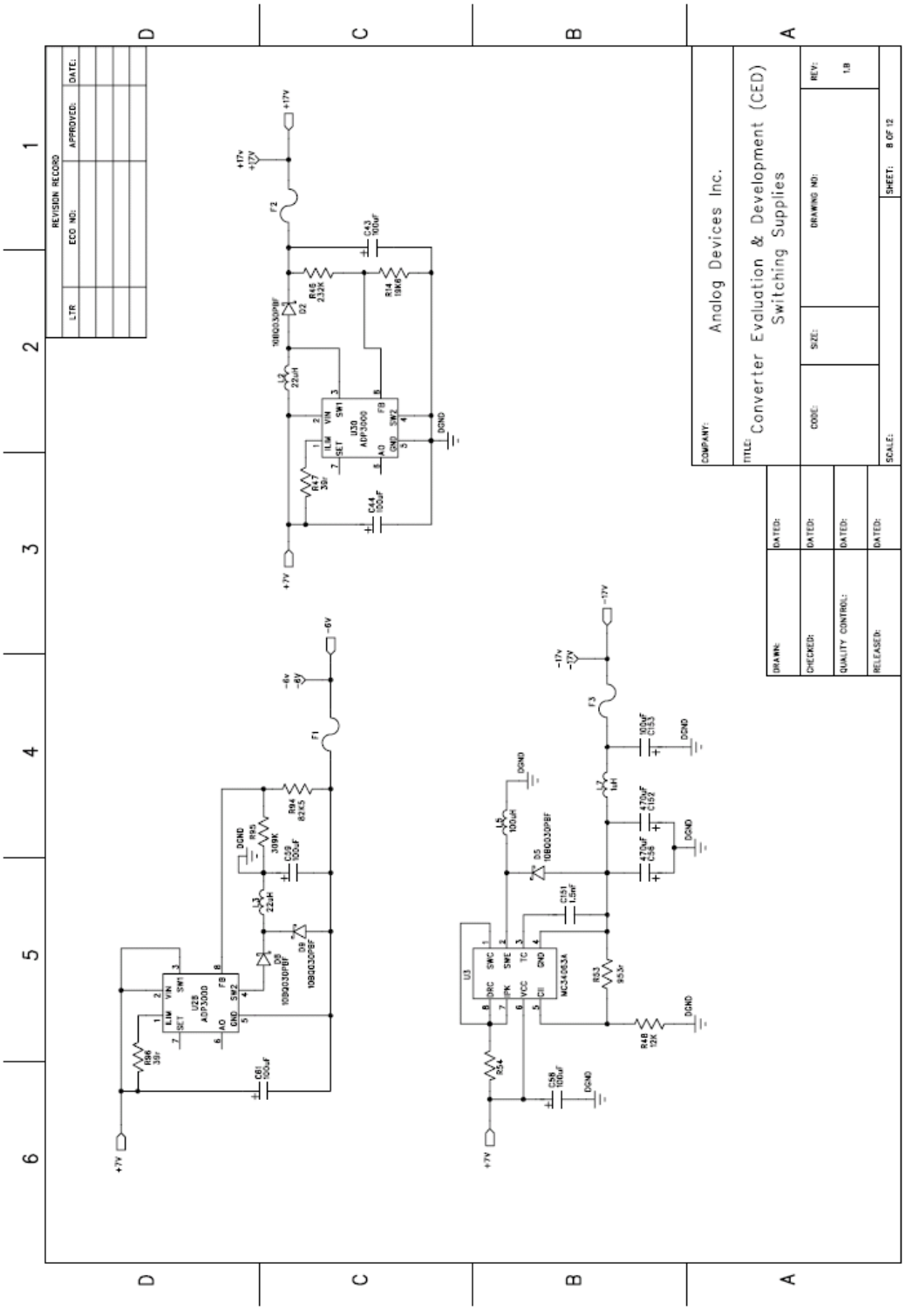
APPROVED:
DATE:
DRAWN:
CHECKED:
QUALITY CONTROL:
RELEASED:
COMPANY:
TITLE:
SIZE:
CODE:
DRAWING NO:
REV:
SCALE:
SHEET: 7 OF 12
AGND
+3.3V_INT
INT_SDA
INT_SCL
+7V
+3V0
+5V0
+VAR0
+VARA
+5VA
ADP3334ACPZ
ADP5052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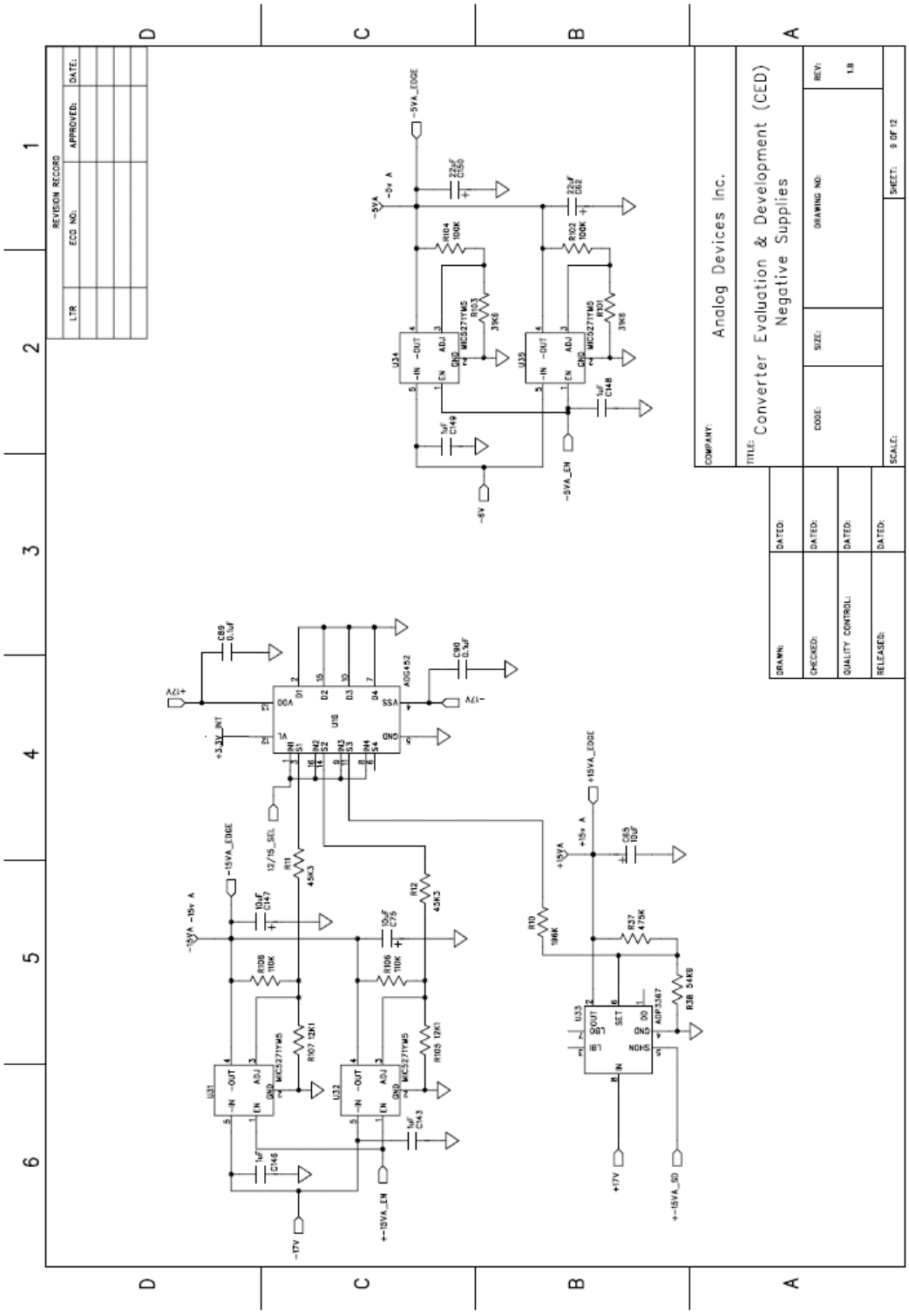
APPROVED:
DATE:
COMPANY: Analog Devices Inc.
TITLE: Converter Evaluation & Development (CED) Switching Supplies
CODE:
SIZE:
DRAWING NO:
REV: 1.0
SHEET: 8 OF 12
DRAWN:
CHECKED:
QUALITY CONTROL:
RELEASED:
DATED:
+17V
-17V
+7V
-6V
DGND
U30 ADP3000
U28 ADP3000
U3 MC34063A
D2 10BQ030PBF
D8 10BQ030PBF
D5 10BQ030PBF
F1
F2
F3
L2 1uH
L3 22uH
L4 22uH
L5 100uH
R46 232K
R14 19K6
R47 39r
R44 82K5
R95 309K
R96 39r
R53 953r
R48 12K
R54 824
C43 100uF
C44 100uF
C28 100uF
C61 100uF
C153 10uF
C152 470uF
C98 470uF
C151 1.5nF
C58 100uF


REVISION RECORD
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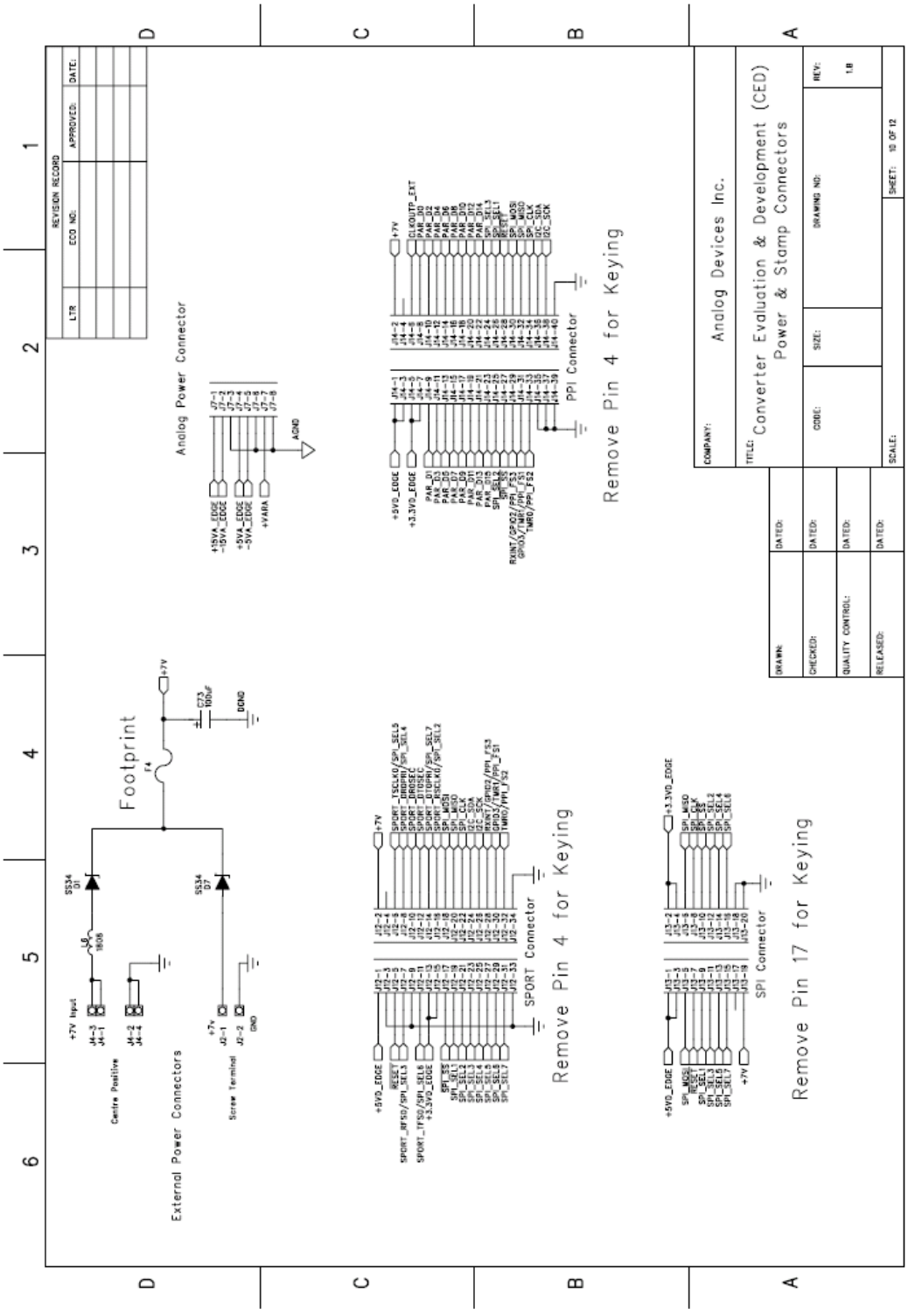
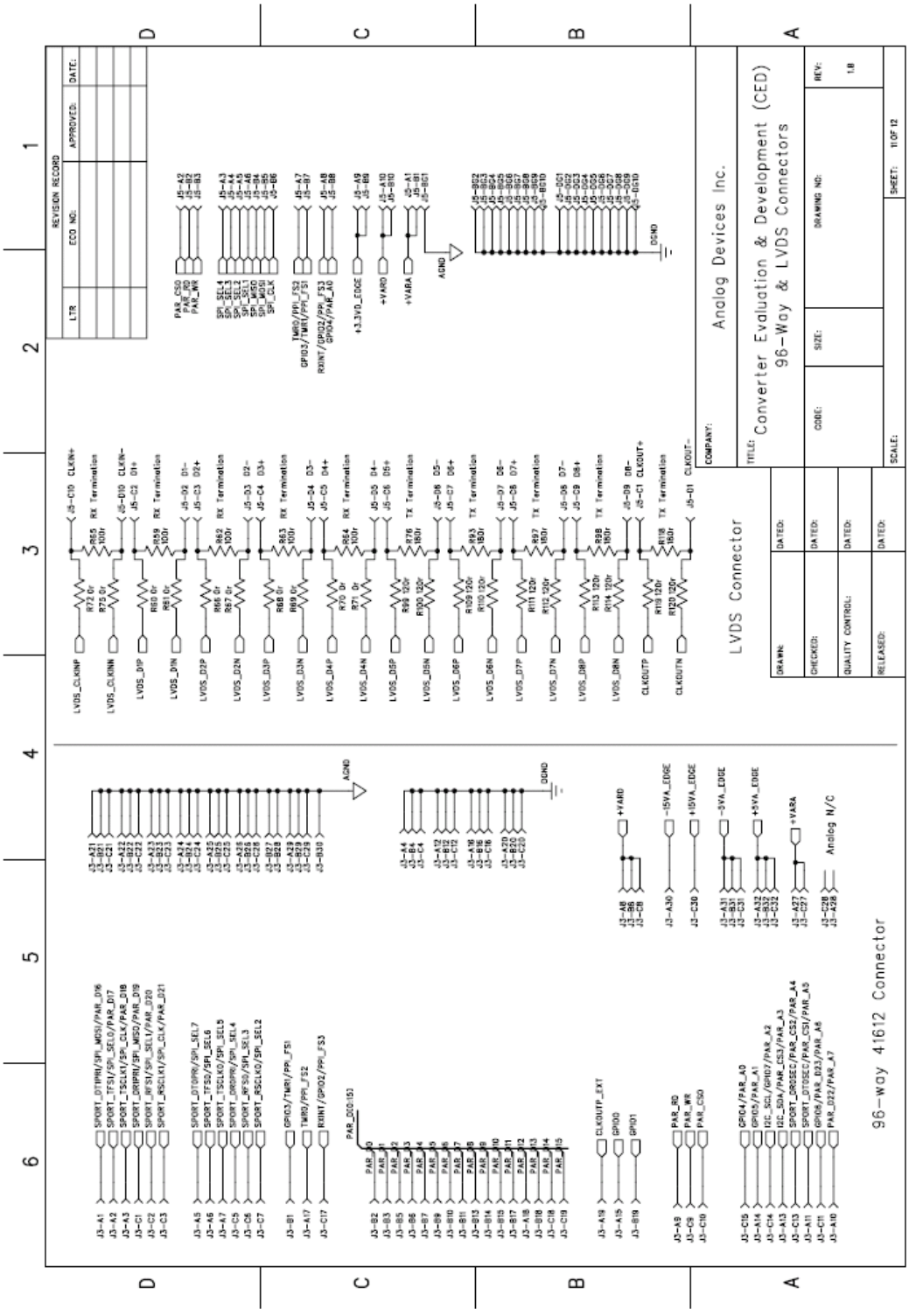
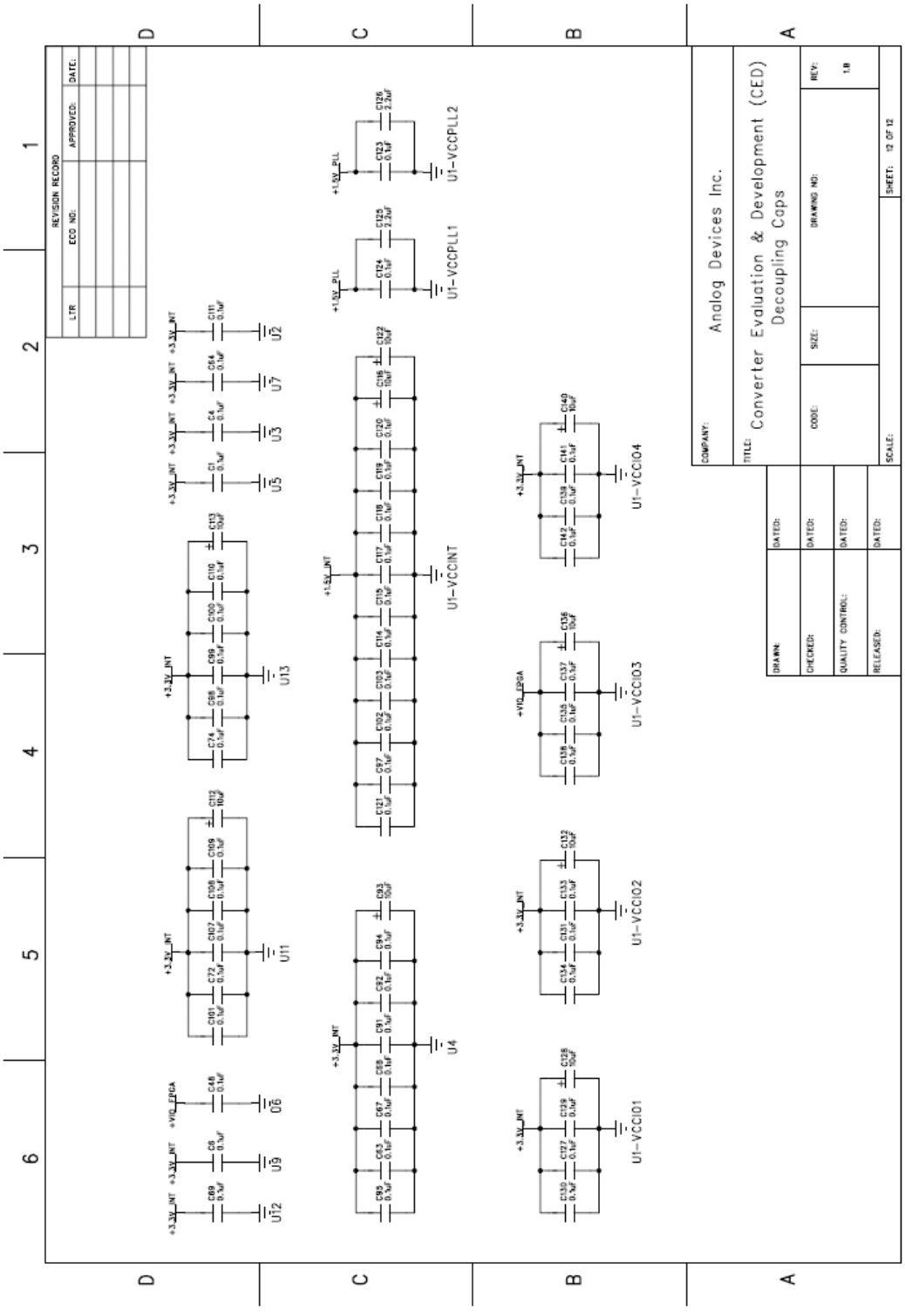
APPROVED:
DATE:
COMPANY: Analog Devices Inc.
TITLE: Converter Evaluation & Development (CED) Negative Supplies
CODE:
SIZE:
DRAWING NO:
REV: 1.0
SHEET: 9 OF 12
SCALE:
DRAWN:
CHECKED:
QUALITY CONTROL:
RELEASED:
DATED:
-5VA_EDGE
-5V
-5VA_EN
+15VA_EDGE
+15V
+17V
+-15VA_SD
-15VA_EDGE
-15V
-17V
+-15VA_EN
12/15_SEL
+3.3V_INT
+12V
-12V


Analog Power Connector
PPI Connector
Remove Pin 4 for Keying
SPORT Connector
Remove Pin 4 for Keying
SPI Connector
Remove Pin 17 for Keying
Footprint
External Power Connectors
Centre Positive
Screen Terminal
Analog Devices Inc.
Converter Evaluation & Development (CED)
Power & Stamp Connectors


REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
LVDS Connector
96-way 41612 Connector
Analog Devices Inc.
Converter Evaluation & Development (CED)
96-Way & LVDS Connectors
COMPANY:
TITLE:
DRAWN:
CHECKED:
QUALITY CONTROL:
RELEASED:
DATED:
CODE:
SIZE:
DRAWING NO:
REV:
SCALE:
SHEET: 11 OF 12
LVDS_CLKNP
LVDS_CLKNN
LVDS_D1P
LVDS_D1N
LVDS_D2P
LVDS_D2N
LVDS_D3P
LVDS_D3N
LVDS_D4P
LVDS_D4N
LVDS_D5P
LVDS_D5N
LVDS_D6P
LVDS_D6N
LVDS_D7P
LVDS_D7N
LVDS_D8P
LVDS_D8N
CLKOUTP
CLKOUTN
RX Termination
TX Termination
AGND
DGND
+VARD
+VARA
Analog N/C


REVISION RECORD
LTR
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APPROVED:
DATE:
Analog Devices Inc.
COMPANY:
TITLE:
Converter Evaluation & Development (CED)
Decoupling Caps
CODE:
SIZE:
DRAWING NO:
REV:
1.0
SHEET: 12 OF 12
SCALE:
DRAWN:
CHECKED:
QUALITY CONTROL:
RELEASED:
DATED:
U1-VCCPLL1
U1-VCCPLL2
U1-VCCINT
U1-VCCIO1
U1-VCCIO2
U1-VCCIO3
U1-VCCIO4

Ordering Information

ORDERING GUIDE

Model	Description
EVAL-CED1Z[1]	Converter Evaluation and Development Board

[1] Z = RoHS Compliant Part.

ESD CAUTION

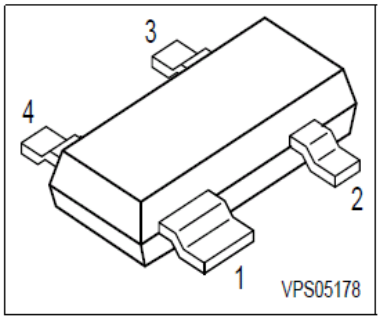
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

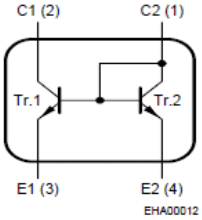
PR07072-0-9/07(PrA)

9.4.4. BCV61 NPN Current Mirror

NPN Silicon Double Transistor

- To be used as a current mirror
- Good thermal coupling and V_{BE} matching
- High current gain
- Low collector-emitter saturation voltage





Type	Marking	Pin Configuration				Package
BCV61A	1Js	1 = C2	2 = C1	3 = E1	4 = E2	SOT143
BCV61B	1Ks	1 = C2	2 = C1	3 = E1	4 = E2	SOT143
BCV61C	1Ls	1 = C2	2 = C1	3 = E1	4 = E2	SOT143

Maximum Ratings

Parameter	Symbol	Value	Unit
Collector-emitter voltage (transistor T1)	V_{CEO}	30	V
Collector-base voltage (open emitter) (transistor T1)	V_{CBO}	30	
Emitter-base voltage	V_{EBS}	6	
DC collector current	I_C	100	mA
Peak collector current	I_{CM}	200	
Base peak current (transistor T1)	I_{BM}	200	
Total power dissipation, T_S = 99 °C	P_{tot}	300	mW
Junction temperature	T_j	150	°C
Storage temperature	T_{stg}	-65 ... 150	

Thermal Resistance

Junction - soldering point[1)]	R_{thJS}	≤170	K/W

[1)] For calculation of R_{thJA} please refer to Application Note Thermal Resistance

Electrical Characteristics at T_A = 25°C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC Characteristics of T1					
Collector-emitter breakdown voltage I_C = 10 mA, I_B = 0	$V_{(BR)CEO}$	30	-	-	V
Collector-base breakdown voltage I_C = 10 µA, I_B = 0	$V_{(BR)CBO}$	30	-	-	
Emitter-base breakdown voltage I_E = 10 µA, I_C = 0	$V_{(BR)EBO}$	6	-	-	
Collector cutoff current V_{CB} = 30 V, I_E = 0	I_{CBO}	-	-	15	nA
Collector cutoff current V_{CB} = 30 V, I_E = 0 , T_A = 150 °C	I_{CBO}	-	-	5	µA
DC current gain 1) I_C = 0.1 mA, V_{CE} = 5 V	h_{FE}	100	-	-	-
DC current gain 1) I_C = 2 mA, V_{CE} = 5 V BCV61A BCV61B BCV61C	h_{FE}	 110 200 420	 180 290 520	 220 450 800	
Collector-emitter saturation voltage1) I_C = 10 mA, I_B = 0.5 mA I_C = 100 mA, I_B = 5 mA	V_{CEsat}	 - -	 90 200	 250 600	mV
Base-emitter saturation voltage 1) I_C = 10 mA, I_B = 0.5 mA I_C = 100 mA, I_B = 5 mA	V_{BEsat}	 - -	 700 900	 - -	
Base-emitter voltage 1) I_C = 2 mA, V_{CE} = 5 V I_C = 10 mA, V_{CE} = 5 V	$V_{BE(ON)}$	 580 -	 660 -	 700 770	

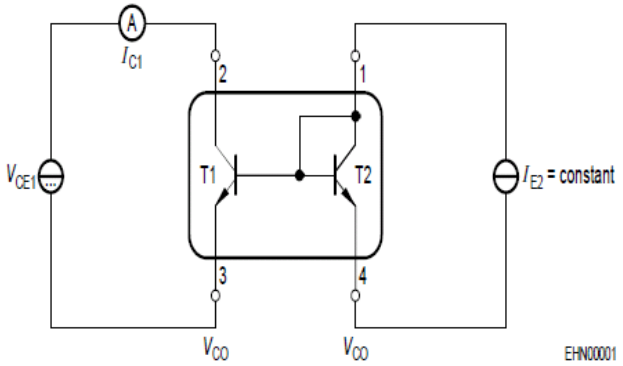
1) Pulse test: t ≤ 300µs, D = 2%

Electrical Characteristics at T_A = 25°C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Characteristics					
Base-emitter forward voltage	V_{BES}				V
I_E = 10 µA		0.4	-	-	
I_E = 250 mA		-	-	1.8	
Matching of transistor T1 and transistor T2	I_{C1} / I_{C2}				-
at I_{E2} = 0.5mA and V_{CE1} = 5V		-	-	-	
T_A = 25 °C		0.7	-	1.3	
T_A = 150 °C		0.7	-	1.3	
Thermal coupling of transistor T1 and transistor T2 [1] T1: V_{CE} = 5V	I_{E2}	-	5	-	mA
Maximum current of thermal stability of I_{C1}					
AC characteristics for transistor T1					
Transition frequency	f_T	-	250	-	MHz
I_C = 10 mA, V_{CE} = 5 V, f = 100 MHz					
Collector-base capacitance	C_{cb}	-	3	-	pF
V_{CB} = 10 V, f = 1 MHz					
Emitter-base capacitance	C_{eb}	-	8	-	
V_{EB} = 0.5 V, f = 1 MHz					
Noise figure	F	-	2	-	dB
I_C = 200 µA, V_{CE} = 5 V, R_S = 2 kΩ,					
f = 1 kHz, Δ f = 200 Hz					
Short-circuit input impedance	h_{11e}	-	4.5	-	kΩ
I_C = 1 mA, V_{CE} = 10 V, f = 1 kHz					
Open-circuit reverse voltage transf.ratio	h_{12e}	-	2	-	10^{-4}
I_C = 1 mA, V_{CE} = 10 V, f = 1 kHz					
Short-circuit forward current transf.ratio	h_{21e}	100	-	900	-
I_C = 1 mA, V_{CE} = 10 V, f = 1 kHz					
Open-circuit output admittance	h_{22e}	-	30	-	µS
I_C = 1 mA, V_{CE} = 10 V, f = 1 kHz					

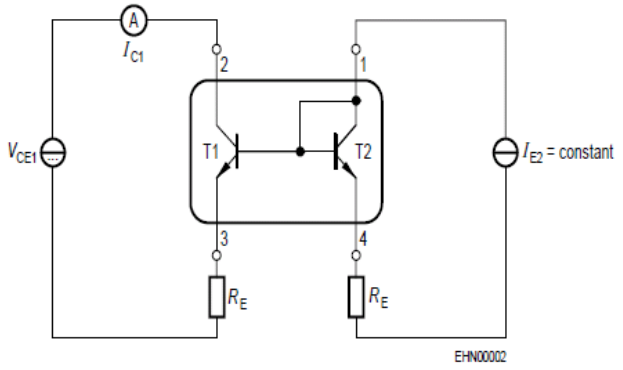
1) Witout emitter resistor. Device mounted on alumina 15mm x 16.5mm x 0.7mm

Test circuit for current matching



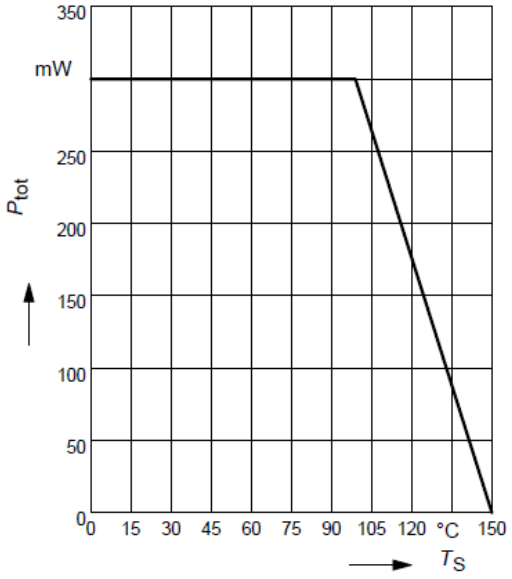
Note: Voltage drop at contacts: V_{CO} < 2/3 V_T = 16mV

Characteristic for determination of V_{CE1} at specified R_E range with I_{E2} as parameter under condition of I_{C1}/I_{E2} = 1.3



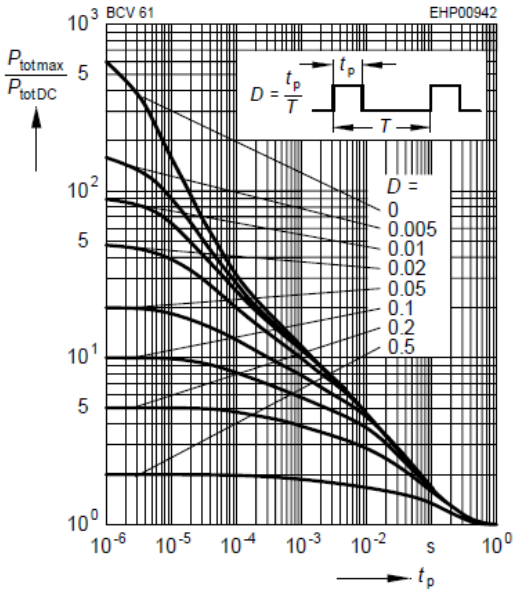
Note: BCV61 with emitter resistors

Total power dissipation $P_{tot} = f(T_S)$



Permissible pulse load

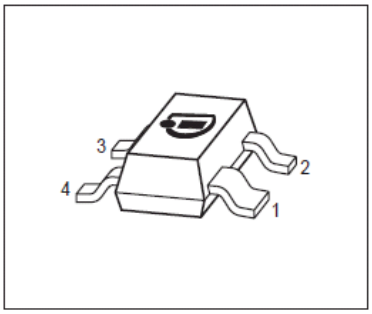
$P_{totmax} / P_{totDC} = f(t_p)$

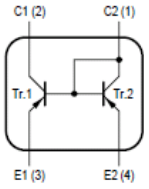


9.4.5. BCV62 PNP Current Mirror

PNP Silicon Double Transistor

- To be used as a current mirror
- Good thermal coupling and V_{BE} matching
- High current gain
- Low collector-emitter saturation voltage
- Pb-free (RoHS compliant) package [1)]
- Qualified according AEC Q101





Type	Marking	Pin Configuration				Package
BCV62A	3Js	1 = C2	2 = C1	3 = E1	4 = E2	SOT143
BCV62B	3Ks	1 = C2	2 = C1	3 = E1	4 = E2	SOT143
BCV62C	3Ls	1 = C2	2 = C1	3 = E1	4 = E2	SOT143

Maximum Ratings

Parameter	Symbol	Value	Unit
Collector-emitter voltage (transistor T1)	V_{CEO}	30	V
Collector-base voltage (open emitter) (transistor T1)	V_{CBO}	30	
Emitter-base voltage	V_{EBS}	6	
DC collector current	I_C	100	mA
Peak collector current	I_{CM}	200	
Base peak current (transistor T1)	I_{BM}	200	
Total power dissipation, T_S = 99 °C	P_{tot}	300	mW
Junction temperature	T_j	150	°C
Storage temperature	T_{stg}	-65 ... 150	

Thermal Resistance

Junction - soldering point[2)]	R_{thJS}	≤170	K/W

[1]Pb-containing package may be available upon special request

[2]For calculation of R_{thJA} please refer to Application Note Thermal Resistance

Electrical Characteristics at T_A = 25°C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC Characteristics of T1					
Collector-emitter breakdown voltage I_C = 10 mA, I_B = 0	$V_{(BR)CEO}$	30	-	-	V
Collector-base breakdown voltage I_C = 10 µA, I_E = 0	$V_{(BR)CBO}$	30	-	-	
Emitter-base breakdown voltage I_E = 10 µA, I_C = 0	$V_{(BR)EBO}$	6	-	-	
Collector cutoff current V_{CB} = 30 V, I_E = 0	I_{CBO}	-	-	15	nA
Collector cutoff current V_{CB} = 30 V, I_E = 0 , T_A = 150 °C	I_{CBO}	-	-	5	µA
DC current gain 1) I_C = 0.1 mA, V_{CE} = 5 V	h_{FE}	100	-	-	-
DC current gain 1) I_C = 2 mA, V_{CE} = 5 V BCV62A BCV62B BCV62C	h_{FE}	 125 220 420	 180 290 520	 220 475 800	
Collector-emitter saturation voltage1) I_C = 10 mA, I_B = 0.5 mA I_C = 100 mA, I_B = 5 mA	V_{CEsat}	 - -	 75 250	 300 650	mV
Base-emitter saturation voltage 1) I_C = 10 mA, I_B = 0.5 mA I_C = 100 mA, I_B = 5 mA	V_{BEsat}	 - -	 700 850	 - -	
Base-emitter voltage 1) I_C = 2 mA, V_{CE} = 5 V I_C = 10 mA, V_{CE} = 5 V	$V_{BE(ON)}$	 600 -	 650 -	 750 820	

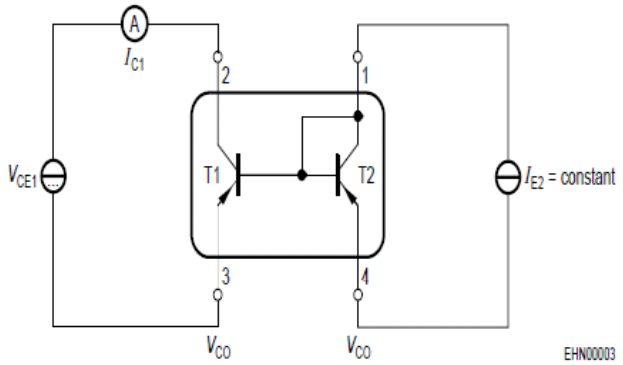
1) Pulse test: t ≤ 300µs, D = 2%

Electrical Characteristics at T_A = 25°C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC Characteristics					
Base-emitter forward voltage	V_{BES}				V
I_E = 10 µA		0.4	-	-	
I_E = 250 mA		-	-	1.8	
Matching of transistor T1 and transistor T2	I_{C1} / I_{C2}				-
at I_{E2} = 0.5mA and V_{CE1} = 5V		-	-	-	
T_A = 25 °C		0.7	-	1.3	
T_A = 150 °C		0.7	-	1.3	
Thermal coupling of transistor T1 and transistor T2 [1] T1: V_{CE} = 5V Maximum current of thermal stability of I_{C1}	I_{E2}	-	5	-	mA
AC characteristics of transistor T1					
Transition frequency	f_T	-	250	-	MHz
I_C = 10 mA, V_{CE} = 5 V, f = 100 MHz					
Collector-base capacitance	C_{cb}	-	1.5	-	pF
V_{CB} = 10 V, f = 1 MHz					
Emitter-base capacitance	C_{eb}	-	8	-	
V_{EB} = 0.5 V, f = 1 MHz					
Noise figure	F	-	2	-	dB
I_C = 200 µA, V_{CE} = 5 V, R_S = 2 kΩ, f = 1 kHz, Δ f = 200 Hz					
Short-circuit input impedance	h_{11e}	-	4.5	-	kΩ
I_C = 1 mA, V_{CE} = 10 V, f = 1 kHz					
Open-circuit reverse voltage transf.ratio	h_{12e}	-	2	-	10^{-4}
I_C = 1 mA, V_{CE} = 10 V, f = 1 kHz					
Short-circuit forward current transf.ratio	h_{21e}	100	-	900	-
I_C = 1 mA, V_{CE} = 10 V, f = 1 kHz					
Open-circuit output admittance	h_{22e}	-	30	-	µS
I_C = 1 mA, V_{CE} = 10 V, f = 1 kHz					

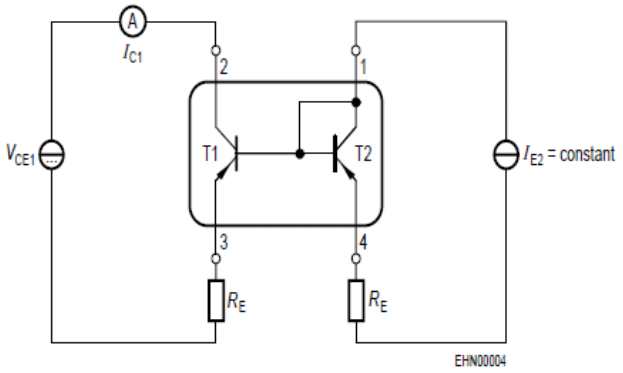
1) Witout emitter resistor. Device mounted on alumina 15mm x 16.5mm x 0.7mm

Test circuit for current matching



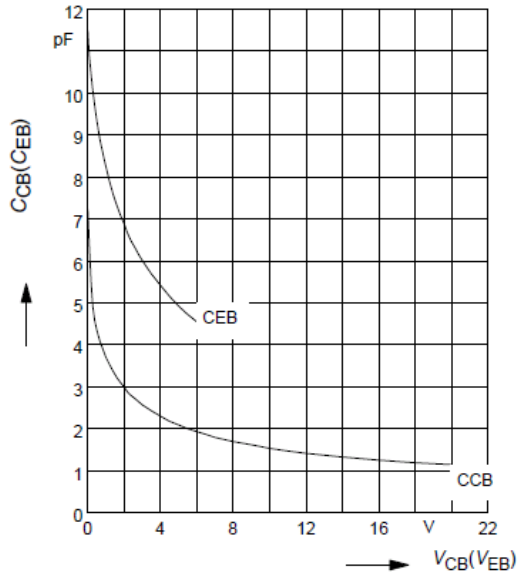
Note: Voltage drop at contacts: V_{CO} < 2/3 V_T = 16mV

Characteristic for determination of V_{CE1} at specified R_E range with I_{E2} as parameter under condition of I_{C1}/I_{E2} = 1.3

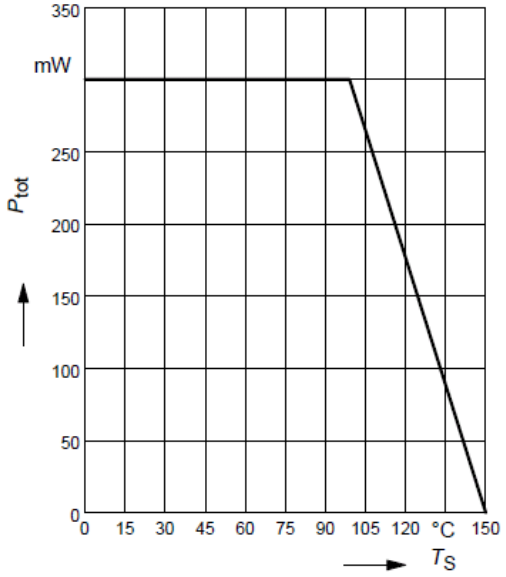


Note: BCV62 with emitter resistors

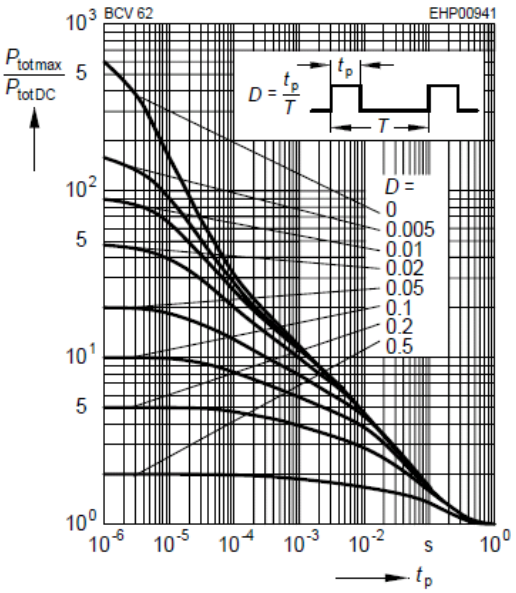
Collector-base capacitance $C_{cb} = f(V_{CB})$
Emitter-base capacitance $C_{eb} = f(V_{EB})$



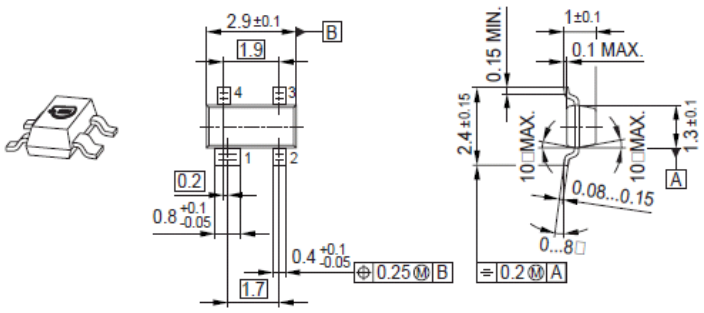
Total power dissipation $P_{tot} = f(T_S)$



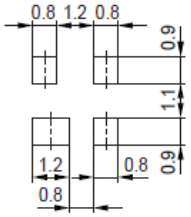
Permissible pulse load
$P_{totmax} / P_{totDC} = f(t_p)$



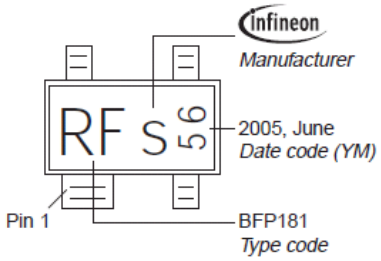
Package Outline



Foot Print

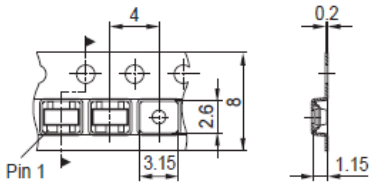


Marking Layout (Example)



Standard Packing

Reel ø180 mm = 3.000 Pieces/Reel
Reel ø330 mm = 10.000 Pieces/Reel



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9.4.6. AD8210 Current Shunt Monitor Datasheet

ANALOG DEVICES

High Voltage, Bidirectional Current Shunt Monitor

AD8210

FEATURES

±4000 V HBM ESD
High common-mode voltage range
  −2 V to +65 V operating
  −5 V to +68 V survival
Buffered output voltage
5 mA output drive capability
Wide operating temperature range: −40°C to +125°C
Ratiometric half-scale output offset
Excellent ac and dc performance
  3 µV/°C typical offset drift
  10 ppm/°C typical gain drift
  120 db typical CMRR at dc
  80 db typical CMRR at 100 kHz
Available in 8-lead SOIC

APPLICATIONS

Current sensing
  Motor controls
  Transmission controls
  Diesel injection controls
  Engine management
  Suspension controls
  Vehicle dynamic controls
  DC-to-DC converters

FUNCTIONAL BLOCK DIAGRAM

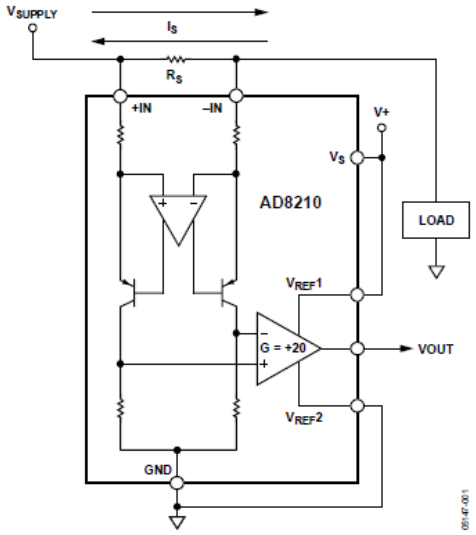

Figure 1.

GENERAL DESCRIPTION

The AD8210 is a single-supply difference amplifier ideal for amplifying small differential voltages in the presence of large common-mode voltages. The operating input common-mode voltage range extends from −2 V to +65 V. The typical supply voltage is 5 V.

The AD8210 is offered in a SOIC package. The operating temperature range is −40°C to +125°C.

Excellent ac and dc performance over temperature keep errors in the measurement loop to a minimum. Offset drift and gain drift are guaranteed to a maximum of 8 µV/°C and 20 ppm/°C, respectively.

The output offset can be adjusted from 0.05 V to 4.9 V with a 5 V supply by using $V_{REF}1$ pin and $V_{REF}2$ pin. With the $V_{REF}1$ pin attached to the V+ pin, and the $V_{REF}2$ pin attached to the GND pin, the output is set at half scale. Attaching both $V_{REF}1$ and $V_{REF}2$ to GND causes the output to be unipolar, starting near ground. Attaching both $V_{REF}1$ and $V_{REF}2$ to V+ causes the output to be unipolar, starting near V+. Other offsets can be obtained by applying an external voltage to $V_{REF}1$ and $V_{REF}2$.

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REVISION HISTORY

4/06—Revision 0: Initial Version

SPECIFICATIONS

T_A = operating temperature range, V_S = 5 V, unless otherwise noted.

Table 1.

Parameter	AD8210 SOIC[1] Min	Typ	Max	Unit	Conditions
GAIN					
Initial		20		V/V	
Accuracy			±0.5	%	25°C, $V_O \geq 0.1$ V dc
Accuracy Over Temperature			±0.7	%	T_A
Gain Drift			20	ppm/°C	
VOLTAGE OFFSET					
Offset Voltage (RTI)			±1.0	mV	25°C
Over Temperature (RTI)			±1.8	mV	T_A
Offset Drift			±8.0	µV/°C	
INPUT					
Input Impedance					
Differential		2		kΩ	
Common Mode		5		MΩ	V common mode > 5 V
Common Mode		3.5		kΩ	V common mode < 5 V
Common-Mode Input Voltage Range	−2		+65	V	Common mode, continuous
Differential Input Voltage Range		250		mV	Differential[2]
Common-Mode Rejection	100	120		dB	T_A, f = dc, V_{CM} > 5 V
	80	95		dB	T_A, f = dc to 100 kHz[3], V_{CM} < 5 V
		80		dB	T_A, f = 100 kHz[3], V_{CM} > 5 V
	80			dB	T_A, f = 40 kHz[3], V_{CM} > 5 V
OUTPUT					
Output Voltage Range	0.05		4.9	V	R_L = 25 kΩ
Output Impedance		2		Ω	
DYNAMIC RESPONSE					
Small Signal −3 dB Bandwidth		450		kHz	
Slew Rate		3		V/µs	
NOISE					
0.1 Hz to 10 Hz, RTI		7		µV p-p	
Spectral Density, 1 kHz, RTI		70		nV/√Hz	
OFFSET ADJUSTMENT					
Ratiometric Accuracy[4]	0.499		0.501	V/V	Divider to supplies
Accuracy, RTO			±0.6	mV/V	Voltage applied to $V_{REF}1$ and $V_{REF}2$ in parallel
Output Offset Adjustment Range	0.05		4.9	V	V_S = 5 V
V_{REF} Input Voltage Range	0.0		V_S	V	
V_{REF} Divider Resistor Values	24	32	40	kΩ	
POWER SUPPLY					
Operating Range	4.5	5.0	5.5	V	
Quiescent Current Over Temperature			2	mA	V_{CM} > 5 V[5]
Power Supply Rejection Ratio	80			dB	
TEMPERATURE RANGE					
For Specified Performance	−40		+125	°C	

[1] T_{MIN} to T_{MAX} = −40°C to +125°C.
[2] Differential input voltage range = ±125 mV with half-scale output offset.
[3] Source imbalance <2 Ω.
[4] The offset adjustment is ratiometric to the power supply when $V_{REF}1$ and $V_{REF}2$ are used as a divider between the supplies.
[5] When the input common mode is less than 5 V, the supply current increases. This can be calculated with the following formula: $I_S = -0.7 (V_{CM}) + 4.2$ (see Figure 21).

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	12.5 V
Continuous Input Voltage (V_{CM})	−5 V to +68 V
Reverse Supply Voltage	0.3 V
ESD Rating	
HBM (Human Body Model)	±4000 V
CDM (Charged Device Model)	±1000 V
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Output Short-Circuit Duration	Indefinite

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

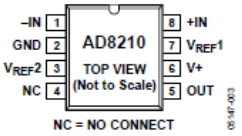


Figure 2. Pin Configuration

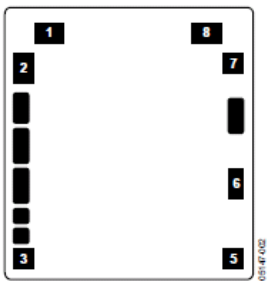


Figure 3. Metallization Diagram

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	X	Y
1	–IN	–443	+584
2	GND	–479	+428
3	$V_{REF}2$	–466	–469
4	NC		
5	OUT	+466	–537
6	V+	+501	–95
7	$V_{REF}1$	+475	+477
8	+IN	+443	+584

TYPICAL PERFORMANCE CHARACTERISTICS

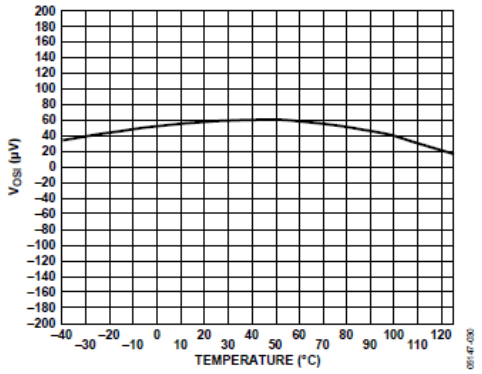


Figure 4. Typical Offset Drift

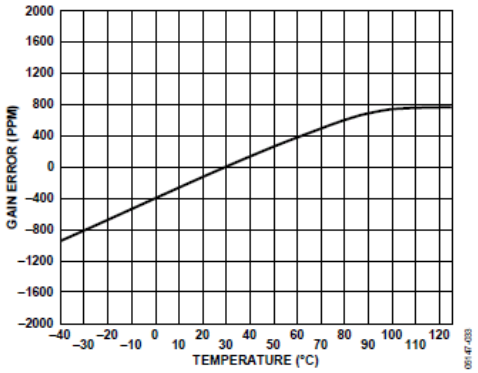


Figure 7. Typical Gain Drift

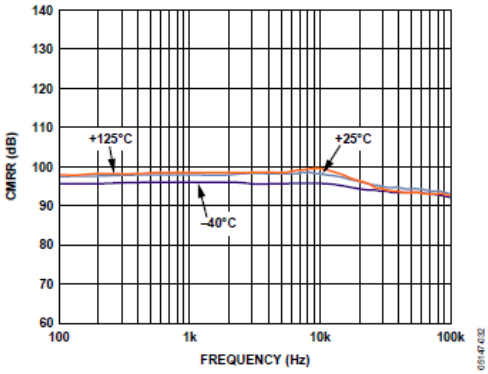


Figure 5. CMRR vs. Frequency and Temperature (Common-Mode Voltage < 5 V)

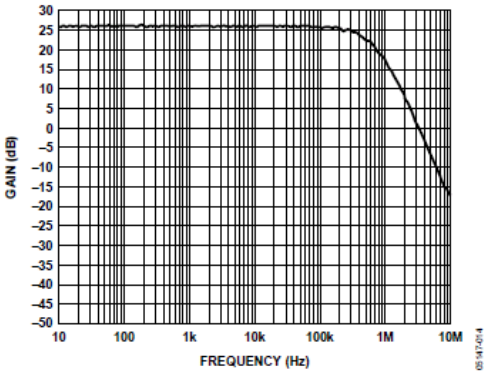


Figure 8. Typical Small Signal Bandwidth (V_{OUT} = 200 mV p-p)

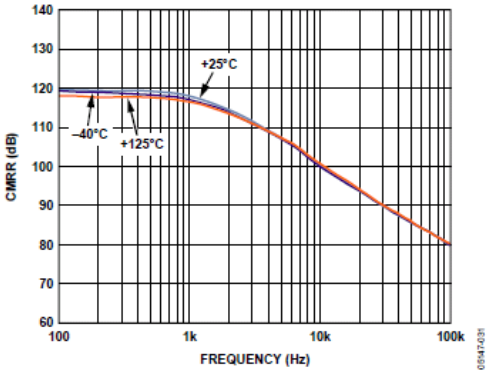


Figure 6. CMRR vs. Frequency and Temperature (Common-Mode Voltage > 5 V)

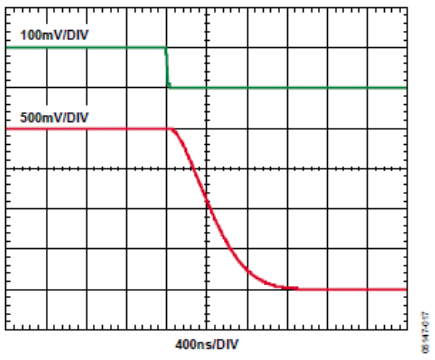


Figure 9. Fall Time

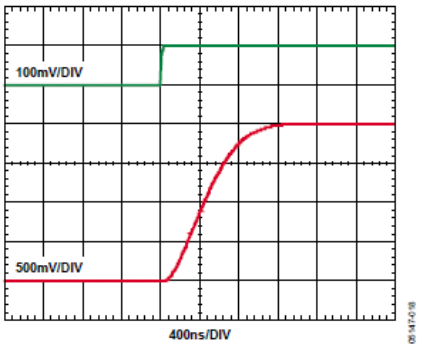


Figure 10. Rise Time

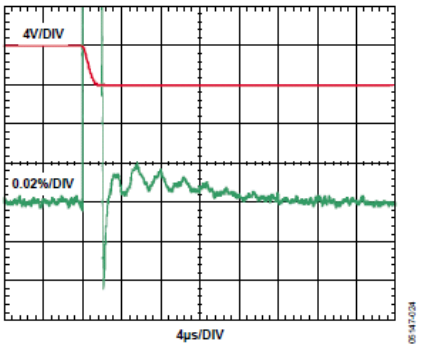


Figure 13. Settling Time (Falling)

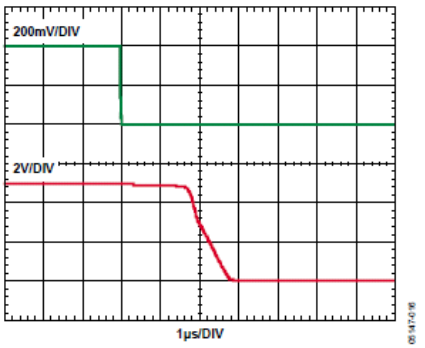


Figure 11. Differential Overload Recovery (Falling)

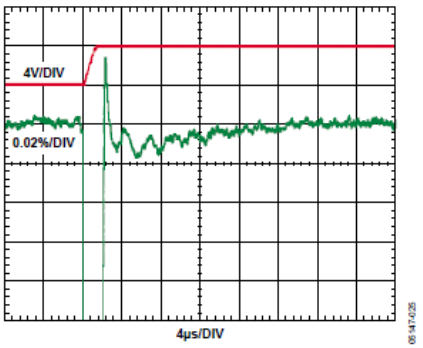


Figure 14. Settling Time (Rising)

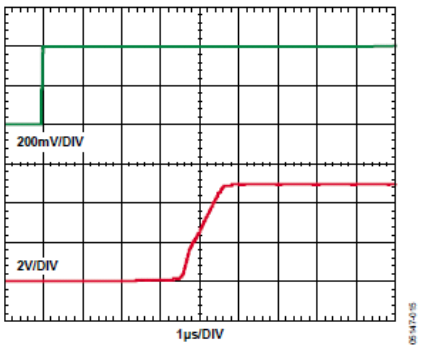


Figure 12. Differential Overload Recovery (Rising)

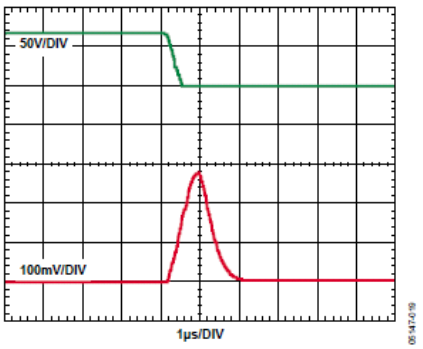


Figure 15. Common-Mode Response (Falling)

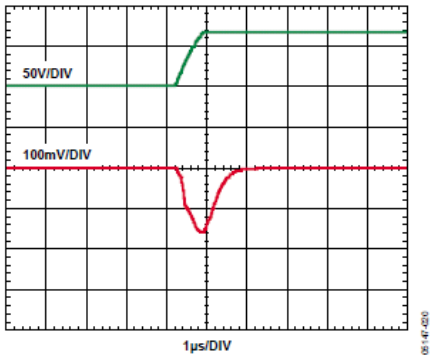


Figure 16. Common-Mode Response (Rising)

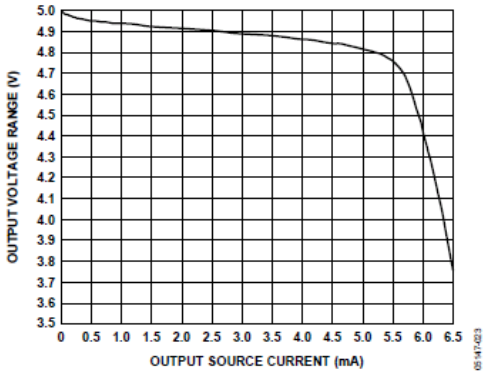


Figure 19. Output Voltage Range vs. Output Source Current

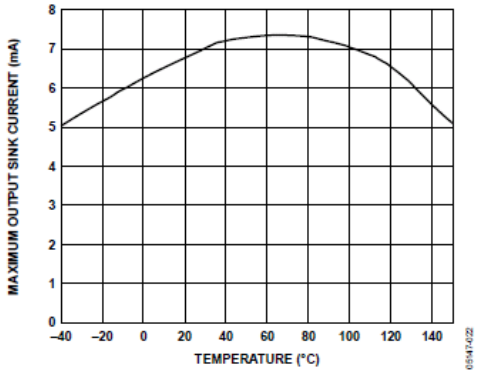


Figure 17. Output Sink Current vs. Temperature

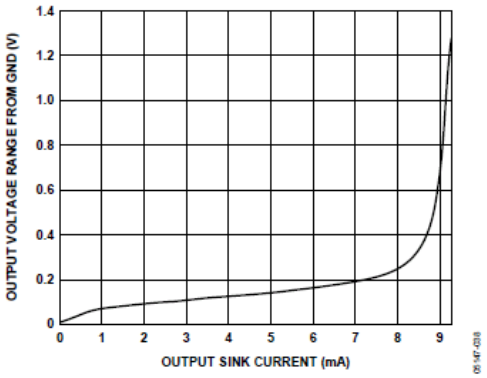


Figure 20.Output Voltage Range from GND vs. Output Sink Current

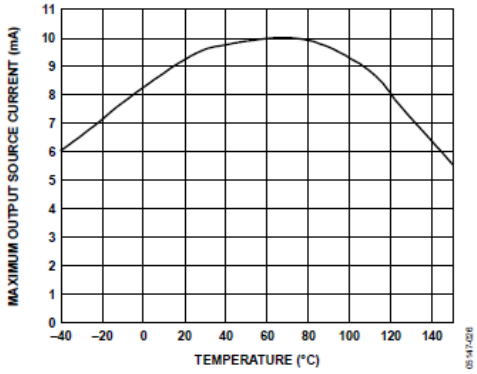


Figure 18. Output Source Current vs. Temperature

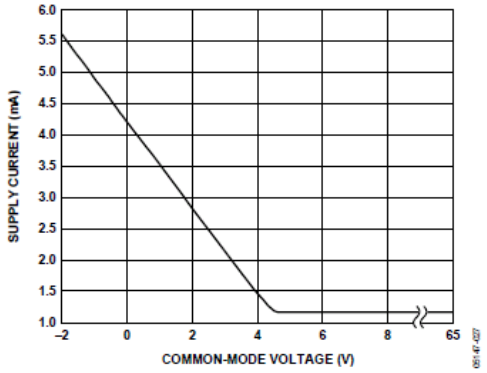


Figure 21. Supply Current vs. Common-Mode Voltage

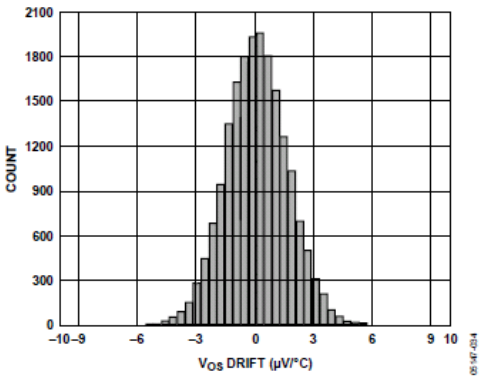


Figure 22. Offset Drift Distribution (µV/°C), SOIC, Temperature Range = −40°C to +125°C

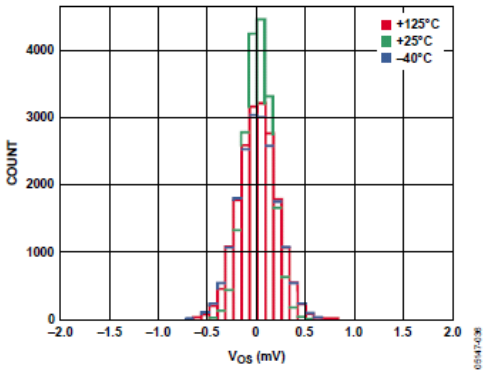


Figure 24. Offset Distribution (µV), SOIC, V_{CM} = 5 V

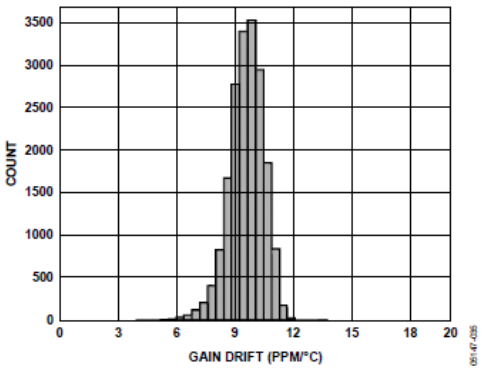


Figure 23. Gain Drift Distribution (PPM/°C), SOIC, Temperature = −40°C to +125°C

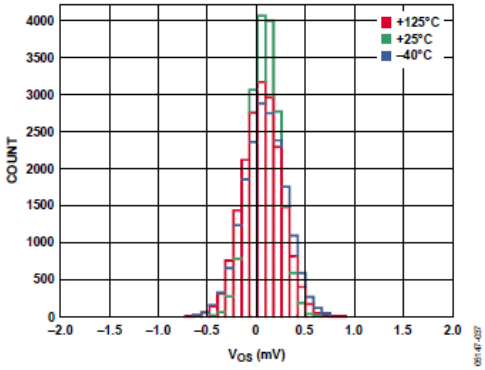


Figure 25. Offset Distribution (µV), SOIC, V_{CM} = 0 V

THEORY OF OPERATION

In typical applications, the AD8210 amplifies a small differential input voltage generated by the load current flowing through a shunt resistor. The AD8210 rejects high common-mode voltages (up to 65 V) and provides a ground referenced buffered output that interfaces with an analog-to-digital converter. Figure 26 shows a simplified schematic of the AD8210.

The AD8210 is comprised of two main blocks, a differential amplifier and an instrumentation amplifier. A load current flowing through the external shunt resistor produces a voltage at the input terminals of the AD8210. The input terminals are connected to the differential amplifier (A1) by Resistor R1 and Resistor R2. A1 nulls the voltage appearing across its own input terminals by adjusting the current through R1 and R2 with Transistor Q1 and Transistor Q2. When the input signal to the AD8210 is 0 V, the currents in R1 and R2 are equal. When the differential signal is nonzero, the current increases through one of the resistors and decreases in the other. The current difference is proportional to the size and polarity of the input signal.

The differential currents through Q1 and Q2 are converted into a differential voltage by R3 and R4. A2 is configured as an instrumentation amplifier. The differential voltage is converted into a single-ended output voltage by A2. The gain is internally set with precision trimmed, thin film resistors to 20 V/V.

The output reference voltage is easily adjusted by the $V_{REF}1$ pin and $V_{REF}2$ pin. In a typical configuration, $V_{REF}1$ is connected to V_{CC} while $V_{REF}2$ is connected to GND. In this case, the output is centered at $V_{CC}/2$ when the input signal is 0 V.

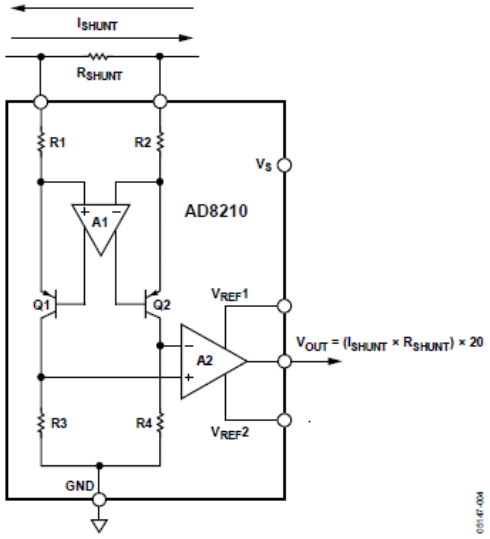


Figure 26. Simplified Schematic

MODES OF OPERATION

The AD8210 can be adjusted for unidirectional or bidirectional operation.

UNIDIRECTIONAL OPERATION

Unidirectional operation allows the AD8210 to measure currents through a resistive shunt in one direction. The basic modes for unidirectional operation are ground referenced output mode and V+ referenced output mode.

In unidirectional operation, the output can be set at the negative rail (near ground) or at the positive rail (near V+) when the differential input is 0 V. The output moves to the opposite rail when a correct polarity differential input voltage is applied. In this case, full scale is approximately 250 mV. The required polarity of the differential input depends on the output voltage setting. If the output is set at ground, then the polarity needs to be positive to move the output up (see Table 5). If the output is set at the positive rail, then the input polarity needs to be negative to move the output down (see Table 6).

Ground Referenced Output

When using the AD8210 in this mode, both reference inputs are tied to ground, which causes the output to sit at the negative rail when the differential input voltage is zero (see Figure 27 and Table 4).

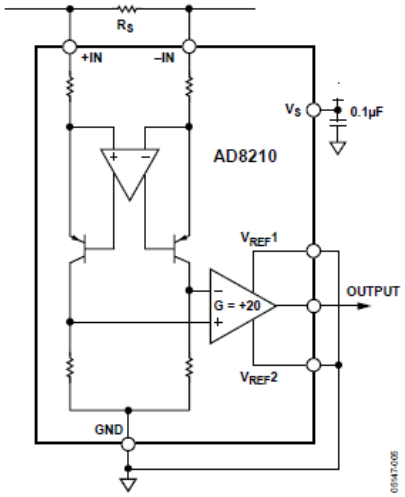


Figure 27. Ground Referenced Output

Table 4. V+ = 5 V

V_{IN} (Referred to –IN)	V_O
0 V	0.05 V
250 mV	4.9 V

V+ Referenced Output

This mode is set when both reference pins are tied to the positive supply. It is typically used when the diagnostic scheme requires detection of the amplifier and wiring before power is applied to the load (see Figure 28 and Table 5).

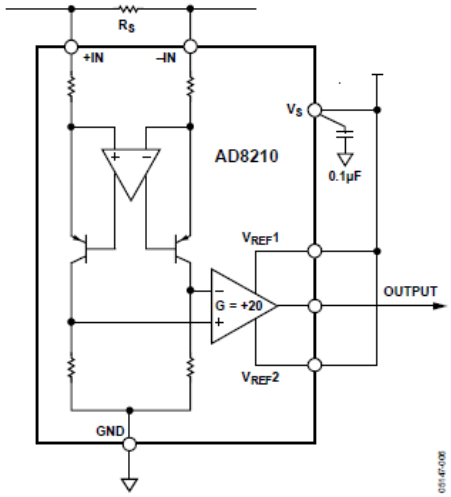


Figure 28. V+ Referenced Output

Table 5. V+ = 5 V

V_{IN} (Referred to –IN)	V_O
0 V	4.9 V
–250 mV	0.05 V

BIDIRECTIONAL OPERATION

Bidirectional operation allows the AD8210 to measure currents through a resistive shunt in two directions. The output offset can be set anywhere within the output range. Typically, it is set at half scale for equal measurement range in both directions. In some cases, however, it is set at a voltage other than half scale when the bidirectional current is nonsymmetrical.

Table 6. V+ = 5 V, V_O = 2.5 V with V_{IN} = 0 V

V_{IN} (Referred to –IN)	V_O
+125 mV	4.9 V
–125 mV	0.05 V

Adjusting the output can also be accomplished by applying voltage(s) to the reference inputs.

External Referenced Output

Tying both V_{REF} pins together to an external reference produces an output offset at the reference voltage when there is no differential input (see Figure 29). When the input is negative relative to the –IN pin, the output moves down from the reference voltage. When the input is positive relative to the –IN pin, the output increases.

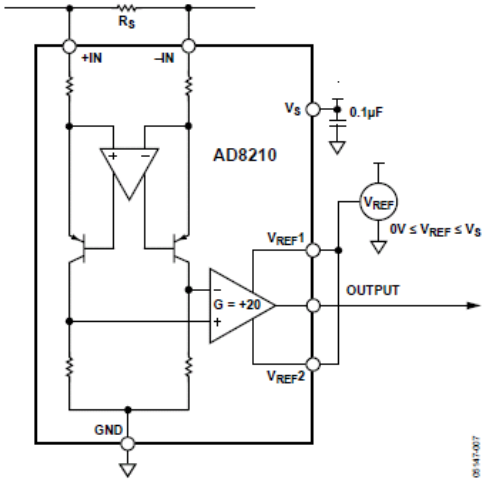


Figure 29. External Reference Output

Splitting an External Reference

In this case, an external reference is divided by two with an accuracy of approximately 0.2% by connecting one V_{REF} pin to ground and the other V_{REF} pin to the reference voltage (see Figure 30).

Note that Pin $V_{REF}1$ and Pin $V_{REF}2$ are tied to internal precision resistors that connect to an internal offset node. There is no operational difference between the pins.

For proper operation, the AD8210 output offset should not be set with a resistor voltage divider. Any additional external resistance could create a gain error. A low impedance voltage source should be used to set the output offset of the AD8210.

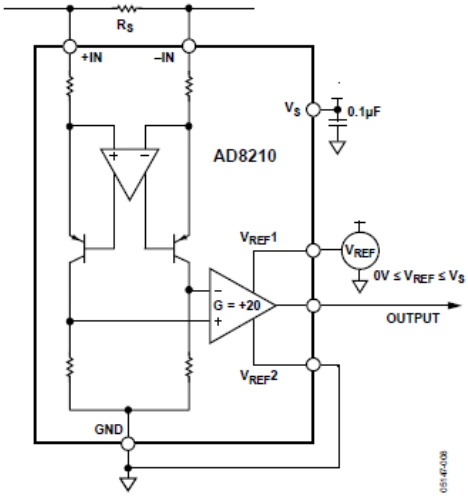


Figure 30. Split External Reference

Splitting the Supply

By tying one reference pin to V+ and the other to the GND pin, the output is set at mid supply when there is no differential input (see Figure 31). This mode is beneficial because no external reference is required to offset the output for bidirectional current measurement. This creates a midscale offset that is ratiometric to the supply, meaning that if the supply increases or decreases, the output still remains at half scale. For example, if the supply is 5.0 V, the output is at half scale or 2.5 V. If the supply increases by 10% (to 5.5 V), the output also increases by 10% (2.75 V).

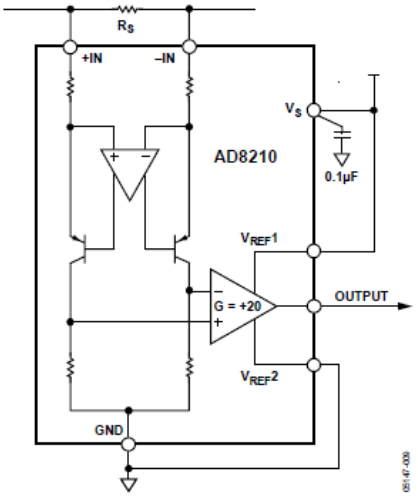


Figure 31. Split Supply

INPUT FILTERING

In typical applications such as motor and solenoid current sensing, filtering at the input of the AD8210 can be beneficial in reducing differential noise, as well as transients and current ripples flowing through the input shunt resistor. An input low-pass filter can be implemented as shown in Figure 32.

The 3 dB frequency for this filter can be calculated using the following formula:

$$f\_3\,\mathrm{dB} = \frac{1}{2\pi \times R_{FILTER} \times C_{FILTER}} \quad (1)$$

Adding outside components such as R_{FILTER} and C_{FILTER} introduces additional errors to the system. To minimize these errors as much as possible, it is recommended that R_{FILTER} be 10 Ω or lower. By adding the R_{FILTER} in series with the 2 kΩ internal input resistors of the AD8210, a gain error is introduced. This can be calculated using the following formula:

$$Gain\ Error(\%) = 100 - \left(100 \times \frac{2\mathrm{k}\Omega}{2\mathrm{k}\Omega - R_{FILTER}}\right) \quad (2)$$

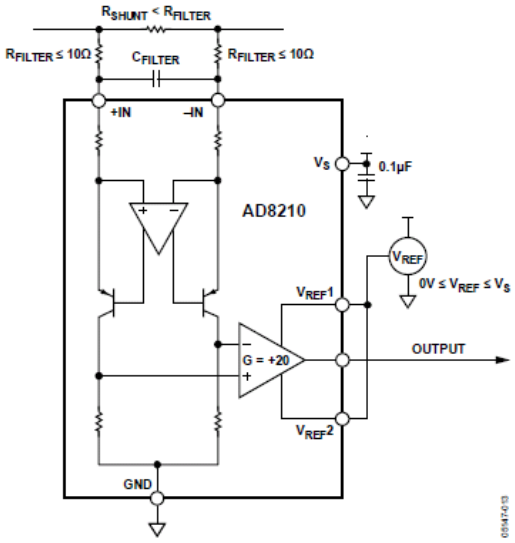


Figure 32. Input Low-Pass Filtering

APPLICATIONS

The AD8210 is ideal for high-side or low-side current sensing. Its accuracy and performance benefits applications such as 3-phase and H-bridge motor control, solenoid control, as well as power supply current monitoring.

For solenoid control, two typical circuit configurations are used: high-side current sense with a low-side switch, and high-side current sense with a high-side switch.

HIGH-SIDE CURRENT SENSE WITH A LOW-SIDE SWITCH

In this case, the PWM control switch is ground referenced. An inductive load (solenoid) is tied to a power supply. A resistive shunt is placed between the switch and the load (see Figure 33). An advantage of placing the shunt on the high side is that the entire current, including the recirculation current, can be measured because the shunt remains in the loop when the switch is off. In addition, diagnostics can be enhanced because short circuits to ground can be detected with the shunt on the high side.

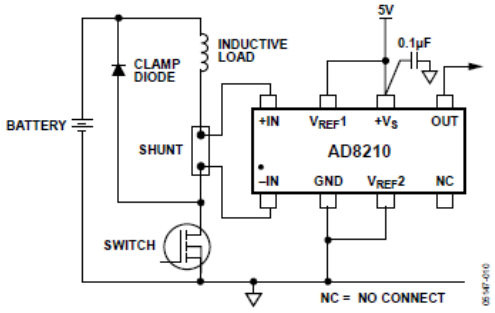


Figure 33. Low-Side Switch

In this circuit configuration, when the switch is closed, the common-mode voltage moves down to the negative rail. When the switch is opened, the voltage reversal across the inductive load causes the common-mode voltage to be held one diode drop above the battery by the clamp diode.

HIGH-SIDE CURRENT SENSE WITH A HIGH-SIDE SWITCH

This configuration minimizes the possibility of unexpected solenoid activation and excessive corrosion (see Figure 34). In this case, both the switch and the shunt are on the high side. When the switch is off, the battery is removed from the load, which prevents damage from potential short circuits to ground, while still allowing the recirculation current to be measured and diagnostics to be preformed. Removing the power supply from the load for the majority of the time minimizes the corrosive effects that could be caused by the differential voltage between the load and ground.

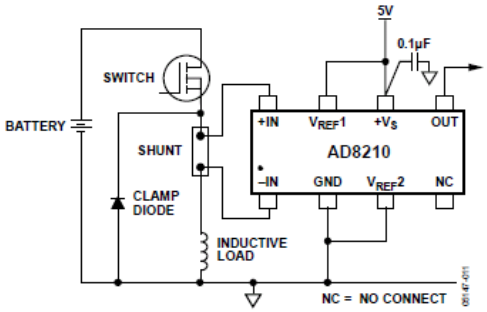


Figure 34. High-Side Switch

Using a high-side switch connects the battery voltage to the load when the switch is closed. This causes the common-mode voltage to increase to the battery voltage. In this case, when the switch is opened, the voltage reversal across the inductive load causes the common-mode voltage to be held one diode drop below ground by the clamp diode.

H-BRIDGE MOTOR CONTROL

Another typical application for the AD8210 is as part of the control loop in H-bridge motor control. In this case, the AD8210 is placed in the middle of the H-bridge (see Figure 35) so that it can accurately measure current in both directions by using the shunt available at the motor. This configuration is beneficial for measuring the recirculation current to further enhance the control loop diagnostics.

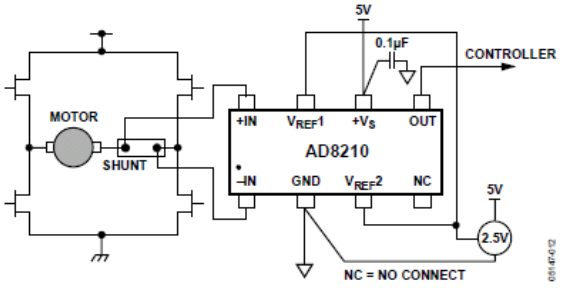
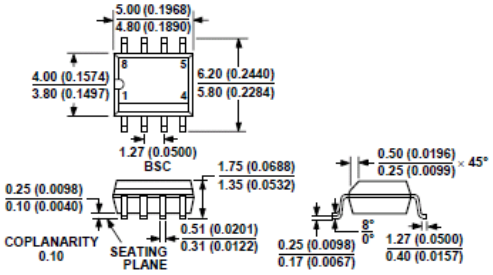


Figure 35. Motor Control Application

The AD8210 measures current in both directions as the H-bridge switches and the motor changes direction. The output of the AD8210 is configured in an external reference bidirectional mode; see the Modes of Operation section.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 36. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8210YRZ[1]	−40°C to +125°C	8-Lead SOIC_N	R-8
AD8210YRZ-REEL[1]	−40°C to +125°C	8-Lead SOIC_N, 13″Tape and Reel	R-8
AD8210YRZ-REEL7[1]	−40°C to +125°C	8-Lead SOIC_N, 7″Tape and Reel	R-8

[1] Z = Pb-free part.

NOTES

9.5. DEMO Software User Manual

The software was written to communicate with the AD7280 evaluation boards as well as the DEMO Board through the CED board and to show off the capabilities of the AD7280. The primary purpose of this software is to display the capability of the AD7280s. For details of how this software is created, refer to Section 6.3 Software Implementation of this report. The software can perform the following functions.

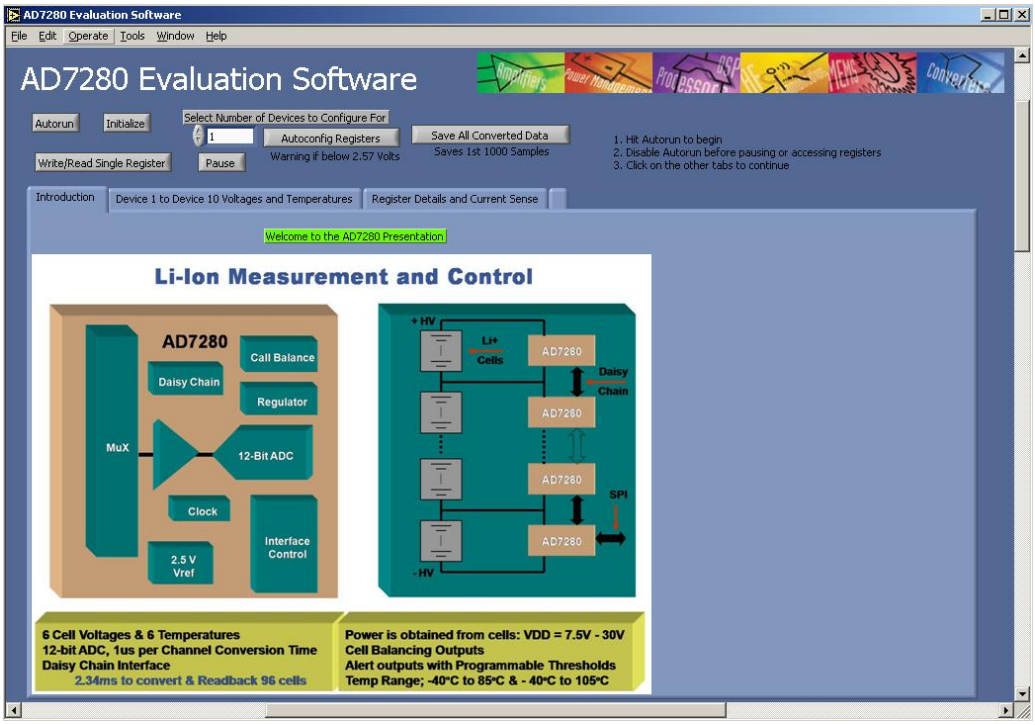


Figure 105 – GUI Main Screen

Figure 105 shows the screen as you open the program. To Start using the program, click the button Initialize and then click the button Autorun. The Initialize button downloads the software to the AD7280 through the CED board. The Autorun button starts the reading of convertion data from the AD7280s. While the program is in Autorun mode, hit Stop Board Actions shown on Figure 105 before configuring registers, writing/reading to registers or saving data.

9.5.1. Board Selection

On the left side, there are 11 Buttons, Activate Board 1 to Activate Board 11. Clicking any of these buttons will show the apropriate board data. For example on Figure 107, when the Activate Board 2 button is clicked, a screen pops up showing the data for the devices on board two. Each board has two devices, hence each tab on the Show Board screens will have two graphs. The Board Selection screen has been moved to the right most tab in the most recent of the software and the text for it has been erased as it did not look pleasing to the eye.

9.5.2. Voltage Readings

Shown on board two on Figure 106 is the voltage readings for all the inputs for board 2 in form of a plot and their coresponding numerical indicators. There are 2 devices on each board and each device has 6 voltage inputs, therefore there are 12 numerical indicators shown in volts on this screen.

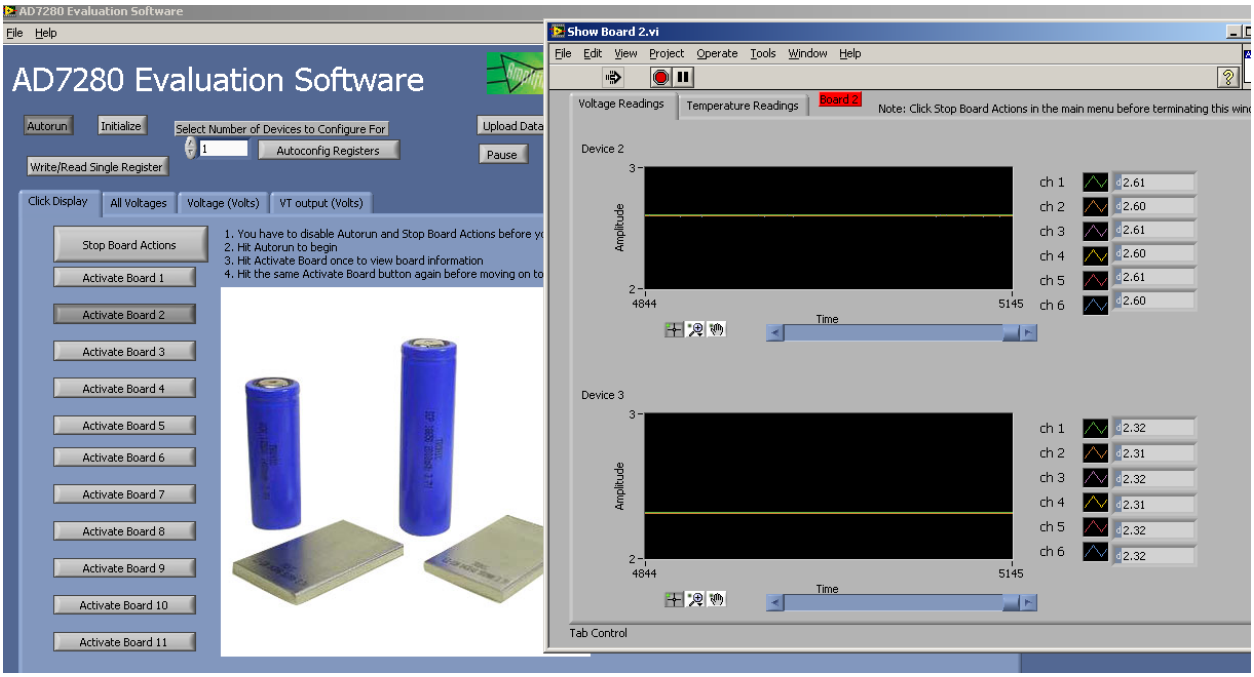


Figure 106 – Cell Voltage Value Screen

9.5.3. Temperature Readings

Each board screen has 2 tabs, Voltage Readings and Temperature Readings. Figure 107 shows what happens to the Show Board 2 screen when the Temperature Readings tab is clicked.

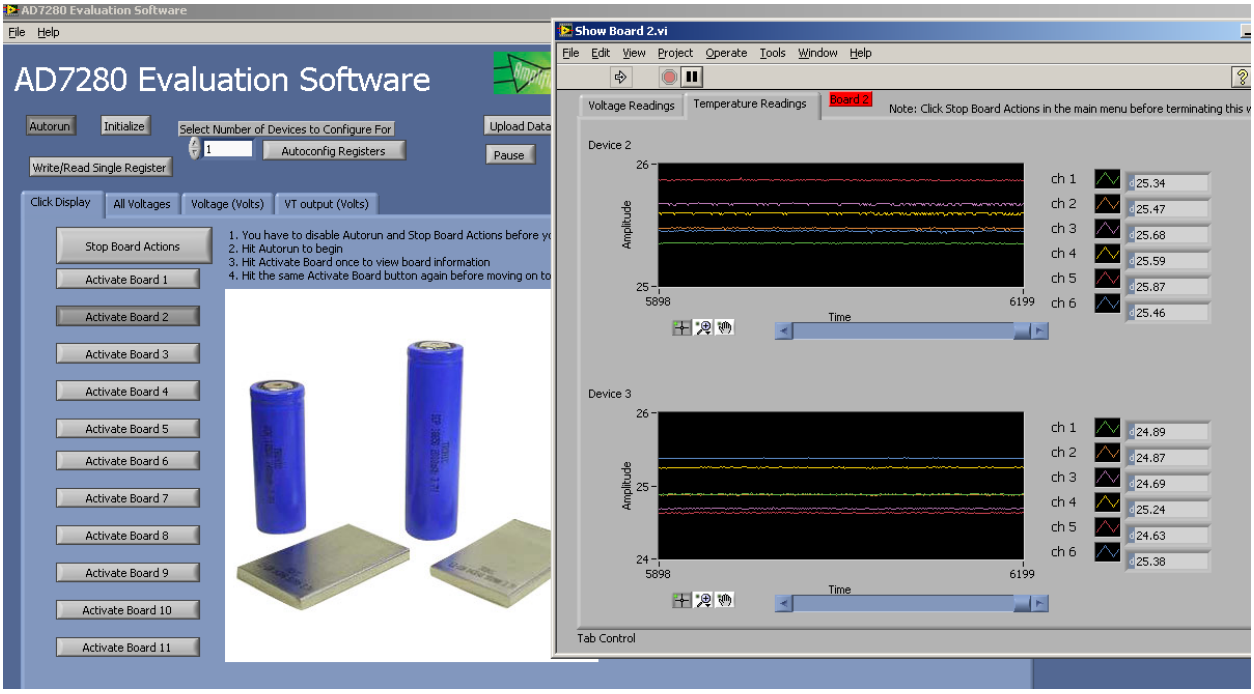


Figure 107 – Temperature Screen

After that tab is clicked the screen shows the thermistor readings in Celsius for the thermistor that are attached to board 2.

9.5.4. Reading from and Writing to all the AD7280 Registers

Before using this function, Stop All Board Actions should be clicked for safety measures. To use this function, click on the button on the upper left hand corner called Write/Read Single Register and a screen shown on Figure 108 should popup.

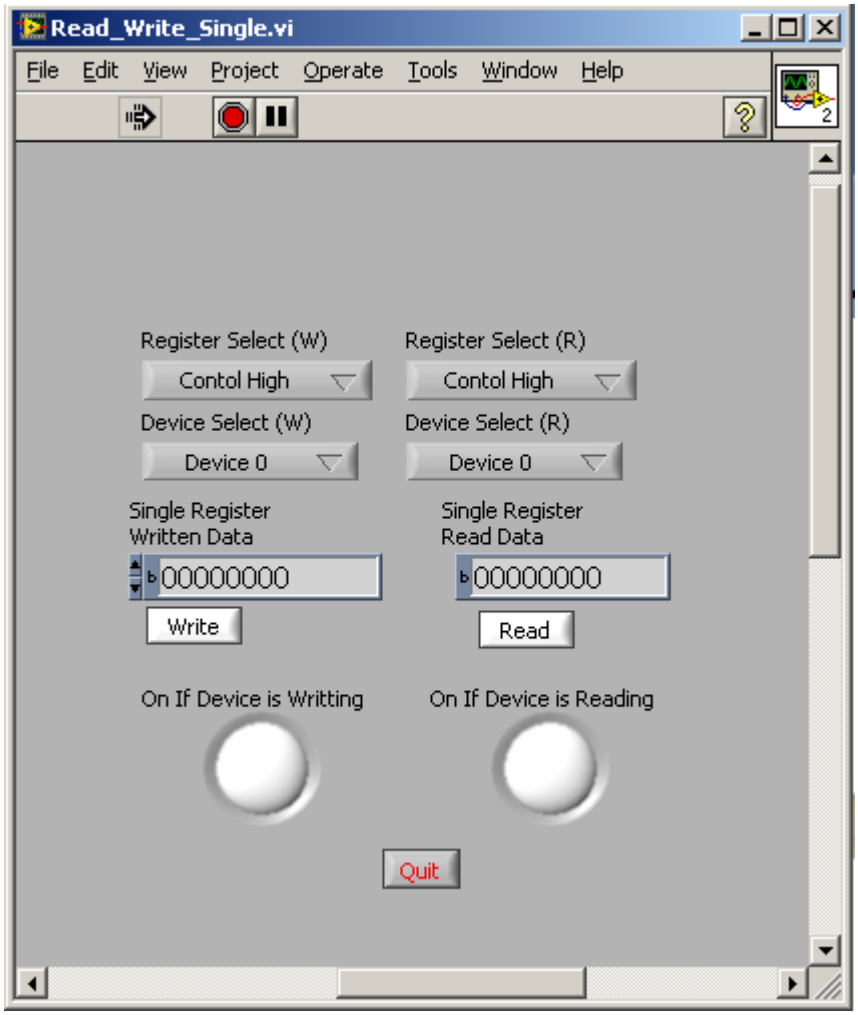


Figure 108 – Register Read/Write Screen

This function allows the user to read from and write to any device for up to 11 boards. That is Device 0 to Device 22. The buttons labeled Device 0 on Figure 108 are drop down menus. Figure 109 shows what happens when the user clicks on them. The buttons on the right side are for reading and the buttons on the left side are for writing.

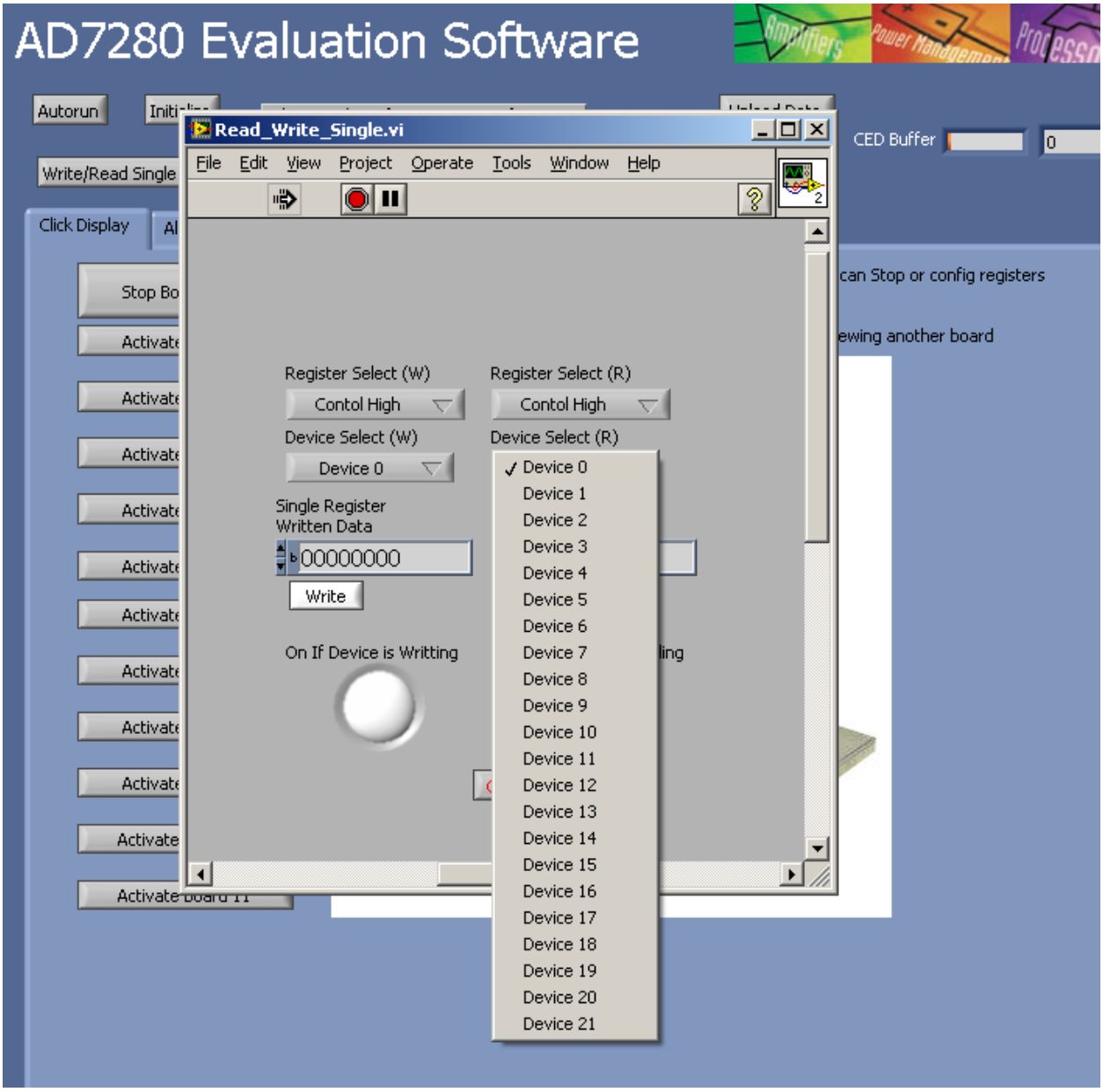


Figure 109 – How to select a device

After clicking on the drop down menu, the user can select which device to write to or read from.

The button Control High is also another dropdown menu. Figure 110 shows what happens when that button is pressed.

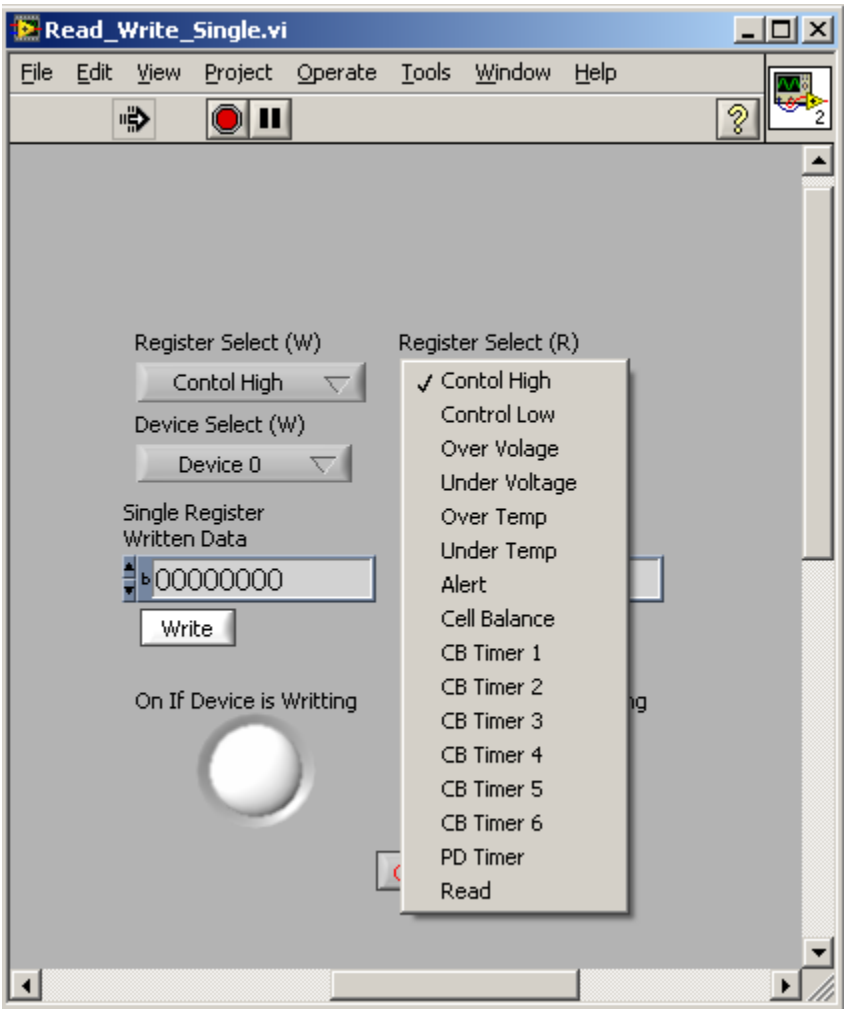


Figure 110 – How to select a register

The button indicated in Figure 110 Figure 33selects a specific register that the user wants to write to or read from.

Lastly, after a specific device is selected and a specific register is selected, clicking the Read button shown on Figure 108 will read the value of that register on that device. The user can also use the Device Select (W) and Register Select (W) buttons shown on Figure 110 and click on the Write button on figure X5 to write to that specific Register on that device.

9.5.5. Automatically Configuring the Alert Function

The AD7280 has a user-configurable alert function. The user can configure the voltage inputs and thermistor inputs in which an alert flag is set by using the Write/Read Single Register function.

Figure 111 shows a button called Autoconfig Registers and a numeric indicator circled in red. This button allows the user to automatically setup the alert condition with a single click. The user needs to enter the number to devices that are being used on that numeric indicator before clicking on Autoconfig Registers.

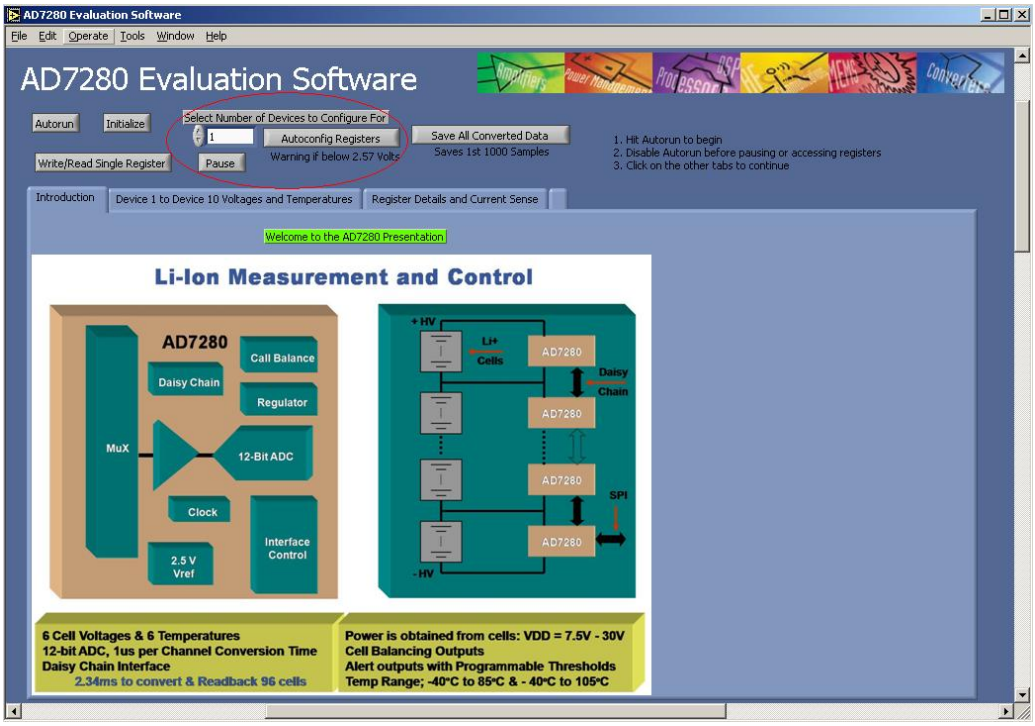


Figure 111 – Button to click on to configure alert condition

Currently, this function is set in such a way that if any input cell voltage is less than 2.5 volts and greater than 5 volts, then the alert flag gets set. This also triggers the LED, D10 on the evaluation board indicating that the alert flag is set. Temperature conditions in which the alert flag is set is not part of this function so the thermistor alert triggering is set to default which is alert when temperature is outside of this range -50 degree C to 150 degree C.

Once Autoconfig Registers is pressed, a screen will show up confirming that the button has been pressed. Press the Write button on that screen for this function to take effect.

9.5.6. Save All Converted Data

Before pressing the button, remember to toggle Autorun and Stop Board Actions off. Pressing the Save All Converted Data indicated in Figure 112 button will prompt you to save to a directory that you select. It is recommended to open the saved file as an excel spreadsheet.

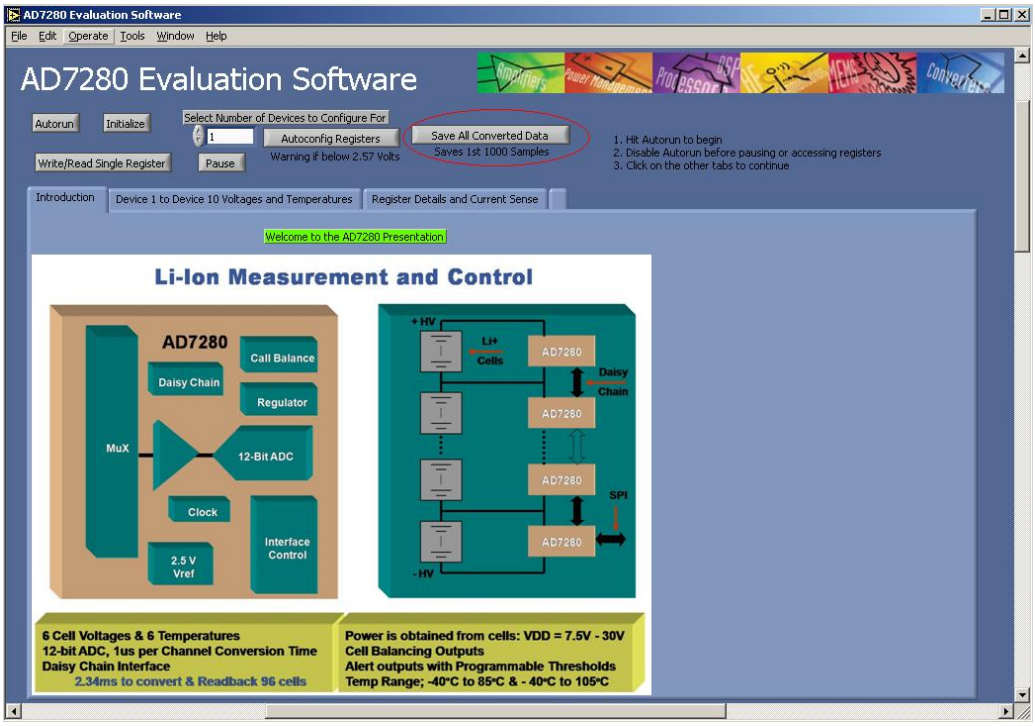


Figure 112 – Button to click on to save data

The saved file has the format shown in Table 8.

Table 8 – How to read the saved data

Device 1												Device 2
Cell 1 Volt	Cell 2 Volt	Cell 3 Volt	Cell 4 Volt	Cell 5 Volt	Cell 6 Volt	Cell 1 Temp	Cell 2 Temp	Cell 3 Temp	Cell 4 Temp	Cell 5 Temp	Cell 6 Temp	…
Data Point 1	Data Point 1	Data Point 1	Data Point 1	Data Point 1	Data Point 1	Data Point 1	Data Point 1	Data Point 1	Data Point 1	Data Point 1	Data Point 1	…
Data Point 2	Data Point 2	Data Point 2	Data Point 2	Data Point 2	Data Point 2	Data Point 2	Data Point 2	Data Point 2	Data Point 2	Data Point 2	Data Point 2	…
Data Point 3	Data Point 3	Data Point 3	Data Point 3	Data Point 3	Data Point 3	Data Point 3	Data Point 3	Data Point 3	Data Point 3	Data Point 3	Data Point 3	…
…	…	…	…	…	…	…	…	…	…	…	…	…

9.5.7. Show 10 Chips

Figure 113 shows a display of 10 devices with their voltage inputs and their temperature readings as well as a battery bar indicator.

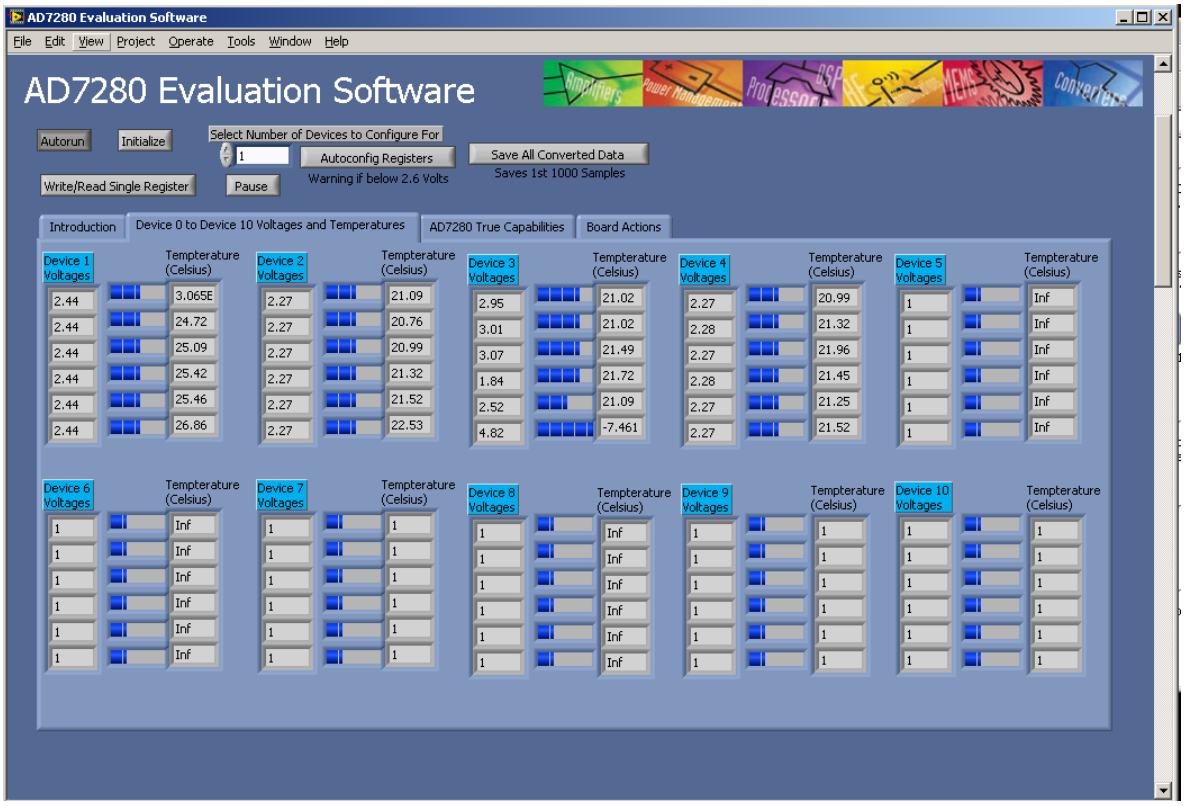


Figure 113 – showing 60 cell voltage and temperature readings

9.5.8. Selectable Detailed Display of all Devices

Figure 114 shows a screen that displays all the function of an AD7280 displaying all its control registers, alert indicator, temperatures, and voltages. It even has a selector to select between difference devices in the daisy chain and a current sense display that shows the current readings coming out of the current sense chip. A special button to note is the Invert Temp Reg button. Since the thermistor readings decrease in voltage drop as temperature goes up, the alert conditions are inverted. Pressing this button will correct this condition by inverted all input values the user sets to the registers.

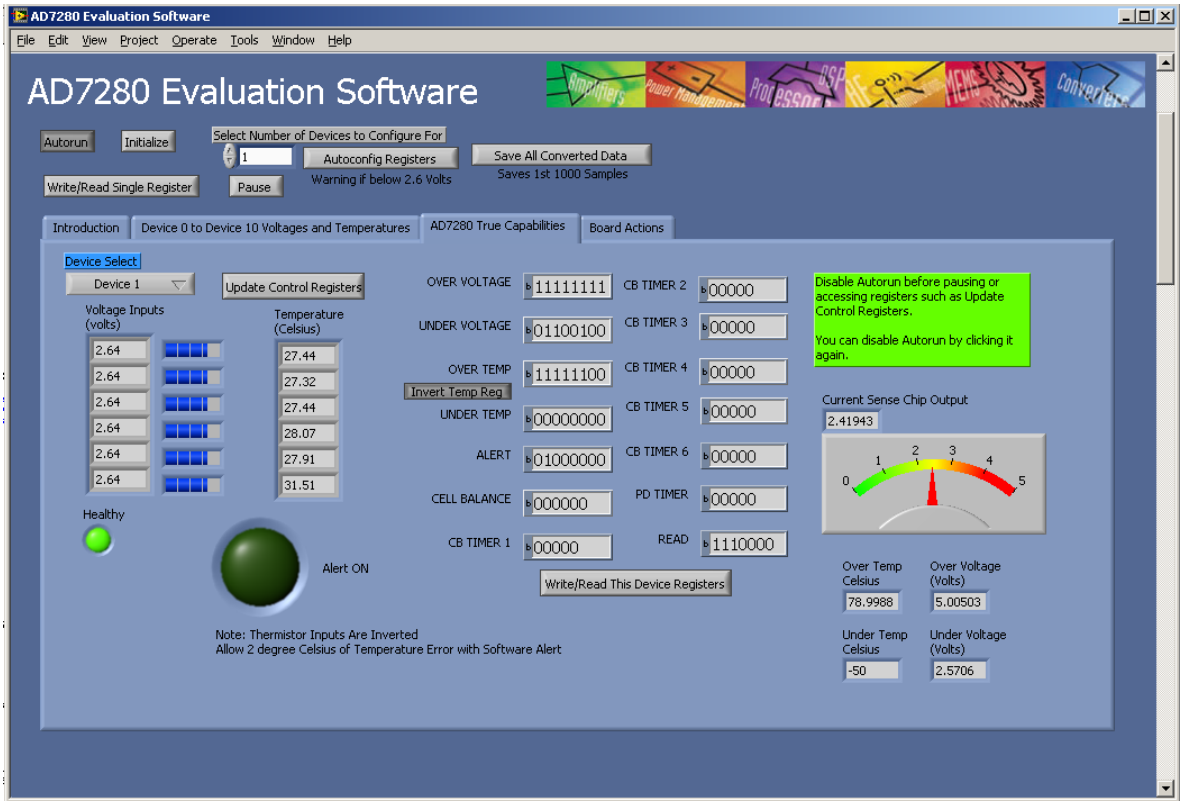


Figure 114 – shows all capabilities of AD7280 in one screen.

When setting registers note the following list:

Under Voltage and Over Voltage Registers:

Range: 1V to 5V, 8-bits total such that 11111111 = 5V and 00000000 = 1V

Under Temperature and Over Temperature Registers:

Range: -50C to 150C, 8-bits total thus, 11111111 = 150C and 00000000 = -50C

Alert in Daisy Chain:

To properly configure the alert register, for the last device on the daisy chain set the alert register as 01000000

For all other devices including the master device set the alert register as 11000000

9.6. DEMO Board Test Procedures

The following list is the steps which were agreed would demonstrate if the DEMO board was working properly when it returned from the manufacturer. The steps listed here were not followed precisely due to three factors. First, we learned during the assembly of the board that they were not soldering the AD7280 chips onto the board because of the clamping option that we used. This enabled us to much more freely test the system without danger of damaging ten chips, we could test two to start and build up. Secondly, due to managerial pressure, we skipped step four, which is related to testing the DEMO board in the series configuration. Finally, the part numbers of the resistors were changed after

this procedure was written. This turned out to not matter, anyway, as step four was skipped as stated previously.

1. Make a *temporary driver board* (TDB) where the inputs to chips 3-10 are grounded. The TDB should be a 64-pin connector attached to a breadboard with a resistor string, powered by the two adjustable power supplies, not the portable supply.
    a. Set the power supplies to apply Vdd=20V. **Do not connect the TDB to the DEMO board.**
    b. Turn on power.
    c. Test the TDB. If it doesn't work, make it work.
    d. Kill power supply output.
2. Connect the TDB to the demo board.
    a. Raise Vdd from 20V to 50V in steps of 5V total by raising the two power supplies in increments of 2.5V each.
    b. If this works, we've proven that we're able to successfully copy an EVAL board. Yippee.
3. Kill power supply output.
4. If the 50V from Section 2 does not smoke the first two chips, perform the following actions **in order**:
    a. Reconfigure the TDB so that we now apply 60V, distributed through chips 1-4. Chips 5-10 should still be grounded. Test the TDB.
    b. Remove R222. Place it at R900.
    c. Place links in positions R950-956.
    d. Remove R109-110.
    e. Set the power supplies to apply Vdd=35V.
    f. Turn on power. Ramp up to 60V as described in Section 2(a).
    g. If steps 4(a)-4(f) work, we've proven that we're able to get two EVAL board equivalents to work successfully in series.
5. Kill power supply output.
6. If the "two eval boards" work in series as described in Section 4, we are ready to test in parallel.
    a. Reconfigure the temporary driver board to provide constant power to all 10 chips. Even chips should receive the same input voltages, and odd chips should receive the same input voltages.
    b. Repeat steps 1(a)-1(d).
    c. Undo the steps described in Section 4(b), 4(c), and 4(d).
    d. Set the power supplies to apply Vdd=20V.
    e. Connect the TDB to the demo board and turn on power.
    f. Ramp up to 50V as described in Section 2.
7. If nothing has broken up to this point, it means that the DEMO board works properly.

9.7. Driver Board Test Procedures

The following steps were followed to guarantee that the driver board worked as expected.

1. Add voltage supply connector to strip board using at least 6 inches of slack wire. This part needs to be external to the box. Verify +48V output with multimeter.
2. Attach regulators to strip board, each with 100kΩ temporary loads to GND. Verify correct output voltages with multimeter.
3. Attach current sensing circuit to strip board with 100kΩ temporary load to GND. Vary input current and observe output voltage changing.
4. Connect constant voltage resistor/capacitor string to strip board. Verify correct output voltages with multimeter.
5. Attach opamps to voltage divider. Verify correct output voltages with multimeter.
6. Build adjustable voltage supply **on a breadboard**.
    a. Using the desk top power supply, **not** the portable one, apply Vcc=10V and verify expected circuit operation.
    b. Insert a 20V zener into the controlling arm. Increase Vcc to 30V. Verify proper current source operation.
    c. Insert the second zener into the controlling arm, and apply 48V. Verify proper current source operation.
7. Attach the adjustable voltage supply to the strip board. Remember to give the pots at least 6 inches of slack wire for all connections. They need to be external to the box.
8. Add 64-pin connector to strip board using at least 6 inches of slack wire for all connections. This part needs to be external to the box.

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