Migration of High Precision PulSAR Analog-to-Digital Converters to Blackfin-based Platforms

A Major Qualifying Project

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Abstract

This Major Qualifying Project sought to migrate Analog Devices' PulSAR line of ADCs to a more modern testing and evaluation platform, the SDP. The project resulted in more extensible daughter cards, a modular driver amplifier system, an integrated power supply design, and a software package to read and analyze the ADC data. Reference schematics were also developed and tested to showcase high performance and low power with the PulSAR converters.

Acknowledgements

This project was made possible through the contributions by many people. These contributions ranged from direct technical advisement to helping coordinate our accommodations while in Ireland. Regardless of the level of contribution, this project would not have been completed without the steadfast dedication of our support team.

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Executive Summary

Access to devices that digitize analog information is becoming more and more prevalent. The amount of digital information created each year is growing exponentially and does not show signs of slowing. Analog-to-digital (ADC) converters are the driving force that is making this progression a reality. Companies that produce ADCs, such as Analog Devices, Inc. (ADI), offer their customers ready-to-use evaluation platforms to assess and test their ADC product lines. Analog Devices, seeking to improve upon older testing platforms, has developed the System Demonstration Platform (SDP). This testing platform is smaller, cheaper, and more flexible than those of the past.

The goal of this project was to help design and develop the ADC evaluation boards associated with the SDP. These daughter cards can be used to test the performance of several of Analog Device's ADCs. These daughter cards looked specifically to work with the PulSAR ADCs, a line of 14-, 16-, and 18-bit successive-approximation register (SAR) ADCs. A new, modular daughter card would simplify the testing process required to evaluate ADC circuits. The project also sought to demonstrate the attainable performance of the PulSAR components by developing reference designs focused on low power consumption and on high AC performance. Lastly, a new software module would need to be written that supported the SDP testing platform. This

software design was based off the features and aesthetics of previous software and would enable users to effortlessly interact with the PulSAR ADCs boards.

To achieve these goals the project was sub-divided into three sections: schematic design, testing and implementation, and software design. The schematic design was comprised of developing fully-differential versions of the daughter card as well as a modular daughter card system that allowed rapid substitution of the ADC driver amplifiers. Experimental testing was used to assess the modular driver system and characterize the other board designs. The schematic design also included an integrated power supply to allow for a single input voltage from a wall adapter for customer ease-of-use.

Each main goal met success. The modular driver system performed within half a decibel of the original evaluation board design, with the added benefit of increased configurability and lower total customer cost. A single-input power supply was designed that supports an expansive range of ICs, and includes proper rail sequencing and options for using a benchtop supply. The low-power reference circuit yielded a signal-to-noise ratio over 85.5dB while only drawing 14mW of power at 1 MSps, and the high-performance reference circuit averaged 100dB or better for signal-to-noise ratio. Finally, the software program was written such that it accurately represents AC performance, regardless of signal spreading at high sample counts, excessive DC components, or other FFT artifacts. The software also provides an intuitive interface that recovers gracefully from error conditions.

Future work considered for this project includes several different recommendations from the group. First, the board designs that were not numerically characterized – such as the in-amp board and the power supply design – should be assessed to confirm performance. Improvements

can also be made in the software. Several of the calculations grand-fathered into the system should be re-evaluated to confirm that they are being calculated properly; however, this group did not have the expertise to determine the validity of their findings.

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Chapter 1: Introduction

1.1 Motivation

The amount of digital information created, captured, and replicated each year is growing exponentially and does not show signs diminishing [**2**]. In 2007, EMC's investigation of the "digital universe" revealed that 161 exabytes – 161 billion gigabytes – of data had been created in 2006 [**1**]. This amount has grown by an order of magnitude in five years, with 2011 on track to surpass 1800 exabytes of created data [**2**]. Such numbers are nearly impossible to conceptualize: "in 2006, if you printed out all the exabytes onto typewritten pages, you'd have enough paper to wrap the Earth four times over" [**1**].

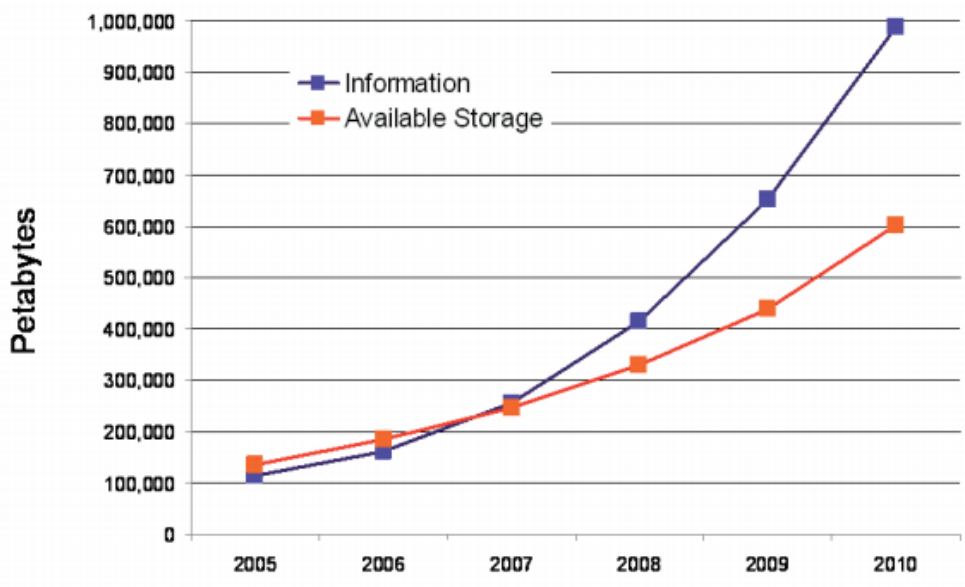


Figure 1: Annual Levels of Created Information and Available Storage [1]

Furthermore, the driving force of this exponential growth is the digitization of analog information into digital formats [**1**]. About one quarter of all created bytes come from still or video images, spurred forward by rising megapixel counts, falling costs of personal cameras and camcorders, and the ubiquity of media-enabled cellular phones [**1**] [**3**]. The rapid rise of image digitization is not restricted to personal photographs; all broadcasted television signals in the United States are now digital by Congressional mandate as per the Digital Transition and Public Safety Act of 2005 [**4**], and even vital medical imaging such as MRIs and CAT scans is transitioning to digital format for greater accuracy and longevity [**5**].

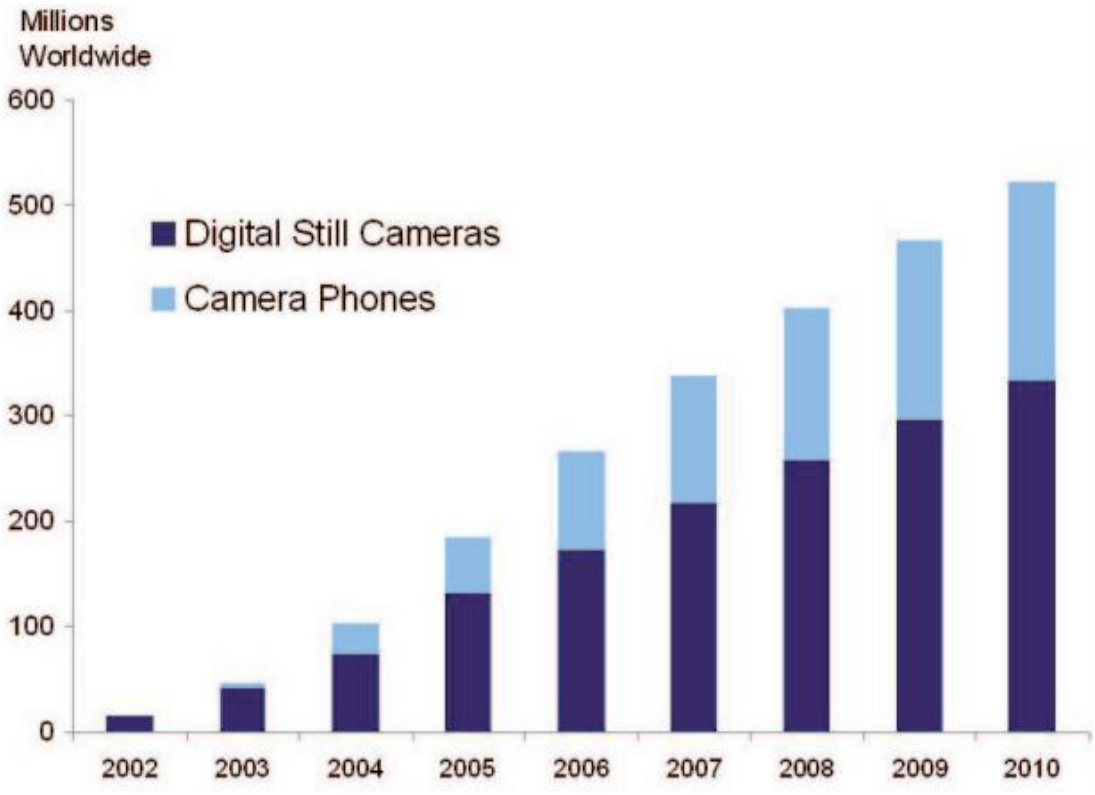


Figure 2: Annual Growth of Image Creation [1]

The proliferation of cellular phones and webcams has also led to a marked increase in bandwidth needed for the digitization of voice. Countless other examples of analog-to-digital creation include the entire music recording industry, the scanning of library collections, and even military

radar and radio applications. Regardless of what type of analog signal is being digitized, analog-to-digital converters (ADCs) are an essential component in the process and thus have become extremely important to the modern way of life.

However, a single ADC design would not accommodate the myriad of industries that depend on it; a diverse selection of internal architectures has been developed to cater to specific applications and performance concerns. Typically, the most important criteria for an ADC are sampling rate and measurement precision while retaining signal integrity [**6**]. As seen in Figure 3, three principal architectures have emerged that offer a continuum of speed versus resolution: pipelined ADCs, successive-approximation register (SAR) converters, and sigma-delta (Σ-Δ) [**7**]. Manufacturing limitations require inherent tradeoffs between the two metrics.

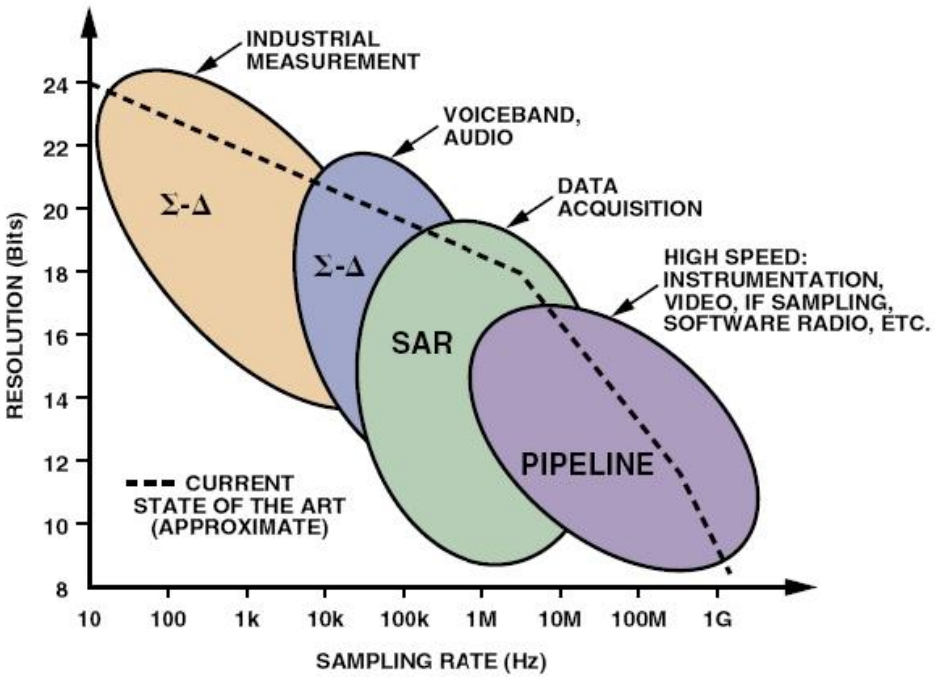


Figure 3: Resolution and Sampling Rates for Σ-Δ, SAR, and Pipeline ADC Architectures [7]

Integrated circuit manufacturers such as Analog Devices, Inc. (ADI) continually try to push the limits of throughput and precision without compromising performance, but increasing the

converters' complexity has led to a corresponding increase in the difficulty of properly using ADCs. Modern datasheets are replete with special grounding concerns, layout requirements, and stringent performance requirements on the surrounding ICs and components (see [**8**] and [**9**]). Seeking to remedy this issue, Analog Devices produces evaluation boards for its ADCs that serve as a demonstration platform of their capabilities and a design guide for applications engineers.

1.2 ADC EVALUATION BOARDS

Rather than examining the full breadth of analog-to-digital converters and their accompanying evaluation boards, this project limits its scope to the PulSAR line of ADCs available from Analog Devices. The PulSAR series is a set of high-resolution (14- to 18-bit) successive-approximation register analog-to-digital converters that are based on charge redistribution inputs [**10**]. Available with supported sampling rates from 100 kSps to 10 MSps, the PulSAR converters are often a respectable choice for data acquisition applications.

There are several evaluation platforms available for the PulSAR line. With little exception, the platforms follow a two board design pattern: there is a daughter card that holds the ADC and a controller board that manages communication with the PC and (oftentimes) regulates the power supply. A test engineer can apply a given analog input to the ADC and the output data will be forwarded to the computer to be interpreted by the supplied Analog Devices software. The software packages make it particularly easy to monitor AC performance levels, waveform shapes, and output code histograms. This allows rapid evaluation of a component at whichever operating conditions are required by the customers.

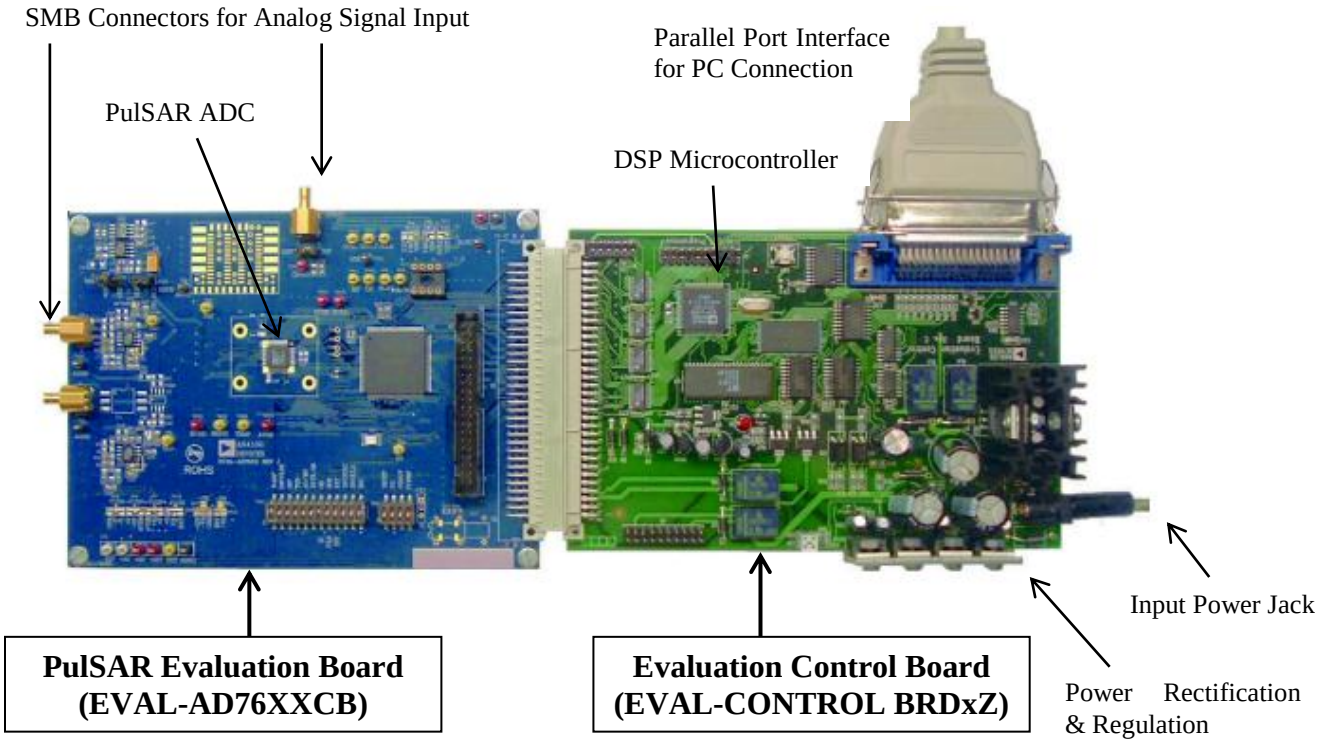


Figure 4: Overall Evaluation Control Board (ECB) Testing Platform [10]

The first and oldest testing platform is referred to as the Evaluation Control Board (ECB) and is shown assembled in Figure 4 [**10**]. The ECB platform is based off the controller card of the same name, the Evaluation Controller Board (EVAL-CONTROL BRDxZ), which is pictured in Figure 5 [**11**]. The controller board collects data from the analog-to-digital converter through the 96-pin connector that joins the two boards. This data is processed by the ADSP-2189 DSP microcontroller and translated into a parallel format for transmission to a PC over the parallel port interface. The usage of the parallel port is a weak point of the design – Analog Devices admits "there exists issues with parallel ports on PCs" [**10**] [**12**] and recommend testing on a

USB-based platform instead. Furthermore, the interface is becoming obsolete and is increasingly difficult to find on a modern computer.

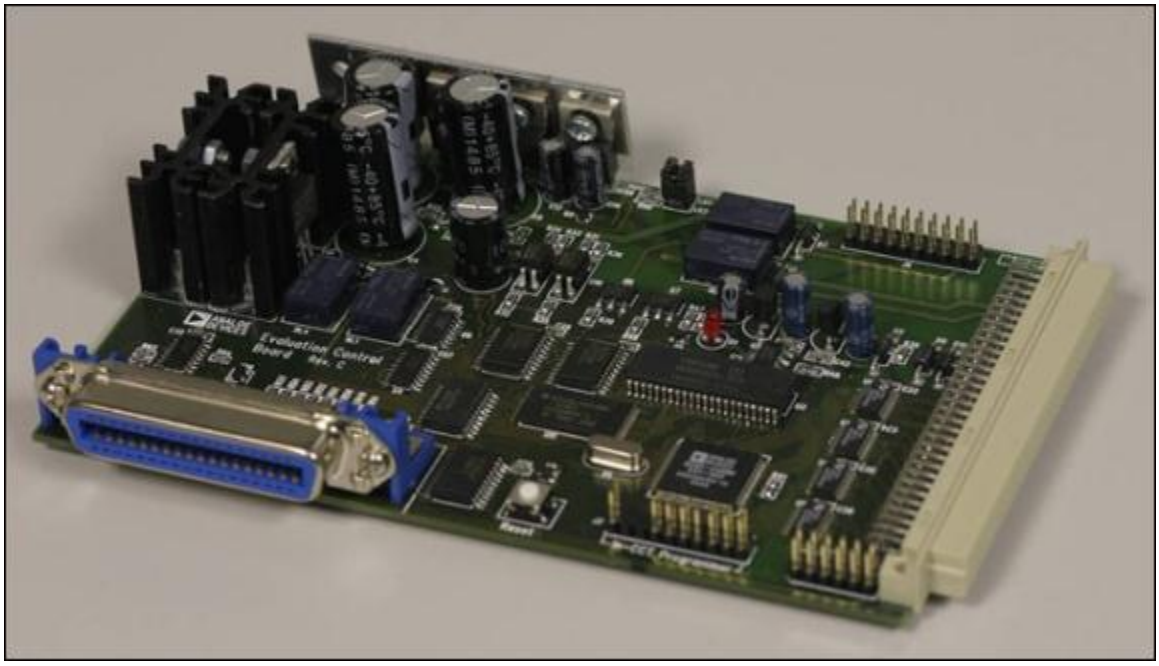


Figure 5: Photograph of the Evaluation Controller Board (EVAL-CONTROL BRDxZ) [11**]**

Additional drawbacks of the controller board include its price ($253.00 as of September 2011 [**11**]) and physical footprint. The board is fairly large but its dimensions cannot be reduced much further due to the length of the 96-pin connector to the PulSAR board. The PulSAR board (EVAL-AD76XXCB) primarily suffers from inflexibility. Without a surface-mount soldering station, neither the analog-to-digital converter nor its support circuitry can be substituted for other components. This limits the ability of customers to recreate their exact operating conditions, and necessitates the purchase of another board for each part. Finally, neither board of the ECB platform is optimized for power draw, making this a poor candidate for evaluating ADCs for mobile or micropower applications. While functional, the ECB testing platform is not ideal.

The second evaluation platform, the Controller Evaluation and Development (CED) Board is the descendent of the ECB and draws heavily from the original design. As pictured in Figure 6, the testing platform is similar to the ECB, using matching 96-way connectors to mate with the same series of PulSAR Evaluation Boards. The most significant difference is that the parallel port is replaced by USB 2.0, increasing compatibility and ease of use.

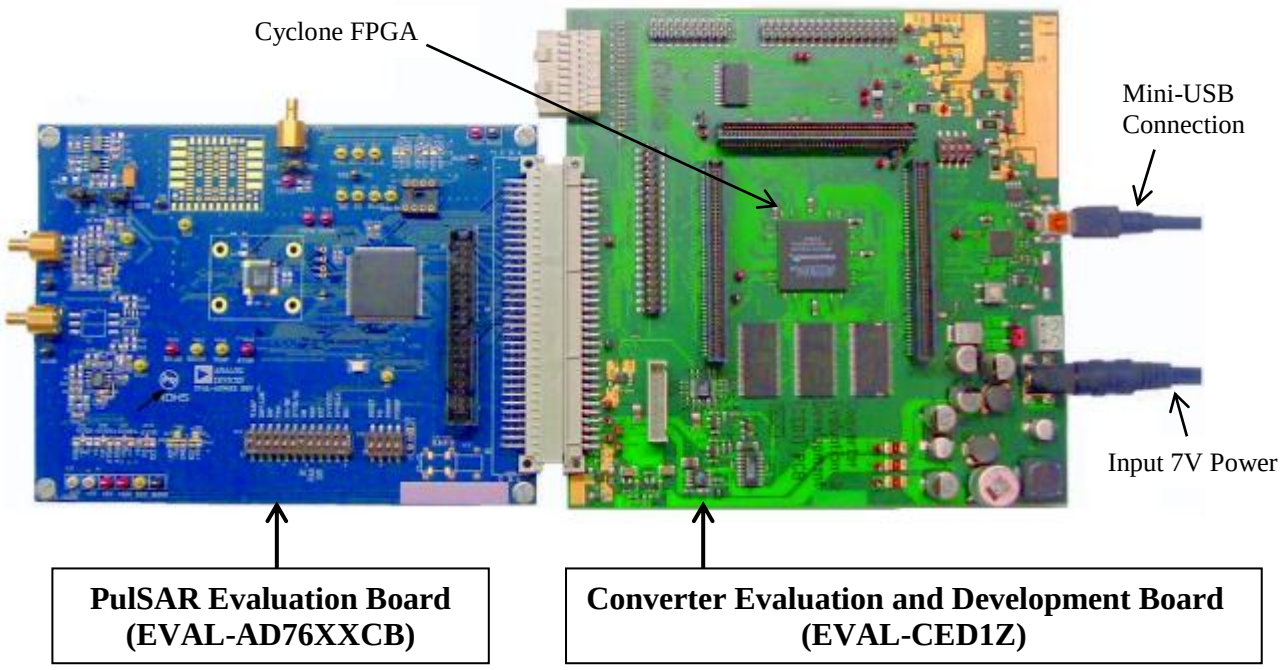


Figure 6: Overall Converter Evaluation and Development (CED) Testing Platform [10]

Unfortunately, many of the same criticisms can be levied against the CED platform. Although the CED boasts additional interfaces and connectors to join to other Analog Devices products, the extra components raised the price to $506 (as of September 2011) [**13**]. Since customers are still required to buy several PulSAR boards if they desire to test multiple components, the price of the CED testing platform is a significant obstacle.

The third and most recent testing platform for Analog Devices' PulSAR line is the System Demonstration Platform (SDP) and is a complete redesign of the testing methodology. As seen in the photograph in Figure 7 [**14**], the SDP board is much smaller than the former platforms, easily fitting in the palm of a hand. The large 96-pin connector between the controller and the evaluation boards has been replaced by a small form-factor PCB-PCB connector, and the Blackfin microprocessor on the SDP communicates easily with computer software through the USB interface. The cost per unit is also reduced to $100 [**15**] to make testing more affordable for customers; however, the PulSAR Daughter Cards are still in development by Analog Devices and this MQP and cannot be purchased at this time.

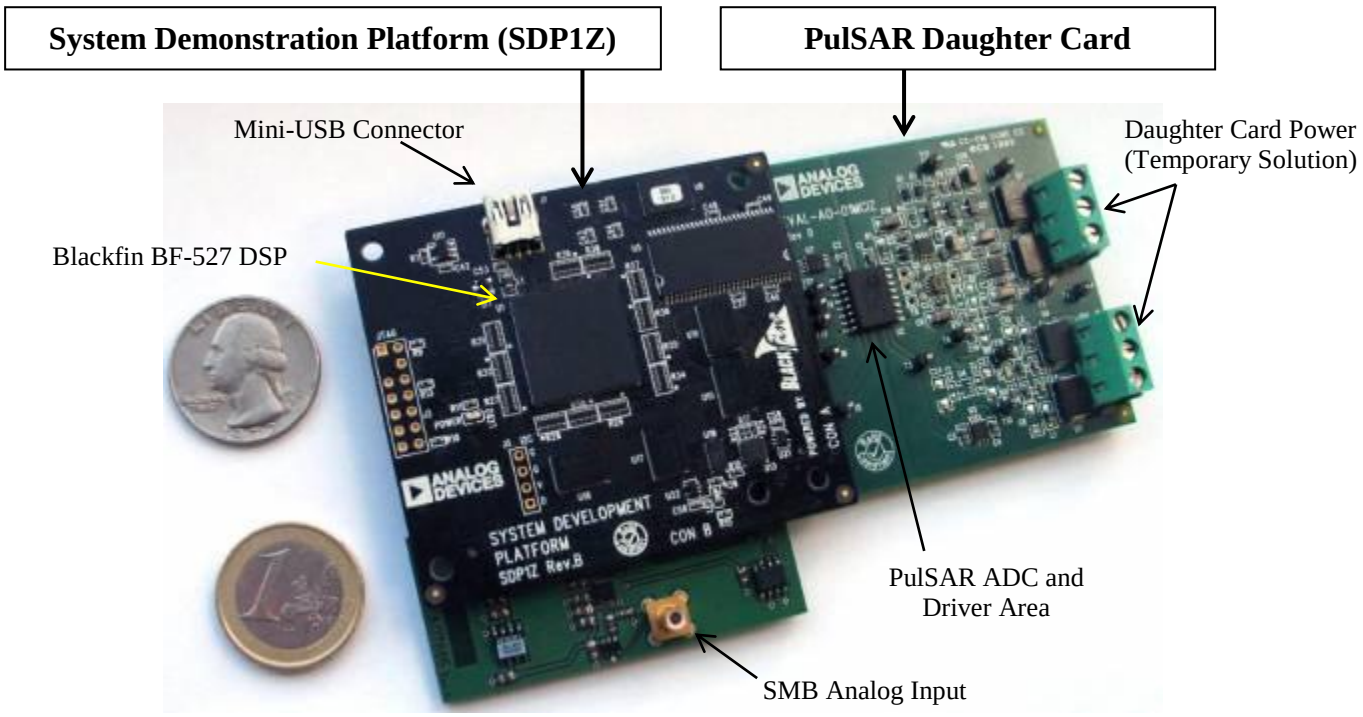


Figure 7: Overall System Demonstration Platform (SDP) with Size Reference [14]

Unlike the ECB and CED testing platforms, the SDP controller board does not supply and regulate the power for the entire system. Instead, the current design powers the PulSAR

Daughter Card with a benchtop supply via screw terminals. This expedites in-house development, but the power design will be replaced before the PulSAR boards are marketed. Also of note is the relatively sparse amounts of circuitry on the daughter card compared to the large EVAL-AD76XXCB boards used with ECB and CED – this makes the SDP a viable candidate for testing mobile or micropower applications of the PulSAR converters.

1.3 PROPOSED DESIGN AND CONTRIBUTIONS

This project aims at enhancing and modifying the design of the PulSAR daughter cards that attach to the SDP. As discussed above, Analog Devices' existing testing platforms are expensive, non-configurable, and are unsuitable for low power applications. A properly designed daughter card can address all of these drawbacks and more. Specifically, this project seeks to:

- Design an integrated circuit solution for power input and regulation. Presently, the daughter cards are powered by benchtop power supplies; end-users would be better served by a single input voltage that is stepped down to create the necessary onboard power rails. Attention will be paid to minimizing noise and ripple on the power lines, as well as sequencing the rails for proper operation of the signal-chain ICs.
- Develop schematics and layouts for surfboards or expansion boards that enable the user to quickly substitute ADC drivers. These boards will support single-ended, differential, and instrumentation amplifiers with a common connector pinout to maximize compatibility with the daughter cards.
- Create demonstration circuits – termed *Circuits from the Lab* in ADI parlance – that show PulSAR designs that cater to (a) low power consumption and (b) high AC performance.

These will be assembled and performance-tested to match data against the theoretical performance.

- Program a software program in LabVIEW that will collect data from the SDP's USB interface. This code can be developed from existing ECB software, but requires a major overhaul of the graphical interface, support for new parts and features, and code refactoring and optimization to ease future support of the program.

Paramount throughout this project is a focus on the performance of the PulSAR analog-to-digital converters. None of the above enhancements should degrade the component's output, and the surrounding circuitry (such as the ADC driver and the voltage reference) must be chosen properly at all times to complement the ADC.

1.4 REPORT ORGANIZATION

This report is presented in a linear fashion. First, Chapter 2 serves to detail background research that was instrumental in the group's ability to amply address the proposed design challenges, as well as discusses other topics imperative to understand the report. Chapter 3 introduces a more formal proclamation of the goals of this project. It also introduces the group's proposed approach and timeline to achieve these goals. Chapter 4 details implementations developed by the group during the 10-week scope of this project. The chapter is divided into four sections: general design, *Circuits from the Lab*, daughter cards and surf boards, and the LabVIEW module. Chapter 5 introduces and contemplates the implications of testing conducted during the project. Last, Chapter 6 reflects upon the project and provides considerations for future work. It also provides conclusions based upon the designs and results achieved during the project.

Chapter 2: Background Research

The following chapter contains the necessary information to understand the operation and evaluation of modern analog-to-digital converters. It presents an explanation of how a successive-approximation register ADC is constructed and functions, how ADCs are objectively evaluated on their dynamic characteristics, how to properly select the ADC's support circuitry for best performance, and outlines methods of serial communication between the ADC and a digital processor.

2.1 Analog-to-Digital Converter Architecture

All analog-to-digital converters serve a similar purpose – they sample an input (often voltage) signal and output an N-bit digital code corresponding to the magnitude of the sample. Two of the most important parameters for an ADC are resolution (also called bit-count) and sampling rate. An N-bit resolution ADC divides the full-scale input range into 2^N unique output codes, so higher bit-counts result in more precise measurements. The sampling rate f_S determines how often a new conversion is started, and should be at least double the maximum frequency present in the input signal if all aliasing effects are to be eliminated.

Limitations in existing manufacturing technology make it difficult to simultaneously have high resolution and sampling rate, and different internal ADC architectures have been developed that

target each combination of the two parameters. As seen in Figure 8, the three predominant architectures are sigma-delta (Σ-Δ), successive-approximation register (SAR), and pipelined [**7**]. The Σ-Δ converters can achieve the highest resolutions and the lowest throughput; while the pipelined ADCs can have unmatched sampling rates with lower bit-counts. The SAR architecture is a compromise between the two extremes, reaching reasonably high precision and speed at the same time.

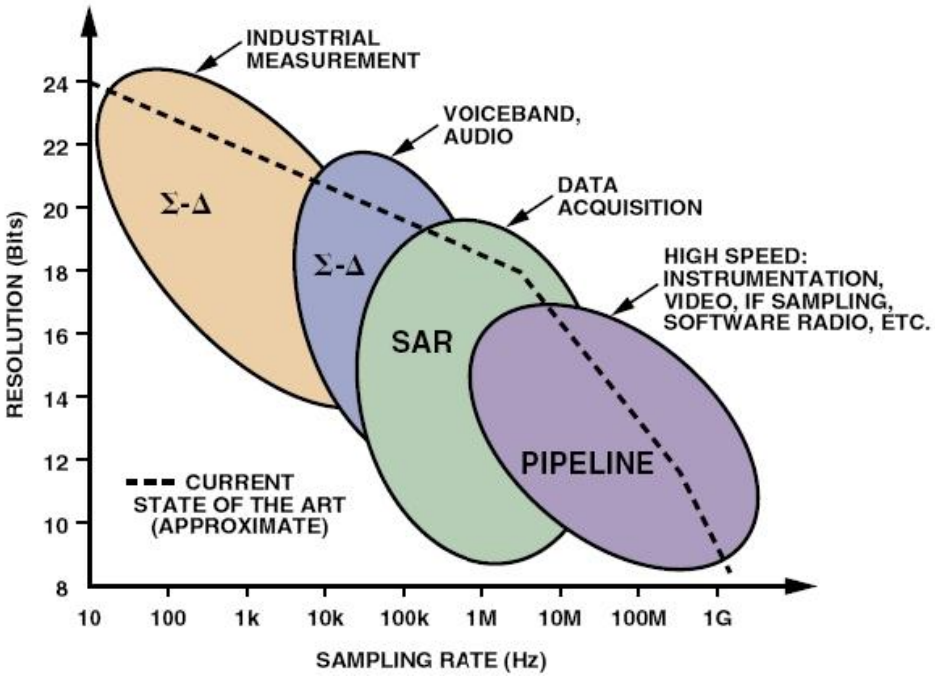


Figure 8: Resolution and Sampling Rates for Σ-Δ, SAR, and Pipeline ADC Architectures [7]

This section examines the physical construction of SAR-based analog-to-digital converters, and how this affects their operation and performance. While also applicable to general-purpose amplifiers, the types of analog inputs are discussed to develop understanding about single-ended, pseudo-differential, and fully-differential ADCs.

2.1.1 Successive-Approximation Register (SAR) ADCs

The SAR architecture converges on the proper quantization level with a binary search, an algorithm that determines an N-bit output code within N iterations. A typical SAR converter is modeled in Figure 9, and consists of three key blocks: a comparator, an N-bit register, and an N-bit digital-to-analog converter (DAC) [**16**].

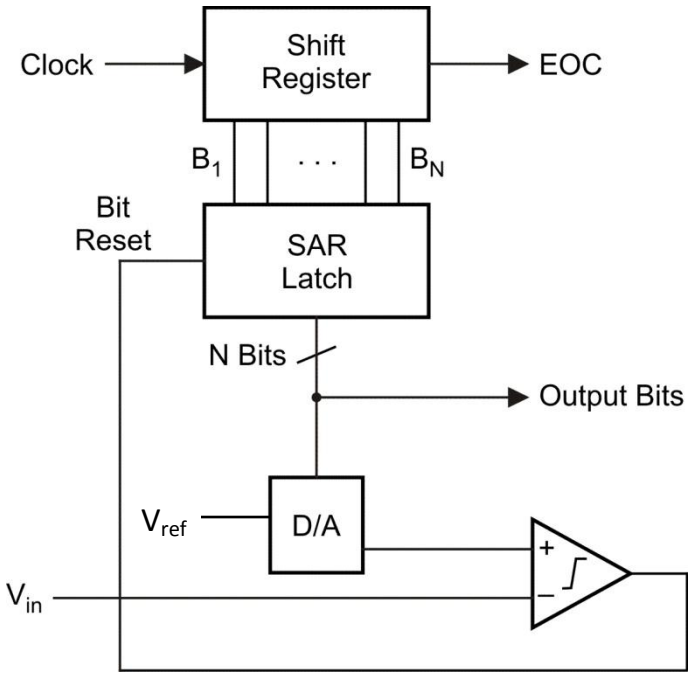


Figure 9: SAR ADC Block Diagram [16**]**

At the start of a new conversion, a 1 is loaded into the most significant bit (MSB) of the register, with the other bits all cleared to 0. This midscale digital bit pattern makes the output of the digital-to-analog converter half of its supplied reference voltage V_{REF}. The DAC voltage is then compared to the input signal and the comparator output feeds back to the register to slowly narrow in on the correct quantization level. The 1 in the MSB is retained if V_{IN} is greater than V_{DAC}; it is replaced with a 0 if V_{IN} is less than V_{DAC}. With the completion of one bit, a second 1 is shifted into the register's next-most significant bit and the process is repeated down to the

least-significant bit (LSB). Once the entire digital word is available, an end-of-conversion (EOC) signal and a data ready (DRDY) signal are passed out of the ADC [**17**].

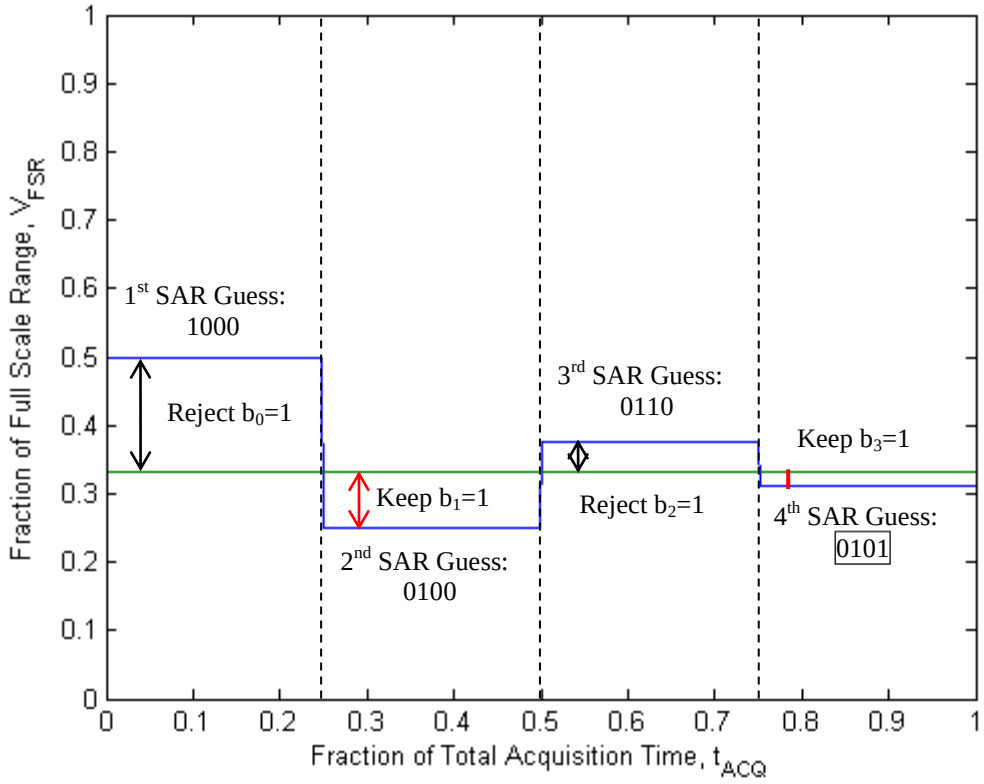


Figure 10: Example Conversion of a 4-bit SAR ADC [17]

The successive approximation register is a sequential logic element and must be clocked in order to function. Since N comparisons need to be completed in one conversion, the input clock must run at least N times faster than the desired sampling rate, but the acquisition time of the ADC's analog inputs (discussed further in Section 2.3.1 Sample-and-Hold Circuit) must also be incorporated for accuracy. As seen in Equation (1), the N comparisons must be made in the sampling period $1/f_S$ minus the acquisition time t_{ACQ}.

$$f_{CLK} = \frac{N}{\frac{1}{f_s} - t_{ACQ}} \text{ [Hz]} \quad (1)$$

Unfortunately, the main clock frequency cannot be raised indefinitely to allow higher sampling rates; each DAC that is built into an SAR ADC has a minimum settling time beyond which accuracy degrades. Aside from the minimal propagation times through the logic circuitry, the DAC settling time is the largest limiting factor in SAR converter speeds [**17**]. Furthermore, doubling the bit count requires more than twice the settling time, making high-speed and high-precision SARs very difficult to design [**18**].

The main DAC architecture used in advanced SAR converters is a switched-capacitor array, also known as a capacitive binary-weighted DAC [**19**]. Illustrated in Figure 11, N-bit switched-capacitor arrays have N capacitors with binary powers of a unit capacitance *C*, and a dummy capacitor is included to bring the total capacitance to $2^N C$. Some literature will instead denote the total capacitance as $2C$, and scale the individual capacitances from *C* for the MSB to $1/2^N C$ for the LSB.

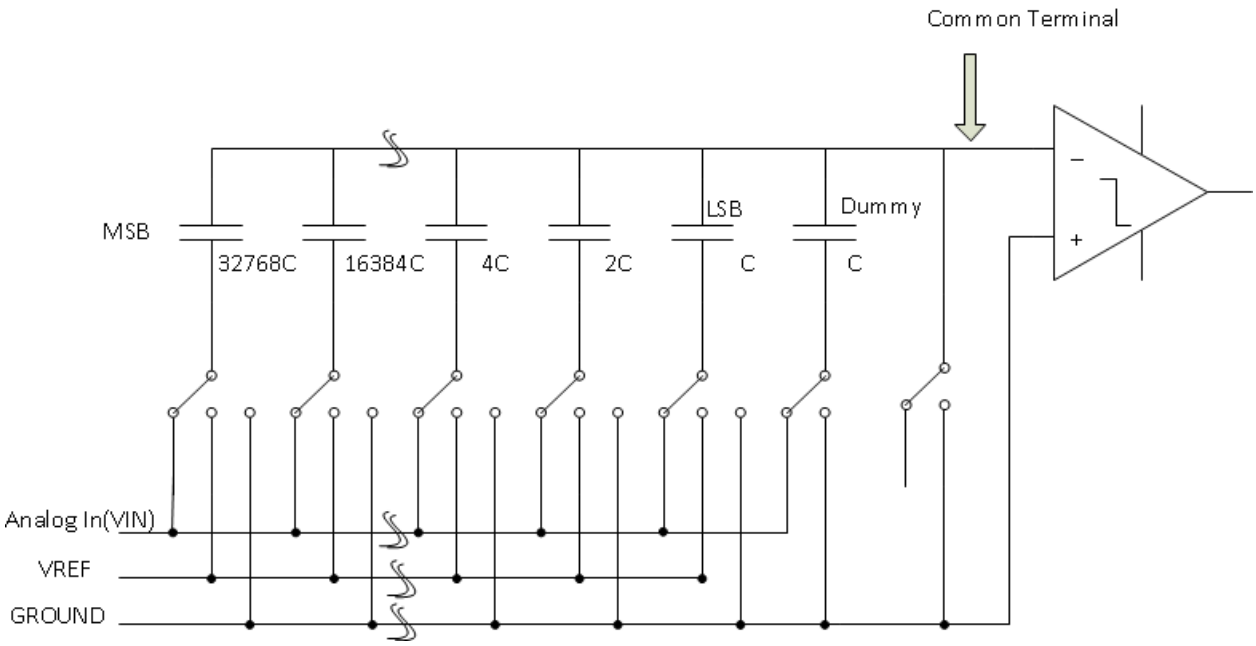


Figure 11: 16-bit Example of a Switched Capacitor Array [17]

Stepping through the operation of an SAR again, the switched-capacitors are initially connected to V_{IN} to track the analog input until the conversion signal is received. The MSB capacitor is connected to V_{REF} to simulate a 1 while the others are driven to ground as 0's. The comparison is performed and the result is shifted into the register, then the next capacitor is connected to V_{REF} to represent a 1. This is completed down to the LSB – the dummy capacitor is never connected to V_{REF} [**20**]. The capacitors experience leakage effects within milliseconds, but these effects are irrelevant since the entire conversion process is typically completed in a few microseconds [**19**].

Building a binary-weighted DAC out of capacitors has two main advantages compared to more familiar resistor networks. First, a capacitive DAC itself behaves as a sample-and-hold circuit, eliminating the need for a separate module and simplifying the overall design [**19**]. Second, resistors are difficult to manufacture precisely over such a large range of values, whereas modern lithography permits such wide ranges for capacitors by controlled etching of plate area [**19**].

Despite advances in lithography, DAC capacitive matching is the principal limitation to overall throughput as well as precision [**17**]. When this problem was encountered with resistive designs, the solution was an R-2R ladder, which only requires two exact values to be manufactured. Unfortunately, a C-2C ladder demonstrates intolerable parasitic capacitances that hinder its accuracy more than capacitive mismatch in the switched-capacitor array [**21**]. Until this problem is sufficiently resolved, the switched-capacitor array remains the predominant DAC technology in SAR ADCs.

2.1.2 Types of Analog Signal Inputs

In today's electronics, there are several different signaling schemes. Two that are most prevalent are single ended and differential signals. Both are produced naturally by different types of transducers and thus the ability to process both is essential. Single ended signal paths are the simplest, made of a single trace allowing a ground-referenced signal to travel along it from one component to another. A differential signal, in contrast, is carried on two conductors as seen in Figure 12 [**22**]. The actual signal is the difference between the voltages carried on each conductor. Differential signaling requires more board traces and more complex input stages for ICs, resulting in a higher cost than single ended signals. However, differential signaling does provide several advantages as well, such as improved common mode rejection, electromagnetic interference, and dynamic range [**23**].

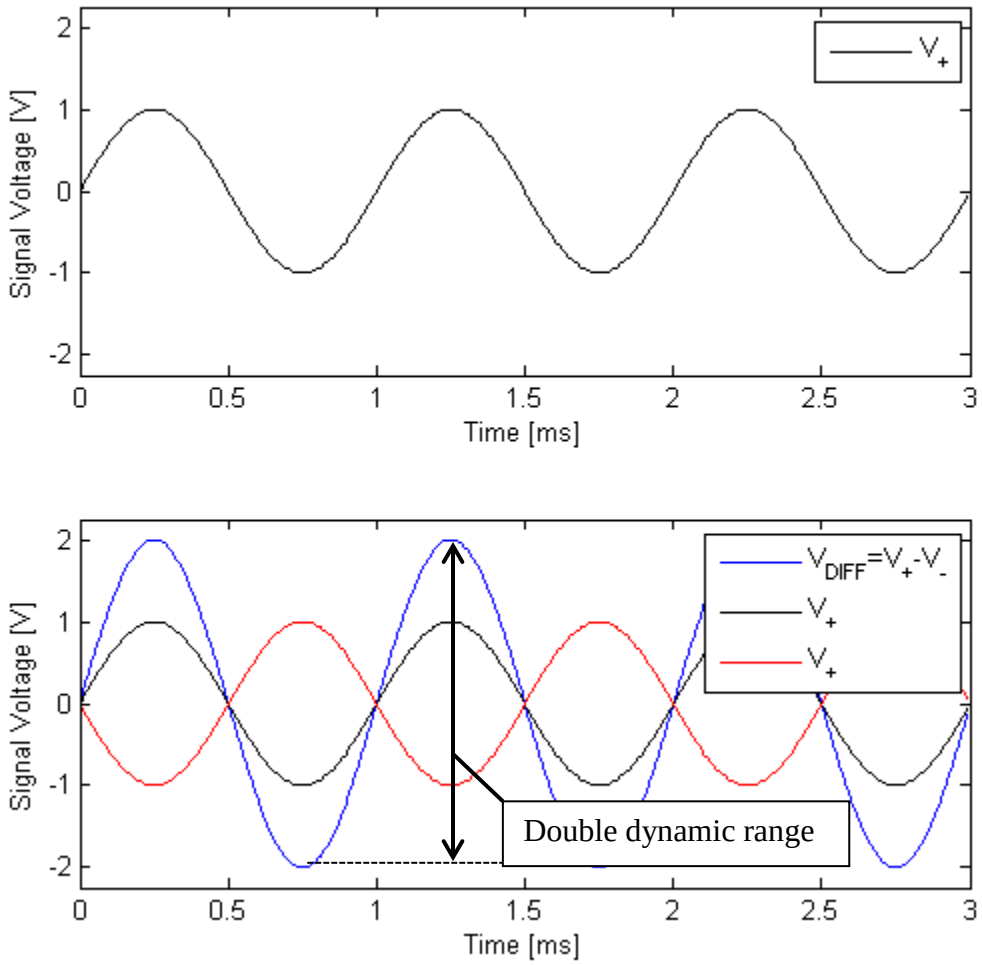


Figure 12: Single Ended Signaling (Top) vs. Differential Signaling (Bottom)

One of the largest advantages that differential signals provide is their common mode rejection ratio (CMRR). Common mode rejection ratio is a term pertaining to how well inputs reject signal discontinuities that are prevalent in both inputs. A simple example of this concept is very useful at demonstrating how a good CMMR can be beneficial to signal communications. Demonstrated in Figure 13, two ADC systems are subjected to the same noisy environment. ADC "X" uses differential signaling, with signals A and B carried on the two conductors. The single-ended ADC "Y" carries a single signal on trace C.

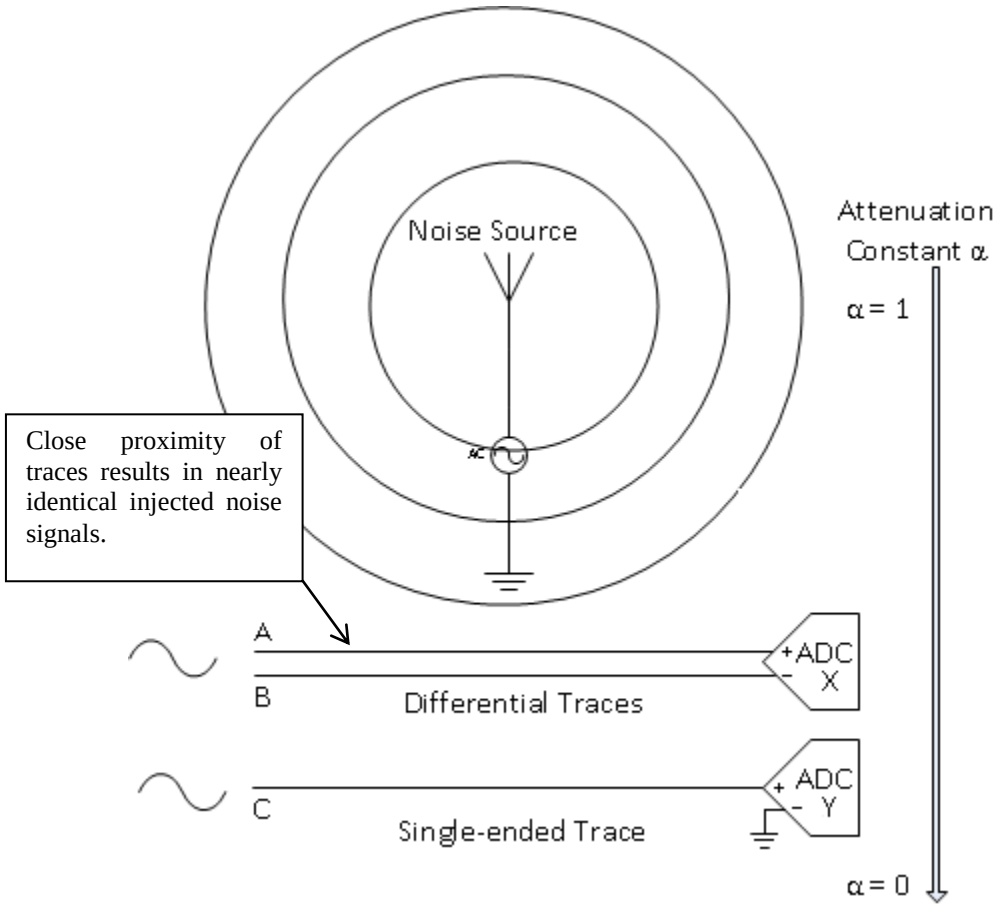


Figure 13: Noise Injection in Single-Ended and Differential Systems

From the definitions of single-ended and differential signaling, the two ADCs have effective input voltages of:

$$X = A - B \tag{2}$$

$$Y = C \tag{3}$$

Based on the strength and distance of the noise source, some level of noise Q will be injected onto the signal traces A, B, and C. The two signaling systems become:

$$X = (A + Q) - (B + Q) \tag{4}$$

$$Y = C + Q \tag{5}$$

The use of dual inverted signals in differential signaling allows the common-mode noise to be cancelled out. In a noiseless environment signals X and Y would be equivalent, but once real-world noise is included in the analysis the differential signal X is more accurate because of the common-mode rejection.

$$X = (A + B) + (Q - Q) \tag{6}$$

$$X = A + B \tag{7}$$

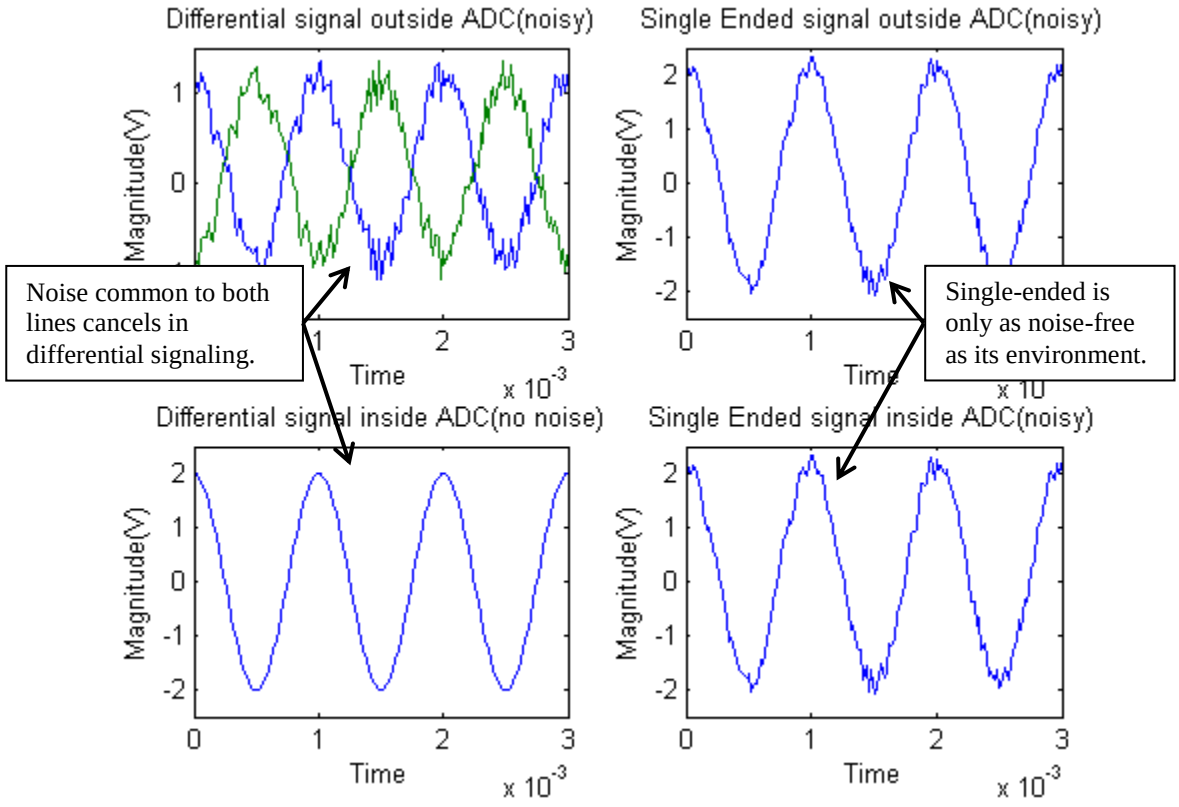


Figure 14: Graphical View of Differential Signaling's Common Mode Rejection

This simple example illustrates how common-mode noise results in an error on a single-ended signal path but is eliminated or reduced when using differential inputs. Differential rejection of common-mode noise is often used practically to make signal lines less susceptible to electromagnetic interference (EMI). In a properly routed signal plane, the traces for differential signals should be run close to each other and of equal length, thus EMI injected onto one trace is likely to also appear on the other [**23**]. Since the signal is differential, this added noise will ultimately be cancelled out. Another consequence of a properly designed differential signal path is that they tend to reduce EMI produced by the signal itself. When routed closely together, the electromagnetic fields created by the two current-carrying wires are ideally equal and opposite in strength, thus destructively interfering to nothing [**23**]. The common-mode rejection of differential signaling can also eliminate even-order harmonic distortion by virtue of a derivation similar to Equations (2) to (6) [**24**].

It is worth noting that in differential signals, little to no current flows through the ground path. The currents produced by the two signal components should typically be equal in magnitude and opposite in polarity. As a result, the two currents cancel each other out in the ground loop, creating an appearance that no current is flowing through either component [**25**]. Differential signals are also largely immune to discrepancies in ground planes. Any discrepancy between a transmitter's ground and a receiver's ground will be cancelled out in a differential signaling scheme, thus rendering it a non-issue.

Lastly, differential signal systems provide double the dynamic range compared to a single ended system with equal signal swing. A signal ended system with a 5V range can only swing between

±2.5V, assuming a 2.5V virtual ground. A differential signal on the other hand, can swing between ±5V since $\pm 2.5 - \pm 2.5 = \pm 5$.

Increased dynamic range is important because it allows for an ADC to accept a larger range of input signal without increasing the supply voltage, which can be valuable assuming resolution is not critical. To achieve equal dynamic range in a single ended system, the voltage rails of the ADC as well as the signal would have to be increased resulting in more power dissipation. Although in some cases this may not be a concern, many of today's ADC applications are for mobile applications where power is a precious resource.

A third signaling scheme is pseudo-differential signaling. Like a differential ended input scheme, a pseudo-differential input scheme contains two signal inputs. Pseudo-differential ADC inputs only sample a single input. The second input is connected to ground during the hold time to help eliminate noise common to the signal and ground [**22**]. Similar to fully differential signals, pseudo-differential signal schemes allows for common mode ground signals to be eliminated. However, they do not reduce any dynamic noise introduced into the signal path [**22**]. Pseudo-differential signals are typical used in applications where a single ended signal is DC-biased to a certain level [**22**].

2.2 ADC PERFORMANCE METRICS

Aside from resolution and sampling rate, other performance specifications must be considered to properly match an analog-to-digital converter to an application. In cases where AC performance is most critical, a designer might select an ADC based on dynamic range, signal-to-noise ratio, or distortion levels; whereas the integral and differential non-linearities are the most important DC

errors. An understanding of these terms is vital to properly selecting and evaluating ADCs, so these performance metrics will be discussed in this section. For the AC analysis, a foreknowledge of the Fourier Transform is assumed and is not detailed here – interested readers are directed to the Stanford University's freely available textbook on the subject [**26**].

2.2.1 Dynamic Range (DR)

Dynamic range (DR) is a representation of the range of input signal levels that can be measured, and is used to quantify the ADC's ability to detect small signal changes in the presence of large amplitude signals [**27**]. Ideally, this simplifies to the ratio of the full scale range and the noise floor of the ADC, since smaller signal changes would merely appear as noise.

$$DR = 20 \log \frac{V_{FSR}}{V_{Noise}} \tag{8}$$

Since Equation (8) is only true if the ADC has sufficient resolution to have different output codes for V and V + V_{Noise}, the equation for the theoretical maximum signal-to-noise ratio is often added so that bit-count is incorporated [**28**].

$$DR = \min \begin{cases} 20 \log \frac{V_{FSR}}{V_{Noise}} \\ 6.201 * N + 1.763 \end{cases} \tag{9}$$

More practically, dynamic range can be assessed by calculating the spurious free dynamic range (SFDR). When a pure sinusoid is applied as the input to an ADC, the output FFT will show several peaks at non-fundamental frequencies. These spurs can occur at harmonics of the input or can be caused by noise or distortion from the ADC circuitry [**18**]. The highest magnitude spur on

the FFT is chosen as the "smallest input signal" for the dynamic range equation, since smaller signals would be blocked by the spurious tone.

$$SFDR = 20\log\left(\frac{V_{FUND}}{V_{SPUR}}\right) \tag{10}$$

The SFDR value is most informative when it is known whether it was calculated with $V_{FUND} = V_{FSR}$ (decibels against full-scale, or dBFS) or if $V_{FUND} < V_{FSR}$ (decibels against carrier magnitude, dBc) [**29**]. Different manufacturers use different standards in their datasheets, but SFDR remains a relevant metric regardless of the unit. The various spurious free dynamic ranges are illustrated in Figure 15. High dynamic range and SFDR is particularly important in communications applications, where a weak received signal must be captured alongside a much stronger transmitted signal [**27**].

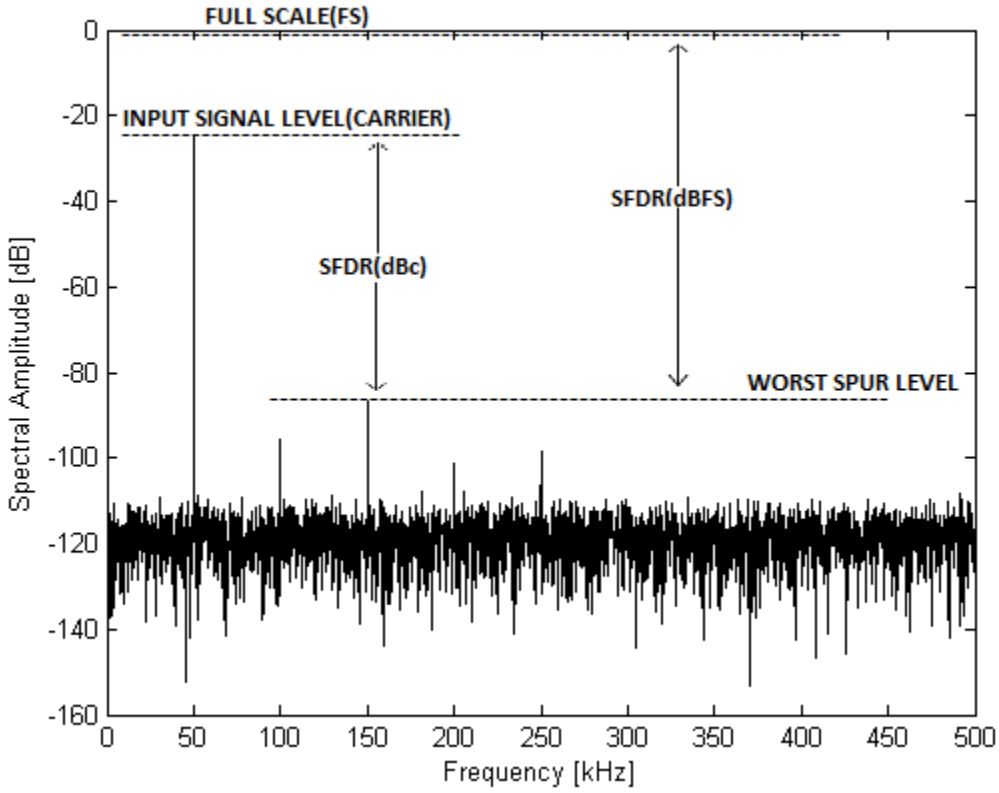


Figure 15: Spurious Free Dynamic Range on FFT Measured in dBc and dBFS [18]

2.2.2 Signal to Noise and Distortion Ratio (SINAD)

Signal to Noise and Distortion Ratio is the ratio of the signal amplitude (measured in V_{RMS}) to the averaged value of all other spectral components except DC (also measured in V_{RMS}) [**27**]. SINAD is usually considered a very good indication of signal strength because all sources of noise and distortion are included in the calculation.

$$SINAD = 20\log\frac{V_{SIGNAL}}{V_{NOISE} + V_{DISTORTION}} \tag{11}$$

The noise and distortion components are included up to the edge of the first Nyquist band at ½ f_S [**27**]. Distortion refers to the elevated strengths of the fundamental's harmonic overtones, and is caused by nonlinearities in the ADC's internal circuitry. Similar to dynamic range, SINAD can

be expressed either in terms of decibels against carrier (dBc) or decibels against full-scale (dBFS) depending on whether the absolute fundamental is used as the reference or the power of the fundamental is extrapolated to the converter's full-scale range.

The theoretical maximum SINAD of an N-bit ADC can be calculated from Equation (11) [**27**]. The equation assumes that the ADC does not cause any distortion of the input signal and the only sources of noise come from quantization error [**30**].

$$SINAD_{MAX} = 6.021 * N + 1.763 \quad (12)$$

Here, the bit-count of the ADC is apparent and the seemingly arbitrary constants arise from the analysis and integration of the quantization noise signal [**30**]. If a digital filter is used to cut out noise past the maximum frequency of interest f_{MAX}, there is an added factor in the equation that is called the processing gain [**30**].

$$SINAD_{MAX} = 6.021 * N + 1.763 + 10 \log \frac{f_S}{2f_{MAX}} \quad (13)$$

The factor $10 \log \frac{f_S}{2f_{MAX}}$ shows that SINAD improves as the sampling frequency f_S is increased above the minimum Nyquist rate of $2f_{MAX}$. This is the result of the finite amount of quantization noise being spread out to $f_s/2$, thus reducing the amount of noise from DC to f_{MAX} [**27**]. This concept of noise-spreading is a key part of the operation of Σ-Δ converters, and is illustrated for that context in Figure 16.

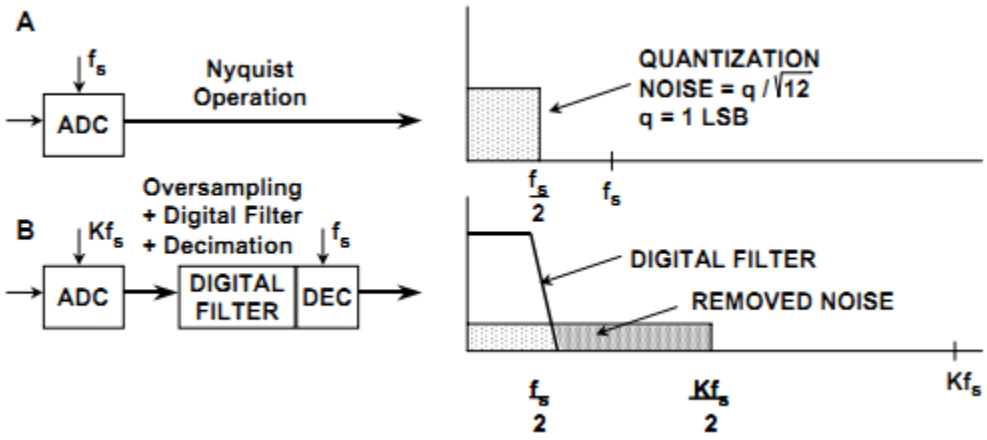


Figure 16: Noise Spreading in Σ-Δ Converter [18]

The reduction of noise in the first Nyquist band via noise-spreading pushes the noise floor down as seen in Figure 17.

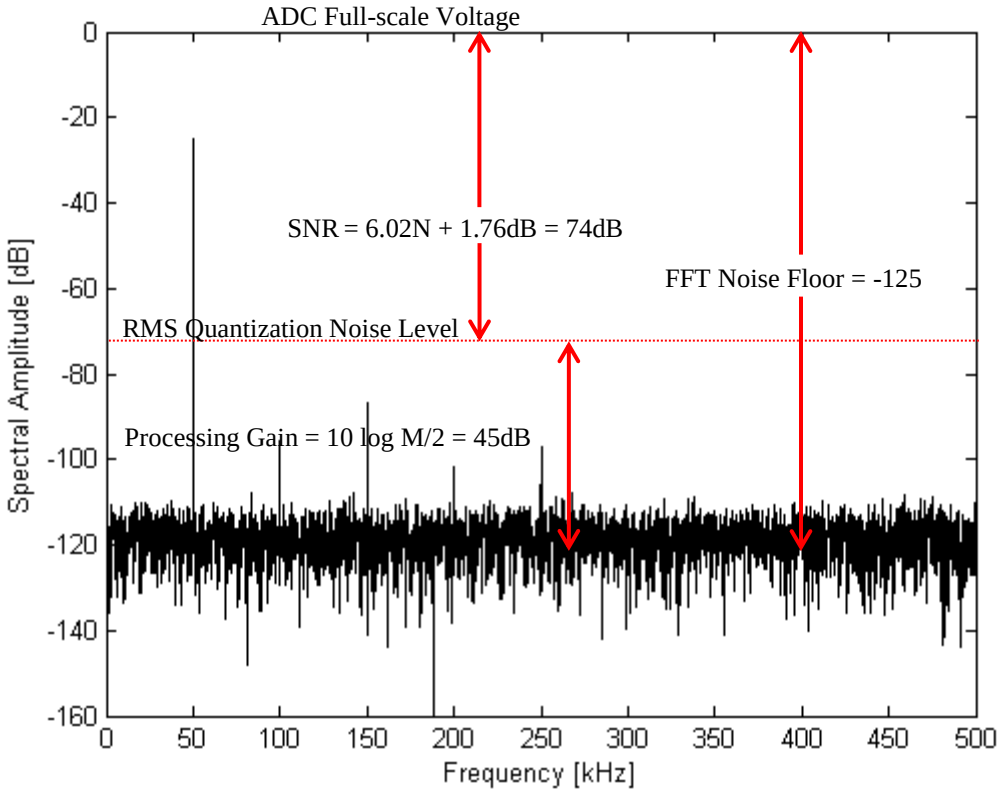


Figure 17: Example Relation between SNR, Noise Floor, and Processing Gain. N=12, M=65536 [18]

In most scenarios no digital filtering is used to suppress out-of-band noise such that the SINAD extends from the full scale range to the quantization noise level. This does not match the visual noise floor, which will have been pushed below the quantization noise level by the processing gain. If filtering is utilized, then the maximum theoretical SINAD is equal to the full dynamic range from the full scale level to the FFT noise floor.

2.2.3 Signal to Noise Ratio (SNR)

Signal to Noise Ratio (SNR) is very similar to the SINAD – it is an evaluation of the signal strength over the existing noise. However, unlike SINAD, the signal-to-noise ratio does not include the harmonic distortion in the calculation and only focuses on noise. Formally, SNR is the ratio of the signal amplitude (measured in V_{RMS}) to the averaged value of all other spectral components except DC and harmonic overtones (also measured in V_{RMS}) [**27**].

$$SNR = 20 \log \frac{V_{SIGNAL}}{V_{NOISE}} \tag{14}$$

In practice, only the first five harmonics of the fundamental frequency are excluded from the SNR equation; after this point the harmonics' amplitudes are so attenuated they have negligible impacts on the SNR value [**27**]. If an ADC is ideal and causes no distortion on the input signal, the SNR would be equal to the SINAD. This results in equations for the maximum theoretical SNR that match the ideals for SINAD. As before, the processing gain factor of Equation (16) increases the SNR provided that digital filtering is used to cut off out-of-band noise after oversampling.

$$SNR_{MAX} = 6.021 * N + 1.763 \quad (15)$$

$$SNR_{MAX} = 6.021 * N + 1.763 + 10 \log \frac{f_S}{2f_{MAX}} \quad (16)$$

Noise sources exist aplenty and creating a noise free system is impossible, making SNR an important design parameter for engineers to ensure optimal system performance.

2.2.4 Effective Number of Bits (ENOB)

The Effective Number of Bits (ENOB) indicates how many bits of the output code are meaningful data. In a system with significant levels of noise, the least significant bits may be changing from a time-variant noise signal and not truly represent a changing input signal [**31**]. ENOB is not a physical parameter of an ADC, but rather a re-arrangement of Equation (15) for the bit-count N:

$$ENOB = \frac{SINAD_{MEASURED} - 1.763 + 20 \log \frac{V_{FSR}}{V_{IN}}}{6.021} \quad (17)$$

A correction factor is added since the SINAD may not be measured with $V_{IN} = V_{FSR}$ [**32**]. ENOB is negatively affected by the same causes of poor SINAD – noise from electromagnetic interference, noise from poor grounding, distortion introduced by the ADC, and the effects of overdriving the filter op-amps to name a few. ENOB can usually be improved by enabling the system to handle noise better, and highlights the fact that increasing the advertised bit-count without simultaneously reducing noise is merely a waste of power and money.

2.2.5 Total Harmonic Distortion (THD)

Total Harmonic Distortion (THD) characterizes the ratio of the sum of the harmonics to the fundamental signal as seen in Equation (18). Note that unlike SNR and SINAD, the input signal strength is in the denominator of the logarithm, so THD improves as it becomes increasingly negative. Typically – for the same reasons as with SINAD – only the first five harmonics are included in the calculation [**27**].

$$THD = 20\log\frac{V_{HARMONICS}}{V_{SIGNAL}} \tag{18}$$

THD is also expressed in terms of dBc or dBFS depending on how it is calculated, and is an important specification in geophysical applications [**33**]. The ideal maximum THD would approach -∞ dB as $V_{HARMONICS}$ diminishes. Since quantization noise is ignored in the THD calculation, there is no finite value to converge to [**27**].

The total harmonic distortion is the third essential dynamic performance parameter along with SNR and SINAD. Given two out of the three, the missing value can be computed given some mathematical manipulation.

2.2.6 Differential Non Linearity (DNL)

Although dynamic performance is often paramount in ADC selection, DC performance characteristics of ADCs, such as differential and integral non linearity, can be just as vital for many applications. The output of an ideal ADC is divided into 2^N uniform steps of equal width. Differential Non-Linearity (DNL) is the maximum deviation from the ideal step width for a

given code bin. Measured in terms of Least Significant Bit (LSB), DNL is a function of an ADC's architecture and its effects cannot be removed with calibration. [**34**]

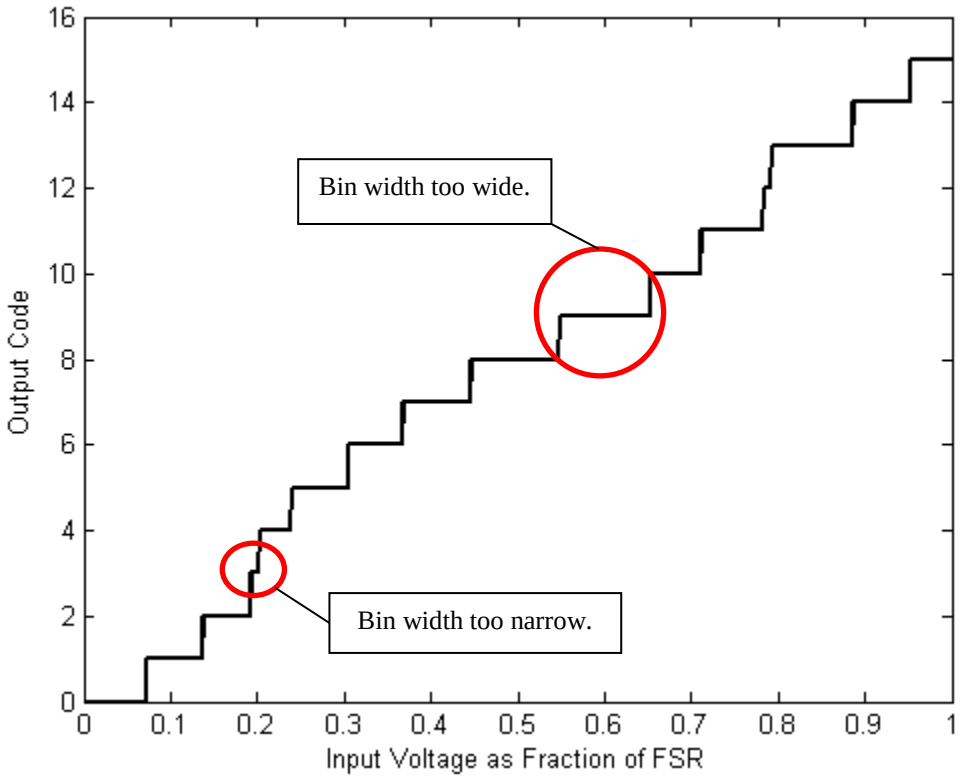


Figure 18: Example of DNL Errors [35]

DNL can be observed when the input signal is set to a linear ramp across the full-scale range of the ADC. Figure 18 shows the resulting transfer function of input voltage to output code, with examples of DNL marked with red circles. The widths of the circled steps are greater or smaller than the other steps, but are only easy to identify visually on low-resolution transfer functions. As the bit-count rises and the bin width narrows, identifying DNL becomes much more difficult.

An alternate method for finding the DNL is to change the input signal from ramp to a full-scale sinusoid. The distribution of the output codes should mimic the plot of the probability density

function (PDF). The PDF of a sine wave $V = A \sin \omega t$ is given by Equation (19), and graphed in Figure 19.

$$PDF = \frac{1}{\pi\sqrt{A^2 - V^2}} \tag{19}$$

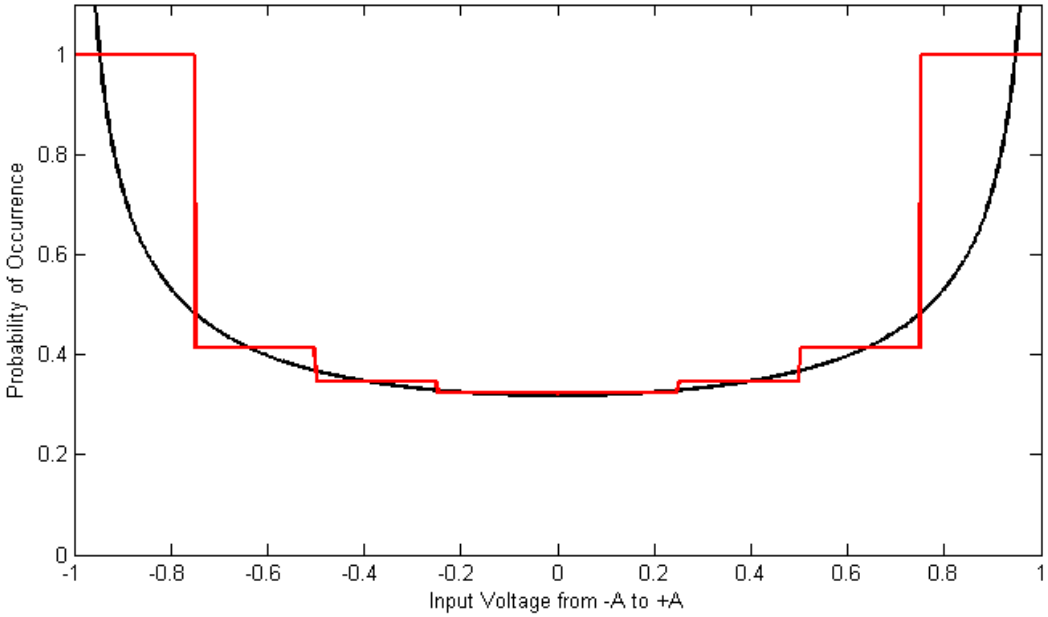


Figure 19: Sine Wave Probability Density Function with Output Code Distribution for N=3 [35]

For the output codes to statistically approach the smooth shape of Figure 19, a very high number of points must be taken during the measurement. At a 99% confidence level, Equation (20) relates the number of required samples M, the ADC resolution N, and the desired precision of DNL values β [**36**].

$$M = \frac{6.636\pi * 2^{N-1}}{\beta^2} \tag{20}$$

To measure the DNL of a 16-bit ADC to within 0.1 LSB, over 2^{26} samples would have to be taken. An example histogram seen at the output of a lower resolution ADC is given in Figure 20. Although the waveform closely resembles the curve of Figure 19, there are still some discontinuities and aberrant heights. The discontinuities are the result of DNL and can be used to calculate the DNL of the n^{th} code using Equation (21) [**37**].

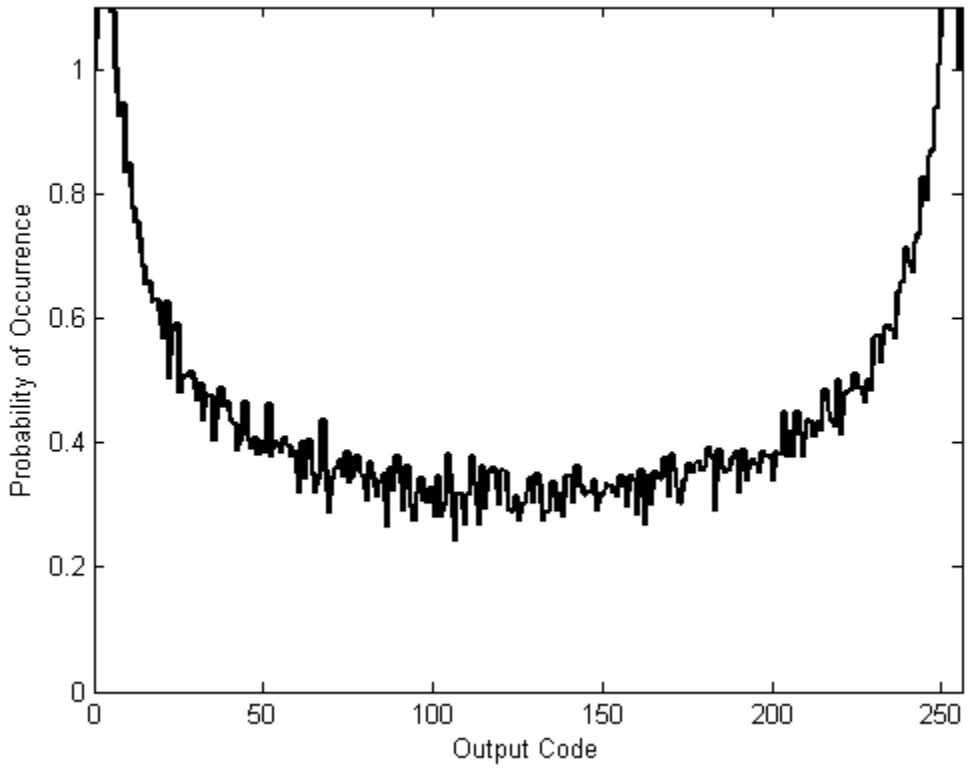


Figure 20: Output Histogram of a Sine Wave Input for N=8 [37**]**

$$DNL = \frac{Actual\ P(n^{th}\ code)}{Ideal\ P(n^{th}\ code)} - 1 \qquad (21)$$

In this equation, Actual P(n^{th} code) is the measured probability of the occurrence for code bin n and Ideal P(n^{th} code) is the ideal probability of occurrence for code bin n.

2.2.7 Integral Non-Linearity (INL)

Integral Non-Linearity (INL) is defined as the deviation of the actual ADC code centers from the code centers of the ideal transfer function. Measured in LSBs, it is a measure of an ADC's accuracy and is a function of the ADC's construction and cannot be calibrated away [**34**] [**38**].

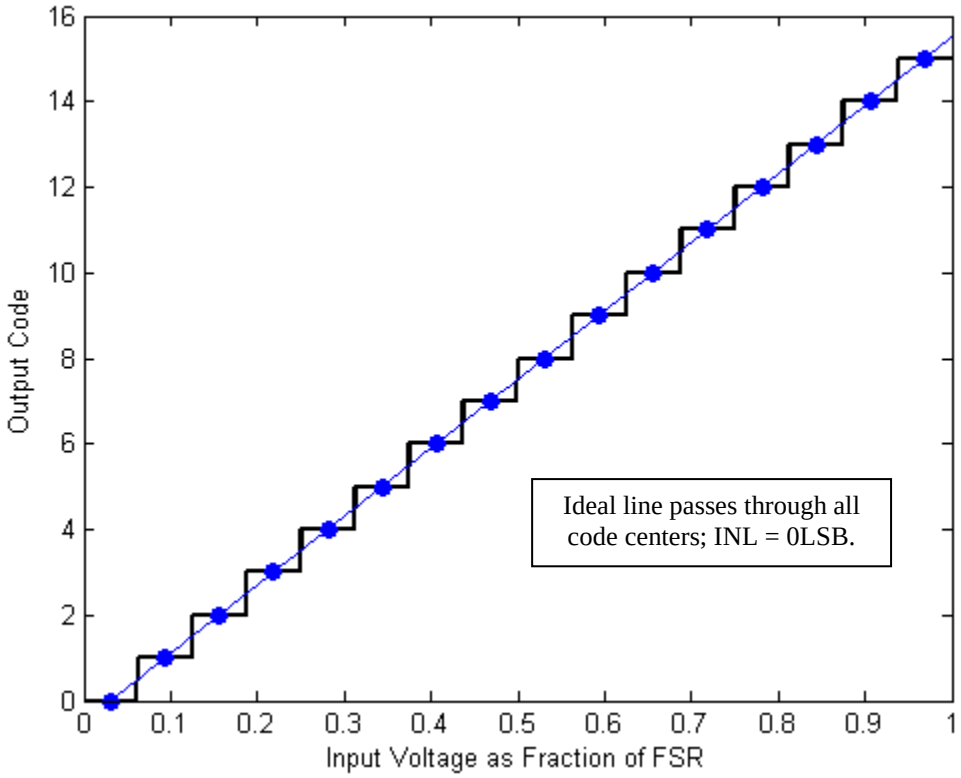


Figure 21: Ideal Transfer Function with INL Line [37]

For an ideal transfer function (shown in Figure 21) the code centers all lie on the ideal regression line. However, practical ADCs have variation in the bin widths as discussed earlier for DNL. This skews the locations of the code centers and is demonstrated in Figure 22.

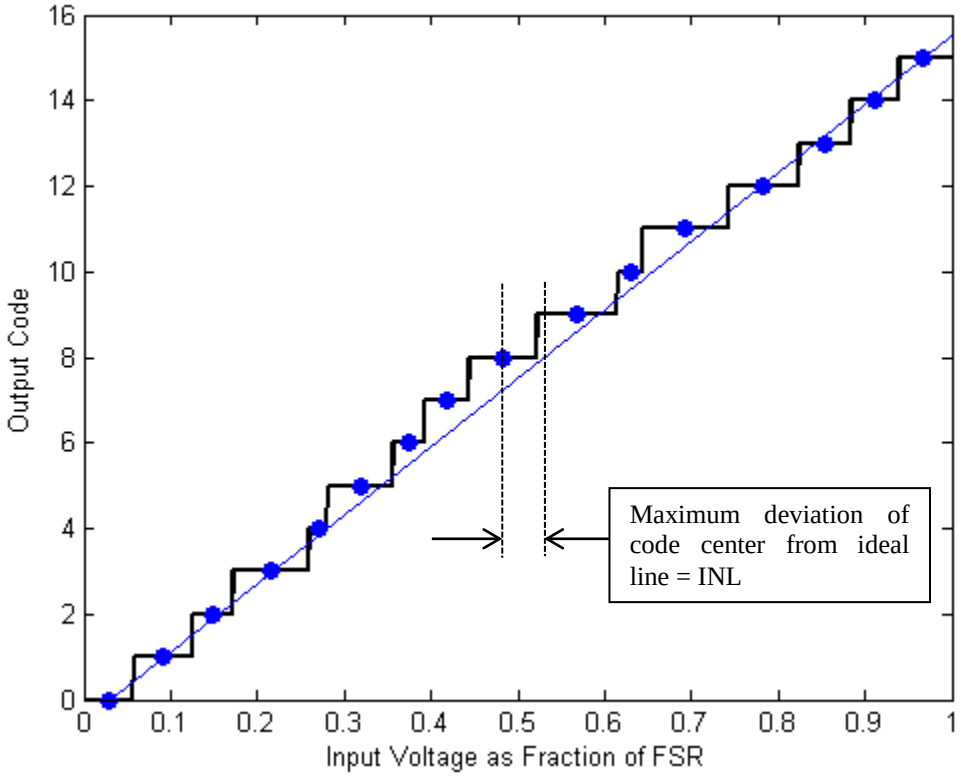


Figure 22: Code Center Errors Result in INL

INL is quantified in one of two ways: either as the maximum distance of a code center from the ideal line of Figure 21, or as the maximum distance of the code center from the best-fit regression line. The second measurement method will always yield a more optimistic value, and it is not always clear which method is used by datasheet publishers.

2.3 ADC Support Circuitry

As with many different parts, ADCs require support circuitry to properly function. An understanding of the purpose of these parts and how their selection affects ADC performance is integral to proper ADC design. Poorly chosen support circuitry can produce much unwanted behavior such as degraded performance or even damage to parts they interact with.

2.3.1 Sample-and-Hold Circuit

Sample-and-hold amplifiers (SHAs) are an integral part of many ADCs. The performance of the SHA is critical in the dynamic performance of an ADC. The purpose of the SHA is to track the input signal until a conversion is ready to be made. At this point the SHA must hold the voltage to within 1 LSB of the ADC so that a successful conversion can take place. Traditionally an SHA contains four parts: an input amplifier, an energy storage device, an output buffer, and some switching circuitry [**39**].

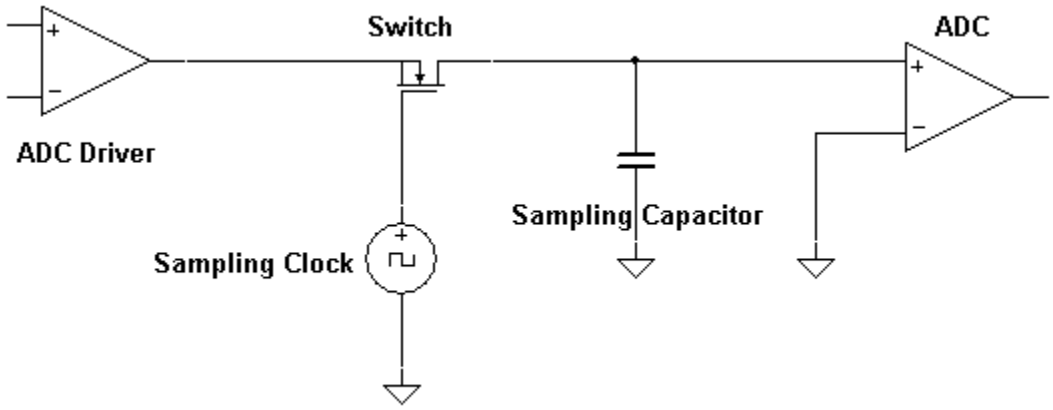


Figure 23: Basic Sample-and-Hold Block Diagram

In this setup the input amplifier acts to present high impedance to the signal as well as current gain to help charge the capacitor. When tracking, the switch is closed, and the capacitor charges to the input voltage. In the hold mode the switch is opened and the voltage presented by the capacitor to the output buffer stays constant. The output buffer is high impedance so that the capacitor cannot discharge prematurely, thus corrupting the ADC conversion. Although the system is oversimplified, it contains the basic building blocks of a typical SHA.

2.3.2 Voltage References

Voltage references are an important part of any analog system. A voltage reference impacts the performance as well as accuracy of a system. Due to this, choosing an appropriate voltage reference is crucial to coercing maximum performance out of devices such as ADCs, which often use precision voltage references for the internal DAC. When selecting voltage references it is recommended to select a reference that closely approaches the required value and accuracy to minimize external trimming and scaling. However, for high resolution applications the reference should not vary by more than ½ LSB (see Equation (21)) and such precise accuracies are difficult to achieve.

$$A = \frac{V_{REF}}{2^N} \tag{22}$$

For example, a 16-bit ADC with a theoretical reference voltage of 5V would require a 76.3µV accuracy, which corresponds to ±0.00153%. Even extremely accurate references are only accurate to ±0.01% [**18**].

The difficulty in obtaining such an accurate reference voltage has led to a shift in thinking: rather than pursuing exactly 5V (for instance), voltage references are now made to be as constant as possible regardless of changing conditions. An error in the initial value (perhaps it is 5.05V) can be compensated for in a digital processing stage, provided that the reference is very stable at that initial value [**18**].

The change in a voltage reference's output due to time and temperature changes is called drift. Drift is typically specified in parts per million (ppm). To obtain the required ppm the following

equation can be used, w here T_C is the temperature coefficient and ΔC is the temperature range in degrees Celsius [**40**]:

$$T_C = \frac{\frac{1}{2^{N+1}}}{\Delta C} \tag{23}$$

Another important consideration of voltage references is the noise they produce. Noise density is typically specified in nV/√Hz. This peculiar unit arises from a desire to express noise in terms of wideband root mean sum (RMS). Volts are used as the noise unit, and hertz are used for the wideband bandwidth. The square root comes from the definition of the RMS. The required noise voltage spectral density to avoid loss of accuracy can be calculated using Equation (24) [**18**]:

$$E_N \leq \frac{V_{REF}}{12 * 2^N * \sqrt{BW}} \tag{24}$$

where V_{REF} is the reference voltage, N is the number of bits, and BW is the bandwidth of the system. For example, for a 16-bit system with a reference voltage of 5V and a BW of 250 kHz the spectral density requirement would be 12.72 nV/√Hz. This number is much smaller than a typical reference's spectral density of 100 nV/√Hz [**18**], so the example system would require additional filtering on the output to further reduce noise. The 2^N factor in Equation (24) causes most high resolution systems (high N) to need extremely low noise and require output filtering on their references.

2.3.3 ADC Drivers

Choosing the input driver for an ADC can have a prodigious effect on its performance. When choosing the proper driver for an ADC it is important to note that different ADCs require

different input drivers, and that some do not require any sort of input driver at all. Typical functions of an ADC input driver include amplitude scaling, single ended signal to differential signal conversion, signal buffering, common-mode offset adjustment, and filtering. Each of these processes plays a role in coaxing maximum performance out of an ADC.

The SNR due to an ADC driver should be greater than that of the ADC itself so that it does not limit the ADC performance. This value can be calculated by using Equation (25) [**41**]:

$$SNR = 20\log\frac{V_{rms}}{\int_0^{\sqrt{BW}} V_n} \tag{25}$$

Where V_{RMS} is the RMS voltage of the input signal, BW is the bandwidth of the driver or any limiting filter, and V_N is the noise spectral density of the driver. Unsurprisingly, ADC analog inputs are not ideal. They have finite complex input impedance capable of producing transient currents. The external driver is used to help isolate the signal source from these transient currents, and thus it must be able to settle in a time less than half the sampling clock period. Typically the bandwidth of the driver is high in comparison with the ADC to help reduce distortion products. As a trade-off though, this means that additional filtering may be required between the driver and the ADC to satisfy Equation (25).

It is also important to note that care must be taken to avoid issues arising at the input of an ADC driver. When working with ADC drivers it is also important to note that resistive networks should be used to match the ADC driver input to the transmission line impedance. In differential systems this is fairly straightforward, whereas with singled ended inputs additional consideration must be taken to also balance the driver's inputs. [**42**].

2.4 Power Supplies

In today's industry options for designing power supplies are plentiful. Many of today's power IC designers produce programs to alleviate the process of power supply design. Even so, a basic understanding of power supply design can greatly improve the performance of a power supply. The following section introduces basic concepts of several power regulation topologies considered in this project.

2.4.1 Low Dropout Regulators

A low dropout (LDO) regulator is one topology of linear regulators. LDO regulators are defined by their ability to provide a given output voltage while requiring a minimum input voltage that is, as its name suggests, not much larger than the output voltage. The basic architecture of an LDO regulator consists of a closed loop system composed of four components: a voltage reference, a feedback voltage divider, a pass transistor, and an error amplifier, seen in Figure 24 [**43**].

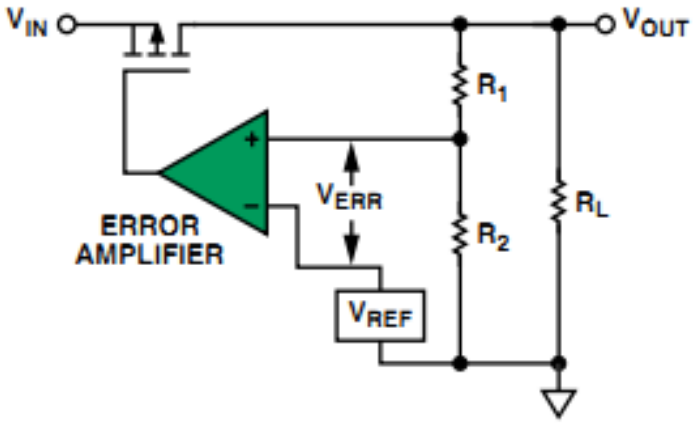


Figure 24: Architecture of a Basic LDO Regulator [43**]**

The pass transistor provides the output drive current for the load, and the drop across the transistor terminals equals the dropout voltage. A fraction of the output voltage is compared to a reference voltage by the error amplifier. The output of the error amplifier controls the pass transistor, pulling the gate of the transistor higher or lower depending on the swing of the error [**43**]. This resultant voltage swing causes more or less current to flow through the transistor resulting in a higher or lower voltage at the feedback voltage divider and output [**43**].

Datasheets for LDO regulators contain many specifications applicable to part selection. Input voltage range specifies the allowable range of V_{IN} that should be adhered to during operation. This specification, along with dropout voltage, is paramount in determining the proper LDO for a given application. Dropout voltage, V_{DO}, is defined as the minimum difference between V_{IN} and V_{OUT} of an LDO regulator [**43**].

$$V_{IN} \geq V_{OUT} + V_{DO} \tag{26}$$

Although these two terms are the general starting point when designing with LDO regulators, there are many other important specifications as well, including: output voltage accuracy, line regulation, and dynamic line (load) regulation. Output voltage accuracy is a measure of how accurate a given regulator is. For example, a 5V LDO regulator with an output voltage accuracy of 0.1% can be expected to produce anywhere from 4.95V to 5.05V. Line regulation, typically specified in mV/V, is a measure of how output voltage is affected by changes in input voltage [**43**]. Load regulation, specified in mV/mA, relates the voltage change seen at the output for a change in load current [**43**]. An analysis of these parameters in worst case scenarios can determine whether an LDO regulator will provide sufficient regulation in a given environment.

LDO regulator datasheets also define several parameters pertaining to noise. Output noise specifies how much noise can be expected on the regulated output. Typically specified in μV_{RMS}, output noise typically originates from noise at the LDO input. The Power Supply Rejection Ratio (PSRR) is a measure of how much the input voltage noise is attenuated [**44**]:

$$PSRR = 20 \log\left(\frac{V_{RIPPLE(INPUT)}}{V_{RIPPLE(OUTPUT)}}\right) \quad (27)$$

For other analog circuitry, such as ADCs, this parameter can be viewed as how well noise on the power supply is decoupled from the signal path. For example, an 18-bit ADC with a 5V reference would have an LSB of 19.07μV. With a PSRR of 80 dB, any noise on the power lines less than 190.7mV would fall below the quantization noise of the ADC.

Although LDO regulators have their applications, they are limited in their utility. LDO regulators tend to be less efficient than well designed switching regulators. They also are only capable of producing voltage lower and of the same polarity as a given input voltage. To allow for a dynamic power supply, LDO regulators must be used in conjunction with switching regulators.

2.4.2 Switching Regulators

Switching regulators are an important counterpart to LDO regulators in power supply system designs. Switching regulators are more diverse in their capabilities than LDO regulators. They are capable of providing output voltages greater in magnitude than their input, opposite in polarity than their input, and voltages that stay constant regardless of whether the given input voltage is greater or lesser in magnitude than the desired output.

The fundamental component of switching regulators is the inductor. Inductors are favored as the fundamental charge storage devices in place of capacitors because the use of inductors allows output voltages high than the input voltage. To achieve this, switching regulators take advantage of the law of inductance, seen below in Equation (28):

$$V = L\frac{dI}{dt} \tag{28}$$

Equation (28) implies that a voltage drop across an inductor only occurs when the current flowing through the inductor is changing with time. It also implies that the current through an inductor cannot change instantaneously (which would cause an infinite voltage) whereas the voltage across an inductor can [**45**]. The law of inductance itself does not evolve into a switching regulator; a pulse width modulation scheme must be used in conjunction with it to create a switching regulator.

Pulse width modulation (PWM) is a power control technique that varies duty cycle of a digital signal. Duty cycle is defined as the ratio of the high or on time of a signal to the total period of said signal:

$$D = \frac{T_{CLOSED}}{T_{CLOSED} + T_{OPEN}} \tag{29}$$

In switching regulators a PWM scheme is used to control the transfer of energy into an inductor. The PWM signal controls a switch (typically a transistor) which in turn switches the voltage drop seen across the inductor. Illustrated examples of this technique can be found in Section 2.4.2.1 Boost Converters and Section 2.4.2.2 SEPIC Converters, although PWM control is implemented in many switching regulator topologies.

2.4.2.1 Boost Converters

One type of commonly used switched mode regulator is the boost converter. A boost converter takes a given input voltage and outputs a voltage of greater magnitude. A basic boost converter consists of an inductor, a switch, a diode, and a capacitor as seen in Figure 25.

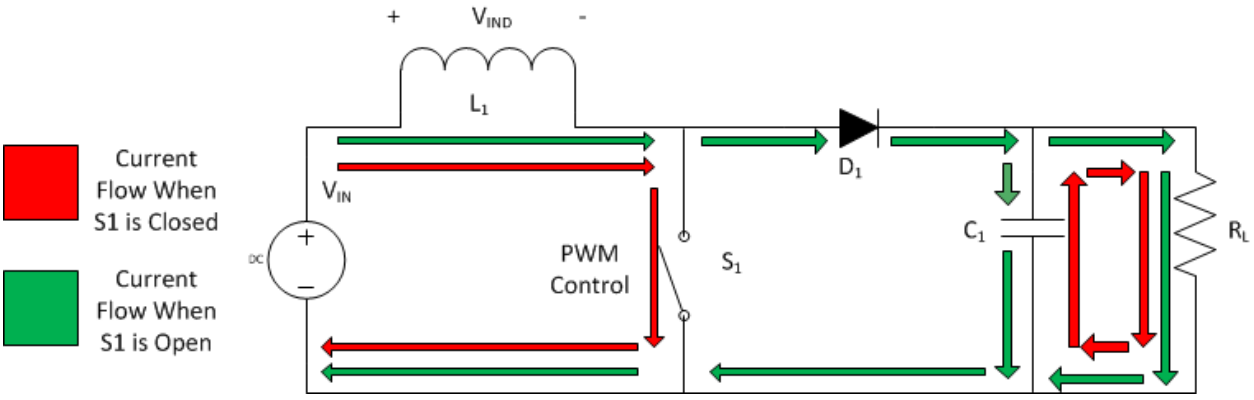


Figure 25: Basic Topology of a Boost Converter with Open and Closed Switch Currents [45]

When operating with DC input voltages the boost converter has two fundamental states: S_1 closed (conducting) and S_1 open (not conducting). When S_1 is closed V_{IN} drops across inductor L_1 causing the current through it to increase linearly as dictated by Equation (28). The current drawn by the load R_L is supplied by the output capacitor C_1 in this state. When S_1 is open the current flowing through inductor L_1 decreases as capacitor C_1 charges; a resultant positive voltage occurs at the diode terminal of the inductor [**45**]. This positive voltage forward biases diode D_1 allowing the capacitor C_1 to charge to a higher voltage than the input voltage V_{IN} [**45**]. In this state inductor L_1 not only charges the capacitor C_1, but it also provides current to the load R_L.

This process can also be described mathematically starting with Equation (28). First, solving Equation (26) for *dI* and integrating both sides of the equations yields:

$$\Delta I = \frac{V\ \Delta T}{L} \tag{30}$$

Where ΔI is the change in inductor current, V is the voltage drop across the inductor, ΔT is the change in time, and L is the inductance of the inductor. Next, the currents during both the closed (switch conducting) and open (switch not conducting) states of the circuit are observed:

$$\Delta I_{ON} = \frac{(V_{IN} - 0)\ T_{CLOSED}}{L} \tag{31}$$

$$\Delta I_{OFF} = \frac{(V_{OUT} - V_{IN})\ T_{OPEN}}{L} \tag{32}$$

Setting Equation (31) and Equation (32) equal to each other and solving for V_{OUT} reveals:

$$V_{OUT} = V_{IN}\ \frac{T_{CLOSED} + T_{OPEN}}{T_{CLOSED}} \tag{33}$$

Equation (33) can be combined with the duty cycle equation to find the dependence of the output voltage on the PWM duty cycle:

$$V_{OUT} = V_{IN}\ \frac{1}{1 - D} \tag{34}$$

The equations derived above assume ideal components and, although useful for comprehension, do not reflect real-world conditions. Resistances in the inductor and diode as well as leakage current from the capacitor would lower the converter's efficiency. The saturation current of the inductor would limit the high end of the output voltage. Figure 26 ignores these inefficiencies to accurately reflect the equations given in Equation (31) through Equation (34).

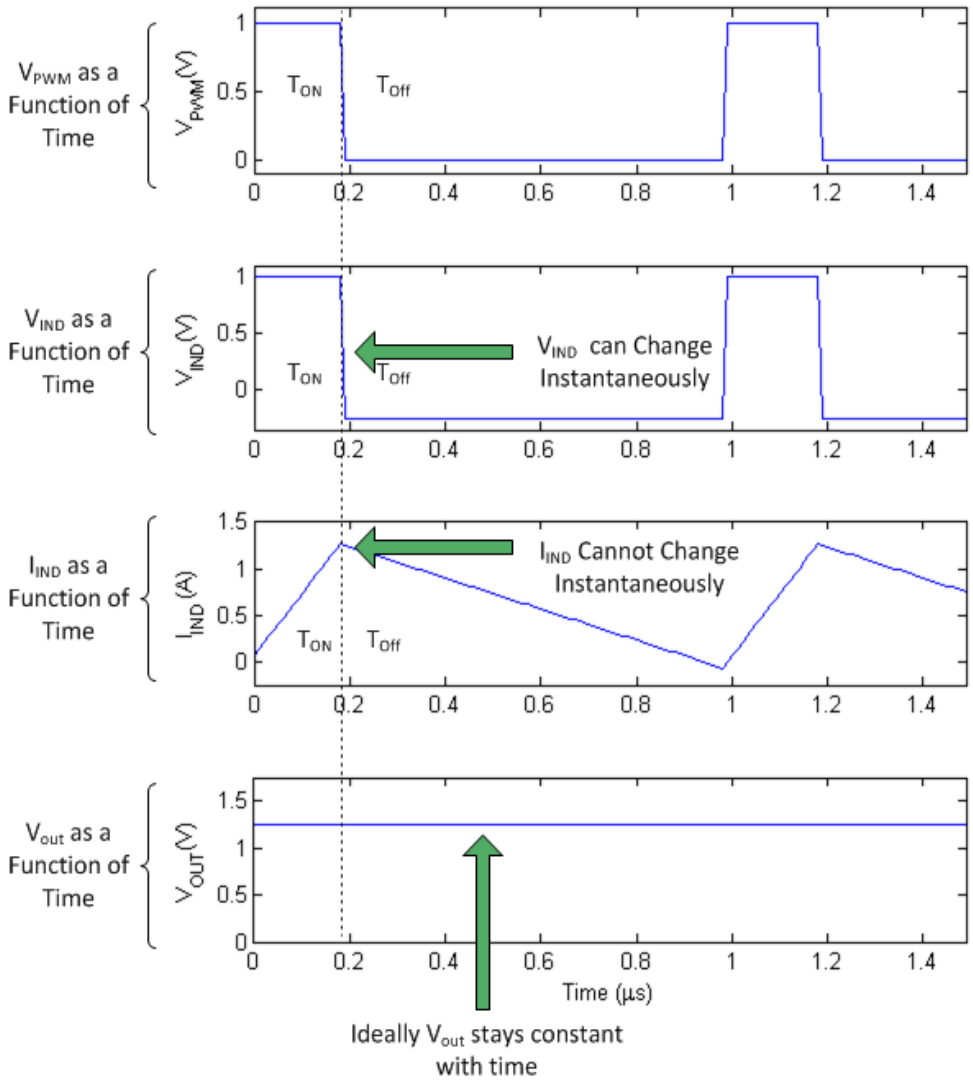


Figure 26: Voltage Analysis of an Ideal Boost Converter

Figure 27 illustrates the effect that changing the duty cycle has on the output voltage of the ideal boost converter in Figure 25.

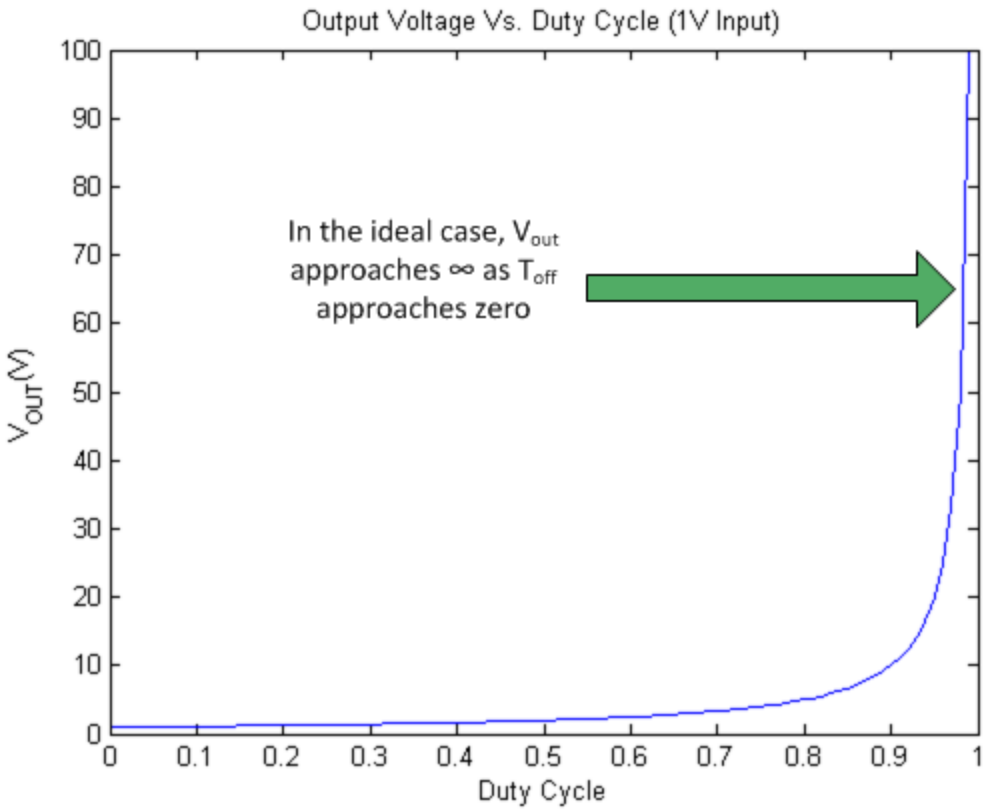


Figure 27: V_{OUT} of an Ideal Boost Converter as a function of duty cycle

Although boost converters are a helpful tool in power supplies, like LDO regulators, their applications are limited; they cannot produce negative voltages or output voltages less than their input voltages. More complicated circuitry, such as the SEPIC and Cùk topologies are required for more these dynamic supply requirements.

2.4.2.2 SEPIC CONVERTERS

A Single-Ended Primary-Inductor Converter (SEPIC) is a switching topology that allows for more dynamic applications than a boost converter. SEPIC converters are capable of proper operation regardless of whether the input voltage is less than, equal to, or greater than the output voltage. The basic SEPIC consists of three capacitors, two inductors, a switch, and a diode, seen in Figure 28 [**46**].

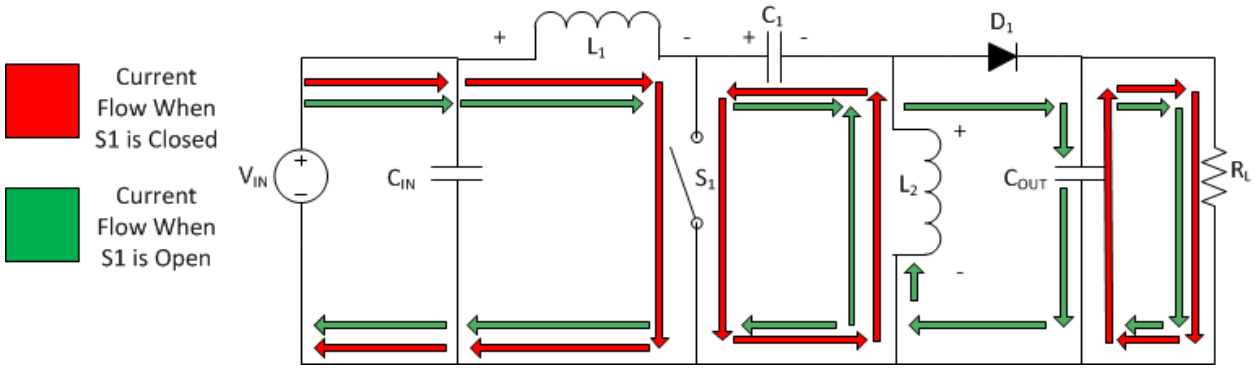


Figure 28: Basic SEPIC Converter Topology [46]

Although this circuit appears daunting, a steady state analysis of the system can ease its understanding. Similar to the boost circuit in Section 2.4.2.1 Boost Converters, the SEPIC configuration has two basic states: S_1 closed and S_1 open. One key component to this analysis is that in a steady state, the voltage across the capacitor C_1 is always V_{IN} [**46**]. Applying Equation (28) to both states of the circuit yields:

$$\Delta I_{L1\ Closed} = -\Delta I_{L2\ Closed} = \frac{V_{IN}\,\Delta T_{CLOSED}}{L} \tag{35}$$

$$\Delta I_{L1\ Open} = -\Delta I_{L2\ Open} = \frac{V_{OUT}\,\Delta T_{OPEN}}{L} \tag{36}$$

Next, Equation (35) is set equal to Equation (36) and solved for V_{OUT}:

$$V_{OUT} = V_{IN}\frac{\Delta T_{CLOSED}}{\Delta T_{OPEN}} \tag{37}$$

Finally, Equation (37) is rearranged to yield:

$$V_{OUT} = V_{IN} \frac{D}{1 - D} \tag{38}$$

The form of Equation (38) makes it clear that varying of the duty cycle D allows a SEPIC converter to swing from an output voltage of 0V to ∞V regardless of the input voltage in the ideal case. Of course, just as the boost converter, imperfections in real parts yield these idealities impossible in application. A SEPIC converter is very sensitive to imperfections in its parts and as a result the selection of parts in a SEPIC converter is an intricate process.

2.4.2.3 Cùk Converters

Another switching topology similar to the SEPIC configuration is the Cùk converter. A Cùk topology contains the same parts as a SEPIC configuration, just connected differently as seen in Figure 29.

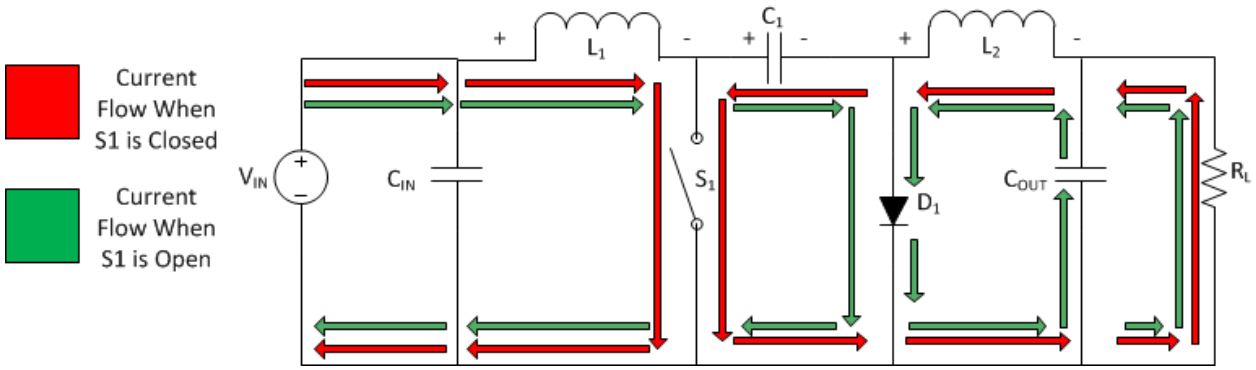


Figure 29: Basic Cùk Converter Topology [46]

A similar analysis can be applied to the Cùk converter, as done in the previous two sections, but has been omitted for brevity. The most important difference of the Cùk topology is that it produces an output voltage opposite in polarity from its input [**46**]:

$$V_{OUT} = V_{IN} \frac{-D}{1-D} \quad (39)$$

Since the two topologies share many commonalities such as inductor currents, duty cycle, and voltage at switch S1, the two topologies can be connected at switch S_1 to create a single converter that creates both a positive and a negative output voltage [**46**]. Like the SEPIC converter selection of parts can be difficult. If more information is desired on this topic, it is suggested that Analog Device's application note AN-1106 is consulted [**46**].

2.5 TIMING PROTOCOLS

Once the ADC has completed a conversion, the resultant digital code must be read from the output terminals and is typically sent to a digital processor. For high performance converters, it is just as necessary to design the data retrieval as it is to design the ADC circuitry itself. The communication interface must have sufficient throughput to handle N-bit words at the sampling frequency, and will usually need some signaling to indicate when the conversion is complete and data is available. For low-resolution ADCs, a parallel interface is occasionally used with one pin per bit -- this is faster than serial solutions, but as the bit-count rises the space and cost associated with parallel communications is prohibitive. Today, most high performance ADCs use serial protocols, and SPI and SPORT are both viable options for the PulSAR ADCs from Analog Devices.

2.5.1 Serial Periphery Interface (SPI)

One of the most prevalent hardware interfaces today is the Serial Periphery Interface (SPI) that was developed by Motorola in the 1980s [**47**]. The protocol features full-duplex communication

between a master device and (possibly multiple) slave devices. A four-signal scheme is used, where SCLK is the serial clock generated by the master to synchronize the data transmissions, Master Out Slave In (MOSI) is used for transmitting data from the master device, Master In Slave Out (MISO) is used for transmitting data from the slave device, and Slave Select (SS) is used to choose between multiple slaves if applicable; these are diagrammed in Figure 30.

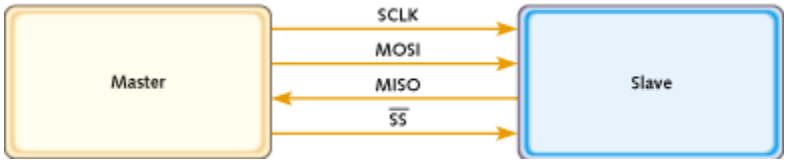


Figure 30: Single-Slave SPI Configuration [47]

One data bit is transferred on the MOSI and MISO lines during each clock cycle – it is up to the master to know if the transmitted/received bit on each line is meaningful or not [**47**]. When idling between words the clock must be gated, and then restarted for the start of the next word [**48**]. This can lead to performance degradation in applications with pauses between each word; ADCs must sit idle during the acquisition time of the sample-and-hold, and the rapid gating can lead to clock inaccuracy. This implies that SPI may not be the best suited communication interface for a high-speed ADC, particularly since the maximum speed of SPI is typically ¼ of the system clock [**48**].

2.5.2 Synchronous Serial Periphery Port (SPORT)

Seeking to improve upon SPI, Analog Devices developed the Synchronous Serial Periphery Port (SPORT) for use with its Blackfin processors and other products. As the name implies, SPORT is only functional for synchronous serial data transfers, and is ideal for high-throughput communication with peripheral devices [**48**]. The SPORT interface is quite configurable: it can

operate at up to ½ the system clock, transmit data words from 3 to 32 bits in length, transmit and receive simultaneously at full performance, and offer primary and secondary data lines to enhance throughput [**48**]. The full duplex operation does require extra data lines, which is a disadvantage over the four-wire SPI interface. An example signal list is shown in Table 1 and demonstrates the dual channel and duplex functionality of a real SPORT module.

Table 1: SPORT Signals for BF527 Blackfin

Pin	Description
DTxPRI	Transmit Data Primary
DTxSEC	Transmit Data Secondary
TSCLKx	Transmit Clock
TFSx	Transmit Frame
DRxPRI	Receive Data Primary
DRxSEC	Receive Data Secondary
RSCLKx	Receive Clock
RFSx	Receive Frame Sync

The data lines DTPRI and DTSEC are synchronized to TSCLK while the DRPRI and DRSEC signals are synchronized with RSCLK, although oftentimes the DxSEC lines are disabled because high throughputs can be achieved with a single data line [**48**]. The frame sync signals TFS and RFS indicate the start of a data word for the transmitter and the receiver, respectively.

There are numerical restrictions placed on the various clock speeds and their ratios. The two serial clocks TSCLK and RSCLK are functions of the main system clock frequency (f_{SCLK}) and a 16-bit integer divider as shown in Equation (40) [**48**]. If f_{SCLK} is 120 MHz the maximum speed of the SPORT clocks is 60 MHz and as the minimum speed is ~915 Hz.

$$f_{TSCLK} = \frac{f_{SCLK}}{2 * (TSCLK_{DIV} + 1)}, \qquad 0 \leq TSCLK_{DIV} \leq 2^{16} - 1 \tag{40}$$

Similarly, the frame sync clock signals TFS and RFS are functions of the SPORT clocks and a 16-bit integer divider as shown in Equation (41) [**48**]. Since the denominator of this equation represents the number of SPORT clock cycles that pass between frame assertions, TFS_{DIV} + 1 should not be less than the desired word length.

$$f_{TFS} = \frac{f_{TSCLK}}{TFS_{DIV} + 1}, \qquad 0 \leq TFS_{DIV} \leq 2^{16} - 1 \tag{41}$$

The values of the clock dividers – along with a multitude of configuration settings – are stored in the SPORT interface registers, and need to be properly initialized in the processor. The behavior of the frame sync signal is particularly complex and is controlled by the register values. The frame sync is typically active-high and triggers on the rising edge, but can be set to pulse immediately before the first bit (normal framing) or remain high for the whole word (alternate framing) [**48**]. The timing diagrams of Figure 31 and Figure 32 show these two timing schemes with a 4-bit word. The framing period is six clock cycles long and the interface achieves 66% throughput for the given RSCLK rate.

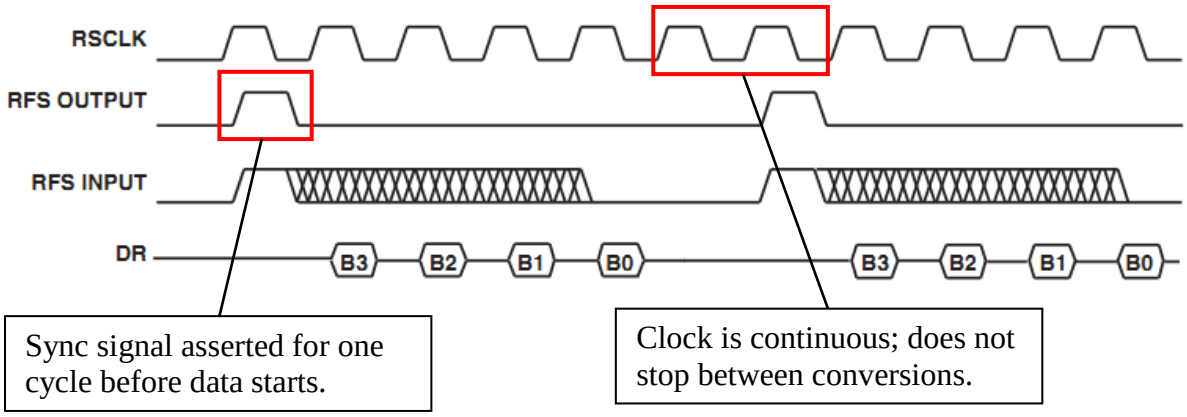


Figure 31: SPORT Timing Diagram with Normal Framing [48]

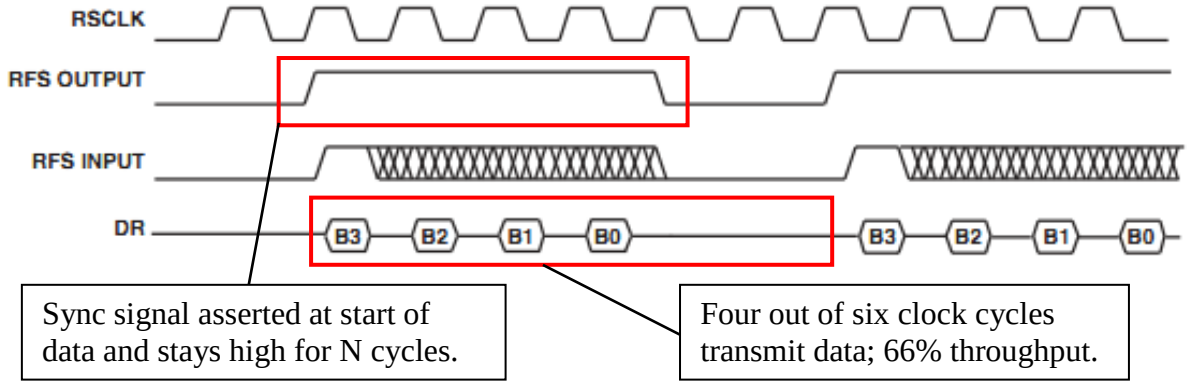


Figure 32: SPORT Timing Diagram with Alternate Framing [48]

For a full description of the SPORT interface's capabilities and configurations, see Analog Devices' hardware manual for the Blackfin processors.

2.5.3 Effect of Timing Jitter on ADC Performance

Proper operation of an ADC depends on the synchronous operation of its individual components. In particular, the switching time of the sample-and-hold amplifier is often overlooked as a source

of error in ADC performance. Termed the aperture time t_a, the SHA takes a finite amount of time to transition between high and low impedance [**49**]. Rather than consider the various nonidealities of the sample-and-hold, it is often easier to consider the aperture time as a delay in the clock signal called the aperture delay t_e – mathematically, these two views are equivalent [**49**].

A constant aperture delay would cause no errors in digitizing the input signal. However, the SHA circuitry is not ideal and there is some variation in the precise time the switch transitions. Typically measured in picoseconds, the aperture jitter causes the input signal to be read at a slightly different position and causes error. The same error results from jitter in the clock source itself or from jitter in the input signal, so the effects are often referred to as merely jitter regardless of the source.

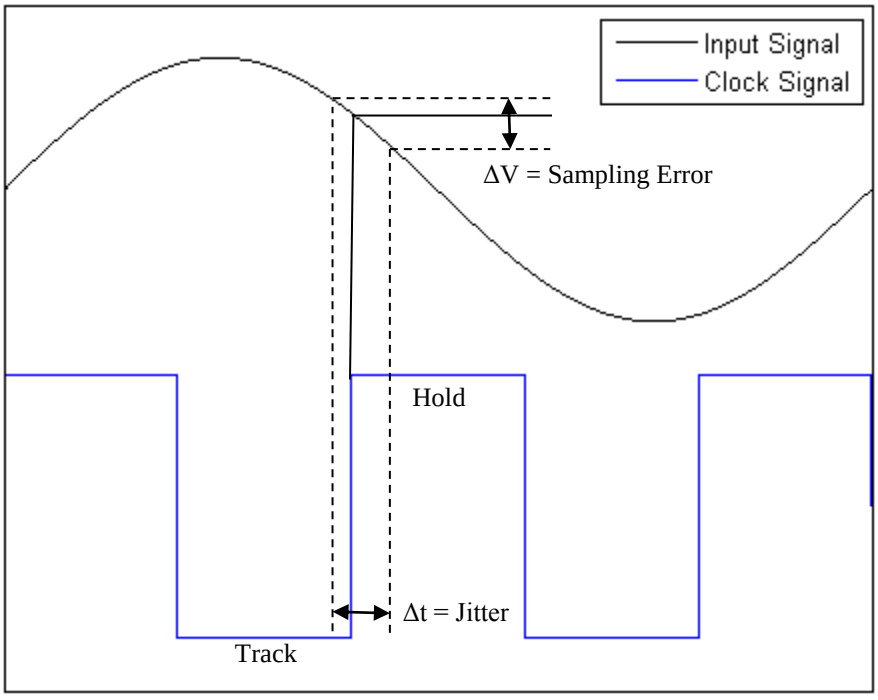


Figure 33: Sampling Error from Clock Jitter [49]

As evident in Figure 33, the magnitude of the sampling error increases as the rate-of-change of the input signal increases. The error can be quantified by taking the derivative of the input signal and multiplying by the total jitter [**49**]. Assuming a sinusoid of amplitude A and frequency *f*:

$$\Delta V = A * 2\pi f * \Delta t \tag{42}$$

If the jitter-induced error is the only source of noise in an ADC with infinite resolution, it becomes the limiting factor for SNR (jitter is rarely the predominant source of error in a circuit, but this clearly demonstrates the impact of increasing Δt).

$$SNR = 20\log\frac{A}{A * 2\pi f * \Delta t} = 20\log\frac{1}{2\pi f\ \Delta t} \tag{43}$$

The plot of Equation (43) shows that SNR falls 20 decibels for every decade increase in the total system jitter.

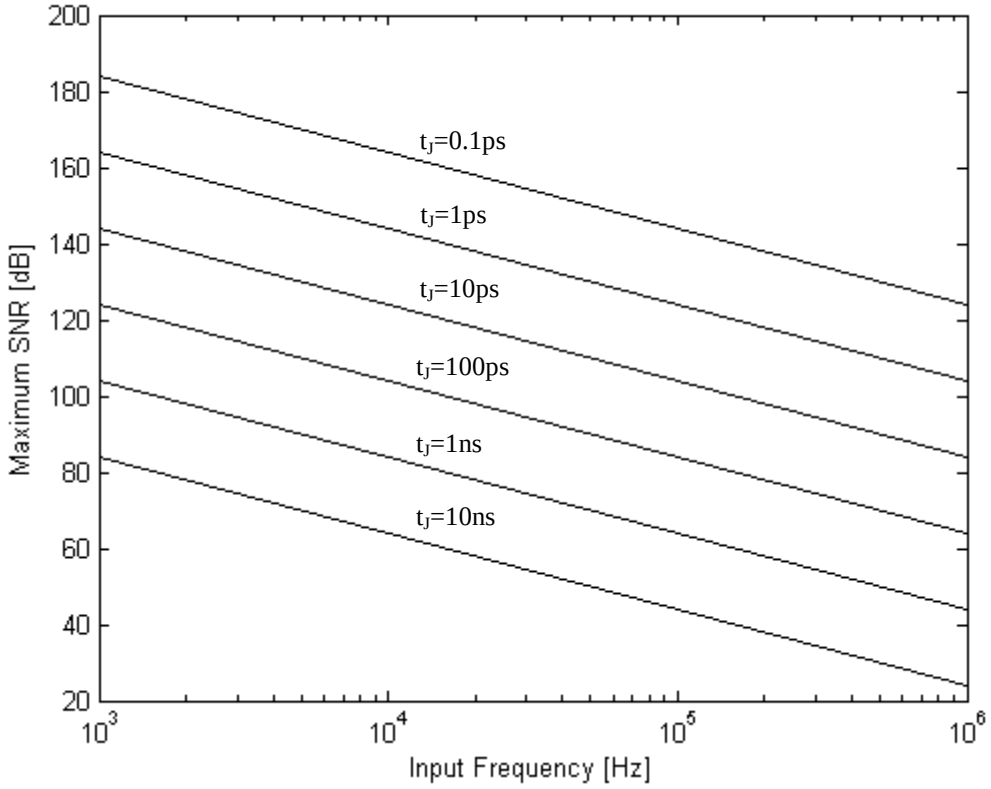


Figure 34: Maximum SNR with Only Jitter Error as Noise [49**]**

2.6 INTERPRETING DIGITAL OUTPUT DATA WITH LABVIEW

Equally important to coaxing maximum performance out of an ADC is being able to process the digital output efficiently. In many cases, component manufacturers will deploy software with the converters that will interpret the serial data stream and display the information in an accessible manner. Analog Devices uses the LabVIEW development environment to create these software packages. LabVIEW is a graphical programming interface developed by National Instruments that allows scientists and engineers to create sophisticated measurement, test and control systems. First released in 1986, LabVIEW uses graphical icons that are interconnected to mimic a flow diagram. LabVIEW also provides users with options to integrate with thousands of

hardware devices and the thoroughness of its built-in and online libraries makes it possible to perform even complex tasks [**50**].

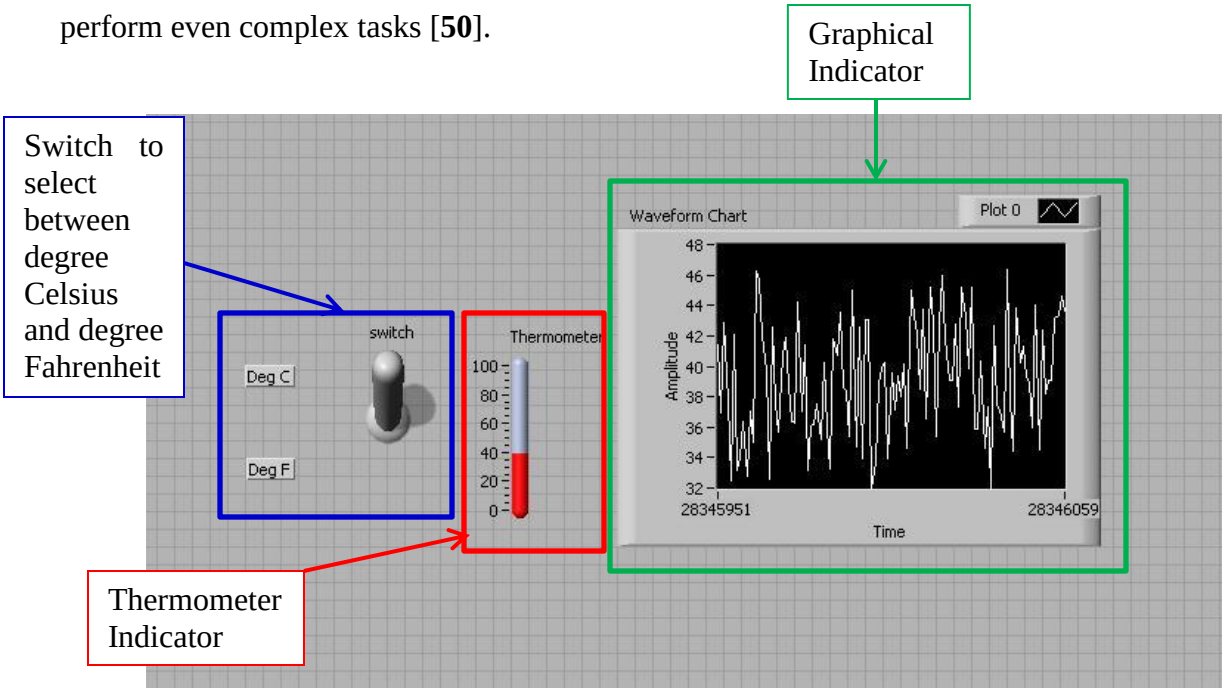


Figure 35: Example LabVIEW Front-Panel for a Thermometer Program

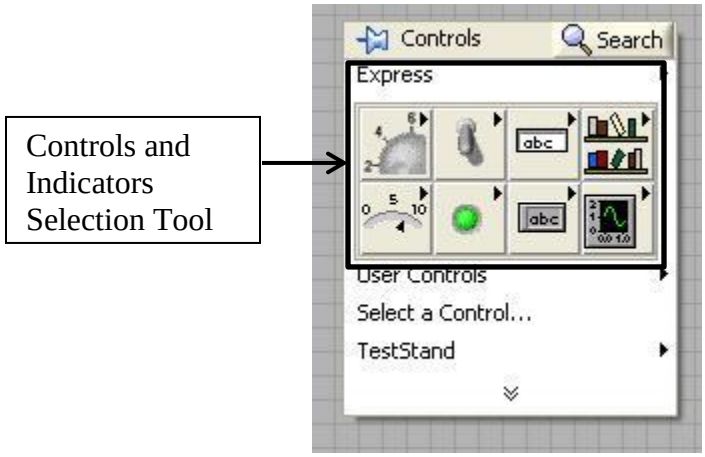


Figure 36: Controls Palette

The software provides a developer with a blank front-panel with a controls-pallet (Figure 35 and Figure 36) at start-up onto which the developer can drag and drop controls and indicators that function as the user-interface for the software. Behind the scenes, the controls and indicators the

programmer makes in the front panel are paralleled in the block diagram, which serves as the "source code" for the LabVIEW programming environment. The user can go to the block diagram view and can connect and manipulate the blocks to implement the desired logic for the software (Figure 37).

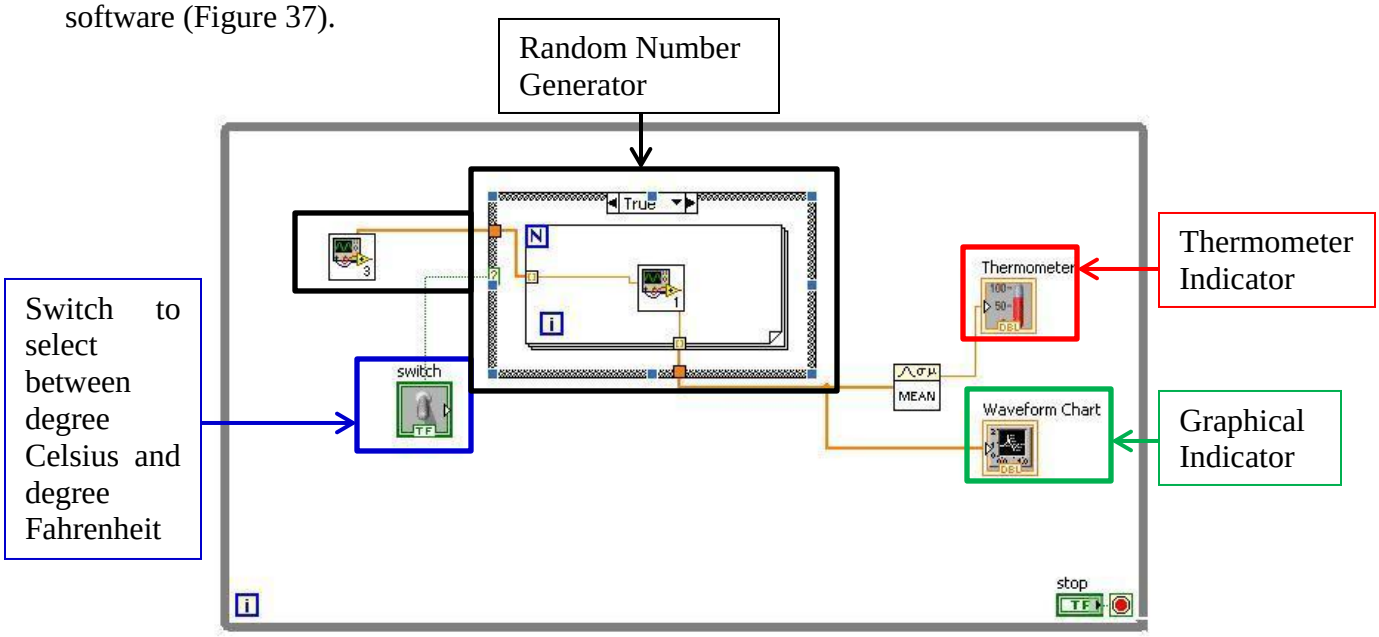


Figure 37: Block-Diagram Associated with the Thermometer of Figure 35

The block-diagram code is very similar to any other code that handles the implementation of an application and is the logical back-bone. The wires connect the various controls, indicators and logical blocks of the application. Just as the controls-pallet provides tools for the front panel, the block diagram comes with a functions-pallet (Figure 38) that provides pre-built logical blocks. LabVIEW automatically detects the type of terminals connected and throws an error if incompatible terminals are connected.

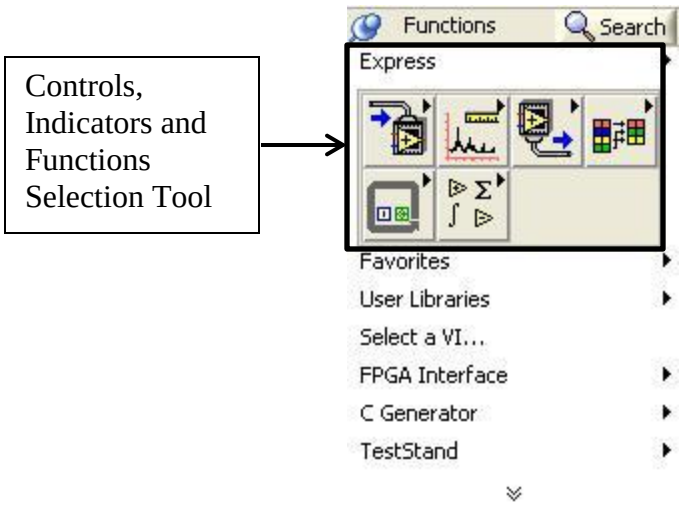


Figure 38: Functions Palette

The code can be tested using the built-in compiler by hitting the run button. After an application has been built, the professional version of LabVIEW allows the user to build executable applications and bundled installers. These can then be packaged and shipped to end users.

Although LabVIEW offers many features, it has drawbacks. Keeping the code modular and readable becomes very difficult as the application gets bigger and the number of features increases. The use of programming architectures like Graphical Dataflow can only simplify things to an extent. The lack of true Object-Oriented Programming in LabVIEW is one of its greatest limitations. Another stumbling block for many would be its price – over $2600 at the time of this report [**50**].

2.7 APPLICATIONS OF HIGH PRECISION ADCS

ADCs today are used in a smorgasbord of applications ranging from digital music to the onboard computer that controls a car. Without ADCs naturally occurring signals could not be digitized to allow for digital processing. To help alleviate the task of determining the proper ADC for a given

application some experts have described the ADC market in four general applications: data acquisition, precision industrial measurement, voice band and audio and high speed applications [**51**]. The SAR architecture ADC, which this paper mainly focuses on, is recognized as being appropriate for data acquisition applications. It should be noted that these are just guidelines, not definitive applications for different architectures [**52**].

The applications of one such PulSAR ADC, the AD7685 by Analog Devices, are listed as follows in its datasheet: battery-powered equipment, medical instruments, mobile communications, personal digital assistants (PDAs), data acquisition, instrumentation, and process controls [**53**]. Different SAR ADCs from Analog Devices list similar applications, varying depending on the speed and bit count of the ADC. As markets become more competitive choosing the best ADC that compromises between the needed performance and price becomes imperative.

By observing the applications list in Figure 8 the importance of the SAR ADCs can be observed. SAR ADCs are extremely palatable for battery-powered applications because of their power dissipation. The power dissipated by an SAR ADC is scaled depending on the sampling rate of the ADC [**17**]. Other architectures such as flash and pipelined ADCs have constant power dissipation [**17**].

ADCs also play an important role in applications such as software radios [**7**]. By converting the incoming signal from the analog to the digital domain signal processing can be done with a digital signal processing (DSP) chip rather than a plethora of analog circuitry. This domain change allows for a large reduction in system price. One of the trade-offs of this though is that by applying digital techniques images from outside the desired band can be aliased back in band

making the DSP process much more intensive. The above discussion illustrates how proper ADC architecture choice can help simplify analog and digital signal processing.

Applications for ADCs are numerous, and so are the different architectures for ADCs. A proper understanding of what applications different ADCs are best suited for allows consumers to make wise purchasing choices. Additionally, a strong comprehension of the parameters used to measure the performance of ADCs can help consumers additionally narrow down their choices. Analog Devices has further enhanced their customers' ability to properly choose between different ADCs and ADC drivers by developing easily switched plug-and-play modules to allow their customers to analyze the performance of these parts themselves.

2.8 CHAPTER SUMMARY

This chapter provided a background for topics pertaining to this report, and contained the same information that was often used to make the engineering decisions in this project. Section 2.1 Analog-to-Digital Converter Architecture provided an explanation of how SAR ADCs in particular are constructed, the main advantages and disadvantages of such a design, and the types of analog inputs that are available on modern converters. This was followed by Section 2.2 ADC Performance Metrics, which discussed the mathematical background for the various AC and DC performance parameters that characterize an ADC. The important facets of ADC driver, voltage reference, and sample-and-hold selection were explained in Section 2.3 ADC Support Circuitry, and the differences between SPORT and SPI were covered in Section 2.5 Timing Protocols. Finally, the LabVIEW software was explained in Section 2.6 Interpreting Digital Output Data

with LabVIEW, and 2.7 Applications of High Precision ADCs concluded the chapter with an overview of ADCs' utility in the modern electronics industry.

Chapter 3: Proposed Design Approach

Designing with analog-to-digital converters can be a daunting task. As the resolution and sampling rate of ADCs become better the implications of AC and DC errors also increase. The previous chapter presented research pertaining to ADC operation and the value of well-designed support circuitry. This information provided a basis for the design decisions of this MQP, which sought to develop evaluation boards for Analog Devices' PulSAR converters. This project followed a divide-and-conquer approach to the necessary tasks, with each group member specializing in specific aspects of the project.

3.1 MAIN GOAL

At the time of this report, ADI offers its customers several solutions for evaluating PulSAR performance. The two current platforms are the Evaluation Control Board (ECB) and the Converter Evaluation and Development (CED) board. Each board has its drawback and Analog Devices is looking to improve upon these designs. The ECB system is depicted in Figure 39, and suffers from the use of parallel port communication which is obsolete on most modern computers. Additionally, the ECB board offers the user the ability to test a plethora of parts other than just the PulSAR family, making the system fairly expensive at $253.00 [**11**]. For customers only looking to test an ADC, this is unnecessary inflation of cost for unneeded features.

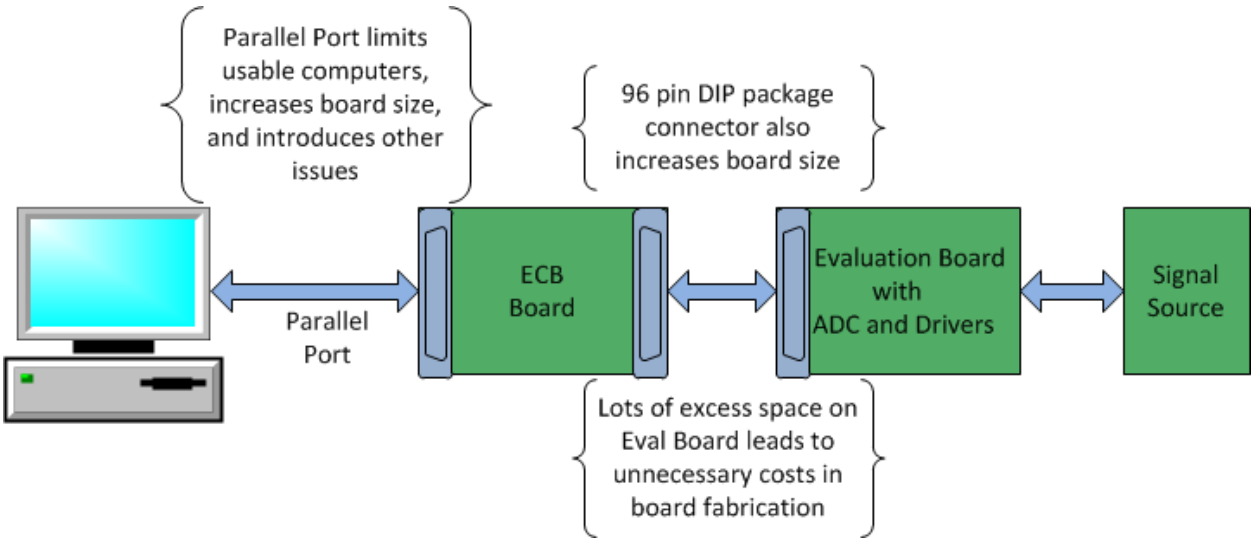


Figure 39: System Flow Diagram for Evaluation Control Board (ECB) Testing Platform

The Converter Evaluation and Development (CED) testing platform has similar drawbacks. Although the antiquated parallel port was replaced with a USB interface, the board is even more costly at $506 [**13**]. Both ECB and CED platforms connect to rigidly inflexible PulSAR Evaluation Boards. None of the circuitry – ADC and ADC driver included – can be easily substituted for customer experimentation, nor is the board optimized for low power testing.

Both of these platforms are to be replaced by the newer System Demonstration Platform (SDP). Based on a Blackfin microcontroller, the SDP mainboard communicates via USB, has a smaller form factor, and is significantly less expensive than the previous control boards. The SDP connects to PulSAR daughter cards that are currently being developed by Analog Devices engineers. This formative design period is an opportunity to address the drawbacks of previous testing platforms and make the SDP-based solution more user-centric. The goal of this MQP is to refine and enhance the PulSAR daughter cards for use with the SDP. The existing, pre-project block diagram for the daughter card operation is depicted in Figure 40.

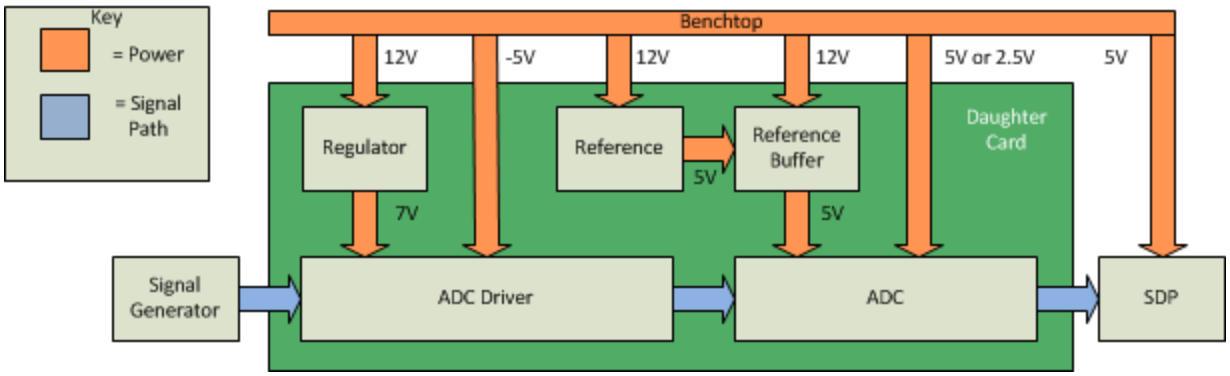


Figure 40: Pre-Project Flow Diagram of a PulSAR Daughter Card

Considering that this project is part of a commercial venture, this MQP group will be working with the Analog Devices applications engineers, who will provide valuable direction and advice during the migration of the PulSAR testing to the SDP platform. In particular, areas of the daughter cards to be refined in the span of this project include: developing an integrated circuit solution for powering the daughter card, designing secondary boards that can attach to the main daughter card that enable rapid substitution of ADC drivers, and writing customized LabVIEW software to provide a user-friendly front-end for viewing and interpreting the output data from the ADCs. Other optimizations and modifications will be made to the original daughter card's schematic (included in Appendix B) as they are discovered during the testing. These changes should transform the block diagram of Figure 40 into that of Figure 41.

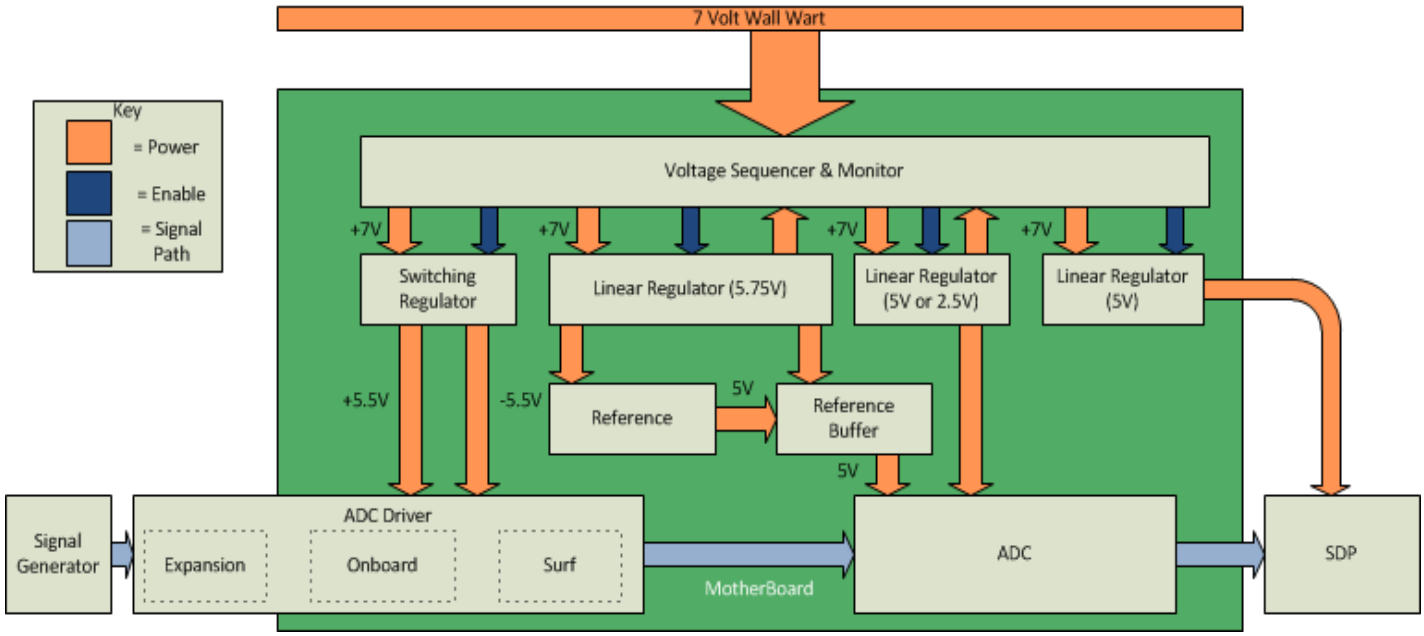


Figure 41: Post-Project Flow Diagram of a PulSAR Daughter Card

Aside from evaluation boards, Analog Devices offers *Circuits from the Lab* (*CftLs*) on its website "for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges" [**54**]. Along with assisting in the migration of the PulSAR ADC testing to the SDP, this project aims to develop *CftLs* to showcase the PulSAR family's ability to achieve high performance results while focusing on reduced power consumption and strong AC performance characteristics.

In summary, the project aims to complete the following items:

- Design an integrated circuit solution for power input and regulation. Present daughter cards are power by bench top power supplies; end-users would be better served by an onboard power system running off a singled input voltage. Attention will be paid to minimizing noise and ripple on the power lines, as well as sequencing the rails for proper operation of the signal-chain ICs.

- Develop schematics and layouts for surfboards or expansion boards that enable the user to quickly substitute ADC drivers. These boards will support single-ended, differential, and instrumentation amplifiers to maximize compatibility with the daughter cards.
- Create demonstration circuits – termed *Circuits from the Lab* in ADI parlance – that show PulSAR designs that cater to (a) low power consumption and (b) high AC performance. These will be assembled and performance-tested to match data against the theoretical performance.
- Program a software module in LabVIEW that will collect data from the SDP's USB interface. This code can be developed from existing ECB software, but requires a major overhaul of the graphical interface, support for new parts and features, and code refactoring and optimization to ease future support of the program.

3.2 PROJECT MANAGEMENT AND TIMELINE

The project was initially divided into 3 broad areas: LabVIEW, schematics and layouts, and testing and characterization. Each of the three group members initially specialized in one specific area in an attempt to accelerate the return time on results. Ultimately each group member contributed ideas and effort to each category.

The objective of the LabVIEW GUI was to build upon older ADI software to offer customers a newer, more user friendly GUI. Although based upon older software, the new GUI also included many new features as well as grandfathered components modified to more appropriately interact with the customer. Accordingly, the LabVIEW expert of the group was required to develop an

extensive knowledge of the LabVIEW visual programming language so these requirements could be met and thoroughly accommodated.

The schematics and layout of boards is important to achieving high quality results. Poorly laid boards can result in parasitic capacitances, leakage currents, and other undesirables that degrade performance considerably. Although a layout engineer is ultimately responsible for final board layouts, one group member was still responsible for a basic understanding of design layout to help alleviate the task of the layout engineer. Along with this task, the group member was also responsible for designing new daughter cards and surfboards at request of the applications engineers the group was working under.

Last, one group member was responsible for the testing and characterization of different parts. The testing of many different parts combinations was important because it provided a physical validation of the theory behind parts choices for different *CftL*s. It was the responsibility of this group member to not only test these parts, but to provide initial postulations on which parts (ADCs as well as drivers) would be most suited for different characteristic optimizations.

In order to complete the project within the span of ten weeks, a Gantt chart was created to keep track of tasks and milestones (Figure 42).

Task	Week 1	Week 2	Week 3	Week 4	Week 5	Week 6	Week 7	Week 8	Week 9	Week 10
Research										
LabVIEW										
Tutorials										
Familiarize with existing Software										
Software solution for PulSAR ADCs										
Software solution of 8 channel daughter cards										
Schematics and Layout										
Learn PADS										
Familiarize with existing schematics										
Modified schematics for power circuit										
Schematics for Surf-boards										
Schematics for In-Amps										
Circuit From The Lab(CFTL)										
Testing and Characterization										
Soldering Training										
Test daughter cards with different ADCs										
Characterize the performance of ADCs										
Build ideal circuits for various applications										
Report										
Introduction										
Background										
Implementation and Design										
Results										
Abstract, Acknowledgement, Executive Summary, Future Work										
Conclusion										
Final Draft Report										

Figure 42: Predicted Gantt Chart

As with any engineering project the theoretical time assigned to each task and the applied time to each task differed substantively. Below is the final Gantt chart representing the actual usage of time across the ten week timeframe:

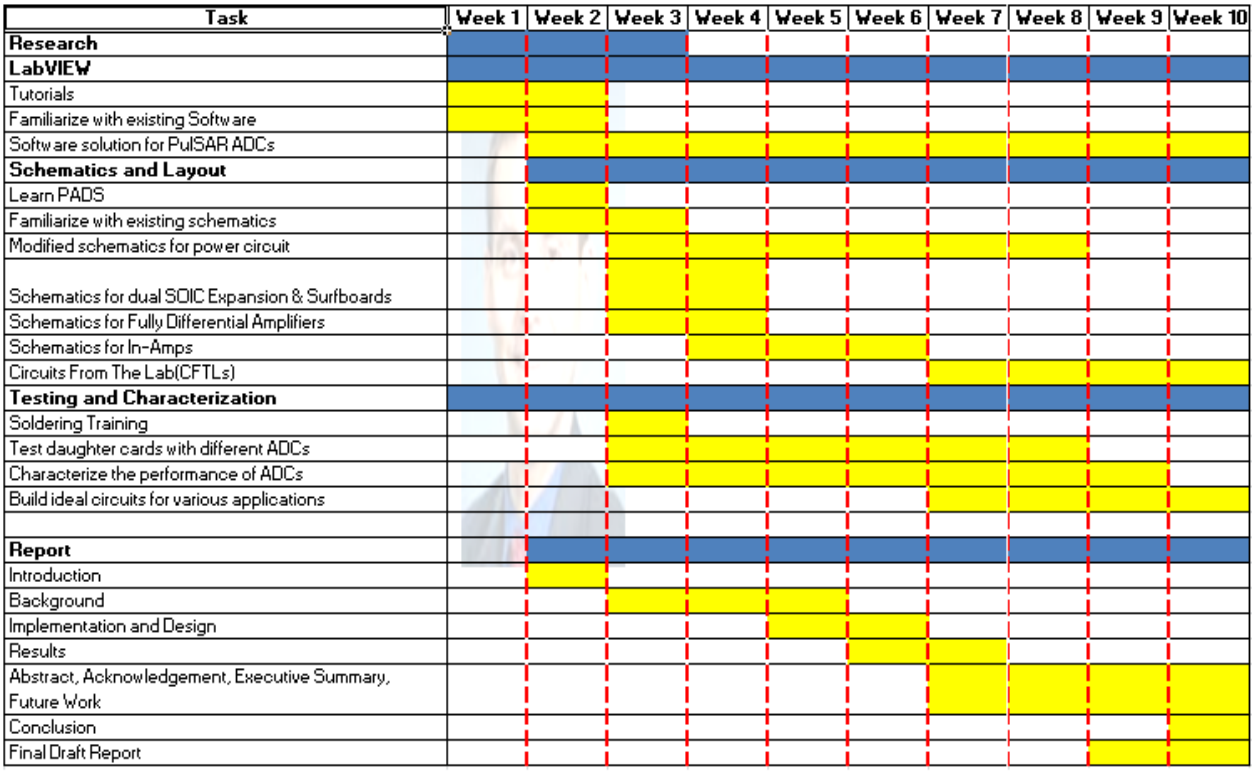


Figure 43: Actual Gantt Chart

3.3 CHAPTER SUMMARY

This chapter detailed the goals and timeline of this project. It was broken down into two sections, each with the purpose of helping the reader develop an understanding of what this project sought to accomplish, and how the group members applied their collective entity to bring this vision to life. The information covered in this chapter served as the foundation with which the group began a metamorphosis of the PulSAR testing platform. The following chapter envelopes the reader in the ten week cocoon created by the group to transform the initial PulSAR testing platform into a more elegant, modular, and complete system ready for consumption by the end user.

Chapter 4: Implementation

The following chapter discusses the thought process behind the implementations of different aspects of this project. The Chapter's organization is such that it flows fluidly from practical schematic design to practical design based upon theoretical qualifications to the software implementation capable of quantifying and visualizing the performance of the different implementations. This organization also follows the division of labor detailed in Chapter 3, transitioning from schematics and layout to testing and implementation to the software module.

4.1 Motherboard, Expansion Board, and Surfboard Design

One of the drawbacks of the ECB and the CED was that each PulSAR evaluation board was rigidly configured for a single driver-ADC pair. If a customer wanted to experiment with different driver amplifiers they would have to solder the new ICs onto the board or purchase an entire new evaluation board with the desired amplifier pre-populated. The original daughter card design shared the same flaw – there was no way to rapidly substitute new ADC drivers.

One of the objectives of this project was to add driver flexibility to the daughter cards. After consultation with the ADI engineers, two methods were devised: an expansion board and a surfboard. The expansion board would be inserted between the daughter card and the signal input, and would connect to the daughter card via the signal Subminiature Version B connectors

(SMBs) and an additional connector for power and ground lines. The surfboard would attach to raised headers on the surface of the daughter card and would provide a three-dimensional solution. A revised version of the daughter card – termed the motherboard – was also drawn up with the necessary headers and connectors to attach to both the expansion board and the surfboard. The initial conceptualizations of the expansion board and the surfboard are shown in Figure 44 and Figure 45.

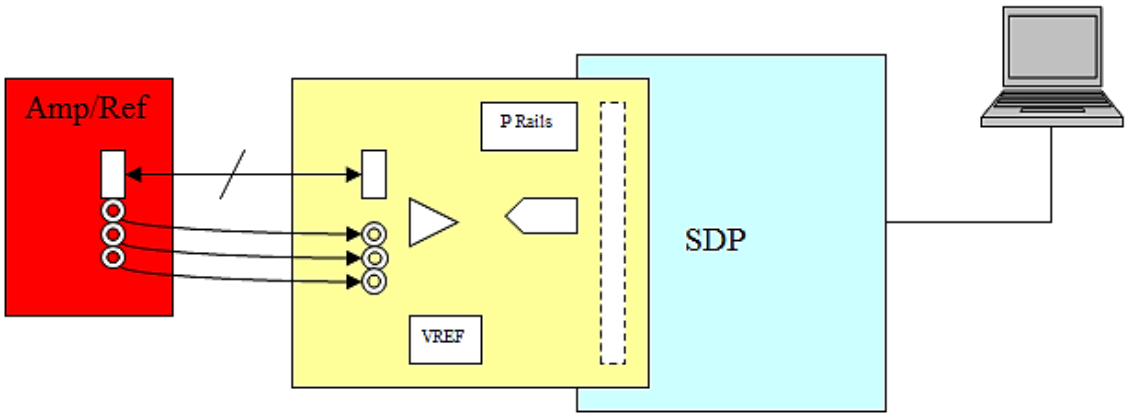


Figure 44: Brainstorm Diagram of Expansion Board (Credit Shane O'Meara)

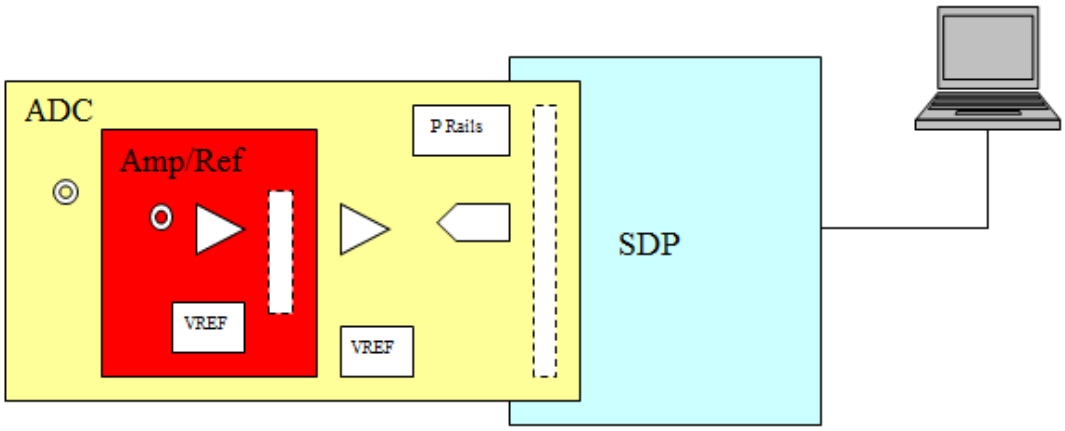


Figure 45: Brainstorm Diagram of Surfboard (Credit Shane O'Meara)

Starting the design process with the expansion board's signal path, the expansion board would require two male SMB connectors to receive the input signals V_{IN+} and V_{IN-}. It would also need

two female SMB connectors on the opposite side of the board for V_{OUT+} and V_{OUT-} to the motherboard. SMBs would be used here for their low resistance (and therefore low signal degradation) and would maintain conformance with the existing daughter board designs.

Since the expansion board would house ADC driver circuitry, there would also need to be connectors to transfer power and ground signals from the motherboard. Driver amplifiers are often dual-supply and require V_{DD} and V_{SS}. Furthermore, the input signals must be level-shifted to be centered on $V_{REF}/2$ rather than 0V, so a V_{CM} signal that is equal to the reference voltage would also need to be passed to the expansion board. The remaining pins of the 5x2 Dual Small Outline Package (DSOP) connector would be used for grounding as seen in Figure 46.

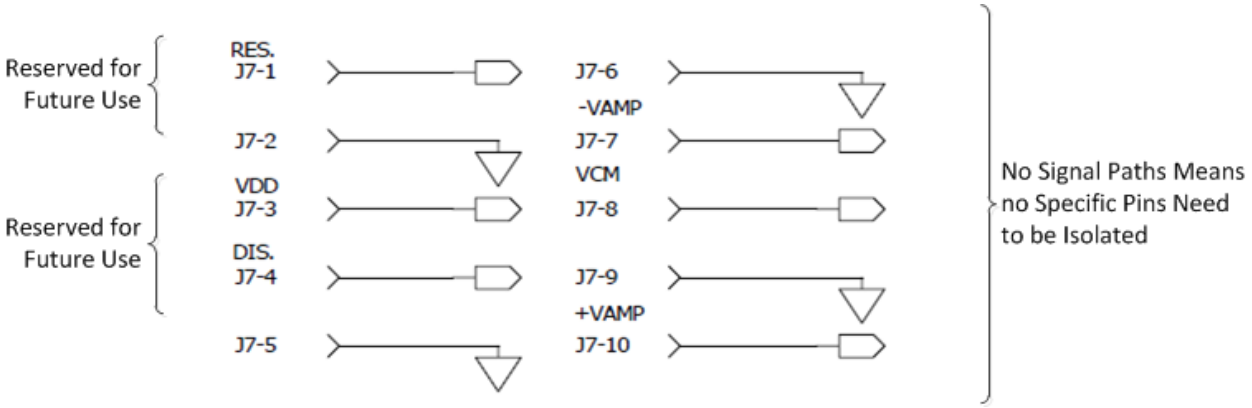


Figure 46: Pinout of the 5x2 DSOP Connector between Expansion Board and Motherboard

The surfboard would connect to the motherboard solely through two riser headers. After considering the number of signals that would need to be transferred between the boards, two seven-pin Single Inline Packages (SIP) connectors were selected. Similar to the expansion board connectors, these headers would provide connections for V_{IN+}, V_{IN-}, V_{OUT+}, V_{OUT-}, V_{DD}, V_{SS}, V_{CM}, and ground. However, since the signal lines would not run over high-quality SMBs, care would have to be taken to reduce cross-talk between the signal lines. On both the inbound and

outbound connectors, the two signal lines would be placed on far ends of the connector next to ground pins, as seen in Figure 47.

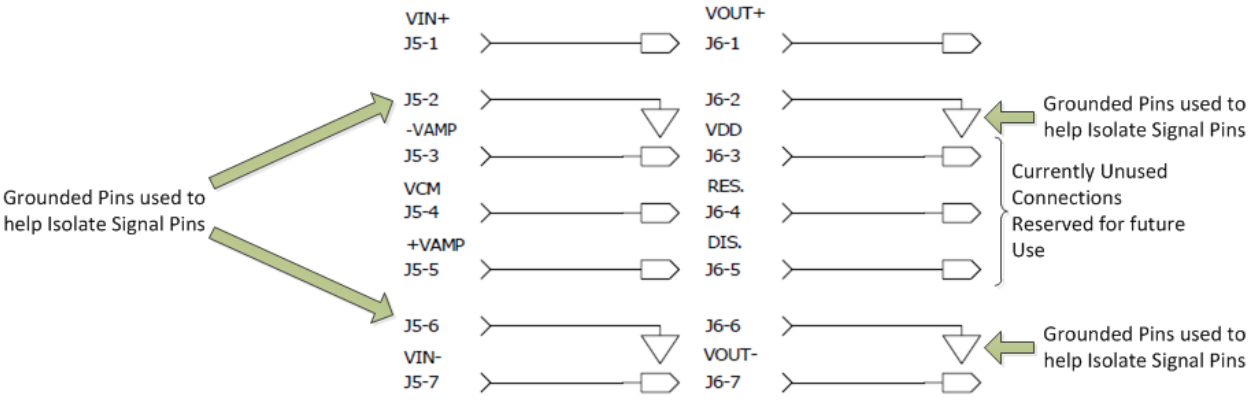


Figure 47: Pinout of the Two 7X1 SIP Connectors Between Surfboard and Motherboard

Finally, the motherboard itself would have to be modified beyond simply adding the connectors and headers for the expansion board and surfboard. Networks of 0Ω resistors would be added to the motherboard to properly route the input and output signals to the ADC drivers on the motherboard, expansion board, or surfboard. Figure 48 below shows the connections that would be used at the V_{IN+} terminals of the motherboard; these would be mirrored at the V_{IN-} terminal.

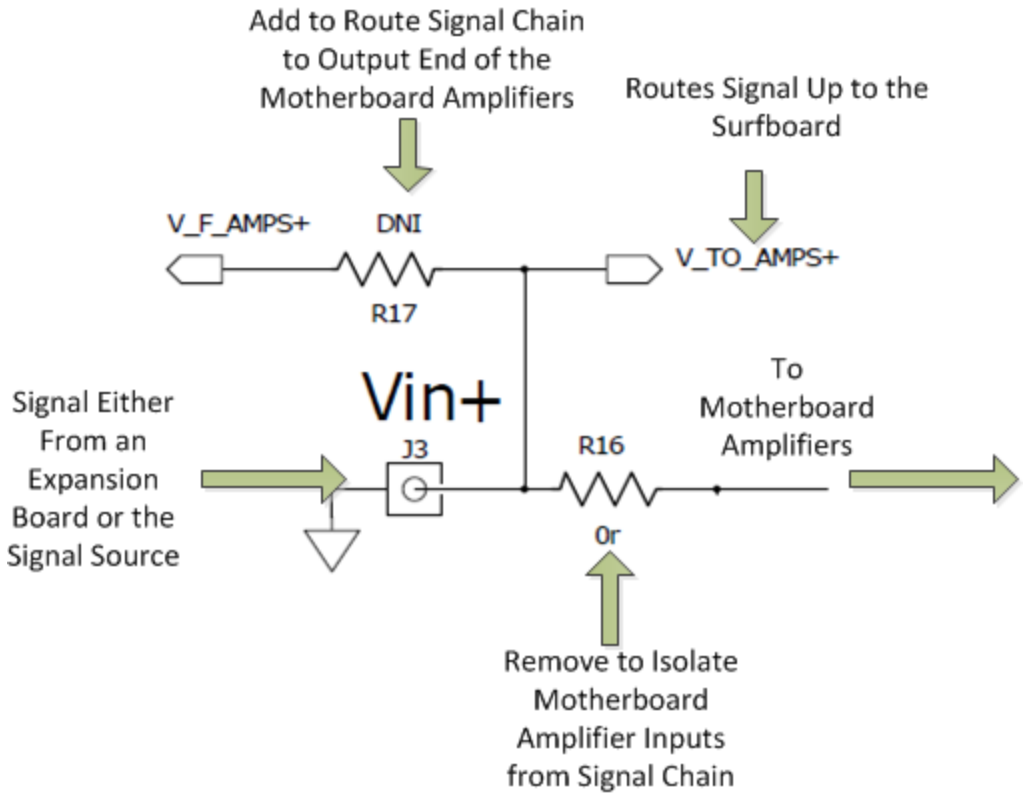


Figure 48: Motherboard V_{IN+} Configuration Scheme

To utilize the drivers on the motherboard the circuit should be left as seen in Figure 48. To use the drivers on an attached surfboard R16 should be removed. This routes the incoming signal up to the surfboard via VIN+ and the connector in Figure 47, where the signal is processed by the amplifiers and then transferred back to the motherboard (as seen in Figure 49). Drivers on an attached expansion card can be utilized by removing R16 and placing a 0Ω resistor onto R17. This routes the incoming signal (which will have already been processed by the expansion board) to the far side of the onboard amplifier, bypassing it. The motherboard can be configured to allow for processing by an expansion board as well as the onboard amplifiers, if such a configuration is desired, by once again leaving the resistors as seen in Figure 48 and simply attaching an expansion board. This information is summarized in Table 2.

Table 2: Summary of Motherboard Configurations

Amplifier(s) to be used	R16 Installation	R17 Installation	R30 Installation
Relevant Figure	Figure 48	Figure 48	Figure 49
Motherboard	0Ω	Not Installed	0Ω
Surfboard	Not Installed	Not Installed	Not Installed
Expansion Board	Not Installed	1.33MSPS	Not Installed
Exp. & Motherboard	0Ω	Not Installed	0Ω

Figure 49 shows the routing options found at the output of the motherboard amplifiers.

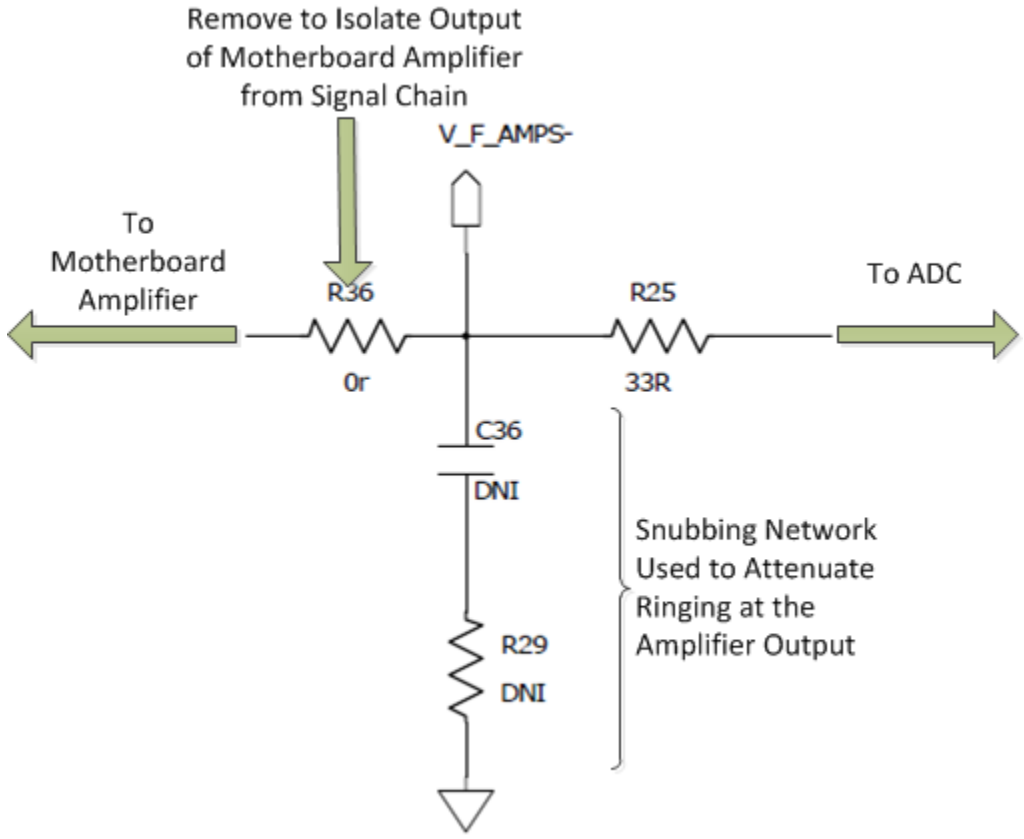


Figure 49: Rerouting Connections on Output of Motherboard Amplifier

The schematics for the expansion board, surfboard, and motherboard were drawn up with Mentor Graphics' PADS 9.1 Logic software. While this project did not involve the physical layout of the PCBs, extensive notes had to be made to the layout engineers to ensure that the mating

connectors on the different boards were properly oriented to attach to each other. In particular, a common problem when flattening three-dimensional connectors to two-dimensions is the accidental mirroring of signals on a connector. This would have disastrous effects – for the surfboard header, it would reverse V_{DD} and V_{SS} and surely damage the components.

4.2 Fully-Differential Amplifier Design

A second limitation of the original daughter card was that it was only designed for use with single-ended driver amplifiers. This topology was well-suited for pseudo-differential ADCs, but the entire driver circuitry had to be duplicated for use with a fully-differential converter. The replication of driver circuitry incurs more monetary expense, consumes PCB space, and can impact performance when compared to a fully-differential driver.

The objective of this section of the project was to design an alternate version of the daughter board that uses a fully-differential driver. Based on the performance demands of the PulSAR ADCs, this design would need to be compatible with the AD8137, AD8138, AD8139, ADA4940, and ADA4941 differential amplifiers. Reading through the datasheets for these parts revealed two specific configurations these op-amps can be used in: differential and single-ended inputs. The daughter board was designed to accommodate these configurations, allowing for the largest range of applicable testing by the end user. The schematic for this design is included in "Differential Amplifier Schematic" of Appendix B.

This design allows for both differential and singled ended inputs. When designing with differential amplifiers for use in a single-ended configuration, external resistors must be used to

properly terminate the source output impedance to balance the load on the amplifier [**55**]. This configuration can be seen in Figure 50.

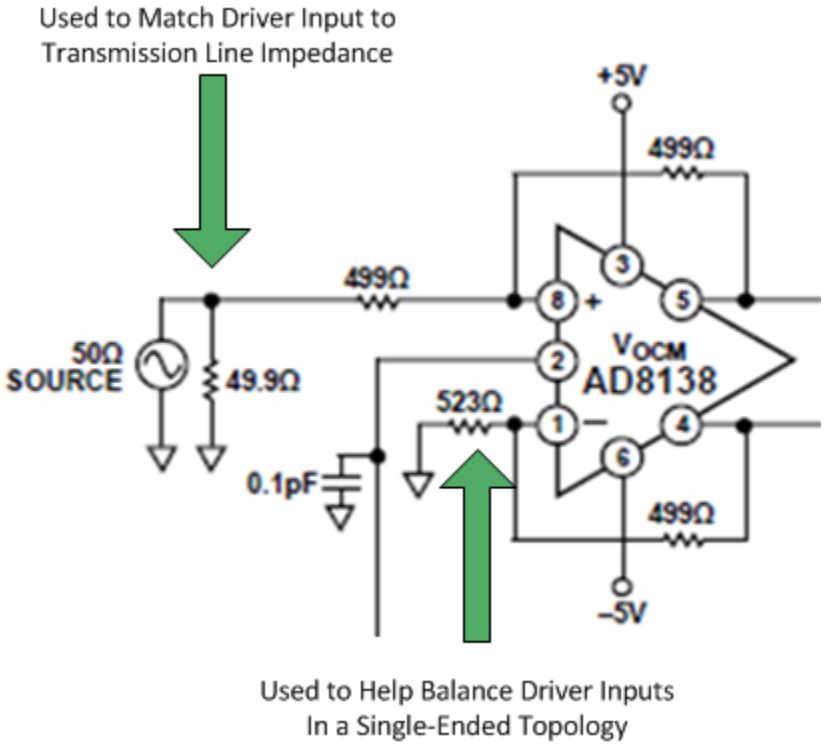


Figure 50: Configuration for a Single Ended Input [55]

Table 3 below lists the installations of different resistors for different configurations. The resistor values in the tables and discussion below refer to Appendix B: Differential Amplifier Schematic. These values can be calculated using the description found in the data sheet for the AD8139 [**56**].

Table 3: Fully Differential Resistor Configurations

Configuration	R7 Installation	R16 Installation	R17 Installation	R18 Installation	R22 Installation	R35 Installation
Fully Differential	0Ω	Uninstalled	Calculated	0Ω	Calculated	Uninstalled
Single Ended (+IN)	0Ω	Calculated	Calculated	Uninstalled	Calculated	0Ω
Single Ended (-IN)	Uninstalled	0Ω	Calculated	0Ω	Calculated	Calculated

Resistors 2, 19, 26, 28, and 34 can be configured to allow for many different levels of common mode voltage. The configurations are detailed in Table 4.

Table 4: V_{CM} Configurations for a Fully Differential Board

Configuration	R2 Installation	R19 Installation	R26 Installation	R28 Installation	R34 Installation	R35 Installation
Default V_{OCM}	Uninstalled	0Ω	Indifferent	Indifferent	Calculated	Uninstalled
User Defined V_{OCM}	Calculated	Calculated	Calculated	Uninstalled	0Ω	0Ω

The negative rail of the amplifier can be connected to an applied voltage by installing R3 or ground by installing R4. Only one of these two resistors should ever be installed at a time. Two RC networks, C31 and R27 as well as C36 and R29 can be used as snubbing networks to reduce ringing on the output of the amplifier.

4.3 Instrumentation Amplifier Schematics

One limitation of the surfboard and expansion board designs was their restriction to eight-pin amplifiers with a specific pinout. Analog Devices also manufactures ten-pin instrumentation amplifiers that can be used in environments where "dc precision and gain accuracy must be maintained within a noisy environment" [**57**]. Alternative versions of the surfboard and expansion boards were designed to accommodate these in-amps, specifically the AD8253.

Similar to the design-process for the differential driver daughter card, close analysis of the instrumentation amplifier datasheets was vital to the schematic design. One common issue found in circuits involving in-amps was the inclusion of RF noise. This problem can be hedged by including low pass filters at the inputs of the amplifier. Figure 51 shows the inclusion of RC

networks for this purpose [**58**]. The components are initially left unpopulated because they are not necessary in all applications. Also, in applications where their use is desirable, the actual values for each part will vary depending on the specific environment that the circuit is being tested in.

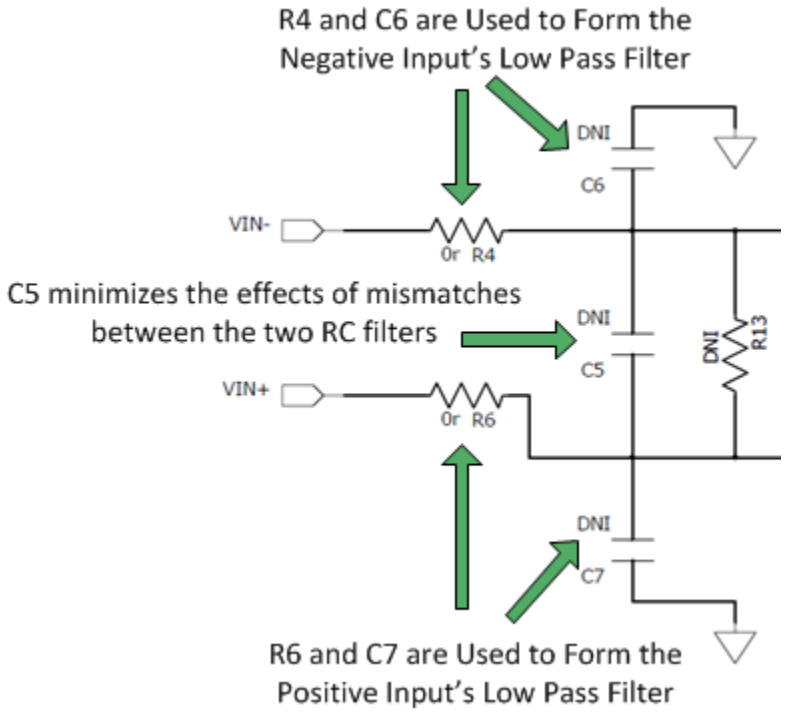


Figure 51: In-Amp Low Pass Filters to Reduce RF Noise

The values for the LPF components can be determined by Equation (44) and Equation (45) [**58**], where R is the value of the resistors, C_C is the value of C7 and C6, and C_D is the value of C5. It should be noted that C_D should be kept at least ten times as large as C_C [**58**].

$$f_{DIFF} = \frac{1}{2\pi R(2C_P + C_C)} \tag{44}$$

$$f_{CM} = \frac{1}{2\pi R C_C} \tag{45}$$

For this specific project, the in-amp needed to be capable of driving both pseudo- and fully-differential ADCs. To allow for this, the single ended output of the in-amp had to be transformed into a differential signal. The circuit seen below in Figure 52was used to create a differential output [**58**].

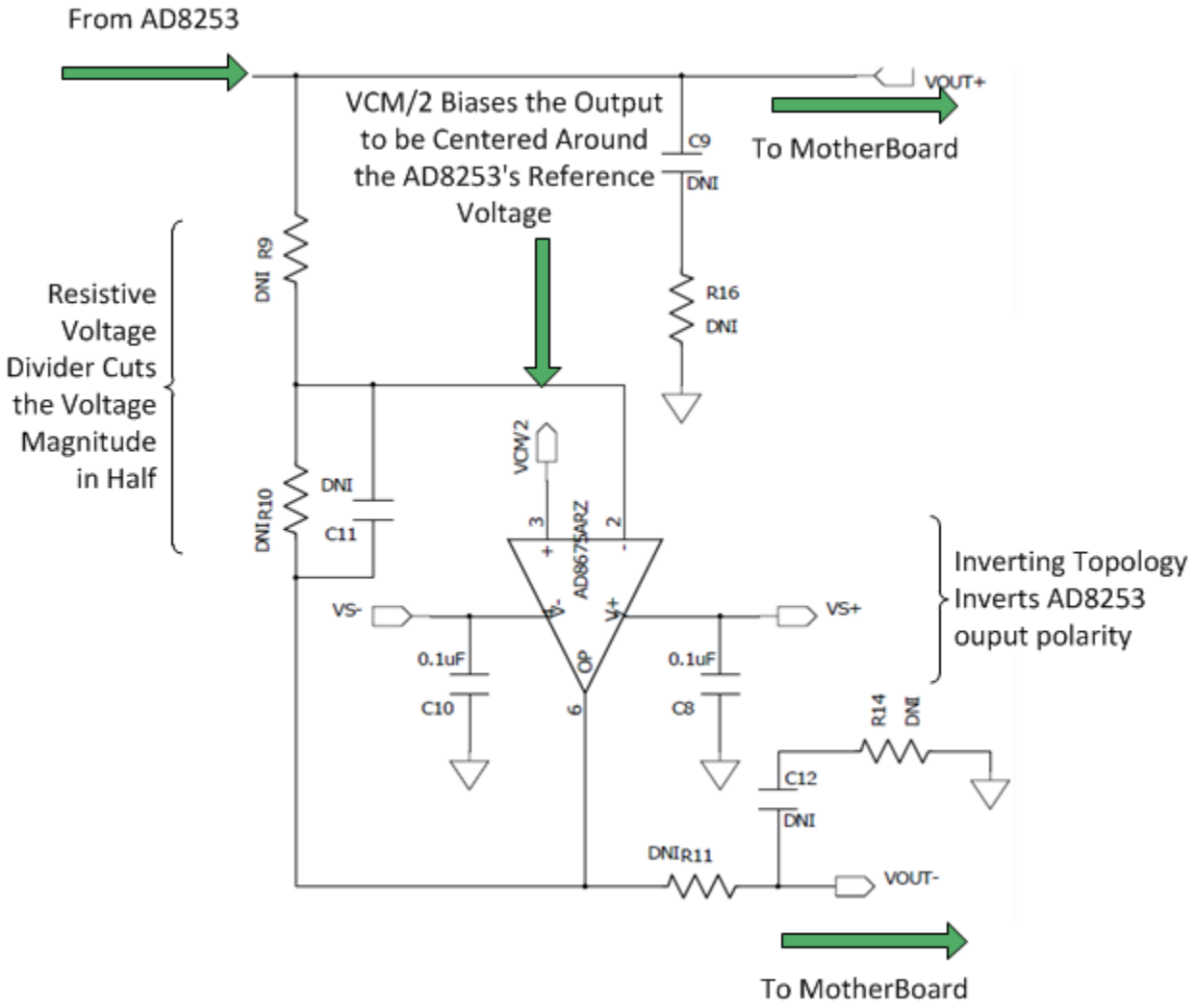


Figure 52: Transformation of Single-Ended In-Amp Output into a Fully-Differential Signal

Table 5 summarizes the resistor configurations used for single-ended and differential outputs. As with the earlier schematics, inserting or removing crucial 0Ω resistors is the technique used for switching between single-ended and fully-differential operation.

Table 5: Resistor Network Configurations for Single-Ended and Differential In-Amp Designs

Signal Configuration	R9 Installation	R10 Installation	R11 Installation
Single Ended	Not Installed	Indifferent	Not Installed
Differential	Equal to R10	Equal to R9	0Ω

4.4 POWER CIRCUITRY DESIGN

The original daughter card did not have a customer-oriented power supply design. The board required three different voltage rails and a ground, all of which were delivered to the board via a benchtop power supply. While well-suited for development and testing, the design excluded customers without multi-outputl benchtops and was more error-prone than an adapter-based solution. A new power supply design was desired to simplify this setup. The new power supply needed to meet several criteria. First, it needed to run off a single input voltage that would be delivered by a single wall wart adapter. A six to eight volt wall wart was preferred to be interchangeable with existing Analog Devices' boards. The single input supply could then be regulated to the other voltage levels needed for the PulSAR circuitry. The requirements for the power circuitry were developed through successive meetings with the Analog Devices engineers, and the design underwent several iterations before the final draft was accepted.

4.4.1 General Daughter Card Power Supply Design

The SDP receives some of its power from the computer via the 5V rail in the USB interface, but restrictions in the USB standard limit the amount of current that can be drawn on this line. To ensure that the SDP was provided adequate current on the 5V line, the daughter card power circuitry was designed to supply the SDP with five volts. The original daughter card was

designed so that the SDP and the ADC shared a single 5V rail; however, this project also incorporated PulSAR ADCs that used a 2.5V supply voltage. This necessitated a split supply, which also helped isolate the ADC V_{DD} from any fast switching effects from the SDP.

The power supply also needed to supply the ADC driver amplifiers; the ADA4841 was often used for this purpose. The voltages supplied to the driver in the original daughter card design were +7V and -5V. Depending on the chosen driver amplifier, these voltages would have to be adjusted to provide adequate headroom for unity-gain signal amplification from ground to V_{REF}. If this was not properly addressed distortion of the signal via voltage clipping would occur. Lastly, the voltage reference and reference buffer needed to be supplied with an appropriate V_{DD}. In the original design these both were powered by a +12V rail, although neither IC requires such a high voltage to operate.

4.4.2 First Revision

The first revision of the power supply design was based around the ADP3336 because it was being used on other boards being produced by the applications group. The ADP3336 is an adjustable LDO regulator with an input voltage range of 2.6V to 12V and an output voltage range of 1.5V to 10V. In this revision three ADP3336s were used to generate the positive rail for the ADC, the positive rail for the ADC amplifier, and a positive mirror of the negative rail for the ADC amplifier. An ADM8860 \was be used to invert the mirrored voltage to the -5V needed for the lower driver supply.

After conducting a worst-case analysis of the current draws on the various ADP3336s, the maximum current draw would be 50mA on the +7 rail by the driver amplifier. At this current, the

ADP3336 has a dropout voltage of 130mV, making it suitable for use in this application [**59**]. Since different models of the PulSAR ADCs can require either a 2.5V or 5V supply voltage, 0Ω resistors were used to allow for interchangeability between these two voltages as seen in Appendix B.

It was decided that the SDP would be powered by the ADP3333. The ADP3333 is an LDO regulator like the ADP3336 except that it comes with standardized output voltages instead of being adjustable. The ADP3333 was chosen over the ADP3336 to reduce components (no feedback resistors are necessary for the ADP3333) in the design. A third regulator, the ADP3367, was chosen to boost the 7V input to 12V. The 12V rail was used to power the ADR435 voltage reference as well as the AD8032 reference buffer. The ADP3367's input and output voltage corresponded to the required voltages and the part required few external components.

4.4.3 Second Revision

After consulting with several members of the applications team, it was determined that the initial power supply design contained many problems. The first fundamental problem with the design was the misuse of the ADP3367. A misreading of the ADP3367 datasheet led to the belief that the part was a boost converter with internal switching circuitry, as opposed to the LDO regulator it is in reality – as discussed in Chapter 2, an LDO can only produce voltages less than its input voltage, whereas a boost converter generates larger voltages than its input. Another failing of the design was the inclusion of a 12V supply for the voltage reference and the reference buffer. This voltage was chosen to match the benchtop voltages used with the original daughter card; however, upon closer examination of ADR435 and AD8032 datasheets, a lower voltage rail

would be more desirable to minimize power consumption at no cost to performance. Lastly, the ADM8660 used for the negative driver supply was based upon switching charge-pump technology and would have introduced noise to the signal path. The applications group had found in the past that charge pump topologies produce intolerable amounts of noise.

The second revision of the power supply design offered sought to improve the problems of the first revision. A power applications engineer, Mr. Luca Vaselli, was consulted and suggested a new LDO regulator being designed by ADI, the ADP7104. The ADP7104 operates at input voltages between 3.3V and 20V with an extremely low dropout voltage. The ADP7104 is available in several fixed output voltages, including 2.5V and 5V, as well as an adjustable output. The ADP7104 has extremely low noise, $15\mu V_{RMS}$, meaning it is a viable option for powering sensitive analog equipment such as the ADCs used in this project.

Table 6: Comparison of LDO Voltage Regulators Considered

Part Number	Input Voltage Range	Voltage Accuracy	Dropout Voltage	Line Regulation	Load Regulation	Output Noise
ADP3336	2.6-12V	±1.8%	130mV @ I_L = 50mA	0.04 V/V	0.04mV/mA	27µV rms
ADP3333	2.6V-12V	±1.8%	185mV @ I_L = 200mA	0.04 V/V	0.04mV/mA	45µV rms
ADP7104	3.3V-18V	±3%	**150mV @ I_L = 150mA**	±0.02%/V	0.0005%/mA	**15µV rms**

A brief example is included below to illustrate this point. The PSRR of the AD7982 is 90dB. The LSB of the 18-bit AD7982 is 19.1µV when configured to use a 5V reference. Using Equation (27) it can be determined that 0.3V of noise on the power supply would be needed to cause a change of ½ LSB in the signal path. Integrating the noise over the input bandwidth of the AD7982 (10MHz) equates to 1.5mV of total noise, meaning the noise produced by the ADP7104

should have little to no effect on the dynamic performance of the AD7982. As a result the ADP7104 was chosen to power the ADC at both 5V and 2.5V.

The ADP7104 was also chosen to power the SDP at 5V. The current sourcing capabilities and dynamic load regulation of the ADP7104 are comparable to the requirements of the SDP, making it an appealing choice. The dynamic load regulation of the ADP7104 is 5ppm, meaning that even if the current draw from the SDP were to change by 200mA the output voltage would only change by 5mV.

Lastly, the ADP7104 was also chosen to power the voltage reference and the reference buffer. The voltage reference for this revision was switched from the ADR435 to the ADR445, another 5V high precision reference that has a much lower dropout voltage than the ADR435. The ADR445 has a PSRR of -80dB which corresponds to a reduction in noise by a factor of 10^4. The noise produced by the reference itself is 90nV/√Hz. The calculation below show that the noise produced by the ADP7104 will be dominated by noise produced by the reference itself, making the ADP7104's contribution inconsequential:

$$(15\mu V_{RMS})(10^{-4}) = \frac{1.5nV}{\sqrt{Hz}} \quad (46)$$

The same calculation can be performed to show that the noise from AD8032 reference buffer would dominate the noise from the ADP7104 used for the power supply. By switching to the ADR445, both the voltage reference and the reference buffer could operate at 5.75V rather than the 7.5V required by the ADR435. The ADP7104 was adjusted for this output voltage to minimize wasted power. The maximum current draw of the reference and the buffer at maximum would be less than 10mA, but even if it were as high as 150mA, the dropout voltage of the

ADP7104 would be 150mV. Even in a worst case scenario, the regulator would hold a stable voltage. Appendix D details an exhaustive numerical analysis of the worst case scenarios pertaining to this power supply design.

The last IC requiring power was the input amplifier for the ADC. In this case, the sources were designed specifically to work with the ADA4841. The ADA4841 has a power supply range of 12V, and runs almost rail-to-rail (within 0.1V of the voltage rails). For the amplifier to properly buffer signals at ground a negative rail needed to be supplied. To achieve this end a combined Sepic_Cùk topology using the ADP1613 to produce ±5.5V was designed with the assistance of a tool on the Analog Devices web page [**60**]. The ±5.5V voltage rails were chosen to avoid damaging the ADA4841, which has a maximum operating range of 12V.

The last step in the second design revision was to properly sequence the voltage supplies. When working with analog circuitry such as ADCs the absolute ratings of these parts must be considered. Table 7 illustrates the PulSAR ADC absolute ratings abided by in the sequencing design.

Table 7: AD7984 Absolute Ratings [61**]**

Parameter	**Rating**
IN+, IN- to GND	-.3V t0 V_{REF} + .3V or ± 130mA
REF, VIO, to GND	-.3V to +6.0V
VDD to GND	-.3V to +3.0V
VDD to VIO	+3V to -6V
Digital Inputs to Ground	-.3V to VIO +.3V
Digital Outputs to GND	-.3V to VIO +.3V

The AD7984 was chosen because it, along with other 2.5V V_{DD} ADCs, had the most stringent requirements. A voltage sequencer circuit was developed so that the analog inputs of the ADC never exceeded V_{REF} + 0.3V; abiding by the maximum ratings would preserve the quality and operation of the converter.

To implement this scheme the ADM1185 voltage sequencer/monitor was used. The ADM1185 compares voltage inputs with 0.6V references and outputs a digital high on a specified control line when a 0.6V input is seen at the output's corresponding input pin. Voltage dividers are typically used to set the voltage at which a given input pin crosses the 0.6V threshold. By connecting the enabling outputs of the ADM1185 to the enable pins of voltage regulators and the outputs of the regulators to the inputs of the ADM1185 a turn-on sequence can be created.

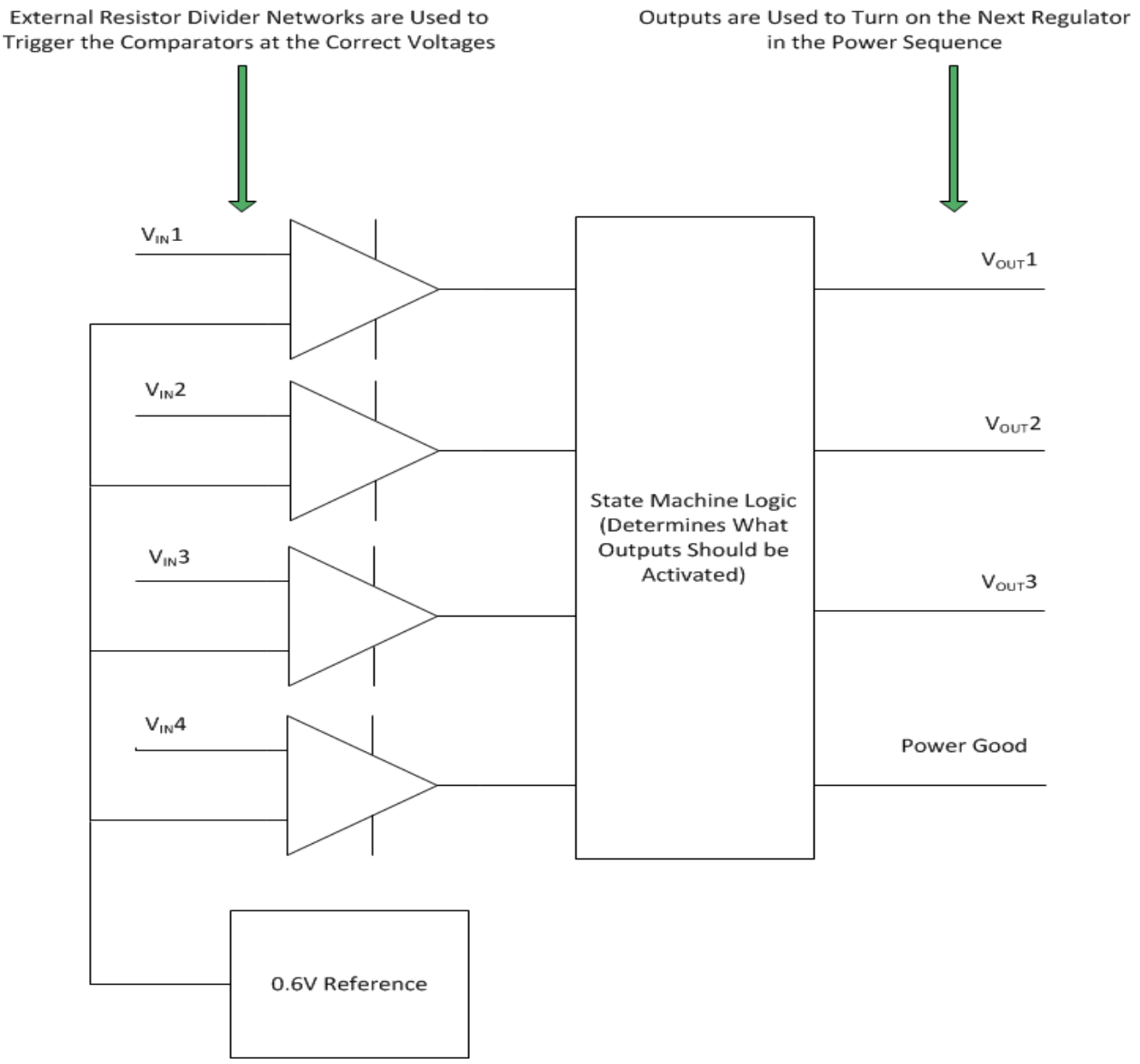


Figure 53: Diagram of ADM1185 Voltage Sequencer

For this design, the first step was to determine the minimum turn-on voltages for each regulator. These voltages should be fairly lenient to avoid the possibility of the system getting stuck at a particular point in the sequencing scheme. Since the system was designed to run at a minimum of 6V, this was deemed a good voltage as the minimum voltage to be viewed as being an acceptable system input. The ADM1185 was configured to enable the LDO regulators powering the ADC and SDP once 6V was seen at the system input. Next the ADM1185 was set up to look for at

least 2V (or 4.25V for a 5V ADC) voltage to appear out of the ADC regulator. This would allow VIO and VDD to come up at the same time (if VIO had not already been applied by the SDP), reducing the likelihood of the absolute voltage difference between the two exceeding the given rating. The next enabling output was tied to the LDO regulator powering the voltage reference. The ADM1185 was configured to wait until a minimum of 5V was being output by this LDO regulator before enabling the switching regulator powering the ADC input driver. A flowchart of the enabling system is provided in Figure 54.

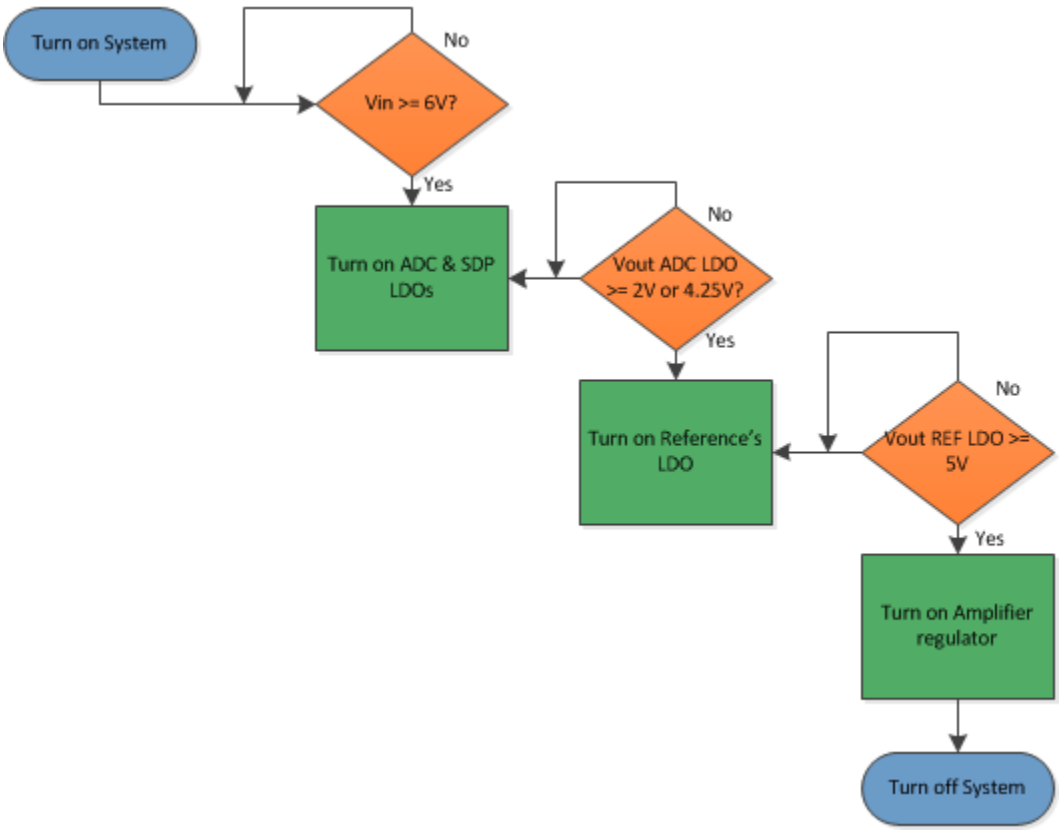


Figure 54: ADM1185 Sequencing System Flow Chart

4.4.4 Third Revision

It was soon realized that a third revision of the power supply would have to be designed. During the course of the Low Power *CftL* testing, it was discovered that a +5.5V voltage rail would be

insufficient for the ADA4841. A close reading of the datasheet revealed that the ADA4841 requires a minimum 1V of headroom between its output and the positive voltage rail in a unity gain configuration, so powering the driver with ±5.5V would clip a 0V to 5V input signal. As predicted, testing the amplifier at ±5.5V with a 10 kHz sine wave yielded unacceptable results.

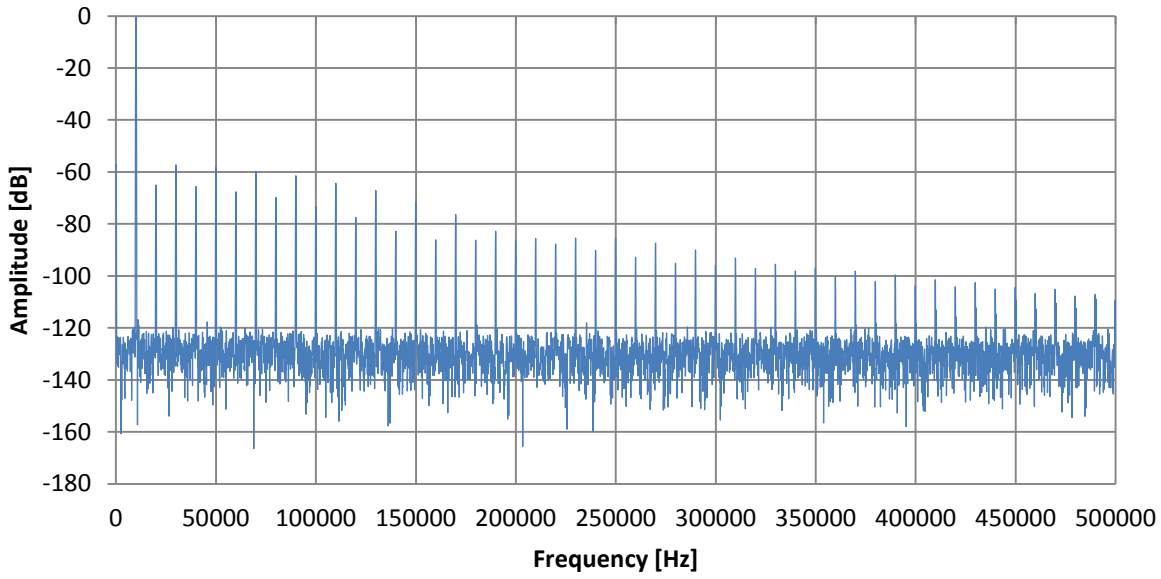


Figure 55: Clipping Distortion from ADA4841 with ±5.5V Supplies

When the positive driver supply was widened to +6V, the distortion disappeared. The Sepic_Cùk regulator was re-designed to generate ±6 volt rails with extremely low voltage ripple on them. Low voltage ripple was especially important in this revision to not only provide optimum performance, but to prevent the absolute maximum voltage rating (12.6V) of the ADA4841 from being exceeded.

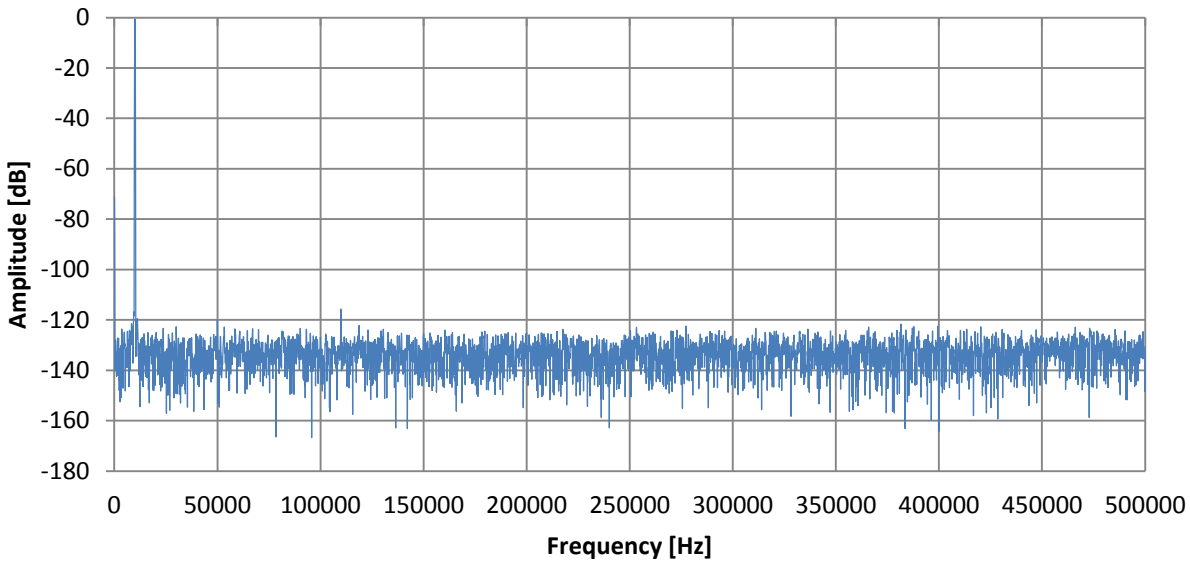


Figure 56: No Distortion from ADA4841 with +6V Supply

The second change to the power supply design was to expand voltage reference support to the ADR435. In the second revision of the power supply, the ADR445 was chosen over the ADR435 so that the voltage rail could be reduced from 7V to 5.75V. After discussions with the ADI applications group and voltage reference group, it was revealed that the ADR435 had a superior compensation scheme. The output impedance of a reference can be represented with an inductor, which when connected in series with the dynamic capacitive load presented by an ADC, creates an LC network [**62**]. Resonant noise formed between the reference output stage and the ADC input stage can severely degrade performance. Unlike the ADR445, the ADR435 has a compensation pin to help stabilize the reference in the presence of high capacitive loads, making it the preferred reference for this design [**62**]. The new supply voltage was created using an ADP1613 in a boost converter topology designed using one of ADI's power supply design tools [**60**]. The boost converter was designed to output 9V, chosen so that the converter could properly operate with an input range of 6V to 8V.

Next, a four connection screw-terminal was added to the design to enable the use of benchtop supplies if the customers desired different voltage rails. Solder links were added to the outputs of each voltage regulator, as well as the expansion board and surfboard connectors, to allow users to choose between the onboard power supply and power provided from a bench top. This option would allow users to more accurately simulate their circuit conditions if specific voltage rails were required in their design. This third and final revision of the power supply design can be seen in Appendix B.

4.5 Selecting Between SPI and SPORT Protocols

One of the early priorities was to determine if SPI or SPORT provided the best transfer protocol for the ADC's serial output. The 96-pin connector between the daughter card and the SDP has signal lines for both interfaces, and the first revision of the daughter card could be configured for either interface by switching the position of three 0Ω resistors. This flexibility would be unnecessary in the release revision if one interface showed a demonstrable improvement in performance, thus simplifying customer set-up of the board and guaranteeing the best results.

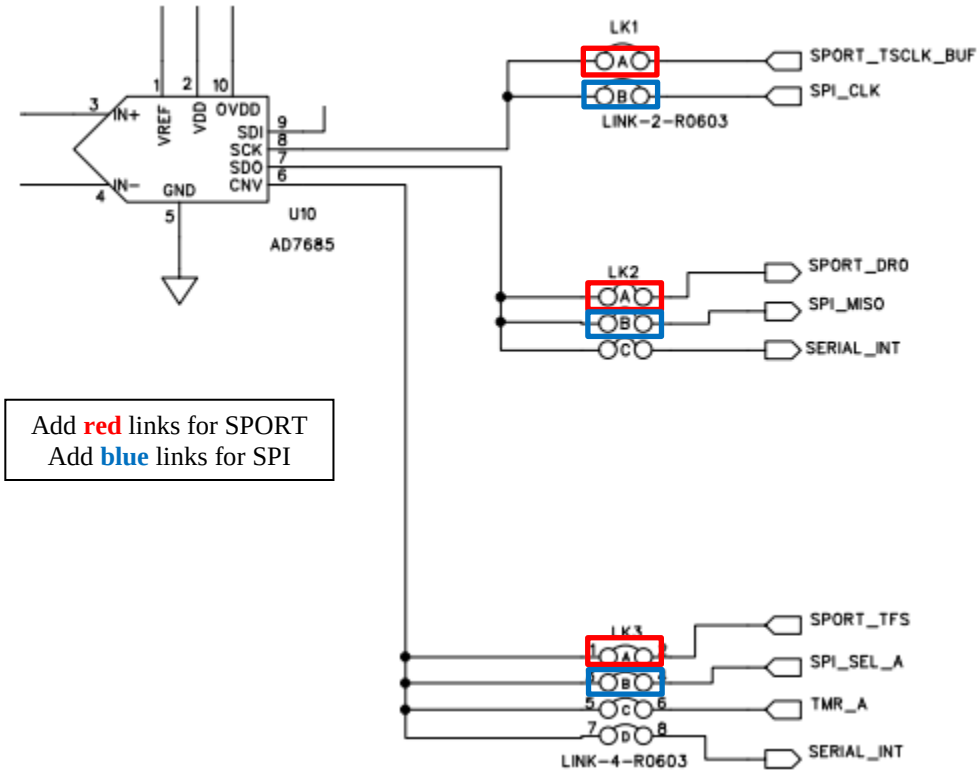


Figure 57: Daughter Card Rev1 Schematic Alteration for SPORT to SPI

Based on its technical details, the SPI interface was predicted to be inadequate for the PulSAR converters. When paired with the Blackfin BF-572 microprocessor that is on the SDP, the maximum system clock that can be used with SPI is 30 MHz [**48**]. Equation (1) can be rearranged to see the effect this limit has on the maximum achievable sampling rate f_S:

$$f_S = \frac{1}{\frac{N}{f_{CLK}} + t_{ACQ}} \tag{47}$$

Using an 18-bit PulSAR ADC such as the AD7984 as an example, the SPI interface will fail to facilitate the full sampling rate of 1.33 MSps even when t_{ACQ} is the minimum value listed in the datasheet, an unrealistic assumption. Furthermore, since SPI is a software-controlled interface it

is gated on/off between data words. At high speeds any jitter on these transitions would translate to quantifiable error in the output data.

Conversely, the SPORT interface seemed well-suited for high speed serial data transmission. As dictated by Equation (40), the maximum system clock for SPORT is 60 MHz. With the same 18-bit AD7984 as used in the example above, the 60 MHz SPORT clock enables a 1.8 MSps data rate while SPI was limited to 1.17 MSps, a 54% improvement. Finally, SPORT is a hardware-based transfer protocol and the clock is continuous.

To quantify any performance differences between SPI and SPORT, an AD7980 (16-bit, 1MSps) was soldered onto a first-revision daughter card. Despite SPORT being able to run at 60 MHz, the system clock for both set-ups was limited to 30 MHz to eliminate the clock speed as a variable. Each was tested at three sampling rates, and each sampling rate was tested at twenty-six input frequencies ranging from 6 kHz to 100 kHz. Further information about the testing procedure can be found in Section

5.1 General Testing Set-Up and Procedure.

4.6 Low Power Design *Circuit from the Lab* with AD7980

As described in Chapter 2, one of the advantages of successive-approximation register converters is that their power consumption scales with sampling rate, making them attractive options for micropower applications. In light of this, this project sought to develop a *Circuit from the Lab* that demonstrated extreme power conservation while retaining adequate performance.

The central component for the low power daughter card design was the PulSAR ADC. To select the most appropriate model several selection criteria were used: the ADC was restricted to a single channel and a single power supply for reduced power, and the sampling rate was to be 500 kSps or higher so the design was more flexible. When the remaining converters were sorted by power consumption, the AD7982 and the AD7980 were the most viable.

Table 8: PulSAR Analog-to-Digital Converter Options for Low Power Design

Part#	Resolution (Bits)	Throughput Rate	Single-Supply	Operating Pwr Diss	Sleep Pwr Diss	Pos Supply
AD7982	18	1MSPS	Yes	8.6E-3	86.0E-6	2.375V-2.625V
AD7980	16	1MSPS	Yes	**10.0E-3**	**100.0E-9**	2.375V-2.625V
AD7983	16	1.33MSPS	Yes	12.0E-3	875.0E-6	2.375V-2.625V
AD7984	18	1.33MSPS	Yes	14.0E-3	2.8E-3	2.375V-2.625V
AD7623	16	1.33MSPS	Yes	55.0E-3		2.37V-2.63V
AD7643	18	1.25MSPS	Yes	80.0E-3		2.3V-3.6V
AD7622	16	2MSPS	Yes	85.0E-3		2.63V-2.37V
AD7621	16	3MSPS	Yes	86.0E-3	600.0E-6	2.37V-2.63V
AD7641	18	2MSPS	Yes	92.0E-3		2.5V-2.5V

Of these, the AD7980 was chosen because it uses 100nW of power when idling compared to the 86µW of the AD7982. The AD7980 is a pseudo-differential, 16-bit, 1 MSps PulSAR ADC that runs on a single supply V_{DD} = 2.5V [**8**].

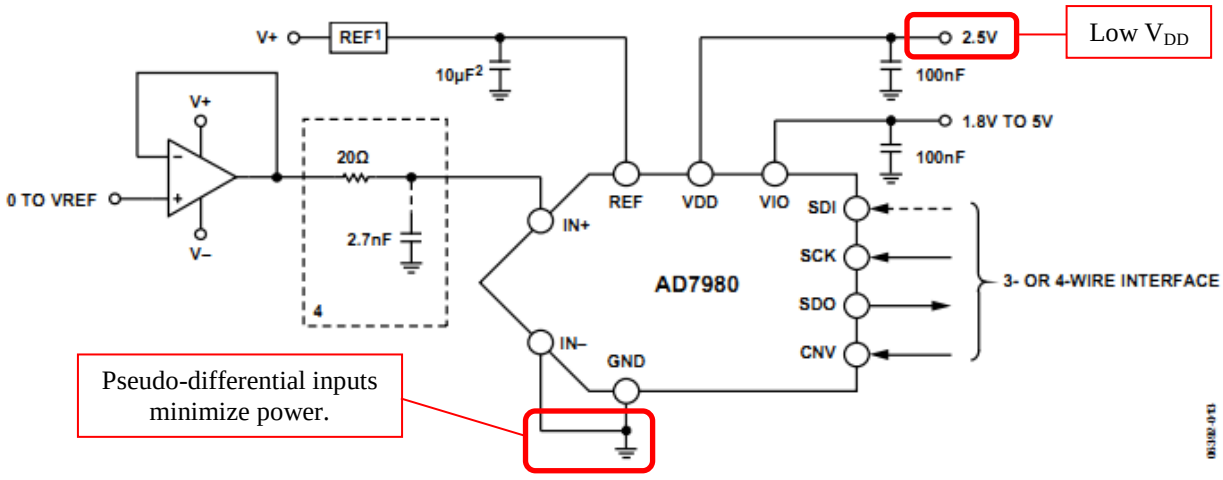


Figure 58: Typical Connection Diagram for AD7980 [8]

In many respects, the AD7980 could be substituted into the existing daughter card schematic (which used the AD7685) with little alterations. The VIO, SDI, SCK, SDO, and CNV pins would all remain configured identically since the SPORT interface and SDP logic levels would not be affected by the new converter. Additionally, The IN- and GND lines would still tie directly to ground since both the old and new ADCs are pseudo-differential.

The circuitry at the remaining pins would have to be modified for the low power design. Most importantly, the supply voltage V_{DD} must be reduced from 5V to 2.5V; continuing to run at 5V would exceed the absolute maximum ratings for the AD7980. The reference voltage V_{REF} was also reduced to 2.5V (the minimum that V_{REF} can go for this ADC) to minimize power consumption. Finally, the analog input at IN+ could only swing from ground to V_{REF}, so the input signal was limited to 0V to 2.5V for this circuit.

Considering the change of V_{REF}, the voltage reference must be changed from the ADR435 to a suitable 2.5V reference. As discussed in the background, the choice of the voltage reference can have significant impacts on the ADC performance. Noise, thermal coefficient, and output inductance are of most concern, but regrettably few datasheets specify the output inductance (a

high L_{OUT} degrades the settling time of the ADC and leads to oscillating output codes). The power dissipation of the reference is also important for this design. Finally, the package type was limited to SOIC-8 to eliminate the need to fabricate a new daughter card. Within these restrictions, the ADR291 consumes the least power and has excellent noise and thermal coefficient performance for its class [**63**].

Table 9: Voltage Reference Options for Low Power Design

Part#	Vout	Ref Out TC (ppm/C)	0.1-10 Hz Noise (uV p-p)	Min V Supply (V)	Line Reg (ppm/V max)	Load Reg (ppm/mA)	Supply Current	Power Dissipation
ADR291	2.5	3ppm/C	8uV p-p	3	30ppm/V	30ppm/mA	1.20E-05	36.0E-6
REF192	2.5	2ppm/C	25uV p-p	2.6	2ppm/V	4ppm/mA	4.50E-05	117.0E-6
AD680	2.5	20ppm/C	8uV p-p	4.5	16ppm/V	40ppm/mA	2.50E-04	1.1E-3
REF43	2.5	25ppm/C	4uV p-p	4.5	1ppm/V	14ppm/mA	4.50E-04	2.0E-3
ADR421	2.5	1ppm/C	1.75uV p-p	4.5	10ppm/V	70ppm/mA	5.00E-04	2.3E-3
ADR03	2.5	3ppm/C	10uV p-p	3.5	30ppm/V	70ppm/mA	1.00E-03	3.5E-3
ADR431	2.5	1ppm/C	3.5uV p-p	4.5	5ppm/V	15ppm/mA	8.00E-04	3.6E-3
AD780	2.5	3ppm/C	4uV p-p	4	4ppm/V	20ppm/mA	1.00E-03	4.0E-3
REF03	2.5	10ppm/C	6uV p-p	4.5	20ppm/V	60ppm/mA	1.40E-03	6.3E-3
ADR441	2.5	1ppm/C	1.2uV p-p	3	10ppm/V	50ppm/mA	3.75E-03	11.3E-3

Unfortunately, the ADR291 datasheet does not list its output impedance, and if poor this could be a factor that degrades the ADC performance. The converter's datasheet only explicitly names the ADR43x series of voltage references as appropriate, and recommends using a low-impedance buffer such as the AD8032 after other references [**8**]. The use of a reference buffer would increase performance (especially at high sampling rates) but would also dissipate additional power. Lacking a better method, the ADR291 would be tested both with and without the AD8032 buffer before the final decision would be made.

The ADC driver is also an important component that should be optimized for the low power design. The input signal to the ADC can swing from 0V to 2.5V, so this was the minimum output

swing of the driver. It should also operate on low supply voltages, ideally close to the 2.8V minimum for the chosen voltage reference and reference buffer. Five drivers remained after selecting based on bandwidth (10MHz to 100MHz), the number of amplifiers per package, the package type (SOIC-8), a rail-to-rail output, and low voltage rails. The ADA4841 and the AD8655 were chosen out of Table 10 based on available inventory. Since predicting driver operation can be nuanced, both would be tested before making the final determination for the *CftL*.

Table 10: ADC Driver Options for Low Power Design

Part#	Small Signal Bandwidth	Slew Rate	Ib	Amplifiers Per Package	V Noise Density	Vcc-Vee	Supply Current	Rail-Rail Out
OP162	15MHz	13V/us	260nA	1	9.5nV/rtHz	2.7V-12V	800.0E-6	Yes
ADA4841	80MHz	13V/us	3uA	1	**2.1nV/rtHz**	2.7V-12V	**1.5E-3**	Yes
AD8031	80MHz	35V/us	450nA	1	15nV/rtHz	2.7V-12V	1.6E-3	Yes
AD8655	28MHz	11V/us	10pA	1	**4nV/rtHz**	2.7V-5.5V	**4.5E-3**	Yes
AD8651	50MHz	41V/us	1pA	1	4.5nV/rtHz	2.7V-5.5V	9.0E-3	Yes

With the IC selection completed, the required voltage rails for the daughter card were determined. The ADC requires a 2.5V supply; since none of the other selected components can operate at this voltage, one of the rails would have to be 2.5V. The other components – ADR291, AD8032, ADA4841, and AD8655 – can all run at 2.8V and up, so 3V was chosen as a common voltage close to this value. Since these voltages can be dialed into the benchtop supply and delivered directly to the board via the screw terminals, the ADP3334 voltage regulator is unnecessary and can be removed. Finally, a negative rail is optional – the ADC driver will distort full-scale input signals less if it can swing to a negative value, but having a negative rail will also consume more power. It was decided to try both 0V and -1V and weigh the performance benefits against the added power.

Table 11 summarizes the eight possible combinations of components selected in this design process, and Variant 4 is depicted in the "Low Power AD7980 Schematic" of Appendix B. The table below also includes rough estimates of the configurations' power consumption, which include the typical quiescent power of each integrated circuit, the power lost in the voltage divider on V_{CM}, and the power for the AD7980 for throughputs from 10 kSps to 1 MSps. The numbers are likely underestimates, since they do not account for loading on the ADC driver or on V_{REF}; the dynamic conditions on these signals make power predictions difficult.

Table 11: Selected Part Options for the Low Power Design

Variant	PulSAR ADC	Voltage Ref	Ref Buffer	ADC Driver	Negative Rail	Estimated Power
1	AD7980	ADR291	AD8032	ADA4841	0V	13.2 mW - 20.2 mW
2	AD7980	ADR291	AD8032	ADA4841	-1V	14.3 mW - 21.3 mW
3	AD7980	ADR291	AD8032	AD8655	0V	26.4 mW - 28.0 mW
4	AD7980	ADR291	AD8032	AD8655	-1V	24.7 mW - 31.7 mW
5	AD7980	ADR291	-none-	ADA4841	0V	7.8 mW - 14.8 mW
6	AD7980	ADR291	-none-	ADA4841	-1V	8.9 mW - 15.9 mW
7	AD7980	ADR291	-none-	AD8655	0V	15.6 mW - 22.6 mW
8	AD7980	ADR291	-none-	AD8655	-1V	19.3 mW - 26.3 mW

4.7 High AC Performance *Circuit from the Lab* with AD7691

A second *Circuit from the Lab* design was desired that strove for maximum performance, regardless of the power cost. The most crucial component in the quest for high SNR and THD is the ADC itself. Thankfully, the choice is straightforward: the AD7690 and AD7691 have significantly better signal-to-noise ratio than any other PulSAR converters. Since the AD7690 and the AD7691 have essentially equivalent performance metrics, the AD7691 was chosen for the lower price.

Table 12: PulSAR Analog-to-Digital Converter Options for High Performance Design

Part#	Resolution (Bits)	Throughput Rate	SNR (dB)	SINAD (dB)	SFDR (dBc)	THD (dB)	ENOBs (Bits)
AD7691	**18**	**250K**	**101.5**	**101.5**	**-125.0**	**-118.0**	**16.6**
AD7690	18	400K	101.5	101.5	125.0	-125.0	16.6
AD7984	18	1.33M	98.5	98.0	112.5	-110.5	16.0
AD7982	18	1M	98.0	97.0	-115.0	-120.0	
AD7693	16	500K	96.0	96.0	120.0	-120.0	15.7
AD7687	16	250K	95.5	95.5	118.0	-118.0	15.6
AD7688	16	500K	95.5	95.0	118.0	-118.0	15.5
AD7685	16	250K	93.5	93.5	110.0	-110.0	15.2

The driver amplifiers are the next most important integrated circuit, since the noise and distortion performance must be commensurate with the laudable performance of the AD7691. Driver amplifiers were considered that were available in an SOIC-8 package and had noise levels less than or equal to the ADA4841 (the default driver on the daughter cards). Those drivers with advertised distortion levels worse than -110dB were excluded, since these would degrade the THD of the overall analog-to-digital conversion process.

Table 13: ADC Driver Options for High Performance Design

Part#	GBP	Slew Rate	V Noise Density	Vcc-Vee	Package	THD
ADA4898-1	65MHz	55V/us	0.9nV/√Hz	9V-33V	SOIC	-116dB
AD797	8MHz	20V/us	0.9nV/√Hz	10V-36V	DIP; SOIC	-120dB
ADA4899-1	600MHz	310V/us	1.0nV/√Hz	4.5V-12V	CSP; SOIC	-123dB
AD8597	**10MHz**	**14V/us**	**1.07nV/√Hz**	**10V-36V**	**CSP; SOIC**	**-120dB**
AD829	120MHz	230V/us	1.7nV/√Hz	9V-36V	DIP; LCC; SOIC	
ADA4004-1	12MHz	2.7V/us	1.8nV/√Hz	10V-30V	SOIC; SOT-23	
AD8009	1GHz	5.5KV/us	1.9nV/√Hz	5V-12V	SOIC; SOT	
AD8011	400MHz	3.5KV/us	2.0nV/√Hz	3V-12V	DIP; SOIC	
ADA4841-1	80MHz	13V/us	2.1nV/√Hz	2.7V-12V	SOIC; SOT	-115dB

Based partly on availability, the AD8597 was the most appealing alternative to the ADA4841 for the high-performance design. The driver features the fourth-best noise performance of all

compatible amplifiers for the daughter card, and is a lower-power and newer version of the AD797. With approximately a 1nV/√Hz noise density, the AD8597 should perform adequately to achieve the rated signal-to-noise ratio of the AD7691.

The voltage reference circuitry should also be updated to minimal-noise ICs. The voltage reference typically populated on the daughter cards is the ADR435, which has $8\mu V_{pp}$. The ADR445 has superior noise performance ($2\mu V_{pp}$) but has diminished output capabilities compared to the ADR435. Neither is clearly better than the other, so both will be considered during the testing phase.

The AD8032 reference buffer, on the other hand, is quite noisy in comparison at $16\mu V_{pp}$. This would seemingly dominate the noise performance of the voltage reference itself, and a higher-quality buffer was sought. When dual-amplifier ICs are sorted by noise density, there are several viable options as seen in Table 14. After excluding the extremely-high-speed amplifiers (which are also more expensive) there are three attractive buffer amplifiers for the high performance design: ADA4004-2, ADA4841-2, and AD8676.

Table 14: Reference Buffer Options for High Performance Design

Part#	GBP	Slew Rate	Vos	I_b	V Noise Density	Vcc-Vee	Package
ADA4004-2	**12MHz**	**2.7V/us**	**40uV**	**40nA**	**1.8E-9**	**10V-30V**	**SOIC; SOP**
AD8002	600MHz	1.2KV/us	2mV	3uA	2.0E-9	6V-12V	DIP; SOIC; SOP
ADA4841-2	**80MHz**	**13V/us**	**40uV**	**3uA**	**2.1E-9**	**2.7V-12V**	**SOIC; SOP**
AD8022	130MHz	50V/us	1.5mV	2.5uA	2.5E-9	4.5V-26V	SOIC; SOP
AD8012	350MHz	2.25KV/us	1mV	3uA	2.5E-9	3V-12V	SOIC; SOP
AD8008	650MHz	1KV/us	500uV	4uA	2.7E-9	5V-12V	SOIC; SOP
AD8676	**10MHz**	**2.5V/us**	**12uV**	**500pA**	**2.8E-9**	**10V-36V**	**SOIC; SOP**

The result of these component decisions yield a high performance design that is based on the AD7691 analog-to-digital converter, the AD8597 driver amplifiers, the ADR435 five volt voltage reference, and the ADA4004-2 buffer amplifier. Although alternatives for these components will be experimented with to verify the logic of the design process, this circuit should provide nearly the highest possible performance from a PulSAR ADC.

4.8 Performance Optimizations

Through the course of the background research, it was discovered that subtle tweaks to the circuitry surrounding the ADC could improve performance. Most often, these optimizations involved refining the matching between the ADC driver and the ADC, or aiming to reduce noise on the voltage reference (as seen in Equation (22), small amounts of reference noise can result in code errors).

4.8.1 Matching the RC Filter to the Driver and ADC

Despite the necessity of a sample-and-hold amplifier, modern SAR converters do not require a separate SHA; the switched-capacitor networked used in the internal DAC can serve the same function without duplicating circuitry [**39**]. While the switched-capacitor network truly has a structure per Figure 11, it can be modeled by a much simpler series resistance and capacitance, represented by R_2 and C_2 in Figure 59.

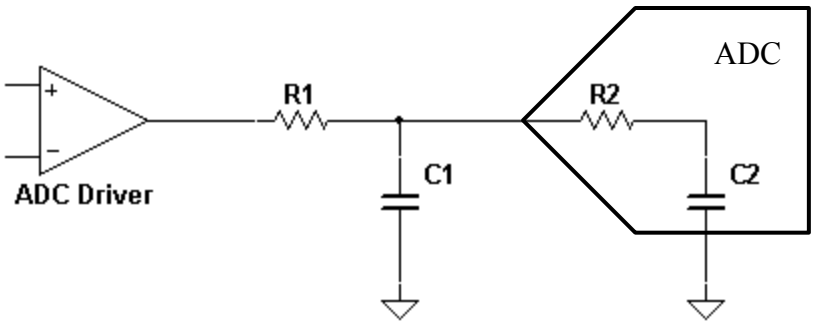


Figure 59: Typical Sample-and-Hold Input to a SAR ADC

In practice, an external RC network – shown by R_1 and C_1 – is used to present a predictable timing constant to the ADC driver. The values of the ADC's internal resistor and capacitor are subject to higher tolerances, making the acquisition time of the ADC more easily controlled by an external RC network. When choosing the resistor and capacitor values for the external network, the effective load impedance at the ADC driver must be considered; certain loading conditions can cause the amplifier to become unstable and oscillate. The effective load resistance and capacitance can be derived by first finding the total impedance presented by Figure 59.

$$Z_{SAR} = R_1 + \frac{1}{j\omega C_1 + \frac{1}{R_2 + \frac{1}{j\omega C_2}}} \tag{48}$$

Equation (48) will first be simplified to the resistor-capacitor network shown in Figure 60, with expressions for R_S, R_P and C_P in terms of R_1, R_2, C_1, and C_2.

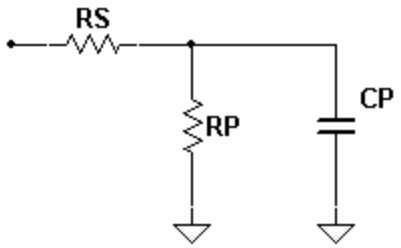


Figure 60: Partial Simplification of Z_{SAR}

The equivalent impedance of the intermediate network is given by Equation (49).

$$Z_{INTER} = R_S + \frac{1}{\frac{1}{R_P} + j\omega C_P} \tag{49}$$

Equations (48) and (49) are in the same form, so the constant factors can be equated.

$$R_1 = R_S \tag{50}$$

The remaining complex terms of Equation (48) and (49) can also be equated. Here, the left hand side of Equation (51) is a simplified form of the second term in Equation (48).

$$\frac{\omega R_2 C_2 - j}{\omega(C_1 + C_2) + j\omega^2(R_2 C_1 C_2)} = \frac{1}{\frac{1}{R_P} + j\omega C_P} \tag{51}$$

Once both sides of Equation (51) are inverted, then the real component of the left side must equal the real component of the right side, yielding a solution for R_P:

$$\frac{1}{R_P} = \mathrm{Re}\left\{\frac{\omega R_2 C_2 - j}{\omega(C_1 + C_2) + j\omega^2(R_2 C_1 C_2)}\right\} \tag{52}$$

$$R_P = \frac{(\omega R_2 C_2)^2 + 1}{\omega^2 R_2 C_2^2} \tag{53}$$

Similarly, the imaginary component of each side of Equation (51) must be equal, which gives an expression for C_P:

$$\omega C_P = \mathrm{Im}\left\{\frac{\omega R_2 C_2 - j}{\omega(C_1 + C_2) + j\omega^2(R_2 C_1 C_2)}\right\} \tag{54}$$

$$C_P = \frac{\omega(\omega^2 C_1 R_2^2 C_2^2 + C_1 + C_2)}{(\omega R_2 C_2)^2 + 1} \tag{55}$$

With the intermediate form of Figure 60 solved, the effective load resistance and capacitance can be solved. Most ADC driver datasheets model the load as a parallel resistor and capacitor from the output to ground as in Figure 61.

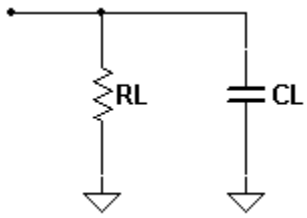


Figure 61: Effective Load Impedance at ADC Driver Output

The impedance expression for this circuit is given in Equation (56):

$$Z_{EQ} = \frac{1}{\frac{1}{R_L} + j\omega C_L} \tag{56}$$

Equations (49) and (56) are both inverted and equated. The real components can then be used to find R_L:

$$R_L = \mathrm{Re}\left\{ R_S + \frac{1}{\frac{1}{R_P} + j\omega C_P} \right\} \tag{57}$$

$$R_L = \frac{R_S^2 + 2R_S R_P + R_P^2 + \omega^2 R_S^2 R_P^2 C_P^2}{R_S + R_P + \omega^2 C_P^2 R_P^2 R_S} \tag{58}$$

A similar process can be done to equate the imaginary part of Equation (49) to the imaginary part of Equation (56). This results in C_L:

$$\omega C_L = \mathrm{Im}\left\{ R_S + \frac{1}{\frac{1}{R_P} + j\omega C_P} \right\} \tag{59}$$

$$C_L = \frac{R_P^2 C_P}{R_S^2 + 2R_S R_P + R_P^2 + \omega^2 R_S^2 R_P^2 C_P^2} \tag{60}$$

The expressions for R_S, R_P, and C_P can be substituted into Equation (58) and (60) from Equations (50), (53), and (55). For the design of the daughter card with the PulSAR converters, the external RC network typically has $R_1 = 33\Omega$ and $C_1 = 2.7\text{nF}$. The values for R_2 and C_2 are specified in the PulSAR datasheets and are 400Ω and 30pF for the AD7984. With the substitution of these constants, Equations (58) and (60) were plotted with MATLAB (see Appendix C). This resulted in Figure 62 and Figure 63, which show the resistive and capacitive components of the load presented to the ADC driver.

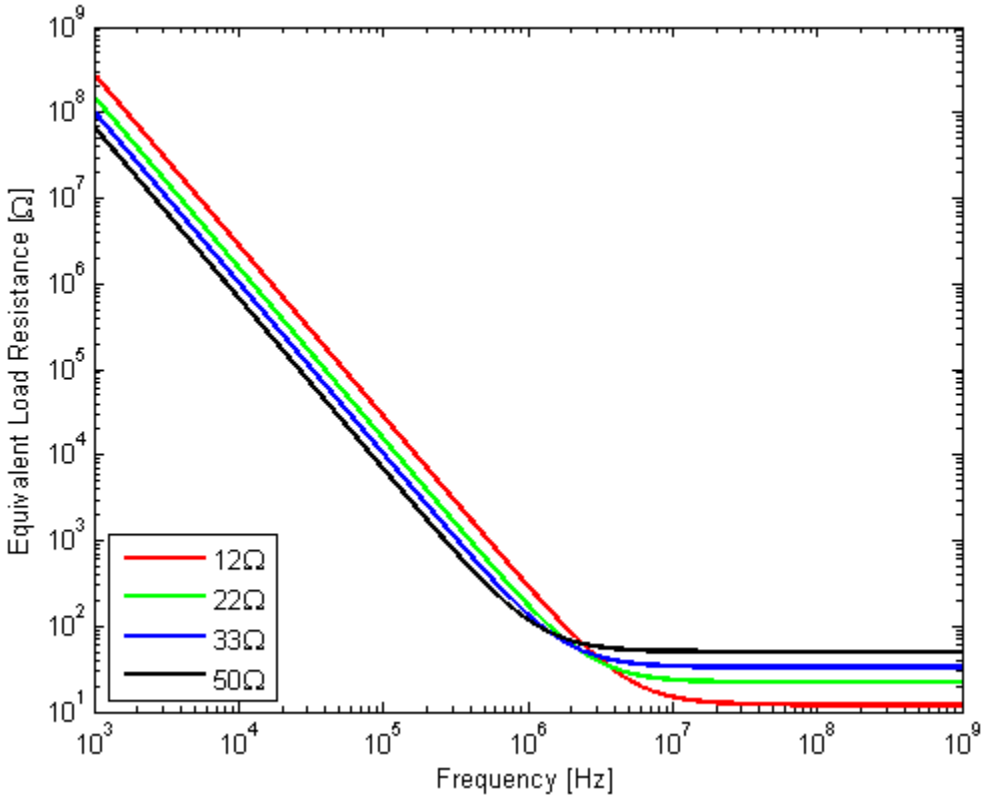


Figure 62: Effective Resistive Load at ADC Driver

This plot shows that for input frequencies from 1 kHz to 100 kHz, the effective load resistance at the ADC driver will be above 10 kΩ. At low frequencies, the two capacitors of Figure 59 become more like open circuits, preventing current flow to ground and making the effective resistance appear in the megaohm range. As frequency rises above 1 MHz, the exponential drop in resistance levels off and converges on the value of R_1.

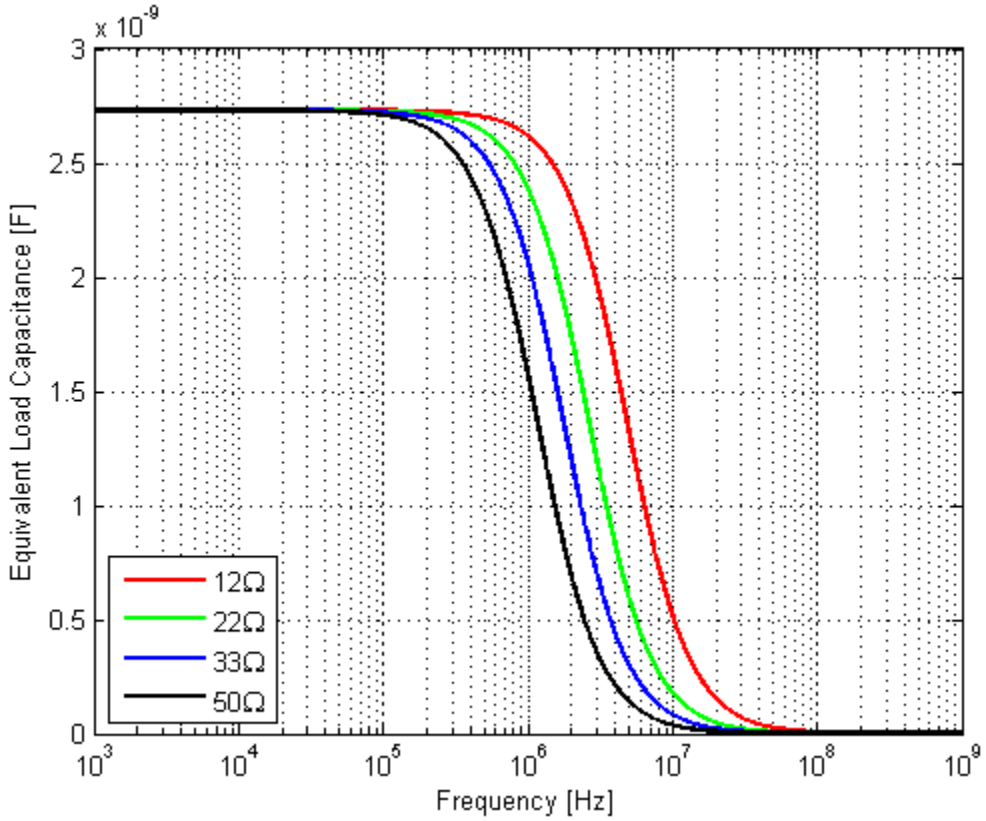


Figure 63: Effective Capacitive Load at ADC Driver

The effective load capacitance remains steady at C_1 for the first five decades of frequency. At higher frequencies, the capacitors of Figure 59 behave more like short circuits, and the plot drops to zero Farad. When constrained to a narrow range of relevant frequencies, the graph shows very little variation of the effective capacitance even when sweeping the values for R_1.

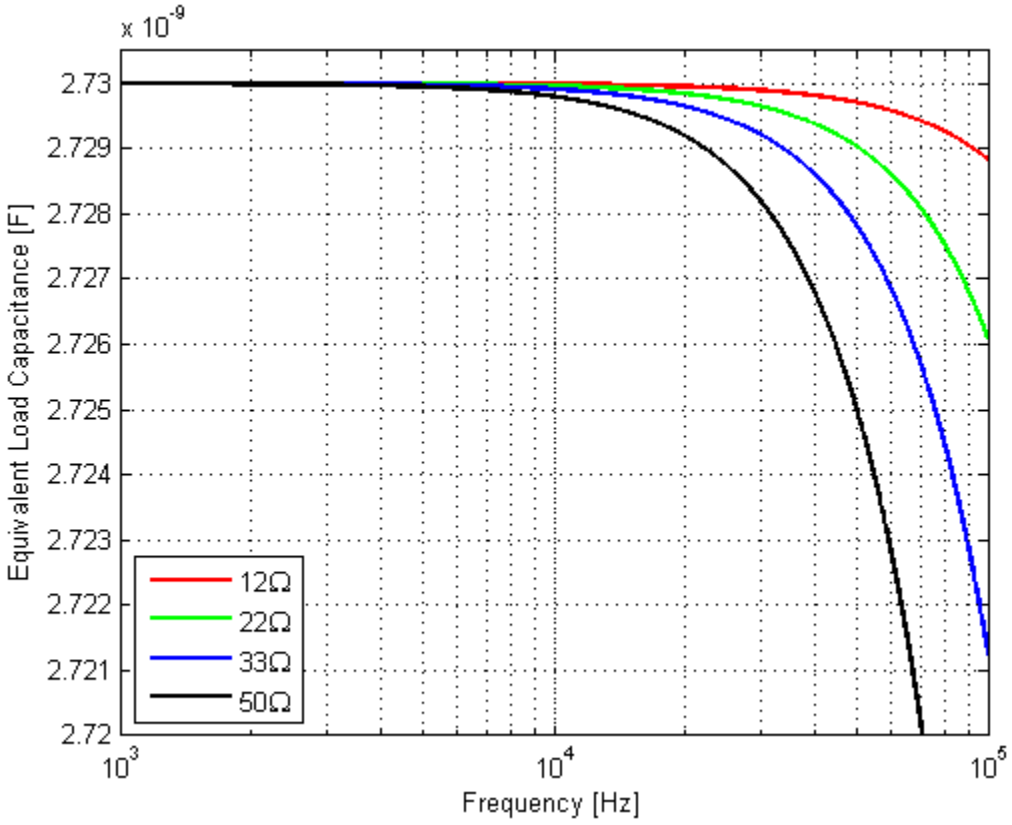


Figure 64: Effective Load Capacitance for Low Input Frequencies

At 100 kHz, tripling the value of R_1 causes less than a 10 pF drop in the effective capacitance. None of the ADC drivers used in the PulSAR daughter boards were sensitive to such small changes in the load, suggesting that moderate changes to R_1 should not visibly affect performance. Based on this mathematical analysis, the 33Ω resistor used in the external RC on the standard daughter board should be suitable for all input frequencies.

4.8.2 Removing the Reference and Common-Mode Buffers

Alternately, if the voltage reference noise is already low enough that a low-pass filter is unnecessary, it could equally unnecessary to have the reference buffer installed. The AD8032 that is in place on the daughter card schematic is a dual-amplifier integrated circuit that buffers V_{REF} to the ADC as well as buffering V_{REF} before it is divided down to V_{CM} for the input signals.

Current is drawn in the V_{CM} voltage divider (a maximum of 4.23mA), although this is often well below the current source capability of a voltage reference IC. The removal of the buffer has the potential to reduce overall power consumption (one fewer integrated circuits) as well as reduce the noise injected by the AD8032. This circuit modification is pictured in Figure 65.

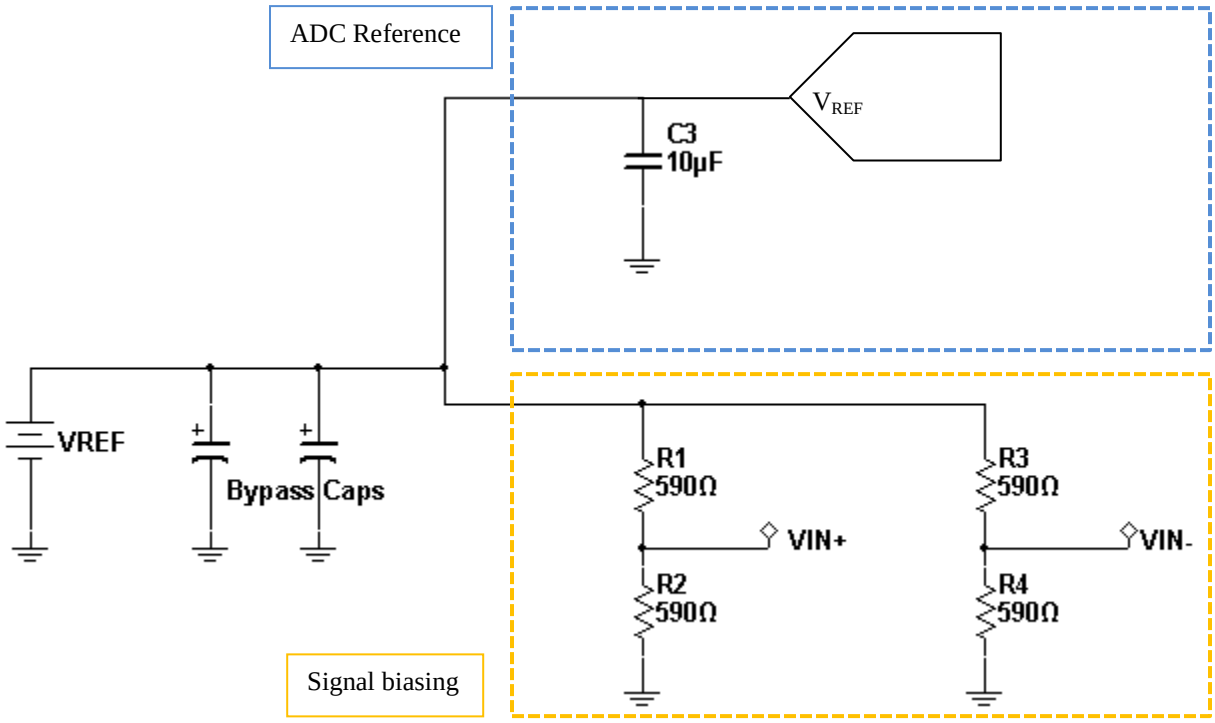


Figure 65: Voltage Reference Circuitry with no Buffers

The potential problem with this alteration comes from the capacitive drive capability of the voltage reference. The ADC reference capacitor is quite large at 10µF and it presents a dynamically switching load as the conversions take place. This can easily destabilize the node and cause oscillations in the ADC output code [**9**]. The datasheets and application notes for the PulSAR ADCs state that a reference buffer can be left unpopulated if the voltage reference is adequate, although it only recommends the ADR43x series for this application.

While left unlisted, it is possible that other references would be sufficient to run PulSAR ADCs at full performance, even if the throughput might need to be reduced for stability. A test plan was drawn up to compare the performance of the ADR435 to the ADR445 (both 5V references with comparable parameters) with and without the AD8032 buffers installed.

4.9 LABVIEW APPLICATION

With the migration of the PulSAR evaluation boards to the System Demonstration Platform (SDP), the software program used to retrieve and analyze the ADC output data had to be rewritten. The older software packages used with the Evaluation Control Board (ECB) and the Converter Evaluation and Development (CED) were not based on a Blackfin microprocessor, and did not necessarily communicate with the SPORT protocol over USB. The low-level internals of the software had to be modified mainly to support the Blackfin, and the software re-design provided an opportunity to remedy other shortcomings in the older software.

4.9.1 ECB and CED Software Programs

When a customer is testing a PulSAR converter, the software interface is the most visual aspect of the entire evaluation system. As such, Analog Devices places great important on developing a consistent look and feel to the user interface (to aid company recognition) and ensure that all software features are accessible and intuitive. To minimize the learning curve of the new SDP software, the ECB and CED software packages were examined for areas that could be improved upon.

The software module for the ECB had a much outdated look and feel compared to current Analog Devices' software. The user interface contained excess modules irrelevant to PulSAR

testing cluttering the front panel. The poor layout also hampered the learning curve; the options for viewing the time-domain waveform or the FFT are obfuscated, and even the button to read data is relatively hidden among a myriad of other buttons. Figure 66 points out specific weaknesses in the ECB software design.

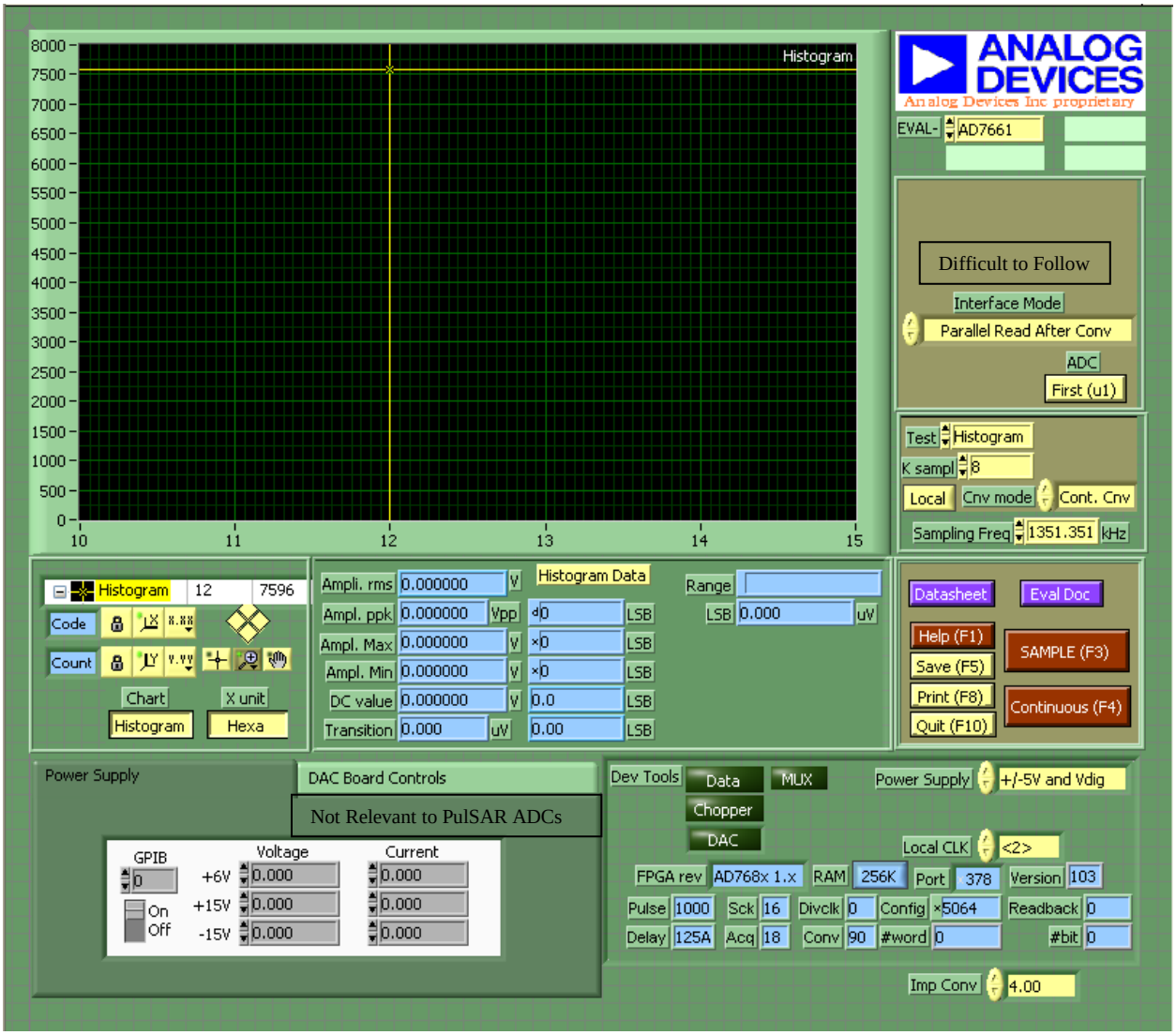


Figure 66: Evaluation Control Board (ECB) Software Front Panel

The ECB's source code was also labyrinthine and sparsely documented, which increased the time needed for future developers to understand or extend the code. When the use of the parallel

port interface and the ADSP-2189 microcontroller are also factored in, any attempt at adapting the ECB code for the new SDP application would have taken longer than creating a new application from the ground-up.

The CED software improved upon the ECB software in several aspects. First, its look and feel was more contemporary. The layout of the software was more user-friendly and it required less of a learning curve to operate. The FFT analysis in ECB was analyzed and necessary changes were made to create a better solution to incorporate into the CED software. Despite having a good FFT, the software lacked a dynamic histogram and automatic recognition for the different ADCs.

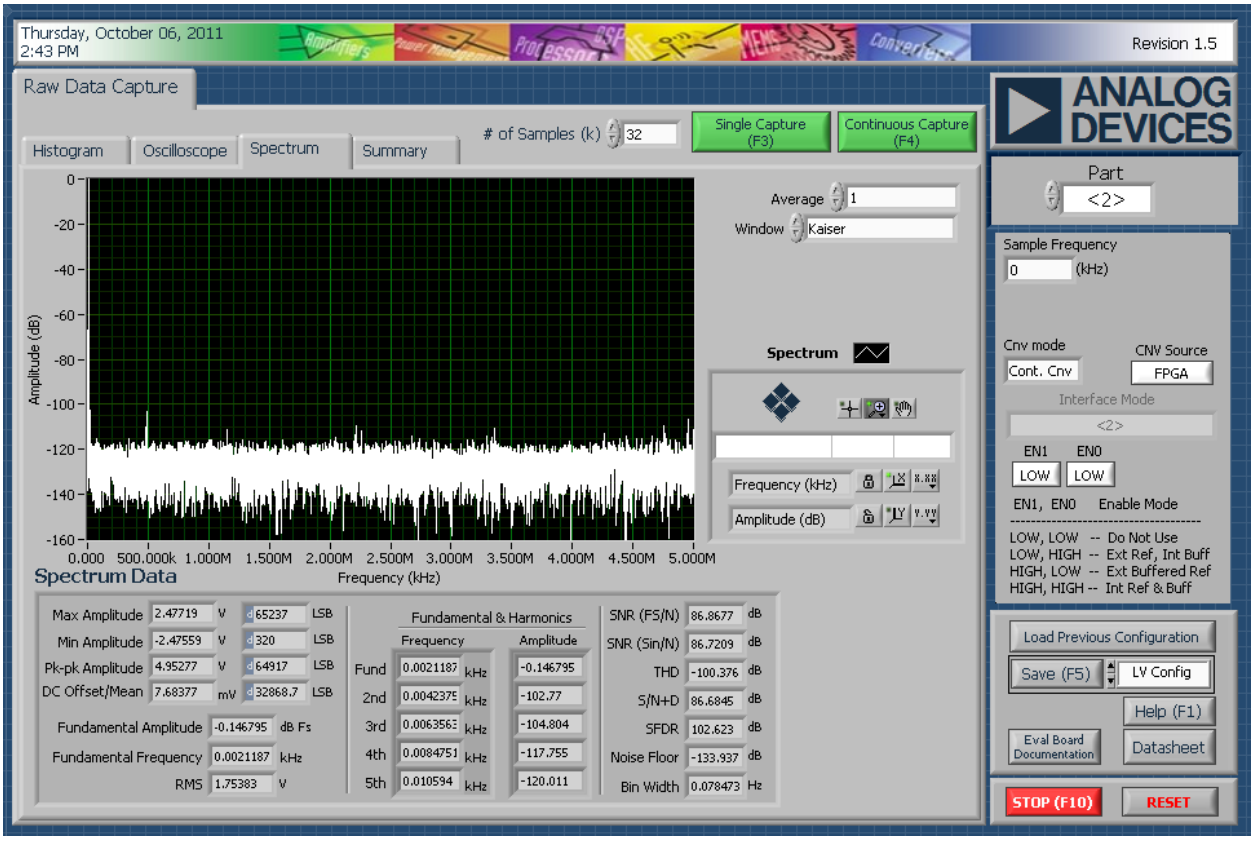


Figure 67: Converter Evaluation and Development (CED) Software Front Panel

4.9.2 Software Basis and Desires

The SPORT testing interface was developed by Analog Device's engineers as an example of communication between the SDP and LabVIEW software applications. This application was basic, lacked a polished user interface, and could only communicate via a breakout board.

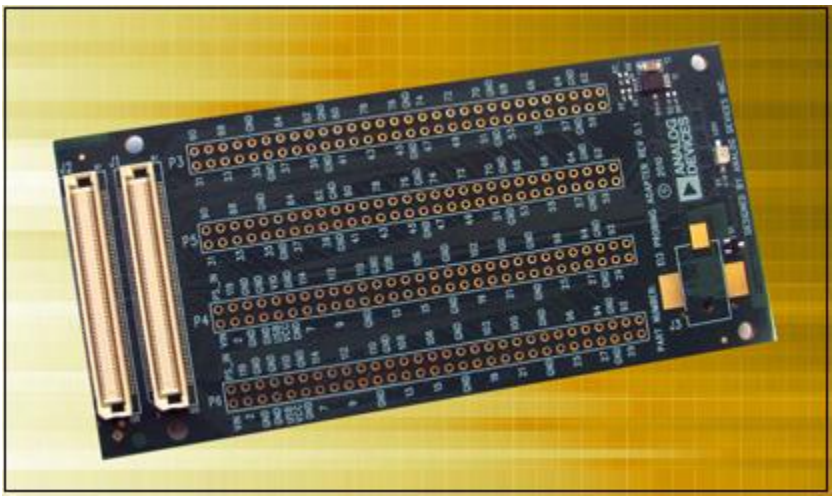


Figure 68: SDP Breakout Board [64**]**

The breakout board, shown in Figure 65 is a tool for use with the SDP to allow easy access to the connections between the SDP and daughter boards. Although the board allows customers to trace each of the data lines, it degrades performance at higher sampling rates. Despite these shortcomings, the SPORT testing interface was used as the initial building block in the design of a new software module. Communication VIs were ported from this software to expedite system design. The SPORT interface front panel, seen in Figure 69, contained many tools for debugging communications which were not ported to the new software, but stilled played a vital role in the new software design.

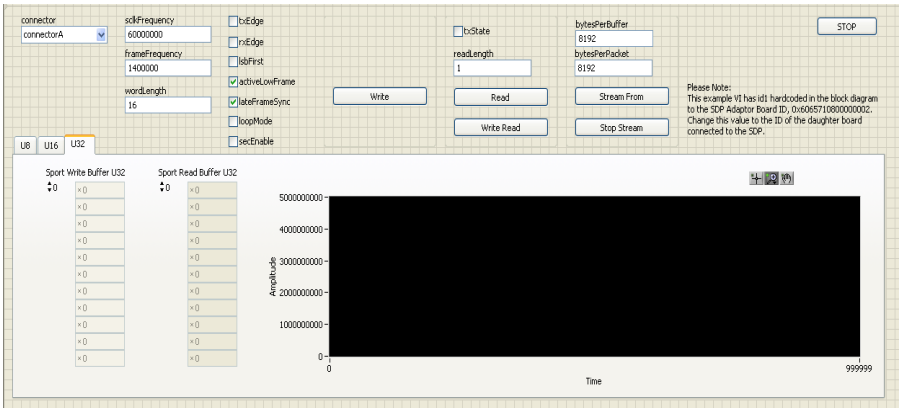


Figure 69: SPORT Interface Front Panel

Throughout the re-design of the software several features were proposed for the software module. These ideas included features to ease use, improve the functionality of the GUI, and improve calculations of ADC parameters. Some of these features were suggested by Analog Device's engineers, but the design and implementation on these features was left to the MQP group. Other features were completely added on initiative by the MQP group.

One feature designed by the MQP group was an automatic data porting system. Data relevant to daughter card testing and characterization, such as SNR, SINAD, THD etc. were saved in a .tsv file. This data could then be imported into excel spread sheets for easy analysis. The application stored data in different files named after the tested ADC. This feature was removed from the final release version as it added files without the consent of the user and could slow down data collection. This slow-down was a result of the application opening and closing the data file each time a reading was taken.

The GUI needed to provide the user with data reading and streaming capabilities. The software also needed to provide a graph of the waveform, FFT, and code histogram. Each of these graphs would provide the user with a specific type of signal analysis: time domain, frequency domain,

and DC performance, respectively. The GUI also needed to allow the user to change the sampling frame length (total amount of samples taken in a single measurement), sampling frequency, as well as the frequency of the SPORT clock used for communication between the SDP and attached ADC.

The application also needed to be able to capture the data and process it to calculate various parameters. Important AC parameters such as SNR, SINAD, THD, and dynamic range were displayed along with the FFT. Parameters pertaining to time domain analysis such as the maximum and minimum voltages were also calculated and displayed in the GUI. Although many of these calculations were ported from the ECB and CED software, testing revealed several of these calculations needed to be modified. These modifications are discussed in Chapter 5.

The application also needed to support single ended input ADCs as well as fully-differential input ADCs. Fully-differential PulSAR ADCs transmit their conversions in two's complement binary. To properly perform calculations with the received data, the system needed to convert data from differential ADCs from two's complement to unsigned binary. The software had to keep intelligently compensating for this change in data type so the time domain and histogram graphs would properly reflect the received data.

It was decided that the software module should automatically determine what ADC was attached to it. Each daughter card has an EEPROM on it that is programmed with a code reflecting the attached ADC. The software was designed to check the code read from the EEPROM against a master database containing all relevant EEPROM codes. Automatically determining the attached ADC was a new feature meant to ease use of the overall testing platform.

The software was designed to allow the user to select the data frame length for the system to either read or stream. The software was outfitted with intelligent checks to limit the user to allowable frame lengths depending on the word size from the ADC, the sampling rate, the system clock, and the data collection method (reading or streaming). The software was also outfitted with a check to ensure that the sampling clock is an integer divisor of the SPORT clock. It was also programmed to ensure that the overall data transfer would leave enough settling time for the ADC, as discussed in section 2.3.1 Sample-and-Hold Circuit.

An offline mode capable of re-loading previously saved data was also added. In older software revisions the user would have to establish a connection to a board to be able to load any previously saved data. This meant that a usable board had to be available to view the analysis of saved data. This new feature would allow people who do not have a readily available SDP and daughter card to still view the data analysis. This could be a desirable feature in cases where people in different locations want to view the same data, but it is not guaranteed both would have access to an SDP and daughter card.

An easy link to the datasheet and Evaluation Note of the selected ADC should be available from the software itself. The software should let users save the captured data and reload it for analysis. The software should provide users with an easy way to save images of the waveform and the analyzed data. It should be possible to swap the daughter cards while the software is running and be able to Read/Stream data from the new board.

Chapter 5: Testing and Results

Chapter 4 elucidated the specific steps taken to implement the end goals. The chapter was organized into three separate sections: schematics, testing and applications, and software. The coming chapter examines the results of the experimental investigations. First the chapter details the exhaustive testing undertaken to prove the performance of the motherboard, surfboard, and expansion board. The chapter then elaborates on the conclusions and ramifications of both the low power and high AC performance *CftL*s developed and tested during the scope of this project. The chapter then contemplates the results of several stand-alone tests that were conducted. Some of these stand-alone tests are not discussed in Chapter 4 because their relevance was only discovered midway through the testing phase. Lastly, the final LabVIEW program's features are introduced with explanations of how they ultimately contributed to a more polished user interface.

There are several notable sections missing from this chapter. Time constraints prevented the group from being able to test several of the schematics developed throughout this project. First, the group was unable to build and test the integrated power supply motherboard. The group was also unable to characterize the performance of neither the fully-differential daughter card nor the

in-amp surf and expansion boards. The characterization of these boards is suggested in Chapter 6: Future Work.

5.1 General Testing Set-Up and Procedure

Throughout the project a general hardware testing procedure was developed to prevent discontinuities in the testing setup from skewing the results gathered. First, the voltage rails of the power supply were set to the appropriate levels. A detailed discussion of these power rails can be found in section 4.4 Power Circuitry Design. Next, the power supply was turned off and connected to the daughter card being tested.

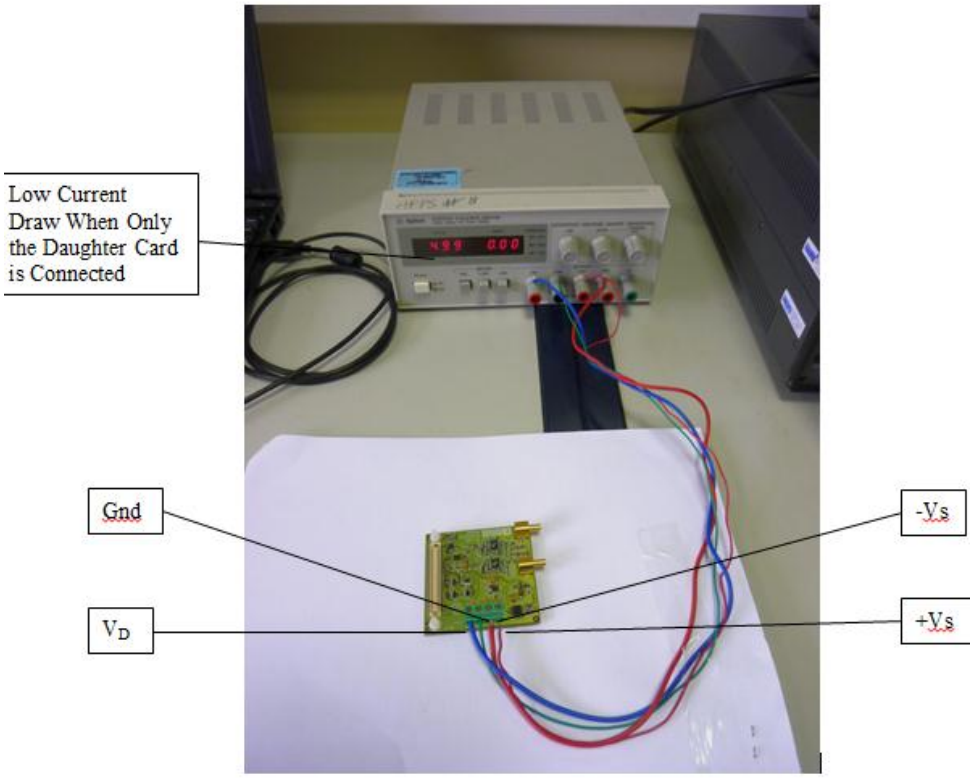


Figure 70: Daughter Card Connected to a Power Supply

The power supply was then turned on and the current being drawn from the power supply was compared against the expected values, listed in Table 15.

Table 15: Current Draw of a Daughter Card

Supply	*Typical Current Draw*
+Vs	0-10 mA
-Vs	2.3-2.4 mA
+V_{DD}	0.4nA-1.05mA

Verification of the current draws by the daughter card ensured proper connection of all components changed since previous tests were conducted. Next, an SDP was attached to the daughter card, shown in Figure 71.

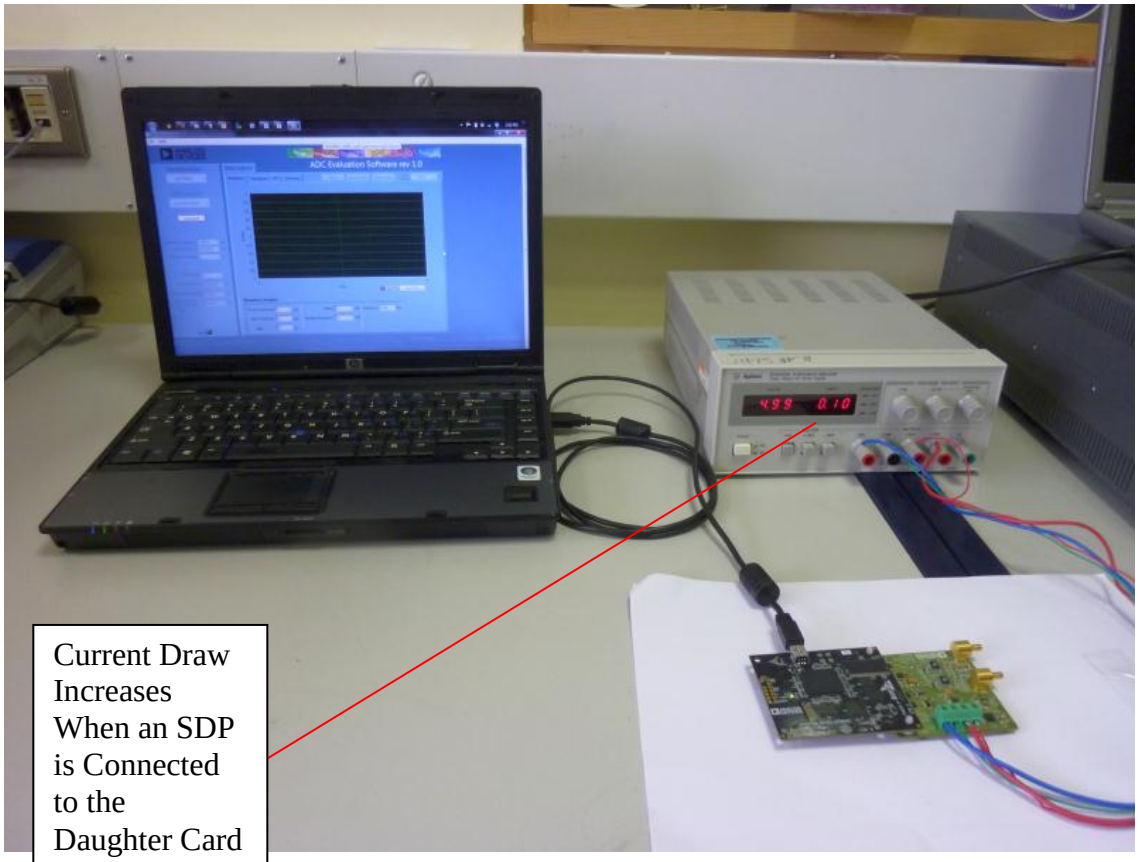


Figure 71: SDP Connected To a Daughter Card

Table 16 shows the current drawn by the testing platform when an SDP was attached. Although the current load presented by the daughter card itself stayed fairly constant, the +Vs supply showed an increase in supply current drawn through the system by the SDP. The current draw changed negligibly due to changes in ADC driver, reference buffer, etc. However, the current drawn by the ADCs ($+V_{DD}$) changed by a considerable amount depending on the ADC.

Table 16: Range of Current Drawn by PulSAR Daughter Cards During Sleep Mode

Supply	*Typical Current Draw*
+Vs	*110-120 mA*
-Vs	*2.3-2.4 mA*
+V_{DD}	*.4nA-1.05mA*

Next the AP sys-2522 precision audio source was attached to the daughter card, seen in Figure 72.

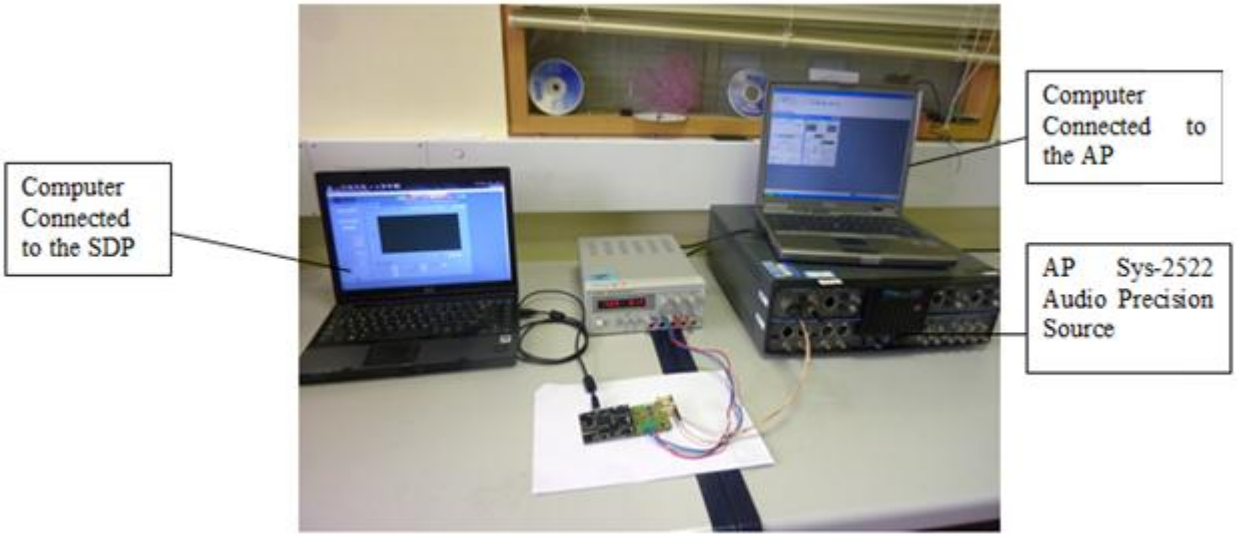


Figure 72: Full Testing Setup

The AP output waveform was set to a sine-wave and the frequency was adjusted to the given ADC's datasheet specification. These values are summarized in Table 17.

Table 17: ADC Input Testing Tones

ADC	SNR Tone	SINAD Tone	THD Tone
AD7685 [65**]**	20 kHz	20 kHz	20 kHz
AD7691 [66**]**	1 kHz	1 kHz	1 kHz
AD7946 [67**]**	20 kHz	20 kHz	20 kHz
AD7980 [8**]**	10 kHz	10 kHz	10 kHz
AD7982 [68**]**	1 kHz	1 kHz	10 kHz
AD7984 [61**]**	1 kHz	10 kHz	10 kHz

Next, a measurement was taken and the current draw was once again verified. Table 18 shows the typical load currents when a measurement is being taken. Since the PulSAR parts are SAR ADCs, their current draw scales with sampling rate. This property is reflected in the third row of Table 18.

Table 18: Range of Current Drawn by PulSAR Daughter Cards During a Conversion

Supply	Typical Current Draw
+Vs	140-150 mA
-Vs	2.3-2.4 mA
+V_{DD}	.1mA -2mA

The AP's output magnitude was then adjusted using the device's software control panel so that the sampled waveform was 0.5dB below full scale. The AP offered dynamic output impedance based upon the output tone's frequency; this meant the output magnitude had to be adjusted at each frequency. 0.5dBfs was not an arbitrary value; it was based on the datasheet specifications as well as two other key factors. First, a signal too large in magnitude would be clipped either by the ADC input amplifiers or the ADC itself. An example of this clipping is shown in the frequency domain in Figure 73.

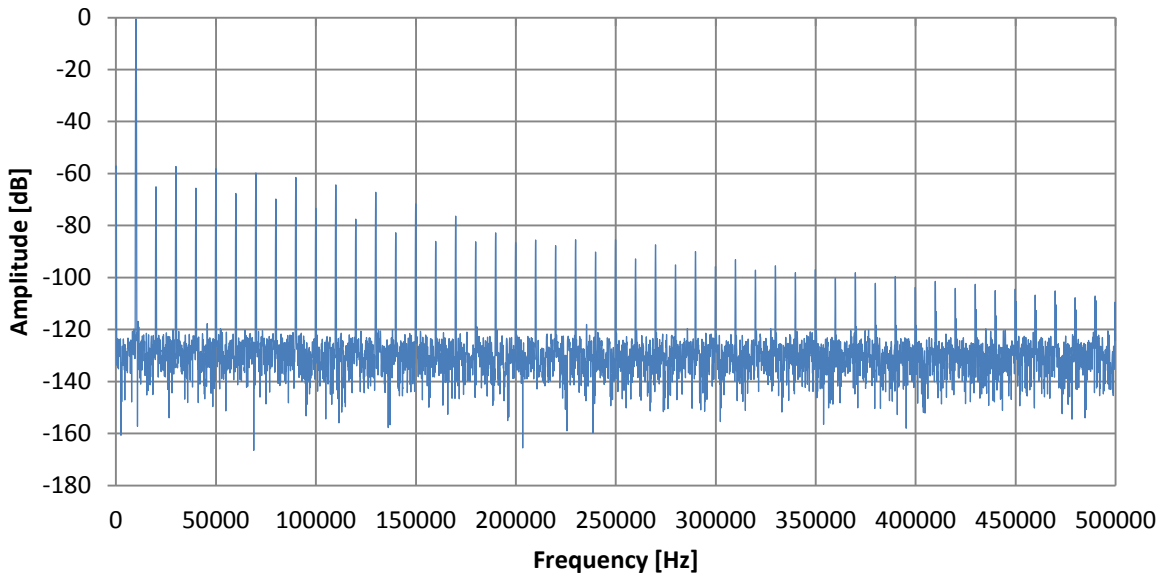


Figure 73: Frequency Domain of a Clipped Sine Wave

If the input tone were too far below full scale, the testing would not evaluate the full potential of the pertinent components. At this point the attached daughter card was ready to be tested and characterized.

Testing and characterization of each board was done in a meticulous fashion. Once the board was ready to be tested it was placed in an initial state. A minimum of twenty-four measurements were taken using the application discussed in Section 4.9.2 Software Basis and Desires. The variable being analyzed was then changed and a new set of measurements was taken. These measurements were then exported to Microsoft Excel where various tables and graphs were created to succinctly display the gathered data. These visuals were then analyzed by the group to determine the next variable that warranted testing.

5.2 Evaluation of Motherboard, Expansion Board, and Surfboard

Despite the several-week delay between designing the three flexible-driver boards and having each fabricated and shipped to the site, all three boards arrived in time for substantial testing. The motherboard (pictured in Figure 74) is similar to the original daughter board in terms of the circuitry and layout, although it has a larger footprint and includes the 5x2 connector for the expansion board as well as two 7-pin headers for the surfboard.

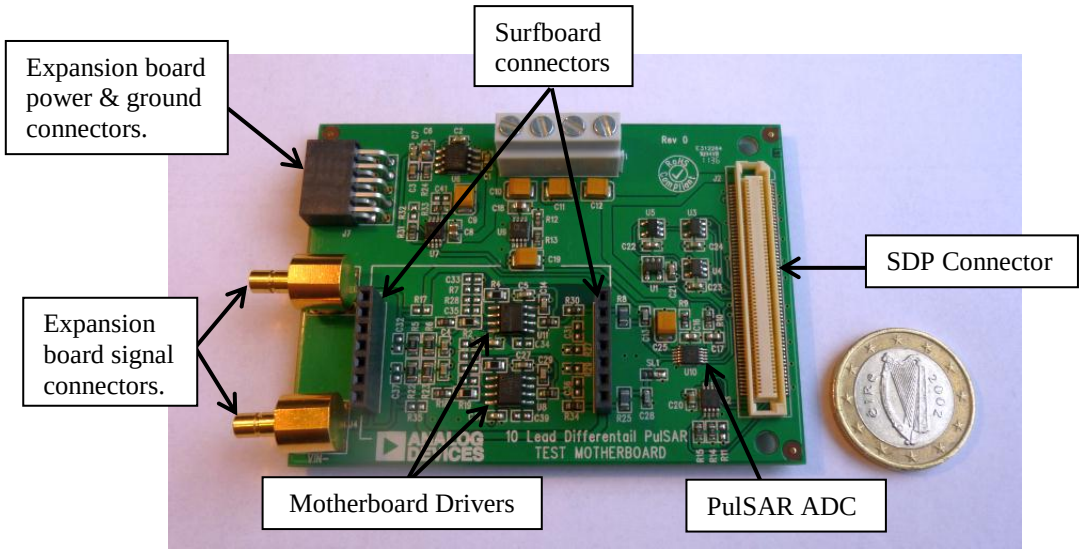


Figure 74: Photograph of the Motherboard

The surfboard is shown in Figure 75 and essentially replaces the motherboard driver circuitry that would lie beneath it. The pins for the motherboard headers extend downwards from the backside of the surfboard and are not visible in the photograph below.

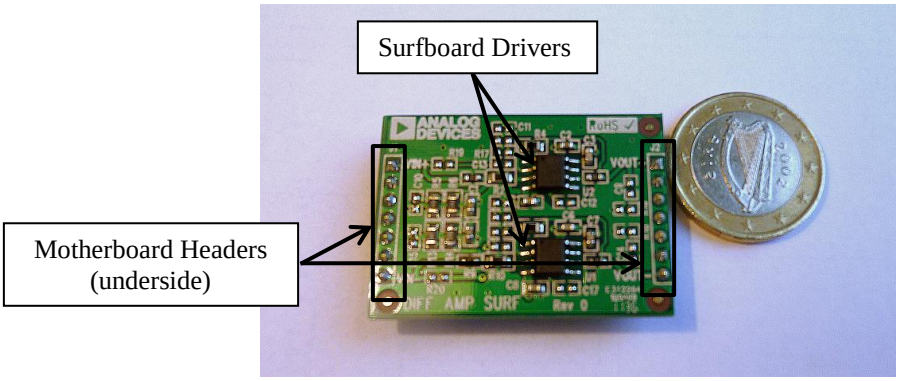


Figure 75: Photograph of the Surfboard

The expansion board is much larger than the surfboard since one edge must be the same length as the side of the motherboard. The driver circuitry is identical to that used on the motherboard and surfboard, although the expansion board uses high-quality SMB connectors for the input and output signals.

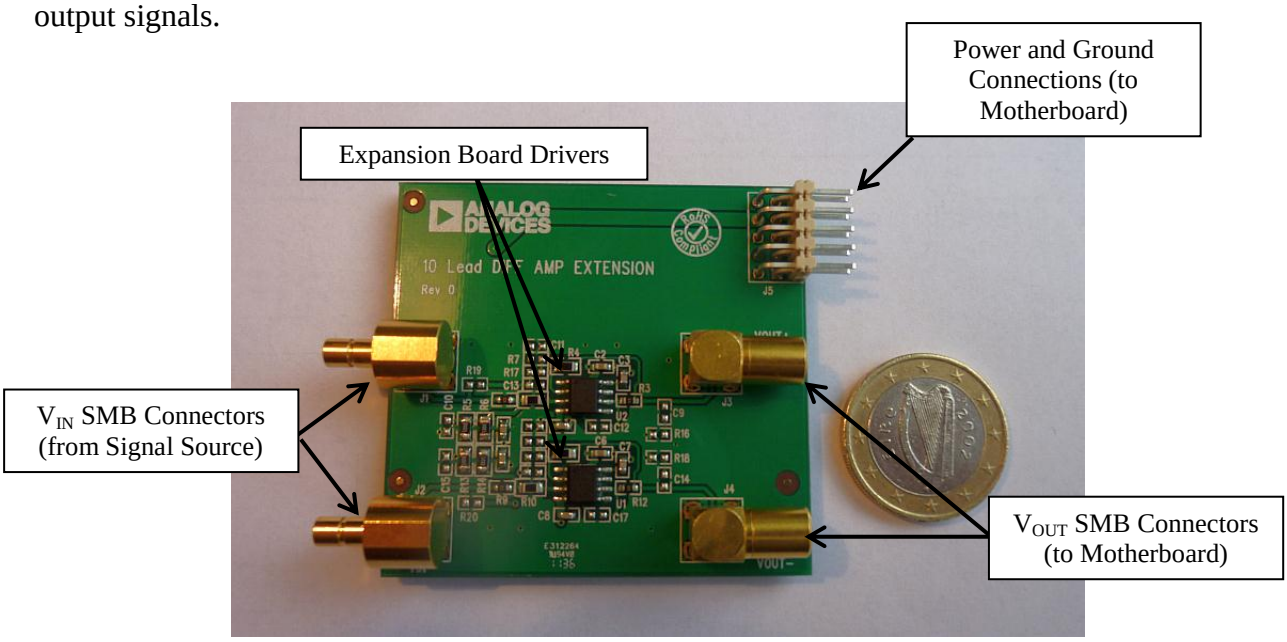


Figure 76: Photograph of an Expansion Board

The first step in evaluating these three boards was to verify that the motherboard maintained performance levels commensurate with the original daughter card. The added connectors and configuration networks were not predicted to degrade performance, but layout changes could have had unexpected effects. Assuming that the daughter card and motherboard are equivalent,

the merits of the expansion board and surfboard could be evaluated to select one or both to be incorporated into the final testing platform design.

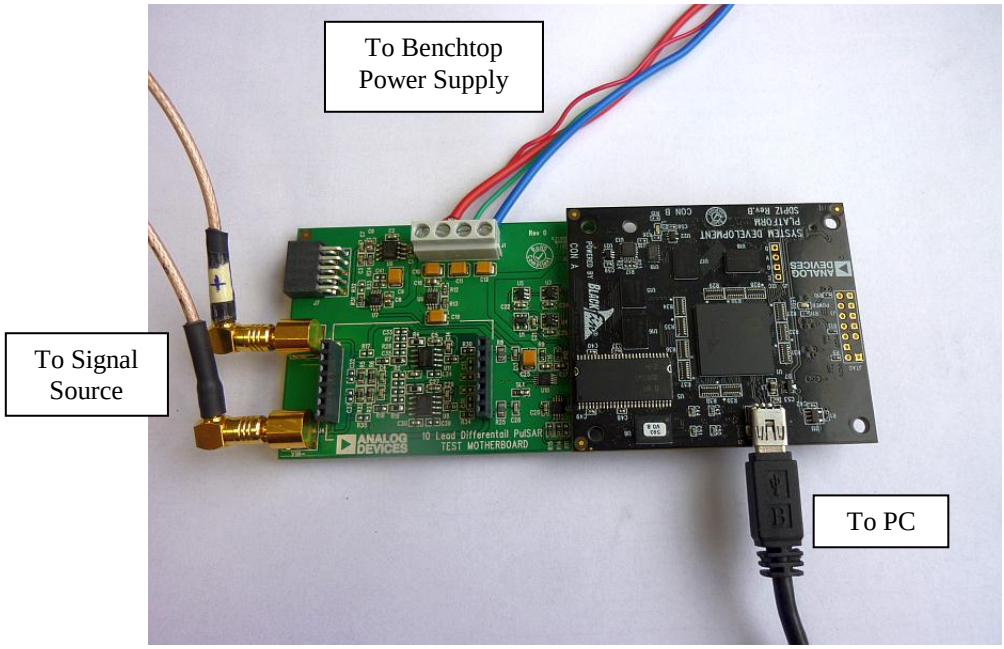


Figure 77: Full Motherboard Setup

As pictured in Figure 77, the motherboard connects to the SDP and the signal source in the same manner as the original daughter card. The motherboard was compared against the daughter card with two different ADCs – the 16-bit AD7685 that operated at a low 250 kSps throughput, and the 18-bit AD7982 at a higher throughput of 1 MSps.

For the AD7685, the sampling rate was swept from 50 kSps to 250 kSps to see the full range of motherboard and daughter card performance. The input tone used was the -0.5 dBFS sinusoid at 20 kHz that was specified in the datasheet. The results – listed in Table 19 – show that both the motherboard and the daughter card had SNRs within one half decibel of each other, suggesting that the motherboard alterations did not negatively impact performance. Peculiarly, the

motherboard had higher metrics than the daughter card, although this could have been a reflection of variation in the individual components on the PCBs.

Table 19: Motherboard and Original Daughter Card Measurements with AD7685

Configuration	Sampling Rate [Hz]	Average SNR	Average SINAD	Average THD
Motherboard	50000	90.244	89.667	-99.374
	100000	90.804	90.351	-101.221
	150000	90.886	90.334	-100.081
	200000	91.428	90.839	-100.304
	250000	91.650	91.073	-100.337
	Total:	**91.006**	**90.453**	**-100.231**
Original Daughter	50000	90.033	89.511	-99.843
	100000	90.521	90.193	-102.376
	150000	90.689	90.324	-101.652
	200000	90.836	90.497	-102.034
	250000	90.746	90.397	-101.630
	Total:	**90.562**	**90.180**	**-101.505**

When the testing was repeated with an 18-bit AD7982, the input tone was switched to a 1 kHz sine wave at -0.5 dBFS (again to match the datasheet specifications). The sampling rate was swept across four values and the typical signal-to-noise ratio for the AD7982 was over 95.5 dB, substantially higher than the lower-resolution AD7685.

Table 20: Motherboard and Original Daughter Card Measurements with AD7982

Configuration	Sampling Rate [Hz]	Average SNR	Average SINAD	Average THD
Motherboard	50000	95.600	95.508	-111.185
	200000	95.618	95.519	-110.995
	800000	95.799	95.672	-110.306
	1000000	95.762	95.647	-110.572
	Total:	**95.713**	**95.603**	**-110.694**
Original Daughter	50000	95.440	95.410	-114.235
	200000	95.491	95.460	-114.203
	800000	95.728	95.692	-114.128
	1000000	95.672	95.645	-114.646

	Total:	**95.581**	**95.551**	**-114.319**

The AD7685 and AD7982 testing indicated that the motherboard did not degrade the daughter card performance, so the group proceeded to evaluating the expansion board and the surfboard. Using the same motherboards as earlier, the expansion board setup (Figure 78) and the surfboard setup (Figure 79) were tested at a range of throughputs to see if there were any performance losses from the lengthened signal paths.

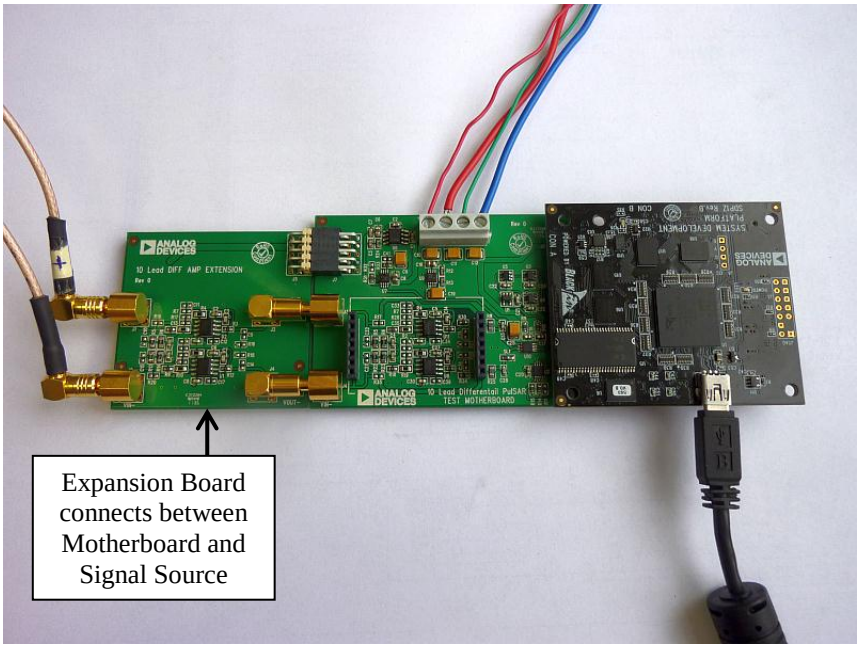


Figure 78: Full Expansion Board Setup

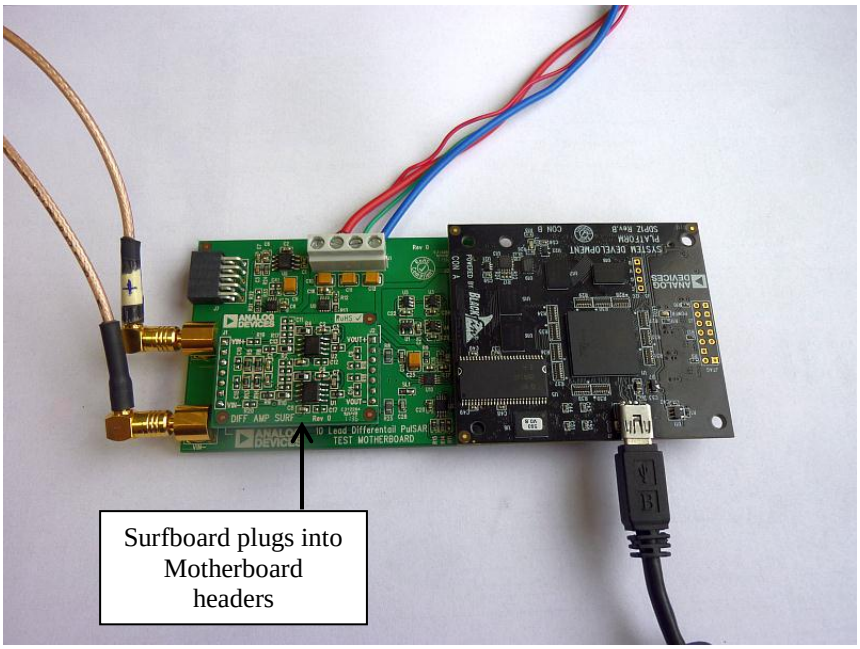


Figure 79: Full Surfboard Setup

When the data was collected with the AD7685 with the same -0.5 dBFS sinusoid at 20 kHz, there was an average drop in SNR of 0.3 dB between the motherboard and surfboard configuration. Peculiarly, the average SNR of the expansion board was higher than the motherboard, although it was unclear if this was the manifestation of sample-to-sample variation or if there was a real performance edge.

Table 21: Expansion Board and Surfboard Measurements with AD7685

Configuration	Sampling Rate [Hz]	Average SNR	Average SINAD	Average THD
Motherboard	50000	90.244	89.667	-99.374
	100000	90.804	90.351	-101.221
	150000	90.886	90.334	-100.081
	200000	91.428	90.839	-100.304
	250000	91.650	91.073	-100.337
	Total:	**91.006**	**90.453**	**-100.231**
Expansion	50000	90.604	89.967	-99.249
	100000	91.295	90.778	-101.141
	150000	91.405	90.792	-100.130
	200000	91.649	91.067	-100.552

	250000		91.563	91.010	-100.459
		Total:	**91.400**	**90.820**	**-100.360**
Surfboard	50000		90.085	89.486	-99.035
	100000		90.618	90.231	-101.972
	150000		90.778	90.244	-100.163
	200000		90.980	90.483	-100.608
	250000		90.914	90.419	-100.323
		Total:	**90.711**	**90.212**	**-100.480**

When only the highest sampling rate was inspected (which would accentuate any differences in performance between the three configurations), the surfboard showed a half decibel reduction in SNR from the expansion board and approximately three-quarters of a decibel from the motherboard. As shown in Figure 80, the SINAD followed the same curve as the SNR except it was negatively offset by the harmonic distortion.

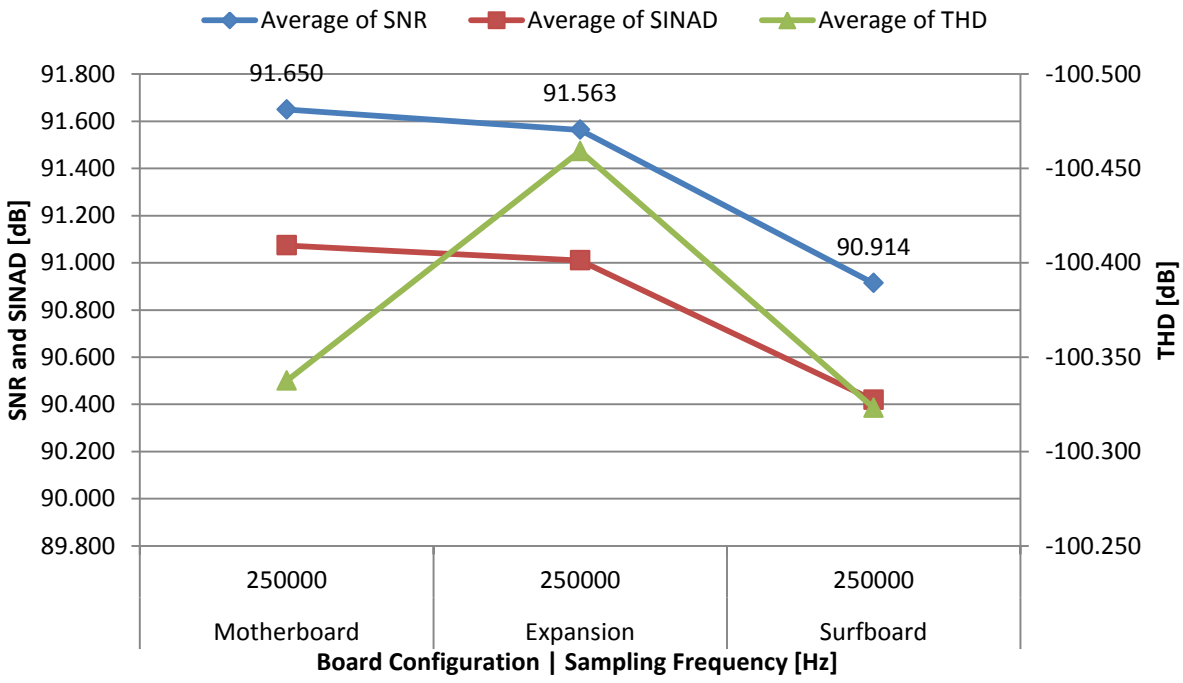


Figure 80: Expansion Board and Surfboard Performance with AD7685

The expansion board and surfboard performed more identically with the faster AD7982. As seen in Table 22, the average performance of the two boards was less than one-tenth decibel below the average performance of the motherboard. Differences this small in magnitude were likely caused by component-to-component variation rather than true differences in board performance.

Table 22: Expansion Board and Surfboard Measurements with AD7982

Configuration	Sampling Rate [Hz]	Average SNR	Average SINAD	Average THD
Motherboard	50000	95.600	95.508	-111.185
	200000	95.618	95.519	-110.995
	800000	95.799	95.672	-110.306
	1000000	95.762	95.647	-110.572
	Total:	**95.713**	**95.603**	**-110.694**
Expansion	50000	95.553	95.453	-110.901
	200000	95.574	95.460	-110.475
	800000	95.766	95.628	-109.946
	1000000	95.683	95.552	-110.008
	Total:	**95.653**	**95.530**	**-110.265**
Surfboard	50000	95.581	95.495	-111.448
	200000	95.575	95.485	-111.231
	800000	95.760	95.638	-110.350
	1000000	95.720	95.607	-110.586
	Total:	**95.648**	**95.548**	**-110.963**

In conclusion, the data suggested that the performance of the motherboard and the original daughter card were approximately equal, and the surfboard and expansion board had a maximum drop of 0.75 dB from the motherboard performance. In most cases, the expansion board offered slightly better performance than the surfboard, which was likely the result of the higher-quality SMB connectors on the signal lines.

Cost was another consideration when comparing the surfboard and expansion board options. Looking solely at the prices of the connectors and headers needed, the expansion board had an

associated expense of $14.29 compared to the surfboard at $2.62. The majority of this difference came from the expensive SMB connectors for the signal lines.

There were also some qualitative differences between the two options. The expansion board was more difficult to connect to the motherboard because there were three parallel connectors that must be lined up; if one connector was populated askew it was impossible to join the two boards. The surfboard was much simpler to attach and was a compact solution to driver-flexibility concerns. As of the writing of the report it is undecided whether future endeavors will include both the surfboard and the expansion board options or just a single option.

5.3 Performance and Power Consumption of Low Power *CFTL*

One of the advantages of a SAR converter is that the power consumption of the ADC scales with sampling rate. This trait was developed into a *Circuit from the Lab* that focused on minimizing the power consumption of the daughter card while retaining adequate performance levels. The designed schematic is attached in Appendix B, and features an AD7980 (a 16-bit, 1 MSps pseudo-differential converter). The choice of the driver amplifier, voltage reference, and reference buffer were narrowed to a small number of options, and this section investigates the results of testing with each combination of ICs. The most significant choice is the driver amplifier, so this section is divided into one part for the ADA4841 driver and one part for the AD8655 driver.

5.3.1 Testing with the ADA4841 ADC Driver

Before testing a multitude of configurations with the ADA4841, some baseline testing was conducted to determine the optimum supply rails for the IC. The desired input signal was a 0V to

2.5V sine wave, so V_{DD} and V_{SS} were initially set to +3.0V and -1.0V to provide headroom. However, at these voltage rails the ADA4841 caused significant clipping to the top half of the input as seen in Figure 81, which was reflected as a heavy harmonic distortion on the FFT (Figure 82).

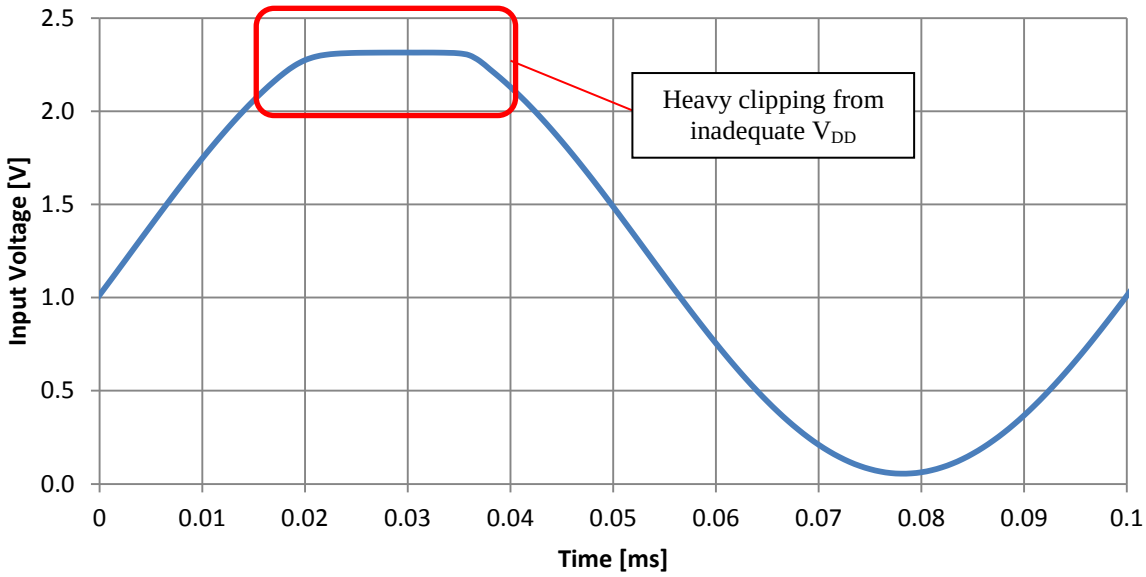


Figure 81: Input Waveform with ADA4841 Supplied with +3V and -1V

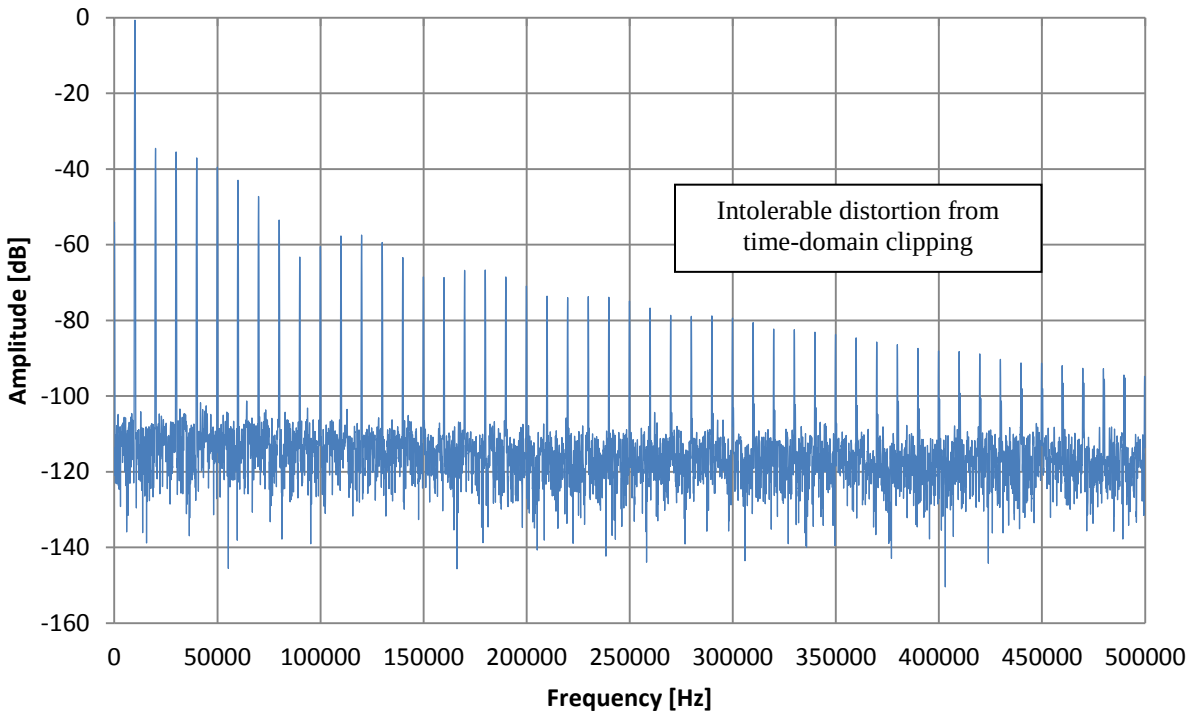


Figure 82: Input Voltage FFT of ADA4841 Supplied with +3V and -1V

Further inspection of the ADA4841 datasheet revealed that the amplifier often needs 1V of positive headroom, although the "lower supply limit is nominally below the minus supply" [**69**]. When the positive rail was increased to 3.5V to provide this margin, the clipping and distortion essentially disappeared.

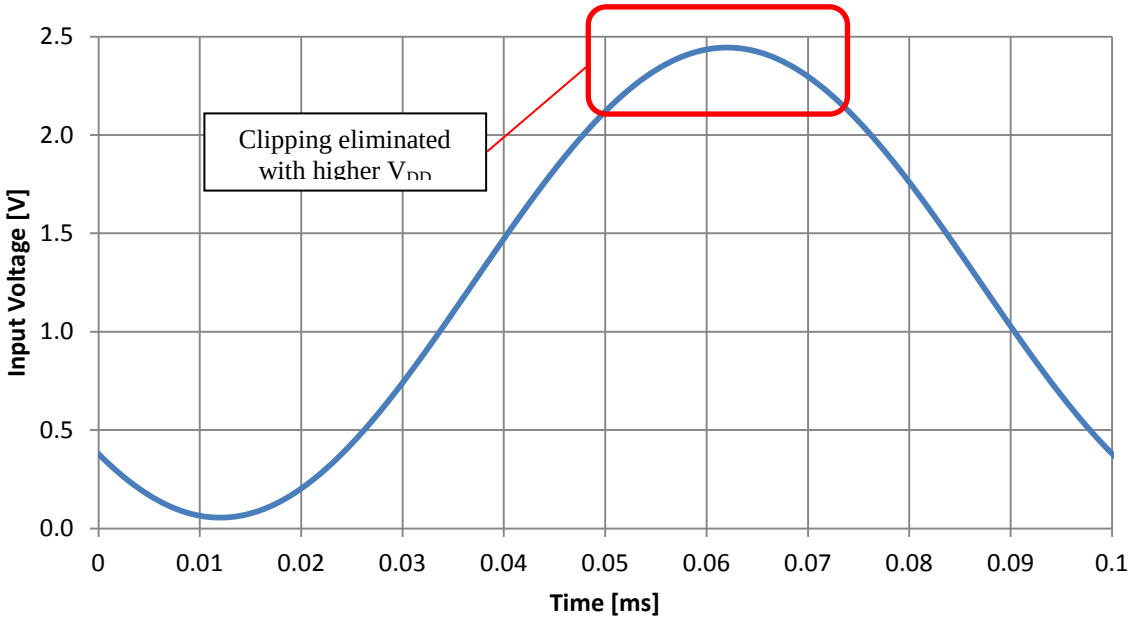


Figure 83: Input Waveform with ADA4841 Supplied with +3.5V and -1V

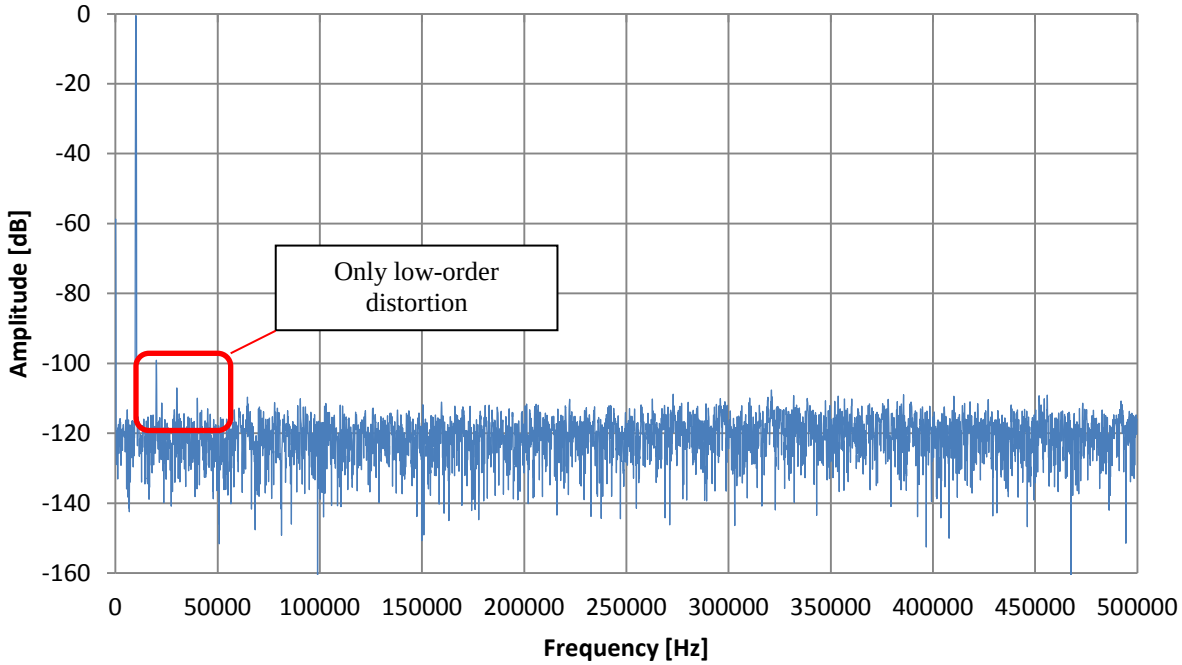


Figure 84: Input Voltage FFT with ADA4841 Supplied with +3.5V and -1V

To quantify the improvement and intelligently select the voltage rails, measurements were taken at six different supply combinations – the other conditions remained constant. As shown in Table

23, the reduction of the negative supply to ground did not impact performance; likewise, little improvement was seen when the positive supply was increased above 3.5V. This supported the choice of 3.5V and 0V as the positive and negative supplies, respectively. The only other integrated circuits on the board – the voltage reference and the reference buffer – could both run on the 3.5V without problem.

Table 23: Low Power Performance by ADA4841 Supplies (with AD8032, ADR441, f_{IN} = 10kHz, f_S = 1MSps)

Driver	V_{DD}	V_{SS}	SNR [dB]	SINAD [dB]	THD [dB]
ADA4841	3.0V	0V	48.208	28.306	-28.378
ADA4841	3.0V	-1V	48.430	29.109	-29.189
ADA4841	**3.5V**	**0V**	**83.024**	**82.933**	**-99.152**
ADA4841	3.5V	-1V	83.012	82.902	-98.440
ADA4841	4.0V	0V	83.106	83.047	-100.783
ADA4841	4.0V	-1V	83.120	83.049	-100.214

With a clearly ideal set of voltage rails, there were four ADA4841-based low-power boards to test. The testing consisted of measuring the FFT performance of 5 kHz, 10 kHz, and 20 kHz sine waves at 200 kSps, 400 kSps, 600 kSps, 800 kSps, and 1 MSps. This would provide a comprehensive view of the configuration's performance across input tones and sampling rates. Since this design was intended to consume minimal amounts of power, the current draw on each rail was also measured at each sampling rate.

An abbreviated summary of the ADA4841 testing is presented in Table 24; the results show several patterns. First, the removal of the AD8032 buffer causes distortion to increase significantly (THD drops from above -95 dB to below -80 dB), but reduces power consumption by approximately 5.5mW. Secondly, the ADR441 appears to provide better performance than the ADR291, although it again trades off with increased power draw.

Table 24: Performance of ADA4841 Low Power Variants (f_{IN} = 5-20kHz, f_S = 200-1000kSps)

Driver	Reference	Buffer	SNR [dB]	SINAD [dB]	THD [dB]	Max Power [mW]
ADA4841	ADR291	AD8032	81.776	81.694	-98.401	20.92
ADA4841	ADR291	None	82.704	69.999	-70.449	16.41
ADA4841	ADR441	AD8032	83.041	82.871	-96.926	31.38
ADA4841	ADR441	None	83.251	75.884	-77.022	25.72

The complete breakdown of performance by sampling rate and by input frequency is included in Appendix A. Inspection of the full data showed that neither the input frequency nor the sampling rate significantly affected the SNR, SINAD, or THD for the ADA4841 boards. The power consumption did scale by sampling rate, as predicted by the knowledge of the SAR architecture and operation. For all four variants, the current draw on the 2.5V rail (that supplies only the ADC) was identical for each sampling rate.

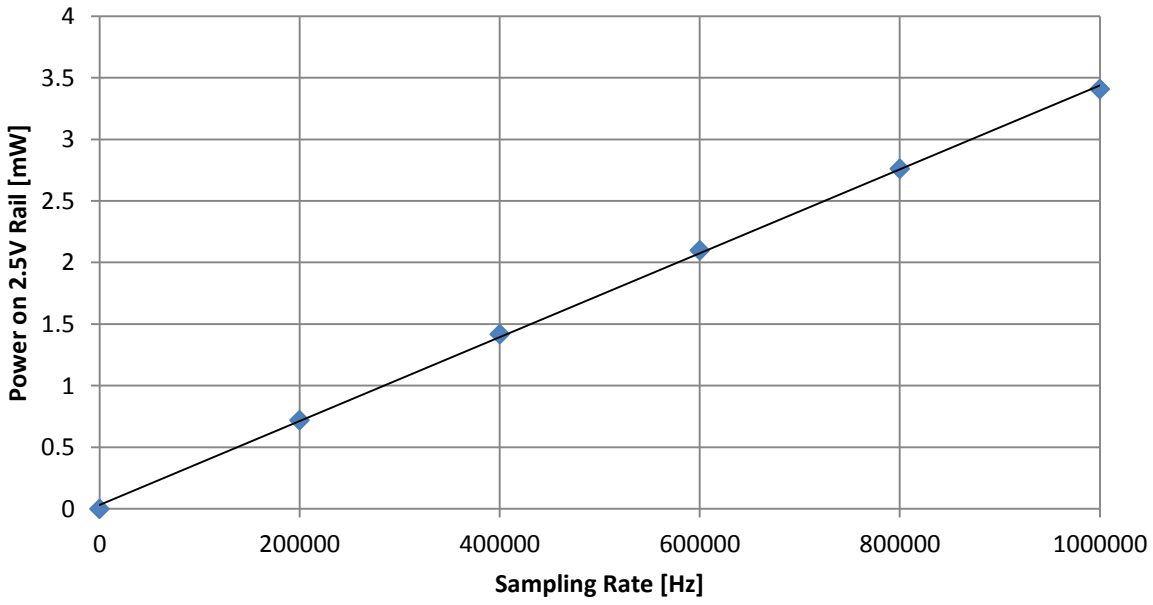


Figure 85: Power Consumption of AD7980 by Sampling Rates

The power measurements on the ADC's 2.5V rail were very linear; the regression line of Equation (61) yields a coefficient of determination of 0.9996.

$$P_{ADC} = 3\text{nW} * f_S + 31.4\mu\text{W} \quad (61)$$

5.3.2 Testing with the AD8655 ADC Driver

While the datasheets listed the ADA4841 as lower-power and lower-noise than the AD8655, the previous experiments required the ADA4841's supply voltage to be raised to 3.5V to provide adequate headroom. Consequently, the voltage reference and the reference buffers also dissipated additional power. The AD8655 can operate at 0V to 3.0V, and the half volt reduction may have resulted in enough power savings to warrant the higher noise parameters.

Similar to the process used with the ADA4841, the AD8655 was first tested to determine its sufficient operating voltages. When first tested with +3V to 0V (the minimum supply voltages needed to operate the other ICs on the board), the waveform demonstrated no clipping but the FFT showed a harmonic series.

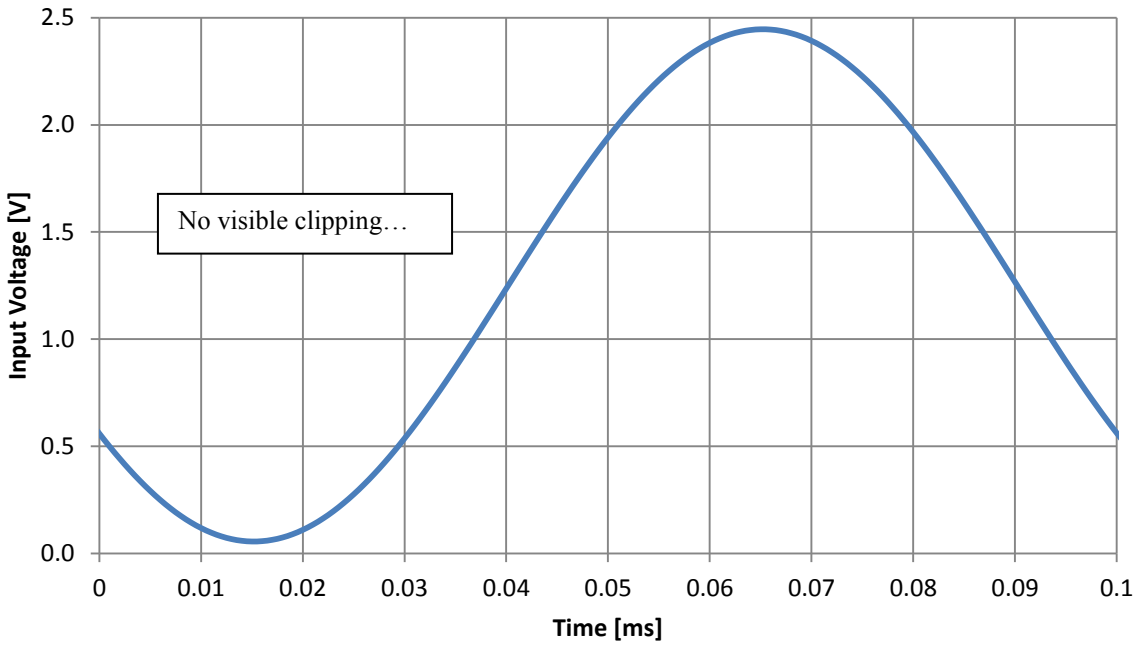


Figure 86: Input Waveform with AD8655 Supplied with +3V and 0V

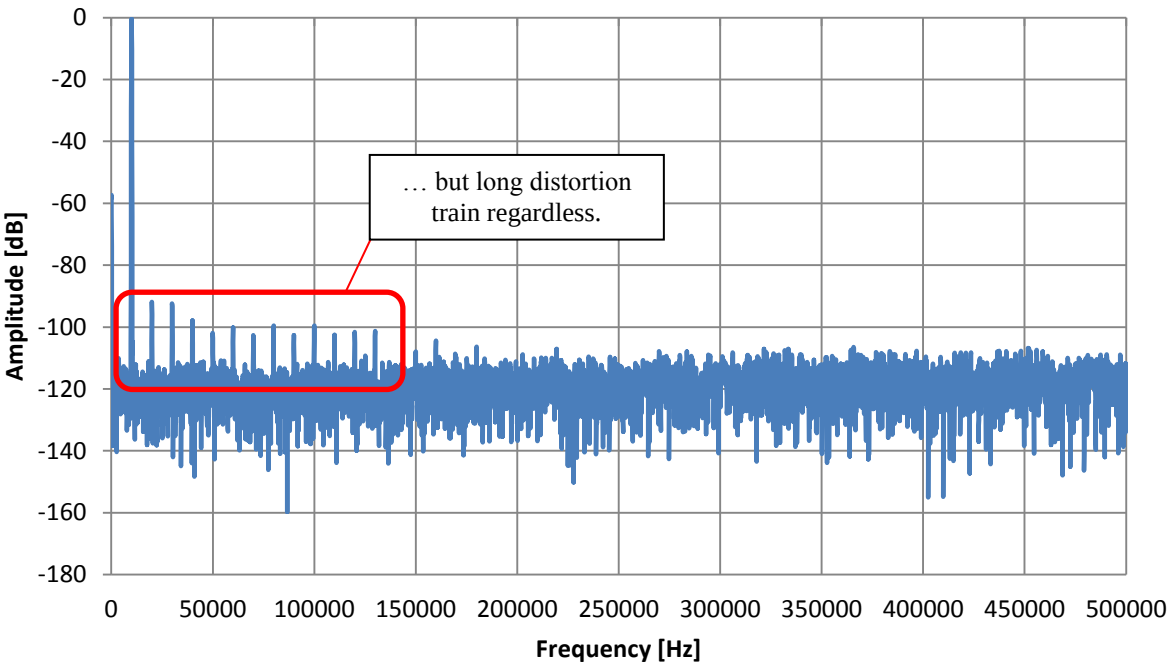


Figure 87: Input FFT with AD8655 Supplied with +3V and 0V

When the positive supply was widened to 4V, the SNR and THD both climbed less than one decibel; adding a -1V rail had a more significant impact on THD but did not change the SNR. Oddly, making both changes simultaneously (driving the AD8655 from +4V to -1V) yielded a THD nearly 10 dB better than any other tested combination. These findings are summarized in Table 25.

Table 25: Low Power Performance by AD8655 Supplies (with AD8032, ADR291, f_{IN} = 10kHz, f_S = 1MSps)

Driver	V_{DD}	V_{SS}	SNR [dB]	SINAD [dB]	THD [dB]
AD8655	**3V**	**0V**	**81.353**	**80.285**	**-86.893**
AD8655	3V	-1V	81.174	80.431	-88.422
AD8655	3.5V	0V	81.608	80.253	-85.959
AD8655	3.5V	-1V	81.671	80.858	-88.498
AD8655	4V	0V	81.596	80.628	-87.588
AD8655	**4V**	**-1V**	**81.677**	**81.582**	**-97.636**

Without a clearly superior option for the power rails, it was decided that both 3V to 0V and 4V to -1V would be used for the subsequent testing. As with the ADA4841 boards, the AD8655 solutions were tested at 5 kHz, 10 kHz, and 20 kHz input tones, each at sampling rates of 200 kSps, 400 kSps, 600 kSps, 800 kSps, and 1 MSps. The multitude of performance data was then compared against the power consumption of the entire board to make decisions about the best overall design for the low-power PulSAR card.

The aggregated AD8655 testing data is listed in Table 26; and the results roughly mirror the findings with the ADA4841. The removal of the AD8032 buffer still causes distortion to increase, and the ADR441 still provides better noise performance than the ADR291. For expediency's sake, power measurements were not collected for two of the configurations that were already performing poorly enough to be eliminated from the final design.

Table 26: Performance of AD8655 Low Power Variants (f_{IN} = 5-20kHz, f_S = 200-1000kSps)

Driver	Power	Reference	Buffer	SNR [dB]	SINAD [dB]	THD [dB]	Power [mW]
AD8655	3V to 0V	ADR291	AD8032	81.043	79.751	-86.541	25.17
AD8655	3V to 0V	ADR291	None	81.150	67.450	-67.737	20.69
AD8655	3V to 0V	ADR441	AD8032	83.553	81.563	-86.459	34.04
AD8655	3V to 0V	ADR441	None	82.284	75.254	-76.455	28.65
AD8655	4V to -1V	ADR291	AD8032	81.447	81.302	-96.212	--
AD8655	4V to -1V	ADR291	None	81.555	67.651	-67.925	--
AD8655	4V to -1V	ADR441	AD8032	84.053	82.882	-90.948	47.76
AD8655	4V to -1V	ADR441	None	83.232	76.002	-77.209	41.35

The full data for these AD8655 measurements is also attached in Appendix A, and a close examination of the input frequency performance showed unexpected behavior. Most notable for the boards with the ADR441 and the AD8032 running on 3V to 0V, the performance is significantly higher for low input frequencies (at or less than 10 kHz) than for higher frequencies

(20 kHz and greater). The signal-to-noise ratio for the 5 kHz and 10 kHz with this setup was one decibel higher than with any other board. No other configuration – with the AD8655 or the ADA4841 – exhibited this strong dependence on input frequency.

5.3.3 Choosing the Final Design

Exacting performance comparisons between the AD8655 and the ADA4841 show very little reason to use an AD8655 board for the final low-power design. In nearly every case, all three FFT metrics are reduced with the AD8655, and the power consumption was on par or higher than the equivalent ADA4841 board. This allowed eliminations of the variants as per Table 27, where the green configurations are those retained for consideration.

Table 27: Comparison of Low Power Variants

Variant	Driver	Power	Reference	Buffer	Comment
(1)	AD8655	3V to 0V	ADR291	AD8032	Worse performance and power than (9)
(2)	AD8655	3V to 0V	ADR291	None	Worse performance and power than (10)
(3)	**AD8655**	**3V to 0V**	**ADR441**	**AD8032**	**Best performance at low f_{IN}**
(4)	AD8655	3V to 0V	ADR441	None	Worse performance equal power than (12)
(5)	AD8655	4V to -1V	ADR291	AD8032	Worse power equal performance than (11)
(6)	AD8655	4V to -1V	ADR291	None	Worse performance and power than (10)
(7)	AD8655	4V to -1V	ADR441	AD8032	Worse performance and power than (9)
(8)	AD8655	4V to -1V	ADR441	None	Worse performance and power than (12)
(9)	**ADA4841**	**3.5V to 0V**	**ADR291**	**AD8032**	**2nd lowest power, high SNR and THD.**
(10)	**ADA4841**	**3.5V to 0V**	**ADR291**	**None**	**Lowest overall power consumption**
(11)	**ADA4841**	**3.5V to 0V**	**ADR441**	**AD8032**	**Highest overall performance**
(12)	ADA4841	3.5V to 0V	ADR441	None	Gains over (10) not worth added power

At this point, there was no perfectly objective way to narrow the four options marked in green down to a single "best" design; each provided a different balance of power to performance that would appeal to different customers. For the purposes of this project, the ADA4841 board with the ADR291 and the AD8032 provided the best performance per milliwatt without sacrificing the THD by removing the buffer, and was pursued further for the *Circuit from the Lab*.

Other experimentation and testing showed that extra performance can often be squeezed out of a certain design by tailoring the minor components to the IC choices (see Section 5.6 for details on these optimizations). The most common improvement would come from adjusting the value of the resistor in the RC network between the driver amplifier and the ADC. However, testing showed that the default 33Ω resistor was already ideal for the low-power board. With the other circuit alterations already performed in the design phase (see Section 4.6 for the implementation details), the circuit was considered completed and the performance was assessed.

The noise floor of the converter was measured by removing the input signal. As seen in Figure 88, the noise is typically at -120dB or less. This was reasonably impressive, since low power integrated circuits are inherently noisier.

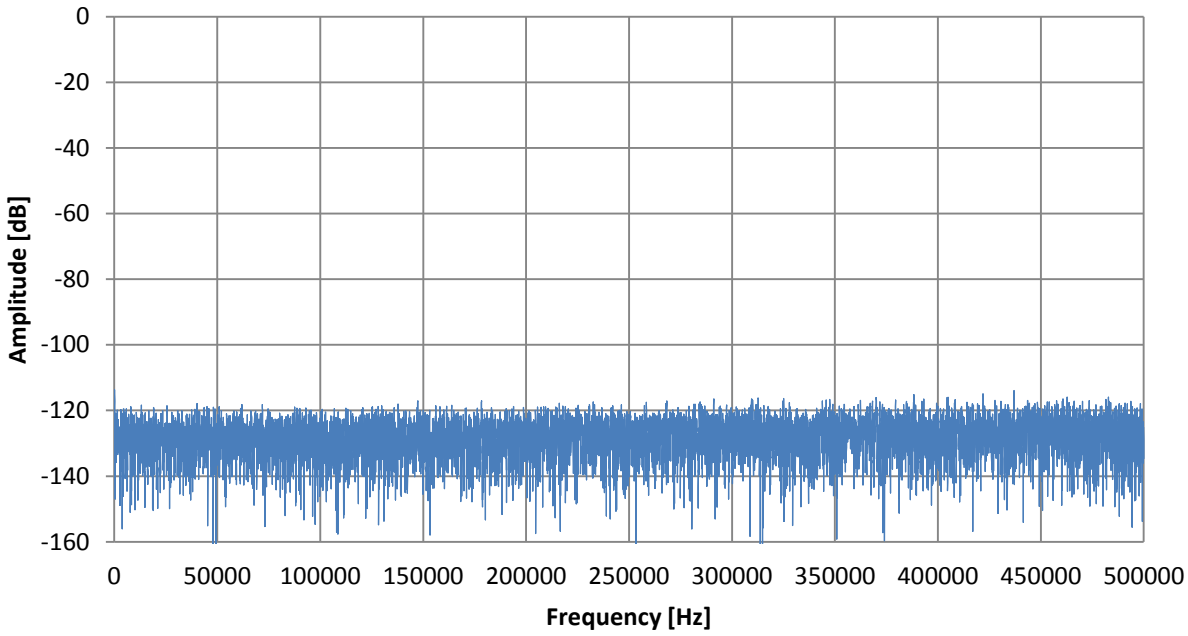


Figure 88: Low Power *CftL* Noise Floor

The performance was better showcased when a signal was applied. The AD7980 is rated in its datasheet with a 10 kHz input tone, so this was the frequency used when making the final

evaluation. The datasheet acknowledges that performance will be degraded when using a 2.5V reference, and claims a typical signal-to-noise value of 86.5dB. The low-power design here was able to consistently obtain 85.5dB or higher SNR, with a THD of -97dB or better. This was considered a success considering the performance tradeoffs willingly accepted to reduce power consumption.

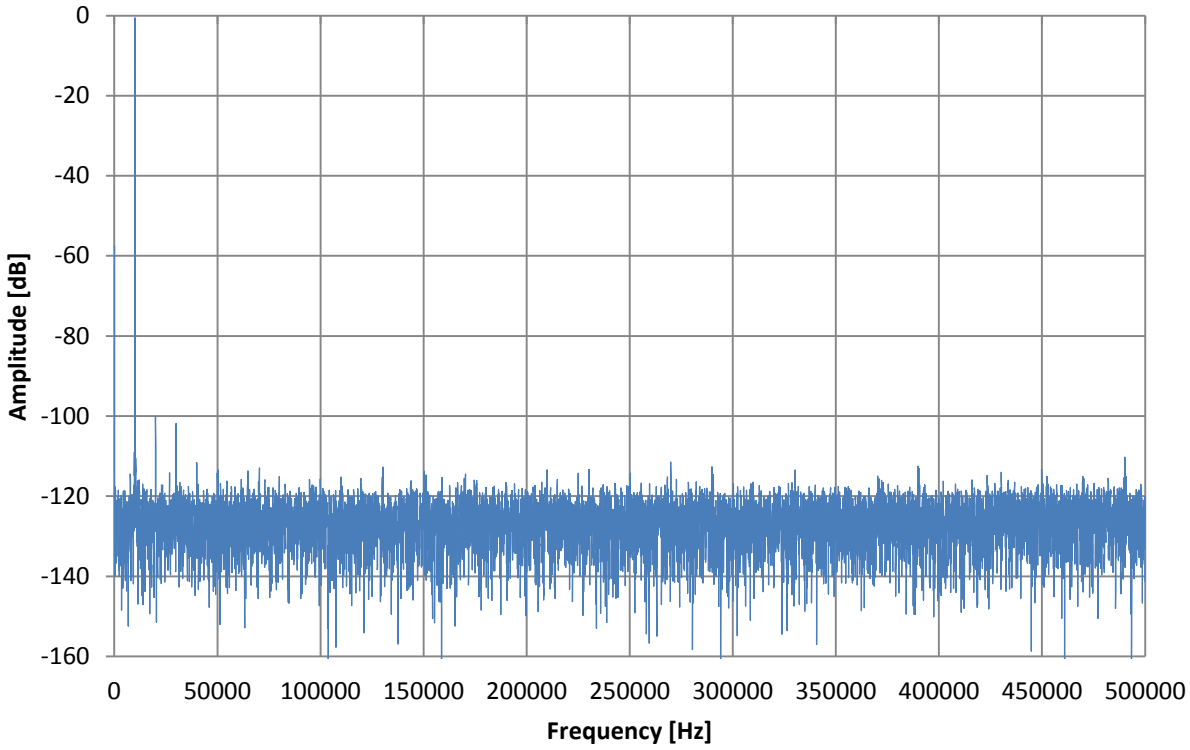


Figure 89: Low Power *CftL* FFT Plot at f_{IN} = 10 kHz

Finally, the numeric performance was logged across three input frequencies and across sampling rates from 50 kSps to 1 MSps. The results – shown in Table 28 – demonstrate slightly better performance at higher throughputs and at lower input frequencies, but the performance at all frequencies is acceptable.

Table 28: Final Low-Power Design Performance Results

f_{IN} [Hz]	f_S [Hz]	SNR [dB]	SINAD [dB]	THD [dB]
4500-5500	50000	84.844	84.356	-94.029
	200000	84.977	84.490	-94.167
	400000	85.048	84.558	-94.229
	600000	85.198	84.711	-94.415
	800000	85.273	84.777	-94.381
	1000000	85.194	84.717	-94.438
9500-10500	50000	85.440	85.093	-96.337
	200000	85.550	85.303	-97.698
	400000	85.564	85.330	-97.943
	600000	85.697	85.456	-97.952
	800000	85.894	85.647	-98.065
	1000000	85.839	85.533	-97.097
19500-20500	50000	84.980	84.715	-97.479
	200000	85.216	85.023	-98.474
	400000	85.379	85.181	-98.478
	600000	85.454	85.262	-98.702
	800000	85.671	85.463	-98.565
	1000000	85.660	85.386	-97.451

5.4 TESTING RESULTS OF THE HIGH AC PERFORMANCE *CFTL*

To experimentally verify the high performance design the daughter card was first populated with the ADA4841, the standard driver amplifier. This would serve as a baseline performance level to measure the modifications against. The first board used the AD7691 with two ADA4841s driver amplifiers, an ADR435 voltage reference, an AD8032 buffer, and a standard 33Ω resistor for the RC network. When measured in this state, the design yielded an SNR of 98.3dB and THD of -116.8dB. These values are significantly below the specifications for the AD7691, and suggest that the stock daughter card configuration is woefully inadequate for reaching signal-to-noise ratios over 100dB.

Table 29: High AC Performance across R_1 Values

R_1 [Ω]	SNR [dB]	SINAD [dB]	THD [dB]
33	98.374	98.324	-116.782
39	98.471	98.417	-116.604
47	98.561	98.506	-116.597
56	98.653	98.592	-116.347
68	98.835	98.773	-116.473
82	98.936	98.876	-116.787
100	99.109	99.045	-116.649
120	99.267	99.210	-117.225
180	**99.561**	**99.503**	**-117.433**
220	99.311	98.993	-110.410
270	98.391	97.266	-103.705

The first alteration was to change the value of the resistor in the RC network. As described in greater detail in Section 5.6.1, increasing the resistor can increase performance by reducing high-band noise, particularly at low sampling rates where the ADC needn't be speedy. Table 29 details the performance levels measured as the resistor was swept from the stock 33Ω to 270Ω. The ideal value was approximately 180Ω, where the SNR peaked at 99.5dB and the THD rose to -117.4dB.

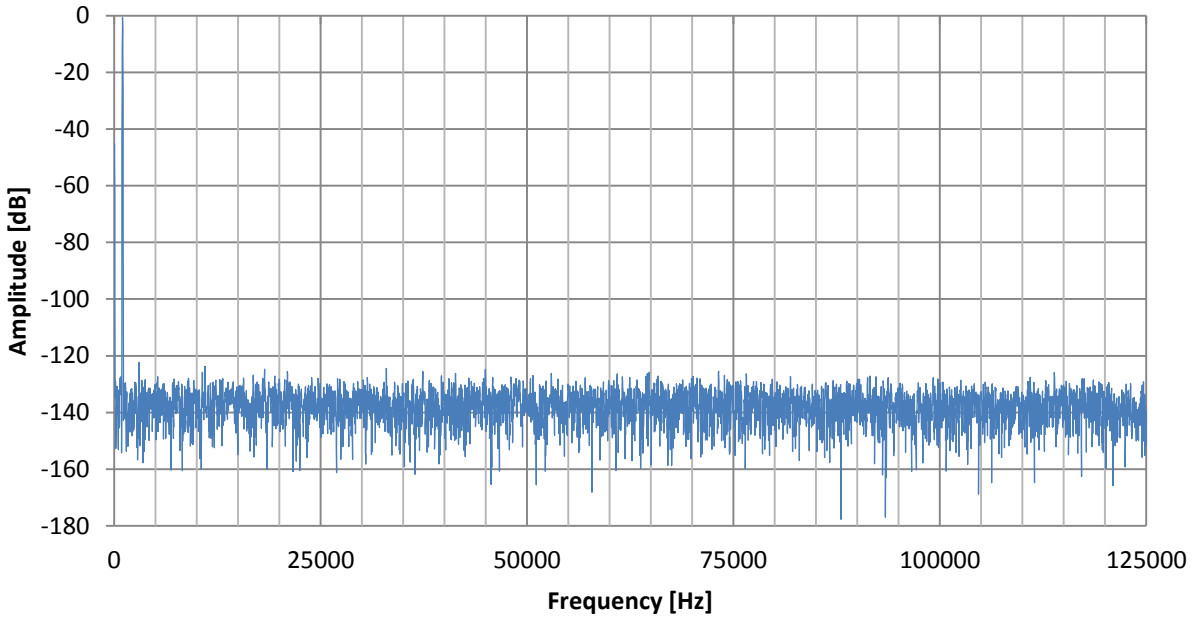


Figure 90: Maximum Performance from AD7691 and ADA4841 -- SNR=99.6dB THD=-119dB

Unfortunately it was difficult to squeeze further performance out of the ADA4841 configuration. The reference was switched with an AD445 (lower noise but less output capability) and a reference filter of various values was tried; these both degraded performance as predicted by the results of Section 5.6. Surmising that the ADC driver was limiting further performance gains, the ADA4841 was switched to the AD8597 selected in Chapter 4. This amplifier features half the voltage noise of the ADA4841 as well as reduced distortion of input signals.

When characterizing the board with the AD8597, the first observation was that the positive amplifier supply was inadequate. The daughter card uses an ADP3334 to regulate the 12V benchtop voltage down to a 7V supply for the driver amplifier, while the negative driver supply is delivered directly from another benchtop unit. However, the AD8597 datasheet specifies that at ±5V operation, the input signal is limited to ±2V. A mere two volt increase of the positive supply would not yield an additional three voltage of input headroom, so it was likely that the 0V

to 5V input signal would be distorted as the input protection circuitry activated. Indeed, Figure 91 illustrates that when powered from +7V to -5V the AD8597 has high amplitude (for a high performance circuit) low-order harmonics.

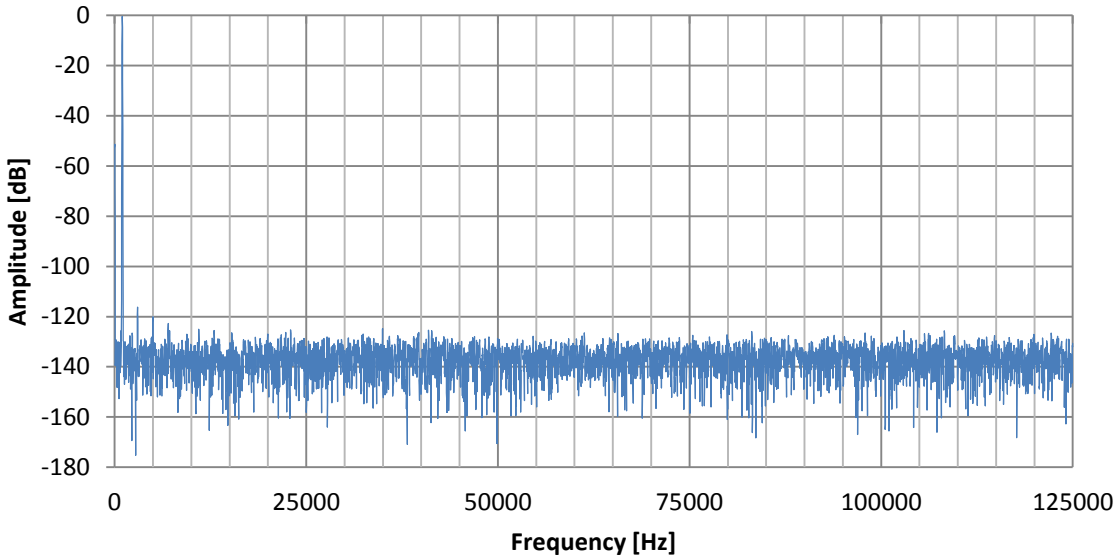


Figure 91: Signal Distortion from AD7691 and AD8597 with +7V Supply -- THD=-112dB

To widen the positive supply, the ADP3334 was removed and the input pins were shorted to the output pins. Since the driver amplifiers are the only integrated circuits sourced off the ADP3334, this effectively powers the drivers off the same benchtop rail the runs the voltage reference and the reference buffer. Considering the supply ranges of all the on-board ICs, the main benchtop supply could be adjusted between 7.5V (the minimum of the ADR435) and 12V (the maximum of the AD8032). When increased above 8V, the distortion of Figure 91 disappears and performance increases to the same levels seen with the ADA4841.

With no significant difference between the ADA4841 and the AD8597, attention was turned to the voltage reference. If the reference was producing high levels of noise, it could be masking any gains seen by the use of the higher-quality driver amplifier. The first attempt at improving

the reference was by switching the ADR435 with the ADR445, a lower noise 5V reference. Unfortunately, this dropped performance slightly and had no perceptible effect on the noise floor of the ADC readings.

Alternatively, the AD8032 that buffers the reference could be the source of the hypothetical reference noise. Several low noise buffers were researched in Chapter 4 and would be viable options for this design; however, the components were foolishly ordered in an SOIC package when an MSOP was necessary. Experimentation with high-grade buffer amplifiers (ADA4004-2, ADA4841-2, and AD8676) will have to be postponed to future work.

The only buffer option available in the timeline of this project was to remove the buffer completely. Since the voltage reference ICs used are mostly capable of driving the highly-dynamic load of the ADC, this alteration went fairly well. The signal-to-noise ratio improved by a few tenths of a decibel (presumably because the noisy AD8032 was absent), while the THD subtly degraded from reference variance.

In summary, the best performance for the AD7691 circuit was seen when paired with an AD8597 running at +12V to -5V, an ADR435 voltage reference, no reference buffer, and a 180Ω resistor in the RC network. The high-performance *CftL* had an average SNR over 100dB and THD under -120dB. A typical FFT is shown below in Figure 92.

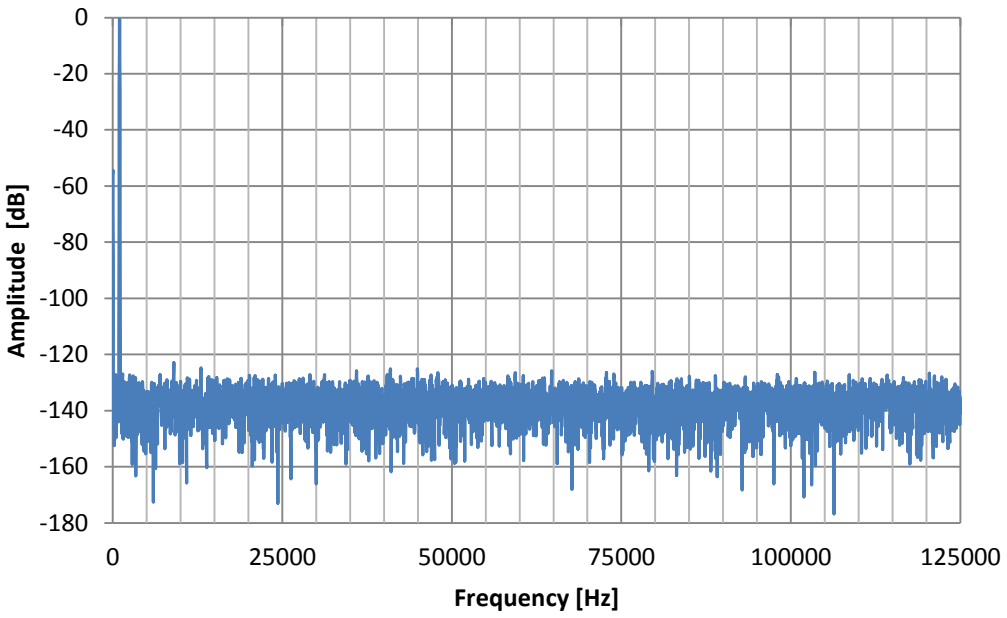


Figure 92: Maximum Performance from AD7691 and AD8597 -- SNR=100.0dB THD=-120.1dB

Regrettably, these performance levels still fall short of the advertised 101.5dB signal-to-noise ratio. When compared against the datasheet FFTs, the noise floor of this design is five to ten decibels above the datasheet plots. Given the available measurements tools, there was no way to determine where such minute levels of noise (approximately $3\mu V_{pp}$ or $2.2nV/\sqrt{Hz}$) were originating. It is possible that the reference buffer could be greatly improved if the buffers are ordered in the correct package. There is also no means to assess the accuracy of the Audio Precision signal generator that was used for the 1 kHz tone. Noise or jitter on the signal line can easily prevent high SNR from being reached. Future work can be done in this area to further optimize this *Circuit from the Lab*.

5.5 RESULTS OF SPORT AND SPI COMPARISON

The SPI and SPORT testing was conducted on an AD7980, a 16-bit converter with a maximum sample rate of 1 MSps. The system clock was set to 30 MHz for both to eliminate f_{CLK} as a variable between trials. If the converter's acquisition time equaled the minimum value published in the datasheet (180 ns) then both protocols should support 1.4 MSps as per Equation (1). However, when the SPORT configuration was tested it was incapable of performing at that rate with the lowered f_{CLK}. The sampling rate was adjusted down until SPORT regained proper performance levels at 857 kSps.

With this alteration, SPORT and SPI were tested at twenty-six input frequencies at sampling frequencies of 857 kSps, 500 kSps, and 250 kSps. To obtain the data for each frequency pairing, approximately twenty measurements of SNR, SINAD, and THD were recorded and then averaged to find the values in Appendix A. This aids in reducing the sample-to-sample variation that is inevitable from background EMI and random noise. From quick comparison of the 857 kSps data, it is evident that SPI is unable to deliver quality data at that throughput rate; the SPI SNR was about twenty decibels below SPORT at this speed. To compare the other sampling rates, the data is plotted without the 857 kSps outliers.

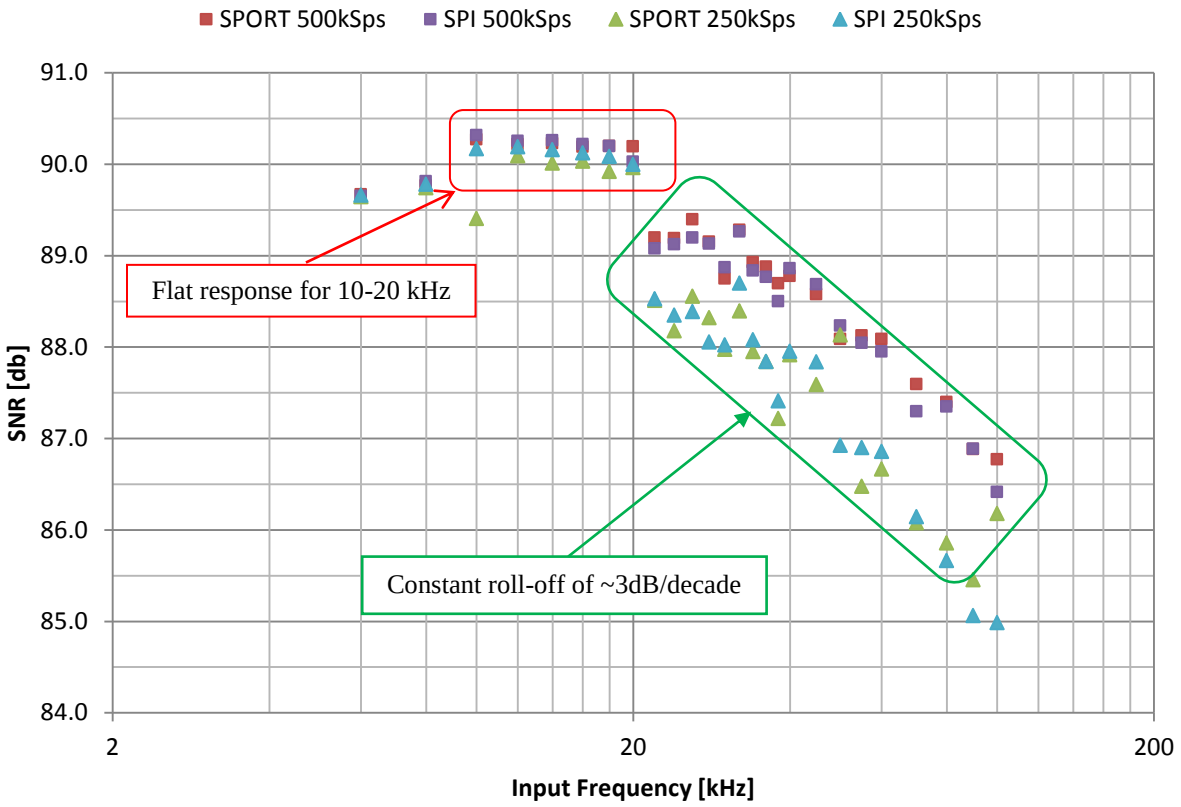


Figure 93: Plot of SPI and SPORT SNR Measurements by Frequency

The SNR graph in Figure 93 shows two regions: performance is fairly constant regardless of sampling rate or protocol when f_{IN} is between 10 and 20 kHz, and then SNR rolls-off above 20 kHz. Particularly in the roll-off region, 250 kSps gives poorer results than 500 kSps. However, the difference between SPI and SPORT at these sampling rates is less definitive; each appears best at certain frequencies. Very similar results are seen for SINAD (graph omitted for brevity).

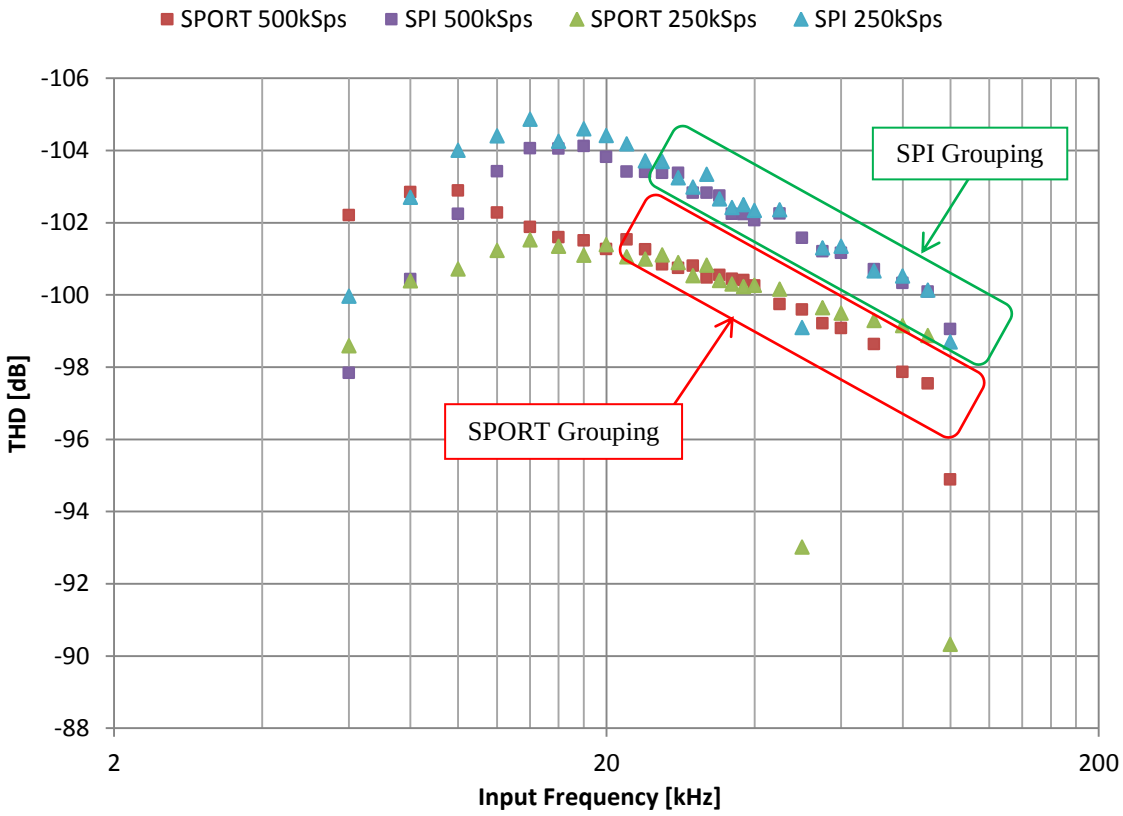


Figure 94: Plot of SPI and SPORT THD Measurements by Frequency

The THD plot of Figure 94 shows substantially different groupings in the data. Rather than divided by sampling rate, the two protocols form two distributions. Both SPI and SPORT reach their best values for THD between 10 and 20 kHz and roll-off similar to the SNR. However, SPORT inexplicably has worse distortion than SPI, although none of the technical predictions suggest this.

Measurements of the AC performance are always tainted by noise and have inherent variability between readings. Considering that some SPI gave better SNR and SINAD for some input frequencies and SPORT for others in a seemingly random pattern, it was suspected that the differences were caused by sample-to-sample variation. To quantitatively test this, the residuals for SNR and SINAD were normalized and the cumulative distributions were plotted against

normal CDFs with the same mean and standard deviation (MATLAB code is attached in Appendix B).

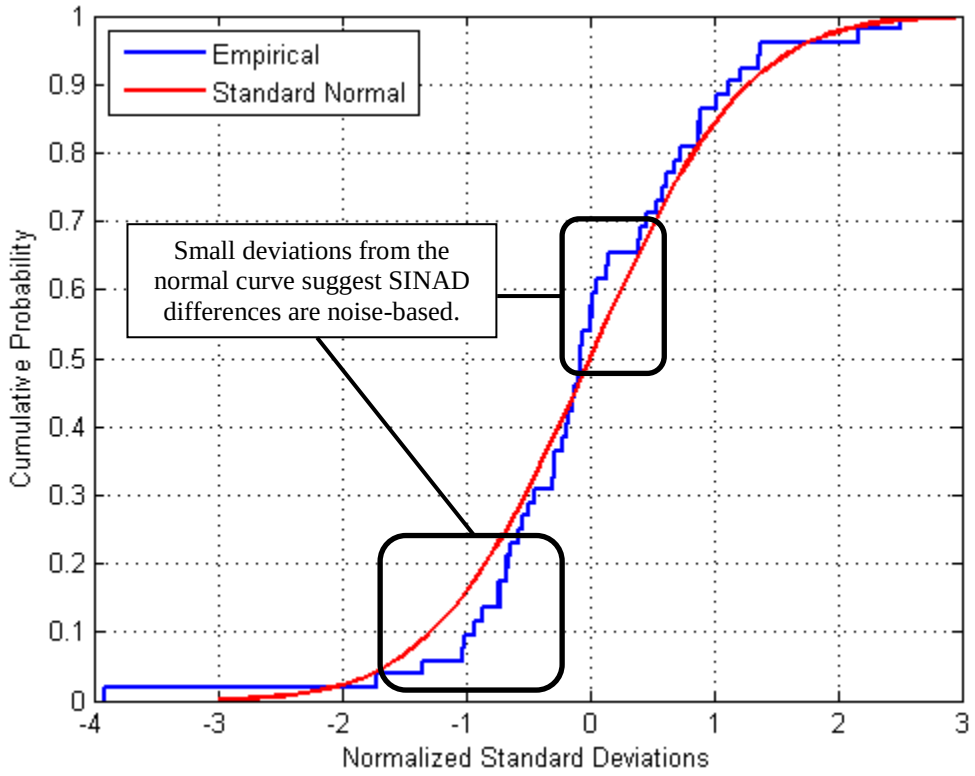


Figure 95: Distribution of SINAD Residuals against Normal

While Figure 95 does not show a perfect overlay of the measured values to an ideal normal curve, MATLAB can perform a goodness-of-fit test between the two populations with the `kstest()` function; at a 95% confidence interval, the SNR and SINAD residuals are normally distributed, supporting the hypothesis that the differences between SPI and SPORT were driven by chance.

Conversely, an analogous analysis for the THD residuals should disprove randomness – the plot in Figure 94 shows two clear populations divided by protocol. Indeed, `kstest()` fails at 95% and the graph of residuals against the normal CDF shows much more deviation than Figure 95.

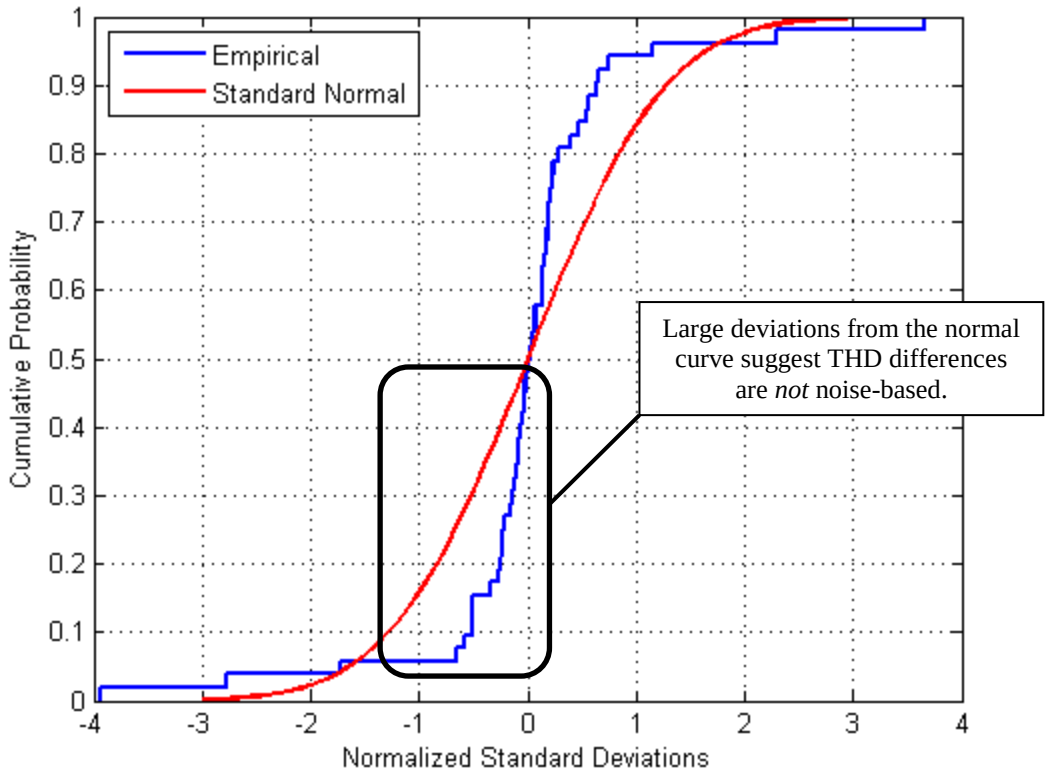


Figure 96: Distribution of THD Residuals against Normal

Evaluation of the above results led to a choice of SPORT for the sole serial interface for future daughter card revisions. While the THD for SPI is demonstrably higher, SPI is unable to handle high throughput ADCs such as the AD7980. Even at the maximum supported system clock SPI could only output data cleanly at about 750 kSps; when f_{CLK} is raised to 60 MHz, SPORT can handle sampling rates in excess of 1.33 MSps. Interestingly, the jitter predictions were never substantiated. As shown by Equation (43), SNR will drop by twenty decibels per decade once it becomes jitter-limited, and the roll-off of Figure 93 is only three decibels per decade. This indicates that other sources of noise greatly dominate jitter-related error at the frequencies under test. Since the AD7980 is one of the faster PulSAR ADCs and the input tones were swept over a broad range, jitter is unlikely to play a significant role in typical customer applications.

5.6 Optimization Results

In this section, the three optimizations presented in Section 4.8 Performance Optimizations were explored. In most cases, the alterations involved attempts to reduce the noise on the voltage reference, although attention was also paid to the interaction between the ADC driver and the ADC itself. Optimizations that actually resulted in a performance boost were utilized in the previously-designed *Circuits from the Lab* and helped enable the SNR and THD measurements seen on those designs.

5.6.1 Acquisition Time Effects of the External RC Filter

The derivation of the effective load impedance on the ADC driver conducted in Chapter 4 predicted that changing the resistor value in the external RC would have little effect on the FFT performance. To verify this, a high-speed AD7982 was paired with two ADA4841 driver amplifiers and tested with four different resistor values. The results of the measurements are listed below in Table 30.

Table 30: Performance Results with Different RC Filters

Resistor R_1	Sampling Rate [Hz]	Average SNR	Average SINAD	Average THD
15Ω	50000	95.426	95.350	-112.298
	200000	95.493	95.414	-112.213
	400000	95.546	95.458	-111.826
	600000	95.558	95.451	-111.129
	800000	95.557	95.436	-110.650
	1000000	95.565	95.432	-110.287
	Total:	**95.527**	**95.427**	**-111.441**
22Ω	50000	95.776	95.688	-112.056
	200000	95.830	95.745	-112.253
	400000	95.830	95.738	-111.977
	600000	95.867	95.767	-111.698
	800000	95.874	95.756	-111.081

	1000000	95.832	95.726	-111.422
	Total:	**95.841**	**95.741**	**-111.671**
27Ω	50000	95.893	95.810	-112.414
	200000	96.021	95.927	-112.077
	400000	96.036	95.927	-111.542
	600000	96.039	95.918	-111.105
	800000	96.036	95.909	-110.946
	1000000	95.737	95.657	-112.423
	Total:	**95.959**	**95.856**	**-111.762**
33Ω	50000	96.003	95.915	-112.273
	200000	96.108	96.015	-112.211
	400000	96.171	96.072	-112.026
	600000	96.186	96.078	-111.724
	800000	96.170	96.064	-111.772
	1000000	94.839	94.752	-111.222
	Total:	**95.920**	**95.823**	**-111.871**

Unexpectedly, the test data indicated that higher resistances resulted in higher signal-to-noise ratios, although raising R_1 too high limited performance at high sampling rates. As seen in the graph of Figure 97, the default 33Ω resistor had the best performance at lower sampling rates, but dropped significantly at 1 MSps. The next-lower resistor, 27Ω, also showed a quantifiable degradation at the full throughput. Experimentally, the best high-speed performance is obtained when $R_1 = 22\Omega$.

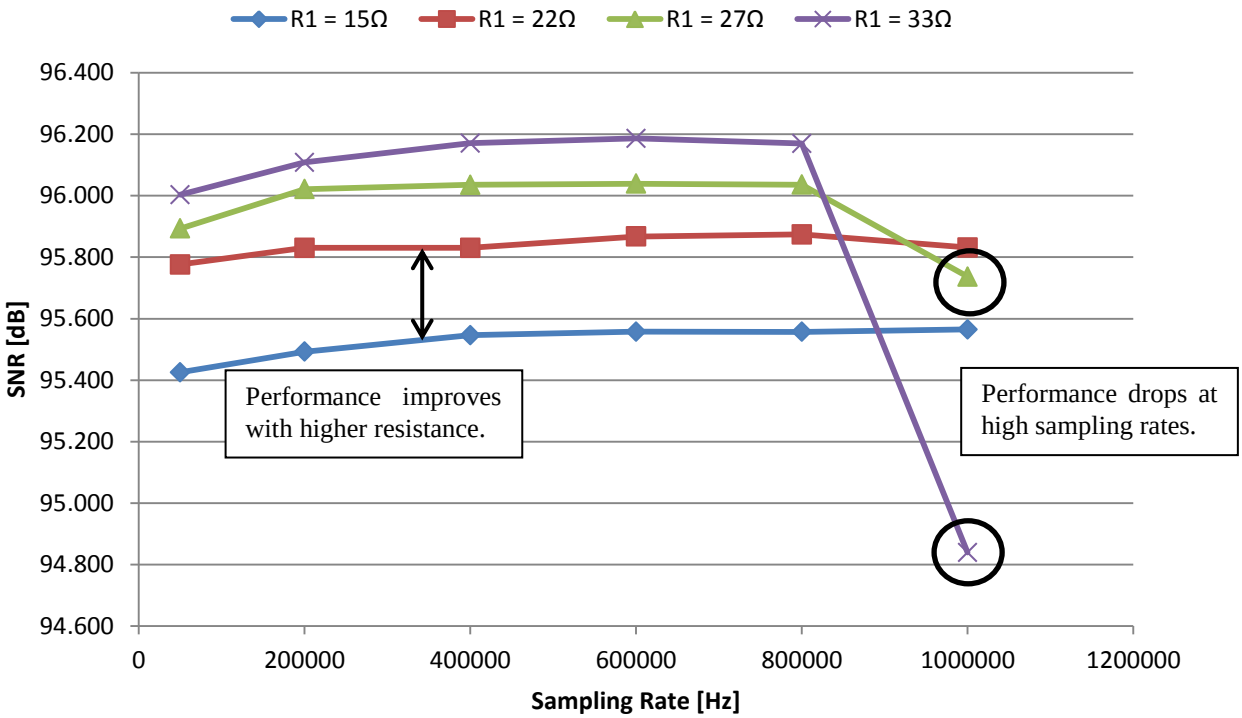


Figure 97: SNR Differences from Changing R_1 in External RC

These results prompted reanalysis of the cascaded RC networks of Figure 59. The dependence on sampling rate implied that the solution was related to timing. Therefore, the intermediate form of Figure 60 can be rearranged into a series resistance and capacitance (Figure 98) that can be used to find the timing constant of this network.

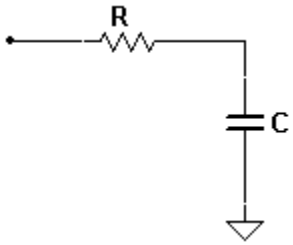


Figure 98: Equivalent RC Network for Time Constant

The impedance for the series RC network is:

$$Z_{RC} = R + \frac{1}{j\omega C} \tag{62}$$

which can be equated to Equation (50) to find expressions for R and C:

$$R = \frac{R_S + R_P + \omega^2 R_S R_P^2 C_P^2}{1 + \omega^2 R_P^2 C_P^2} \tag{63}$$

$$C = \frac{1 + \omega^2 C_P^2 R_P^2}{\omega^2 C_P R_P^2} \tag{64}$$

Finally, Equations (63) and (64) can be multiplied to give the timing constant τ:

$$\tau = RC = \frac{R_S + R_P + \omega^2 R_S R_P^2 C_P^2}{\omega^2 R_P^2 C_P} \tag{65}$$

The internal sample-and-hold of the ADC would charge as an exponential function with the timing constant of Equation (65). In the worst-case analysis, the initial voltage of the SHA would be at ground, and would have to charge up to ½ LSB of full-scale range within the acquisition time of the N-bit ADC.

$$V_{SHA}(t_{ACQ}) = V_{FSR} - \frac{V_{FSR}}{2^{N+1}} = V_{FSR}\left(1 - e^{-\frac{t_{ACQ}}{\tau}}\right) \tag{66}$$

$$t_{ACQ} = \tau \ln(2^{N+1}) \tag{67}$$

Finally, Equation (1) can be rearranged to find the sampling rate that is supported by this acquisition time. This is a worst-case minimum sampling rate because the derivation above assumes the sampling capacitor must always charge the entire full-scale range; this is an

unrealistic assumption but determining the actual initial charge on the capacitor requires advanced equipment [**70**].

$$t_{ACQ} = \frac{1}{f_S} - \frac{N}{f_{CLK}} = \tau \ln(2^{N+1}) \tag{68}$$

Equation (68) was plotted (using Equations (44), (50), (52), and (62) to back-substitute to the R_1, C_1, R_2, and C_2 of Figure 59) to show the dependence of the maximum sampling rate on the value of R_1. A constant input tone of 10 kHz is used to remove the dependence of τ on ω. With this input tone, the sampling capacitor voltage would not have to change an entire full scale range within the acquisition time; an adjustment factor was added to relax the worst-case equations above.

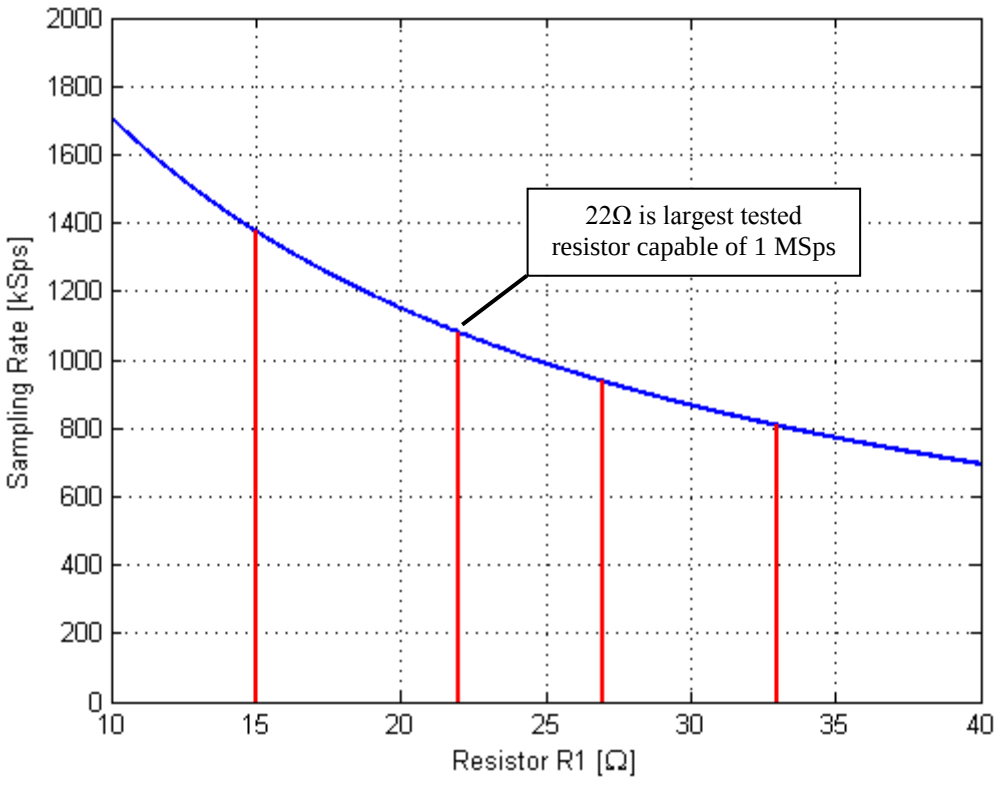


Figure 99: Achievable Sampling Rates with Different External RCs

Figure 99 demonstrates that when 27Ω and 33Ω resistors in the external RC, the maximum sampling rate is under the 1 MSps capability of the AD7982. This helps explain the attenuation at high throughputs that is seen in Figure 97. When the resistor is reduced to approximately 24Ω or below, the converter can operate at full speed. This also correlates with Figure 97, which showed that 18Ω and 22Ω performance did not fall off at 1 MSps. These observations support the conclusion that a timing-based approach to RC analysis is more appropriate than the equivalent impedance derivations of Chapter 4.

Finally, the improvement of SNR as the resistor value increased (seen in Figure 97) was attributed to cutting out more high-frequency noise. The external RC not only controls the speed of the ADC, but is also a low-pass filter with a cutoff frequency f_{3dB} of:

$$f_{3dB} = \frac{1}{2\pi R_1 C_1} \tag{69}$$

As the resistor R_1 is increased, more high-band noise is attenuated and prevented from affecting the ADC accuracy. With typical values of R_1 and C_1, the cutoff frequency can range from 1.5 MHz to 4 MHz – well above the sampling rate and input tone frequencies.

5.6.2 Isolating USB Noise to the SDP

During the course of the testing process, it was discovered that having peripherals, power adaptors, or Ethernet cables connected to the host computer could inject noise into pseudo-differential ADCs. This issue was never encountered with fully-differential ADCs, which were

presumably protected from the interference by the common-mode rejection of differential signaling. An example of the peripheral noise is shown in Figure 100.

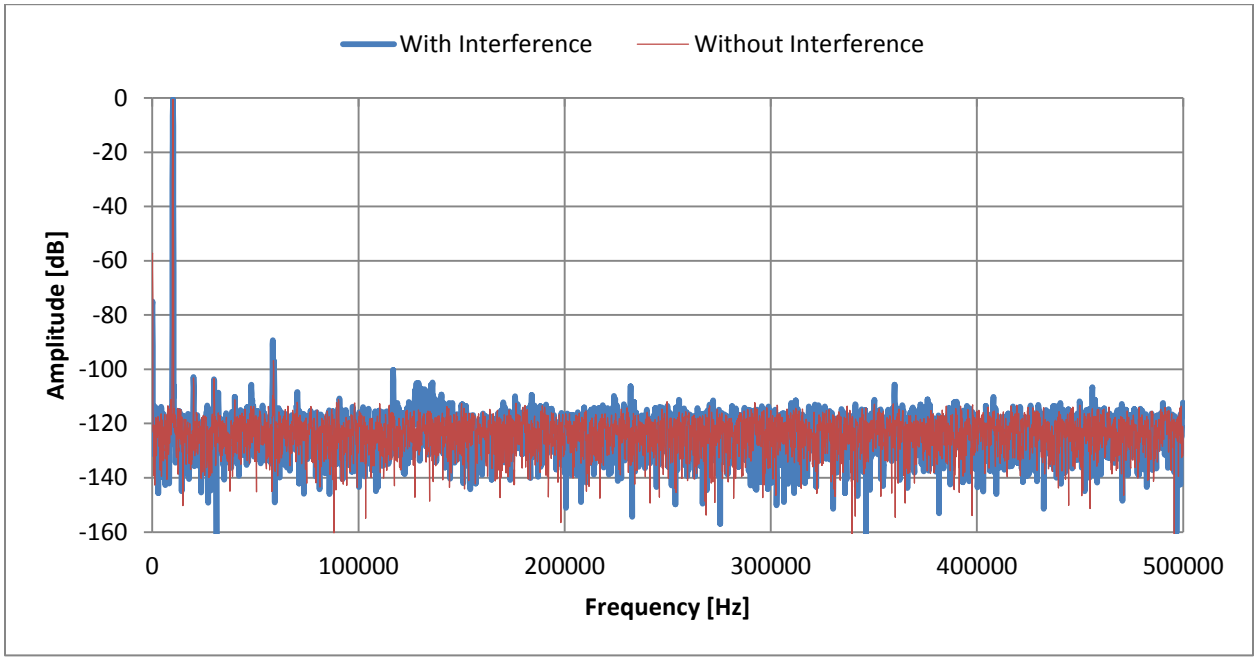


Figure 100: Peripheral Interference on Pseudo-Differential AD7983

The problem itself was difficult to quantify. For a given computer, performance dropped different amounts depending on which USB connector was used to connect to the SDP, even if the peripherals, adaptors, and other cables attached to the host computer remained constant. The effect also varied by the make and model of the host computer itself. For some PCs, the presence of the Ethernet cable made no discernible impact on performance, while on others it reduced the SNR by over four decibels.

These observations led to the conclusion that the interference was caused by poor isolation of the host computer's USB port from other power and signal lines. Unfortunately, the dependence of the phenomenon on the make, model, and peripheral configuration of the particular computer

made it impossible to issue comprehensive setup advice to customers. Therefore, an external USB isolator was investigated to see if the SDP could be shielded from host-PC noise.

Analog Devices manufactures the ADuM4160, a digital isolator for the D+/D- lines of the USB protocol. The integrated circuit contains complex circuitry to interpret the data stream, determine the direction of each packet, and enable/disable the appropriate I/O buffer [**71**]. Rather than deciphering the nuanced behavior of the ADuM4160 itself, the evaluation board provided a much simpler means of experimenting with the isolator. The iCoupler ADuM4160 Evaluation Board (pictured in Figure 101) is powered by an external 5V supply and has two female USB ports for the inbound and outbound data signals.

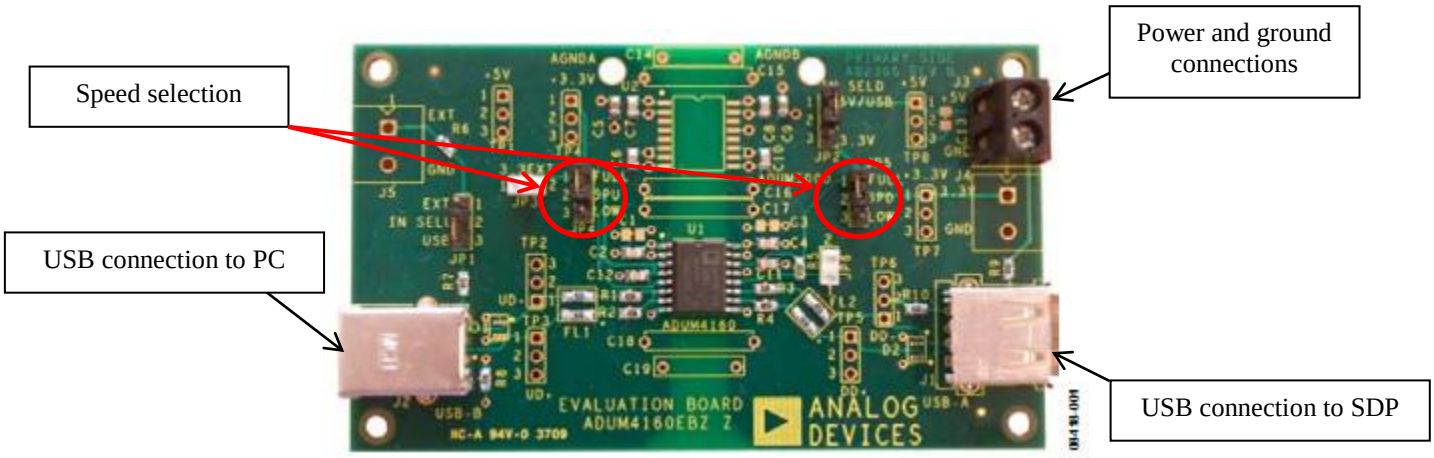


Figure 101: Photograph of the iCoupler ADuM4160 Evaluation Board

The evaluation board can switch the underlying ADuM4160 between full-speed (12 Mbps) and low-speed (1.5 Mbps) by changing the position of the two selector jumpers highlighted in Figure 101. The dual data lines of the USB interface effective double these rates. The multiplication of the sample rate times the bit-count of the PulSAR ADCs suggests that the even the 18-bit, 1.33MHz converters should be slightly under the full-speed throughput limit.

Testing was conducted by assembling a pseudo-differential board (the interference effect is not seen with fully-differential ADCs) and taking measurements with and without interfering peripherals connected. The test was then repeated with the ADuM4160 Evaluation Board attached between the SDP and the host computer. All testing was conducted at three different sampling rates (500 kSps, 1 MSps, and 1.33 MSps) to discover if the throughput limitations of the ADuM4160 affected performance. The results are shown below in Figure 102.

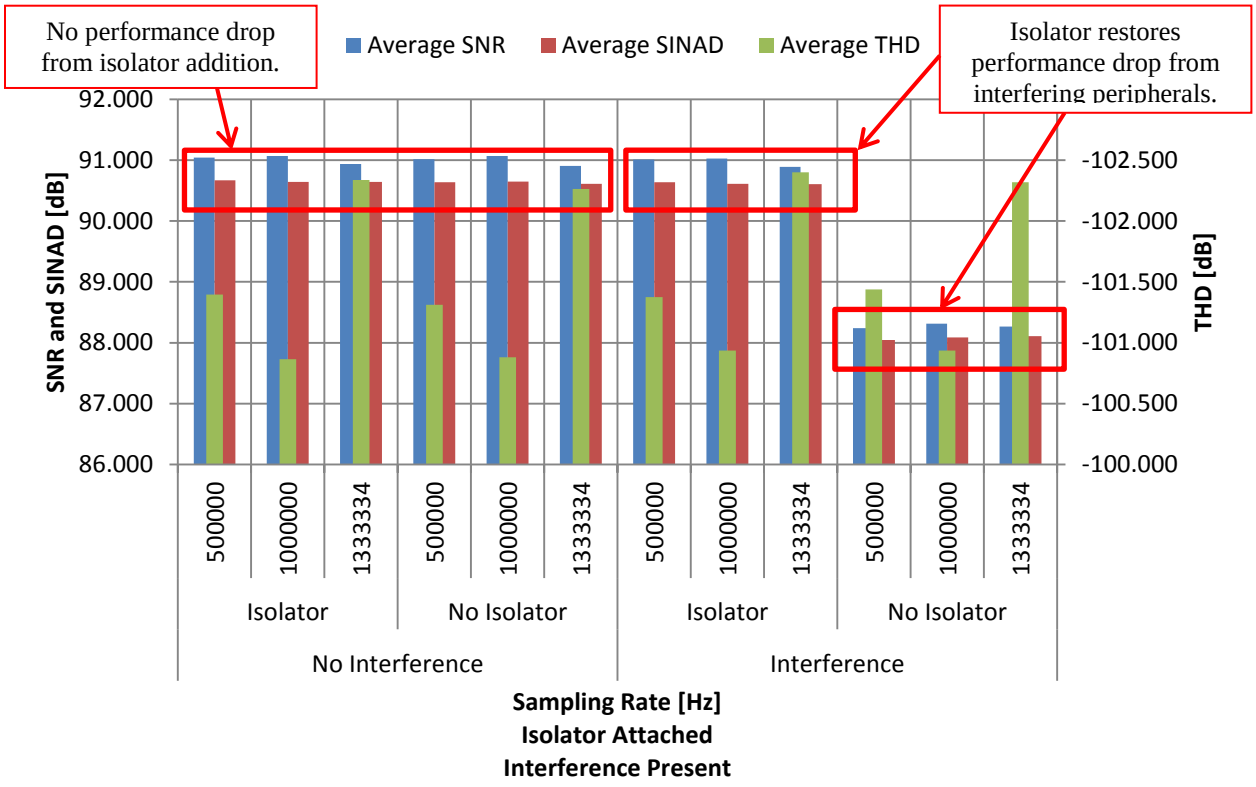


Figure 102: Effects of PC Interference with and without USB Isolator

As seen above, inserting the isolator board does not degrade performance even at the highest sampling rates, and it completely eliminates the performance drop from interfering peripherals. When the testing was repeated with the isolator configured for low-speed (3 Mbps total bandwidth) the computer refused to recognize the SDP as a connected USB device through the

isolator. It seemed as if low-speed operation was insufficient for the Windows device-recognition process to complete successfully.

5.6.3 Effects of Removing the Buffer Amplifiers

Determining the effect of the buffer amplifiers on performance was a straightforward experiment. As outlined in Chapter 4, the theory was that removing the buffer amplifiers from the reference line to the ADC and from the common-mode signal to the inputs would eliminate a source of noise from the signal path and reduce power consumption. To this end, a standard daughter card was assembled with an AD7982 (18-bit, 1 MSps fully-differential converter) and two ADA4841s. The testing involved characterizing the board when it had either the ADR435 or the ADR445 voltage reference and either the AD8032 dual-buffer populated or not. The results of this testing is shown below in Figure 103.

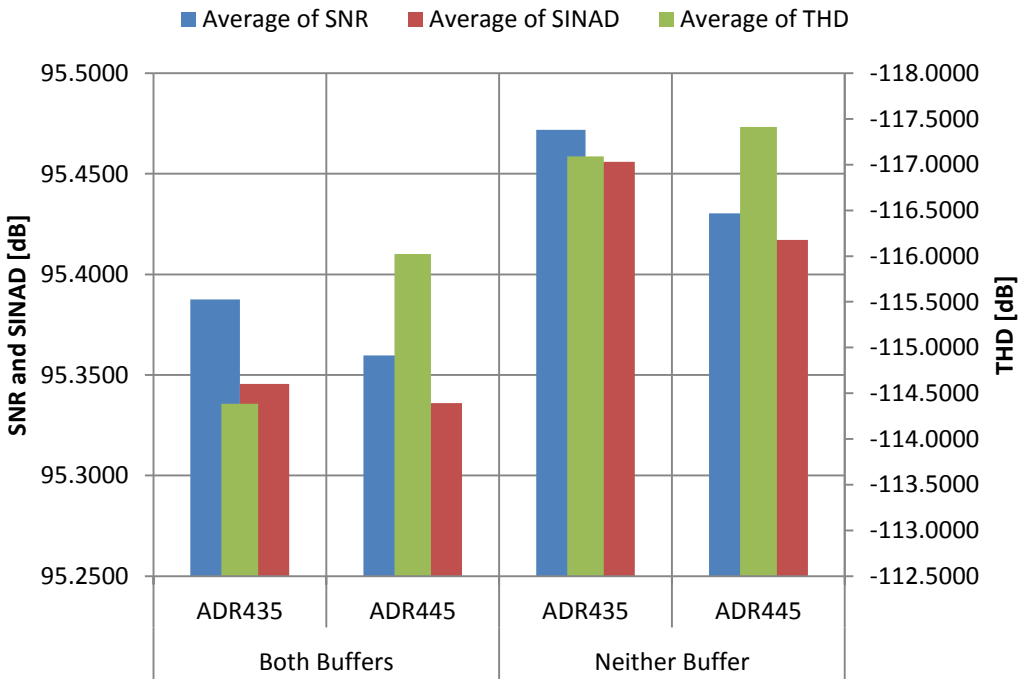


Figure 103: Performance Results of Buffer Removal

The data shows that all three dynamic metrics – SNR, SINAD, and THD – improved when the AD8032 buffer was removed. This correlates to the comparatively high noise levels of the AD8032; the dual-amplifier has 15μV of noise, which is two to four times that of the voltage references. Unfortunately, a third 5V reference was not available for testing. It would have been enlightening to investigate low-output current references to see the code oscillations warned by Martin Murnane [**9**].

5.7 LabVIEW Software

The development of the LabVIEW application was a dynamic process that evolved throughout the scope of the project. The application was initially a module to test ADC daughter cards; however, as the project progressed it grew in scope and complexity. The end product was developed to be a complete package focused specifically on ease of use as well as overall testing value. Utilizing the features drawn from existing applications, this module was built to provide the best of the rest. A linear path through the development process would be arduous and difficult to comprehend. To circumvent this issue, the LabVIEW discussion is broken into three sections, each corralling similar topics together.

Section 5.7.1 Daughter Card Recognition and Software Initialization focuses on communication with the daughter cards. Next, section 5.7.2 Data Collection and Preprocessing deliberates the handling of data received from an attached daughter card. Lastly, Section 5.7.3 Data Processing and Display details the features added to the software application to assist users in properly applying the application. Figure 104 shows the Front Panel of the application. A clear influence

of the existing software modules discussed in 4.9.1 ECB and CED Software Programs can be seen in the overall design and layout and of the application.

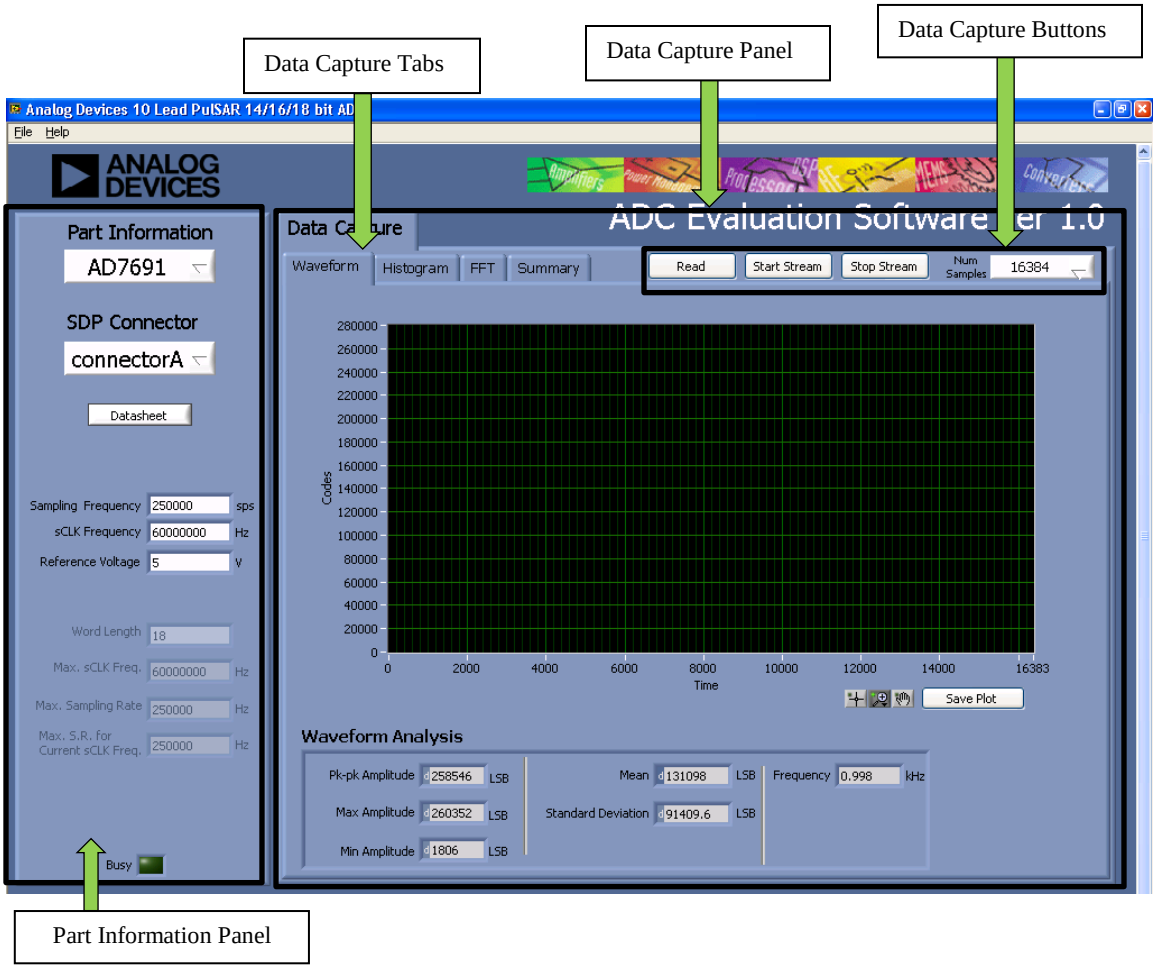


Figure 104: Front Panel

5.7.1 Daughter Card Recognition and Software Initialization

When the application is started the host computer automatically searches for an attached SDP. If no SDP card can be found by the computer, then the dialog box of Figure is displayed. This dialog box suggests that the user attach an SDP and re-attempt to establish a connection with it by hitting the Rescan button. Alternatively, the user can enter Stand-Alone mode by hitting the

Cancel button. Without an attached system, most of the software features are unavailable in Stand-Alone mode, which is discussed later in Section 5.7.3 Additional Features.

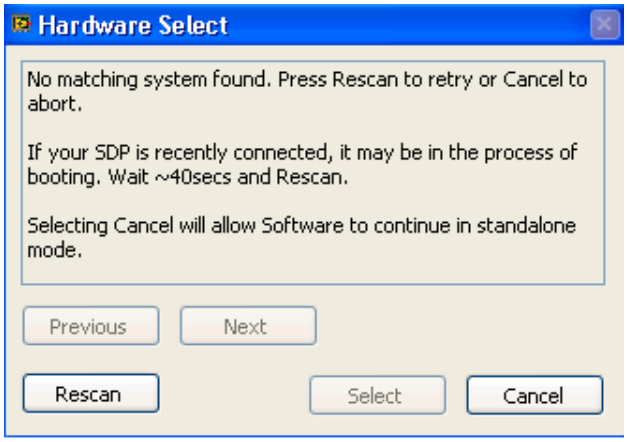


Figure 101: Dialog Box if no SDP is Detected

Next, if an SDP is card is detected, the software can attempt to read the EEPROM of the daughter card through the SDP interface. If the read fails or if the EEPROM code is unrecognized, the software prompts the user to connect a PulSAR evaluation board to commence the testing.

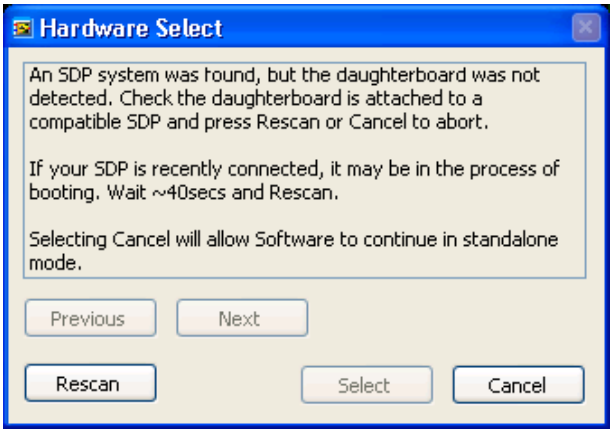


Figure 105 No Daughter Card Found

If both the SDP and a recognized daughter card are detected, the user is notified of the successful detection and all the software features will be available for use.

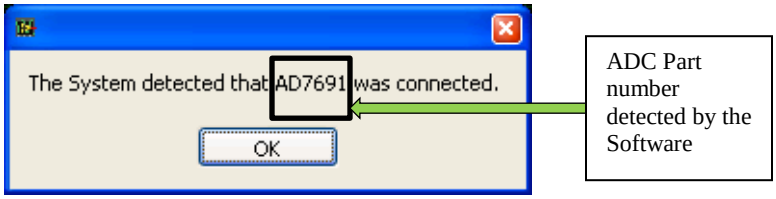


Figure 106: Confirmation Box for Successful Detection of SDP and Daughter Card

The EEPROM code on the daughter card encodes which ADC is populated on the evaluation board. Following the successful detection of both SDP and the daughter card, the information in the EEPROM code is used to initialize various software settings to match the model of the PulSAR ADC. Based on the code, the software can determine if the converter is pseudo-differential or fully-differential, its bit-count, and the maximum sampling frequency for which it is specified. This data is displayed in the Part Information panel of the main software interface.

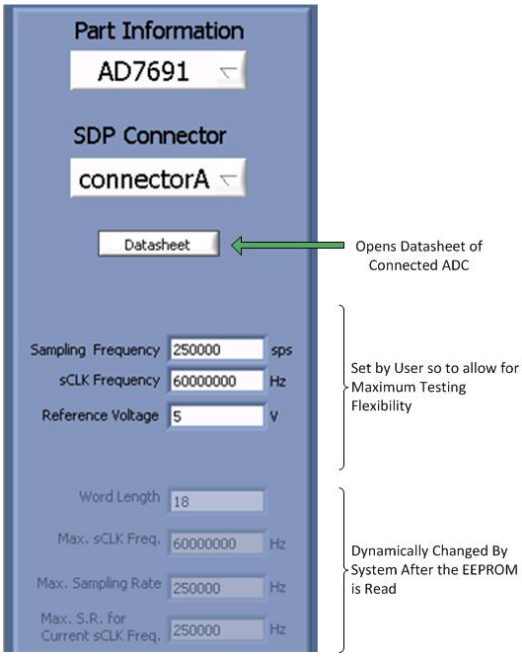


Figure 107: Part Information Panel

5.7.2 Data Collection and Preprocessing

Data can be read from the ADC in two distinct ways: a single packet of specific length or a continuous stream of packets of a specified length. The length of the packet is equivalent to the number of samples per read and can be selected using the dropdown box seen in Figure 108. The number of samples can be any power of two between 2^9 and 2^{20}.

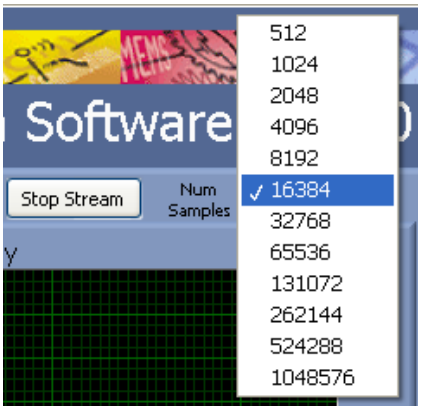


Figure 108: Dropdown for Number of Samples per Read

Unfortunately, the Blackfin processor can transmit a maximum of 2MB at a time due to memory limitations. In practice, this means that when the sample data can fit in a two-byte word (such as for 14-bit and 16-bit ADCs) the full 2^{20} samples can be read at a time; $2^{20} * 16 = 2^{24} = 2$MB. However, the 18-bit ADCs require a double-word per sample, reducing the maximum read length to 2^{19}. If the user selects 1,048,576 samples per read with an 18-bit part, the software automatically reduces the number of samples to 524,288.

A second limitation of the Blackfin processor is that the software data acquisition must occur at least once every second. Failure to maintain this rate results in a stream timeout error. For this reason, the software intelligently determines the maximum sample size to prevent the user from

misusing the software. Using Equation (1) the software also prevents the SDP from taking samples from the ADC before a conversion is completed and alerts the user of the changes made, shown in Figure 109.

Figure 109: Data Rate Change Pop-up

Once the data has been acquired from the SDP, up to two modifications are made to the raw ADC output to prepare it for signal processing by the LabVIEW software. The data must be adjusted if the ADC is fully-differential, or if it has a resolution of 14- or 18-bits. This information is gleaned from the EEPROM code used to originally detect the daughter card.

For the PulSAR series, fully-differential ADCs output data in the two's complement form, whereas the pseudo-differential converters transmit regular binary. The data processing is simplest if the two's complement codes are converted into regular binary as well; if this conversion is neglected a sine wave would resemble Figure 110 instead.

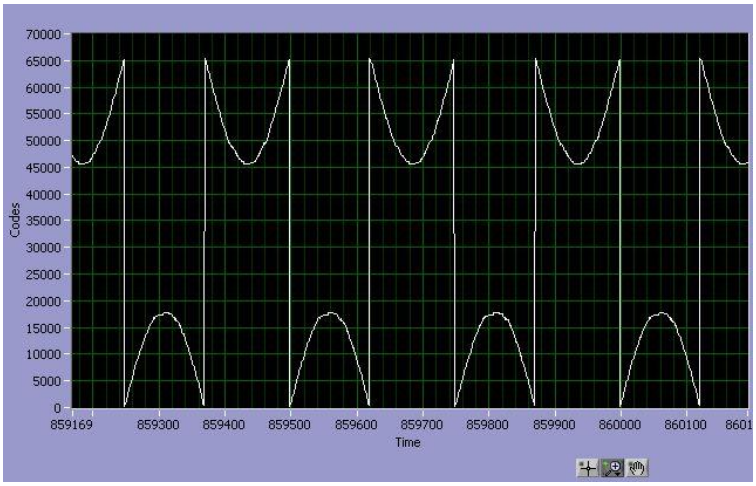


Figure 110: Two's Complement Sine Wave

Additional pre-processing must be done for 14-bit and 18-bit converters. The Blackfin transmits these data samples as part of a 16-bit word (for the 14-bit data) or as part of a 32-bit double (for the 18-bit data). In both cases, additional bits are transmitted that do not encode for real signal data. These extra bits are excised before the processing calculations are performed to prevent superfluous bits from corrupting the results.

5.7.3 Data Processing and Display

After the data has been adjusted for differences between the ADCs, the LabVIEW software creates graphs and statistics to display the signal information to the user in an informative, easy to followmanner. The results are spread across four tabs in the Data Capture panel, which group logically-related information together.

The first of the four tabs is the Waveform tab (Figure 111), which provides time-domain analysis information. The graph replicates the analog waveform sampled by the ADC, and can be manipulated with the zoom tools to magnify any region of interest. The Waveform Analysis inset

displays the maximum, minimum, and average codes observed, which can be converted to real voltages by multiplying by $V_{REF}/2^N$. The waveform tab is most useful for quickly assessing clipping conditions and the DC bias level of the signal.

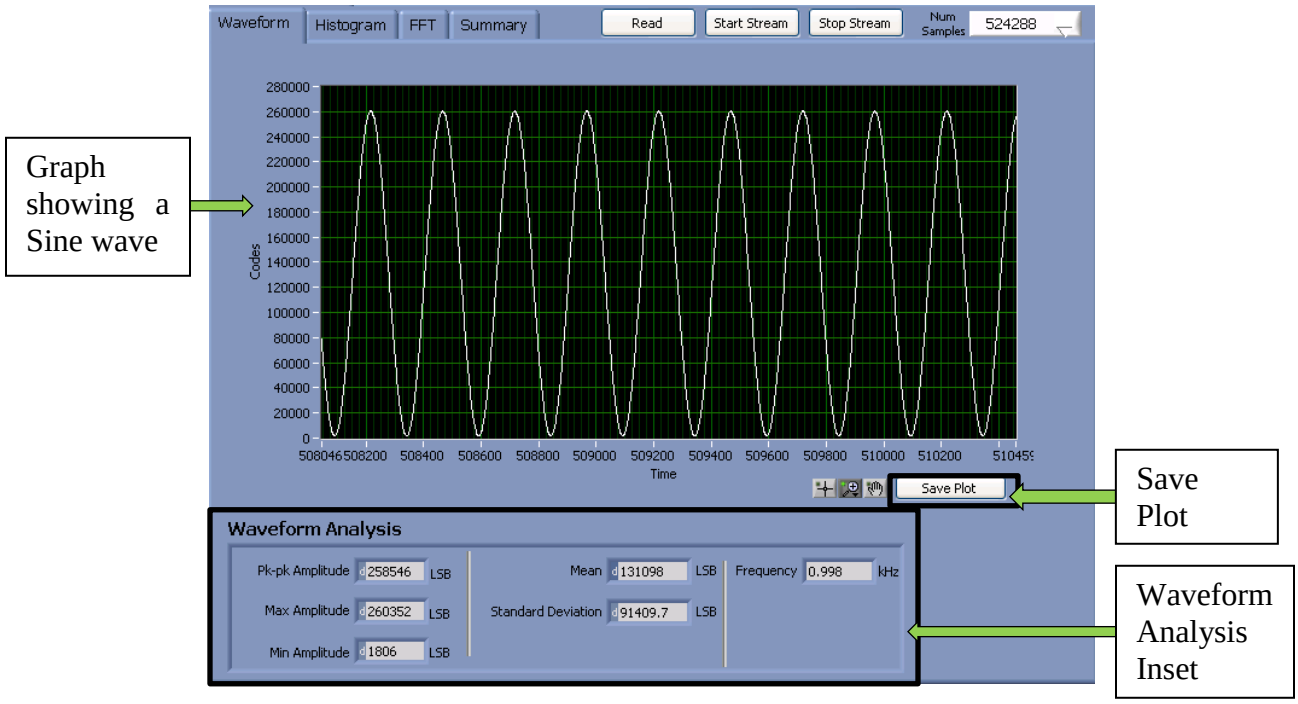


Figure 111: Waveform Tab of the Data Capture Panel

The Histogram tab – shown in Figure 112 – is used to display information about the distribution of output codes. As discussed in Section 2.2, the histogram data is particularly useful for identifying missing codes and quantifying the differential non-linearity (DNL). Basic statistical data about the code distribution is displayed in the Histogram Analysis inset, such as the minimum, maximum, and mean code observed.

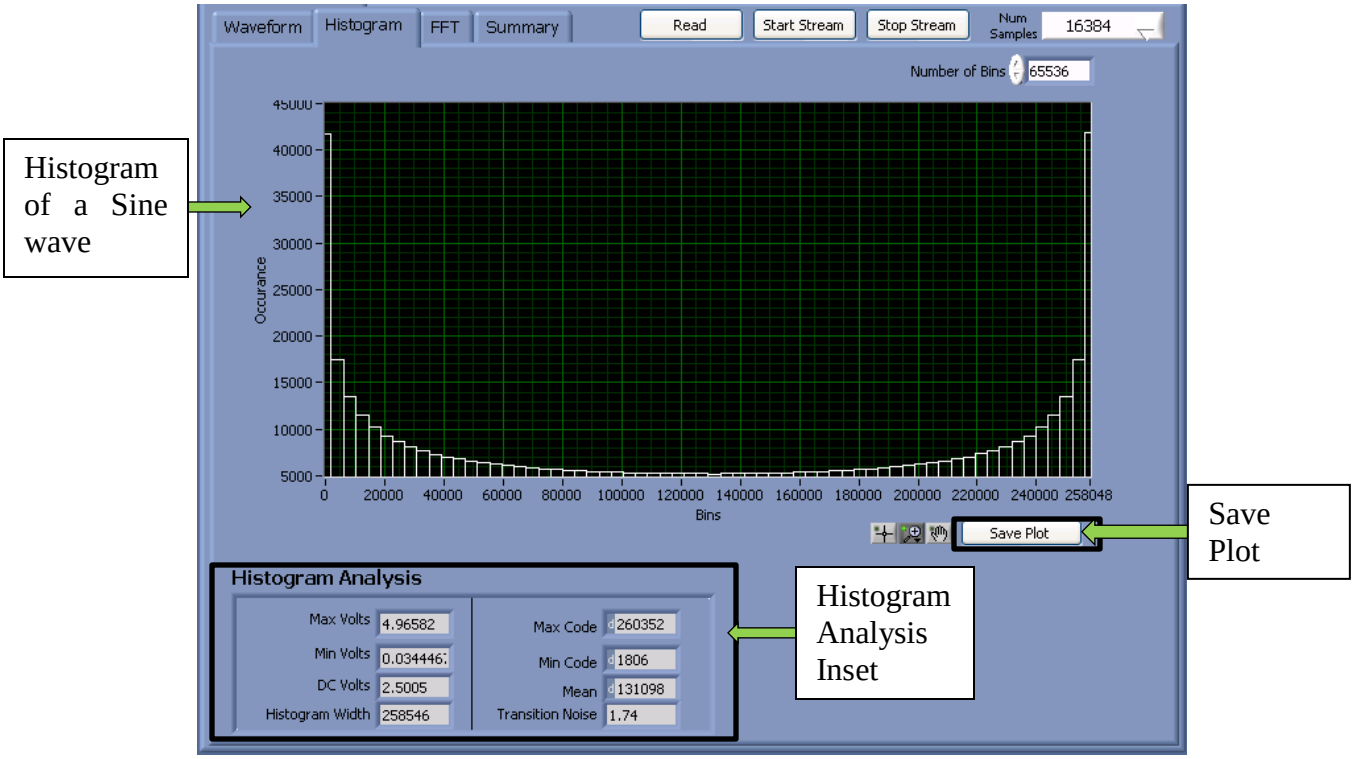


Figure 112: Histogram Tab of the Data Capture Panel

The histogram plot also supports dynamic alteration of the number of bins while keeping the absolute minimum and maximum constant. With a lower bin count, each individual bin is larger and envelopes a greater number of codes and yields a coarser graph. The bin count is preset to provide fine resolution of the distribution curve, although the user can adjust the bin count using the input box above the graph.

The FFT tab (Figure 114) displays frequency-domain analyses of the sampled data. The top half of the tab displays the graph of the Fourier transform. To calculate the FFT, first a 7-term Blackman-Harris windowing function is applied to the signal. A windowing function is a digital filter used to eliminate the effects of spectral leaking. Spectral Leaking is a consequence of a real-world system's inability to sample a signal an infinite amount of times. The signal

discontinuities caused by this reality result in spectral energy from individual frequencies leaking into adjacent frequencies. Of course, windowing functions have tradeoffs. Removing the spectral leakage can result in inaccuracies in frequency domain analysis. Different windows are more appropriate for different calculations. The 7-term Blackman Harris window is a particularly powerful tool when accuracy in AC performance characteristics such as SNR, SINAD, and THD are desired.

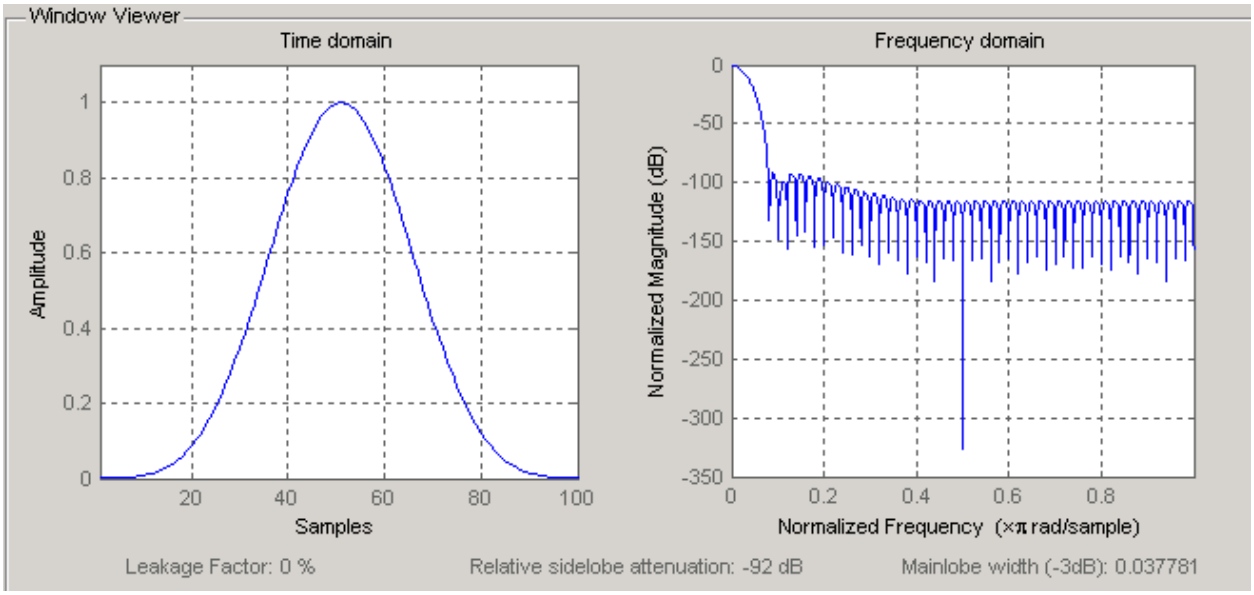


Figure 113: Time Domain Response Frequency Response of a Blackman-Harris Window

Figure 113 shows the time domain response and frequency response of a Blackman-Harris window. The frequency response of the Blackman-Harris s attenuates noise at each frequency allowing for accurate AC calculations. However, the large main lobe of a 7-term Blackman-Harris window makes it unsuitable for analyzing signals made up of multiple sine-waves close in frequency [**72**]. This project mainly focused on meeting the AC characteristics of the ADCs with pure tones so a 7-term Blackman-Harris window was used.

After this windowing function is applied, LabVIEW library functions are used to generate the FFT data, which is further processed to calculate SNR, SINAD, THD, and other dynamic parameters. SINAD is the ratio of Signal to Noise and Distortion in the sample. This calculation excludes the DC value in the sample. Similarly, SNR is the ratio of Signal to the Noise in the sample with DC values and harmonics (usually the first five) removed.

To calculate SINAD and SNR, the first six data bins are removed from the signal to eliminate the DC term. SNR and SINAD compare signal strength to noise and noise and harmonic distortion, respectively; DC terms are ignored in both these calculations and thus need to be removed. The older CED and ECB software removed five DC bins (the bins discussed here are different from the bins discussed in the earlier Histogram discussion); testing revealed this to be ineffective, especially when taking larger number of samples. Larger sampling frames reduce the frequency range each FFT bin corresponds to. At sampling frames in excess of 100,000 samples (each frequency bin less than 5 Hz in width), the DC component was observed spreading into a sixth DC bin. The relationship between frequency bins and frequency is given by:

$$\Delta f = \frac{f_S}{N} \tag{70}$$

where, Δf is the frequency corresponding to each bin, F_s is the sampling frequency and N is the number of samples. For example, if 524288 samples were taken from an 18 bit ADC at 1Msps, then each bin would correspond to 2.5431Hz in frequency domain. If 32768 samples were taken from the same ADC at 1Msps, each bin would correspond to 40.68Hz in frequency domain.

Removing six DC bins instead of five provided more stable dynamic performance over a range or sample sizes.

The harmonics of the signal must also be removed to calculate the SNR. Six bins corresponding to the signal and five bins corresponding to each of the first five harmonics are removed from the sample. These bins are removed because they adequately eliminate the signal and harmonics from the noise floor, which per Equation (14), are not considered in the SNR calculation.

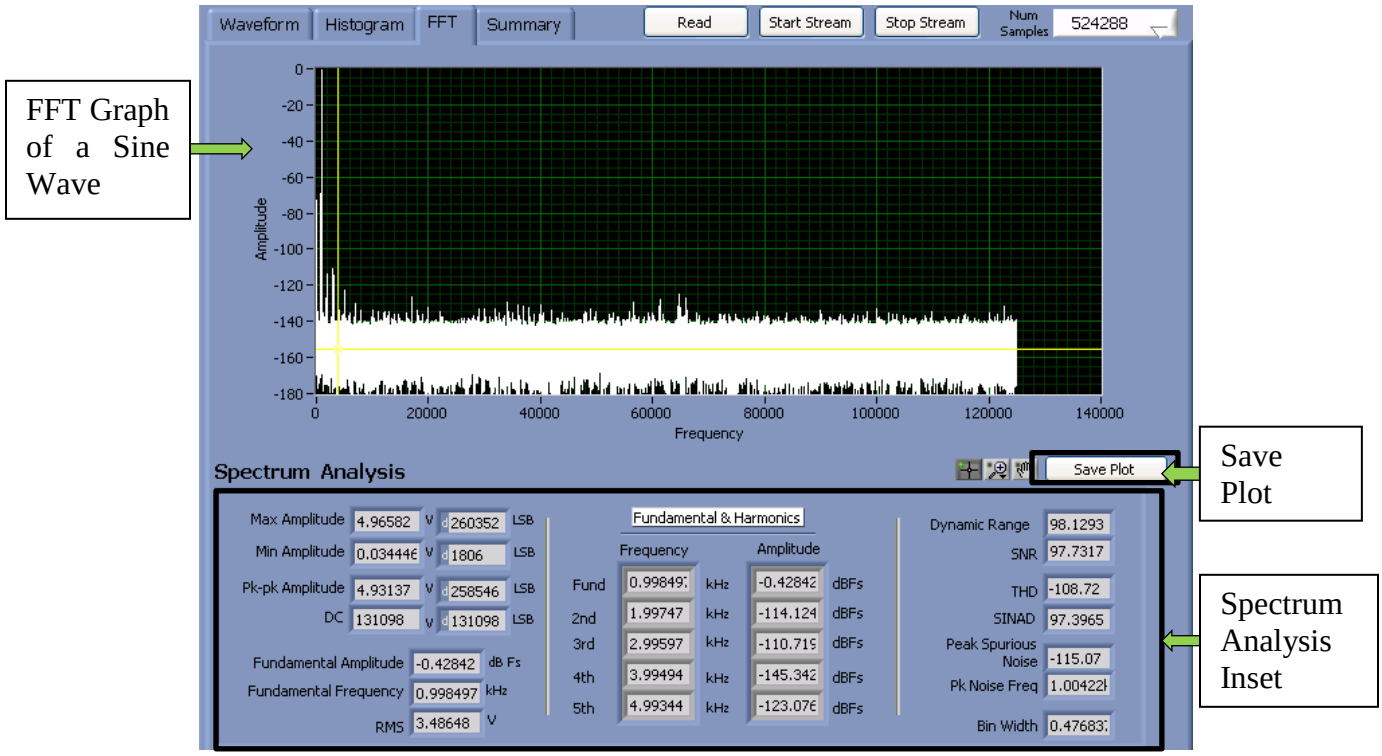


Figure 114: FFT Tab of the Data Capture Panel

As the name suggests, the Summary tab summarizes the three previous tabs and displays them in one window as shown in Figure 115. This tab shows smaller versions of the waveform,

histogram, and the FFT along with the most important values from the previous tabs. This tab was included to make it easier for a user to monitor each distinct analysis at a single time.

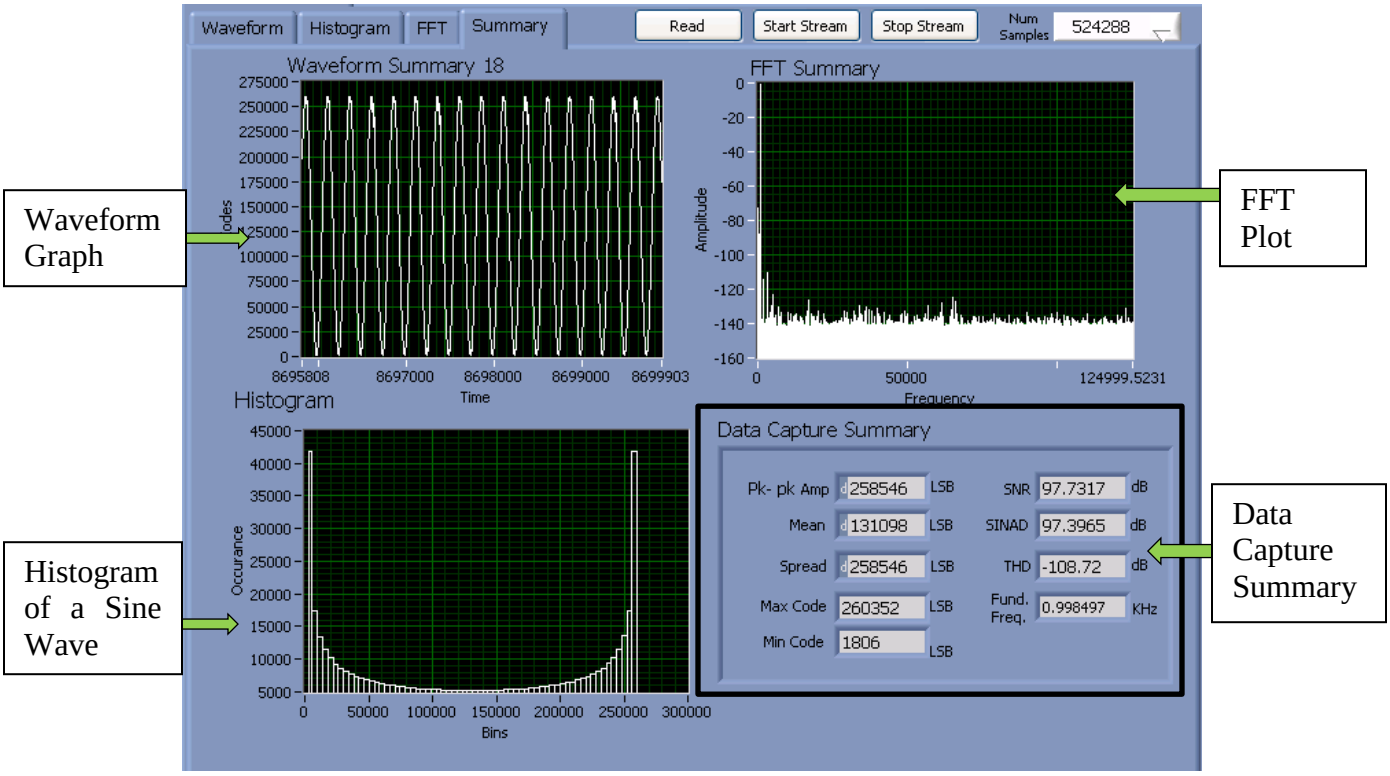


Figure 115: Summary Tab of the Data Capture Panel

To make it easier for users to gather and analyze data, each of the tabs also provides an option to save raw data, take screenshots of the application or load previously saved data. When saving the raw data to a file, the session settings (including sampling rate, clock frequency, and ADC model) are also logged; these settings are used when loading data to display the information in the exact same manner. The Load and Save options can be accessed through the File drop-down menu shown in Figure 116: Load and Save Dropdown.

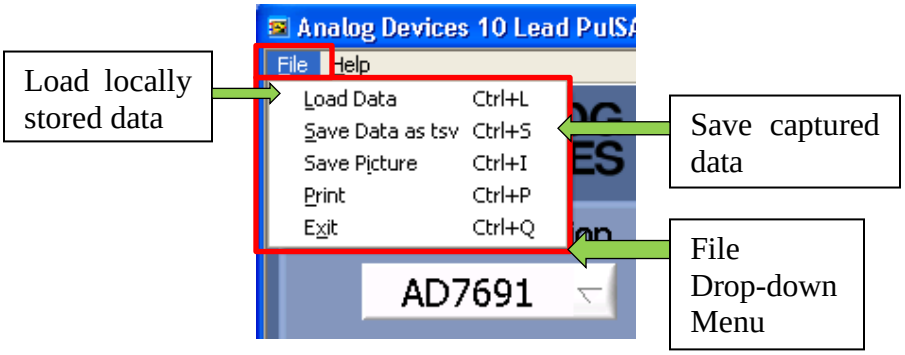


Figure 116: Load and Save Dropdown

5.7.3 Additional Features

In order to differentiate the application from previous software a number of new features were added. These features looked to enhance the user experience and ease of use. The Stand-Alone mode feature was introduced to allow use of the application without having an SDP board physically connected to the computer.

Stand-Alone mode is a new feature introduced to allow the user software functionality without the need to connect an SDP. In this mode the majority of the GUI is inoperable. The user is unable to read or stream a new measurement; they are unable to change any parameters pertaining to taking a measurement as well. However, the user is able to load any previously saved file without the need to connect an SDP. When a .TSV file is loaded, the software dynamically re-performs all the calculations done on a new measurement. This allows the user to view the same exact results as when the loaded measurement was originally taken.

Figure 117 shows the application in Stand-Alone mode. The features that have been disabled in this mode are marked with blue outline and the features that have been enabled for use in this mode are outlined in red.

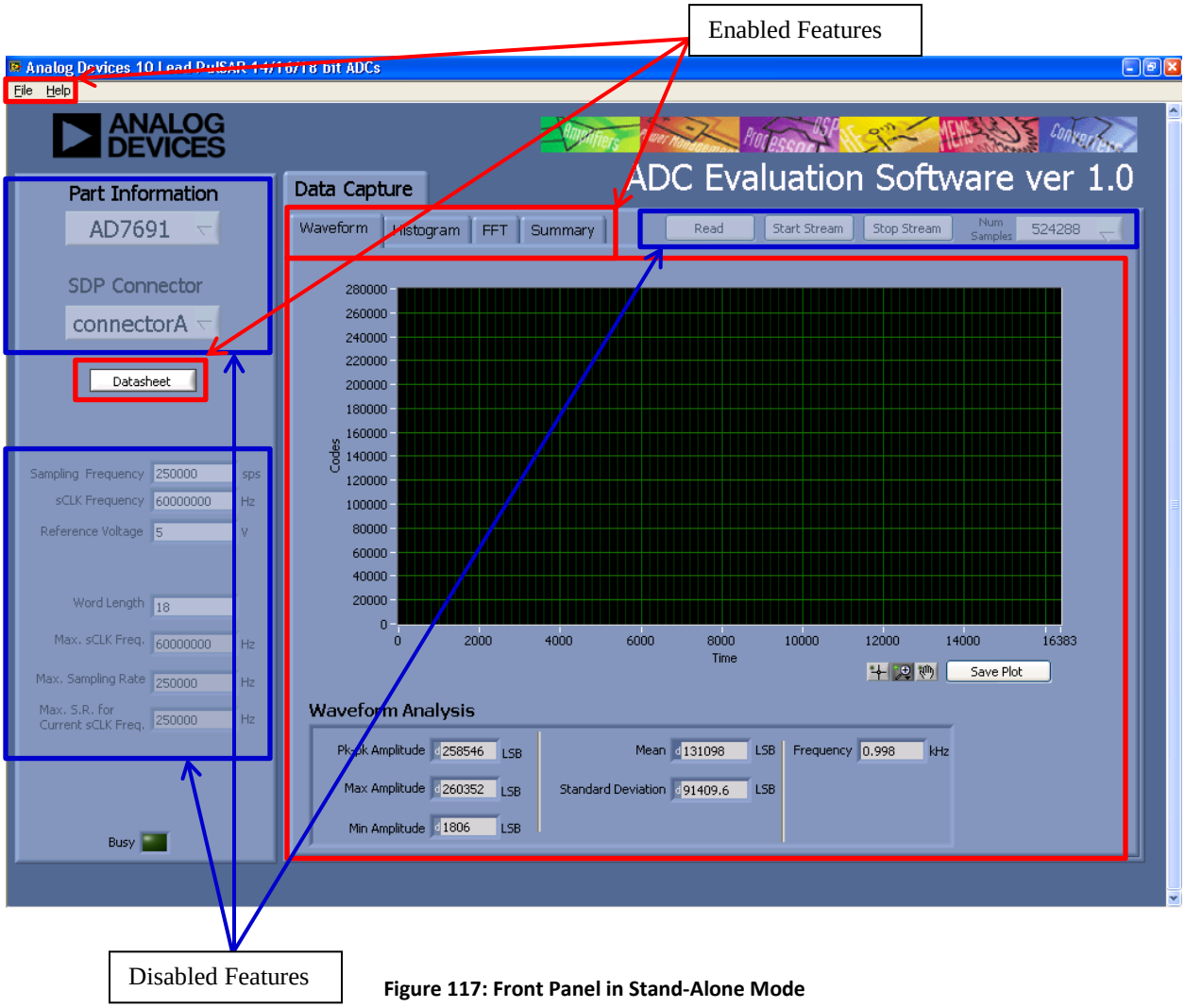


Figure 117: Front Panel in Stand-Alone Mode

The application provides the user with a Datasheet button to allow for quick access to an attached ADC's datasheet. When the button is first clicked, the application attempts to make a connection with the Analog Devices website. If successful, the application proceeds to open up to the appropriate ADC's information page. This page contains the most up to date datasheet of a given component. If the application cannot communicate with the website, a PDF version of the datasheet located in the applications installer is opened instead. Although this datasheet could be outdated pending the creation date of the installer, it still offers the user a quick solution for comparing the datasheet specifications with their results.

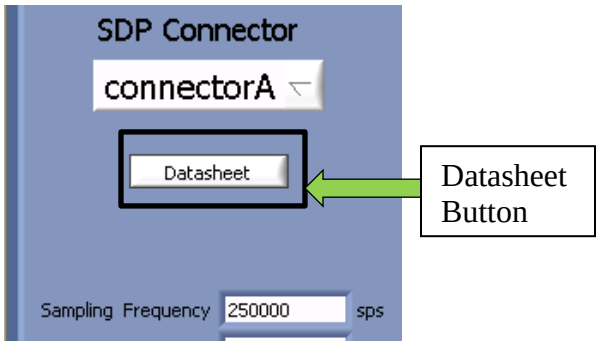


Figure 118: Datasheet Button

The File and Help dropdown menus provide the user with basic features meant to enhance the overall user experience. The File menu contains the Load Data, Save Data, Save Picture, Print, and Exit options. Each of these can be accessed using either the dropdown menu or the shortcut keys associated with each feature.

Table 31: List of Short-cut Keys

Shortcut	Action
Control + F	File drop-down menu
Control + L	Load Data from a file
Control + S	Save Data as .tsv
Control + I	Save Screen-shot
Control + P	Print Window
Control + Q	Exit
Control + H	Help drop-down menu
Control + W	Analog Devices Website
Control + D	Show supported devices

The Help menu has two options; Supported ADCs and Website. Supported ADCs option simply displays a list of PulSAR components supported in the software's revision. The Website option opens the Analog Devices webpage in the default web-browser.

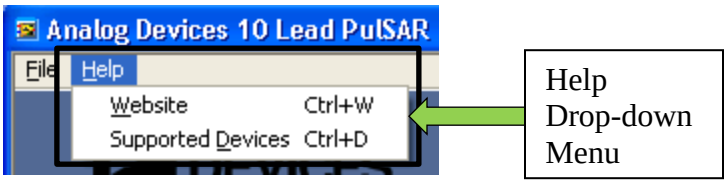


Figure 119: Help drop-down menu

5.7.4 Installer

To make the process of acquiring and using the software easier, an installer was built which bundled all the necessary executables of the software along with the required drivers and documentation. This was accomplished using the bundled installer build tool provided by National Instruments in the LabVIEW suite.

The installer first installs the ’10 Lead PulSAR ADCs’ application after which it proceeds to install the ‘AnalogDevices SDP Driver’. This driver allows the user’s computer to recognize the SDP board. The installer also installs easily accessible short-cuts under the Program-files menu which can be accessed from the Start Menu in the task-bar.

Chapter 6: Conclusions and Future Work

This project aimed to further develop the PulSAR ADC testing platform. It focused specifically on improving upon the original ADC daughter card design to offer a more modular, and all around adaptable testing solution. The group sought to not only improve upon this design, but also offer a low power and High AC performance solution. The group also re-designed older ADI software programs to be compatible with the new SDP testing platform while offering several improvements to enhance user experience.

The first improvement designed by the group was the addition of surfboard and expansion board ADC driver cards. These cards provided an easier, modular solution for testing different ADC driver circuitry. These two solutions were expanded to also include fully-differential drivers as well as instrumentation amplifiers, rather than just the single-ended amplifiers used in the original design. An integrated power solution was also developed to allow users to test PulSAR ADCs off a single 7V wall wart voltage regulator. For those customers desiring to use integrated circuits on the daughter card that are not supported by the standard power solution, the new design also included a benchtop option that bypassed the onboard regulators.

The group also offered a wide range of theoretical discussion and testing pertaining to a low power circuit solution as well as a high performance AC circuit solution. From these conclusions, *Cftls* can be developed to offer ADI's customers quick solutions to specific needs.

Lastly, the group developed software compatible with the SDP testing platform and PulSAR ADC daughter cards. This software built upon older designs to offer a more user friendly environment, while improving upon the actual communication of an ADC's performance. The software module featured new systems, such as automatic part detection, to ease the software's use.

Despite these successful project goals, there is still future work to consider. First, the daughter card with the integrated power supply should be tested to verify performance. This testing should not only include verification of the power supply, but should determine whether this power supply design affects system performance. If it does, the offending parts should be either replaced or redesigned to offer customers the best possible product. Next, the fully differential and instrumentation amplifier expansion and surfboards could not be fabricated in time to be tested by this project group; these boards should be tested to verify no performance loss.

Another possible area for system improvement is the FFT function libraries in the LabVIEW software. The FFT function assumes that a sampled waveform is of infinite length. For practical applications this is inherently impossible. An implication of this property is that an FFT calculation also assumes that a periodic waveform is of an integer number of cycles [**73**]. The majority of systems are not able to synchronously sample the input waveform to continuously produce sample sets that are integrally cyclical in nature. As a result sharp ends are created on the plot of a sampled waveform.

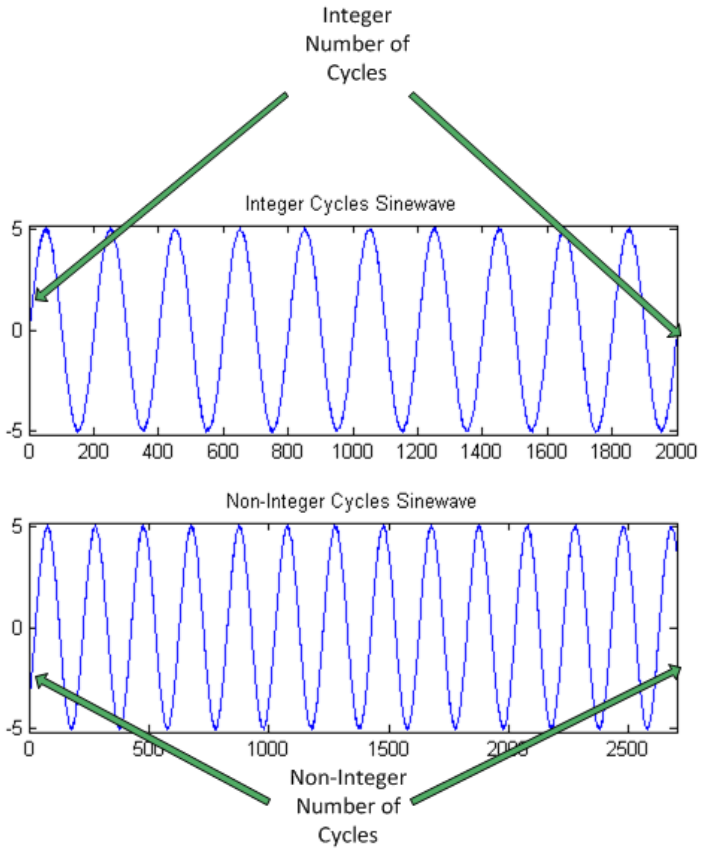


Figure 120: Integer Vs. Non-Integer Number of Sampled Cycles

The resultant abrupt changes in amplitude lead to an effect known as spectral leakage. Spectral leakage causes signal energy to disperse across many different FFT bins whereas all said energy should be concentrated in a single frequency bin [**73**]. This effect is illustrated in Figure 121.

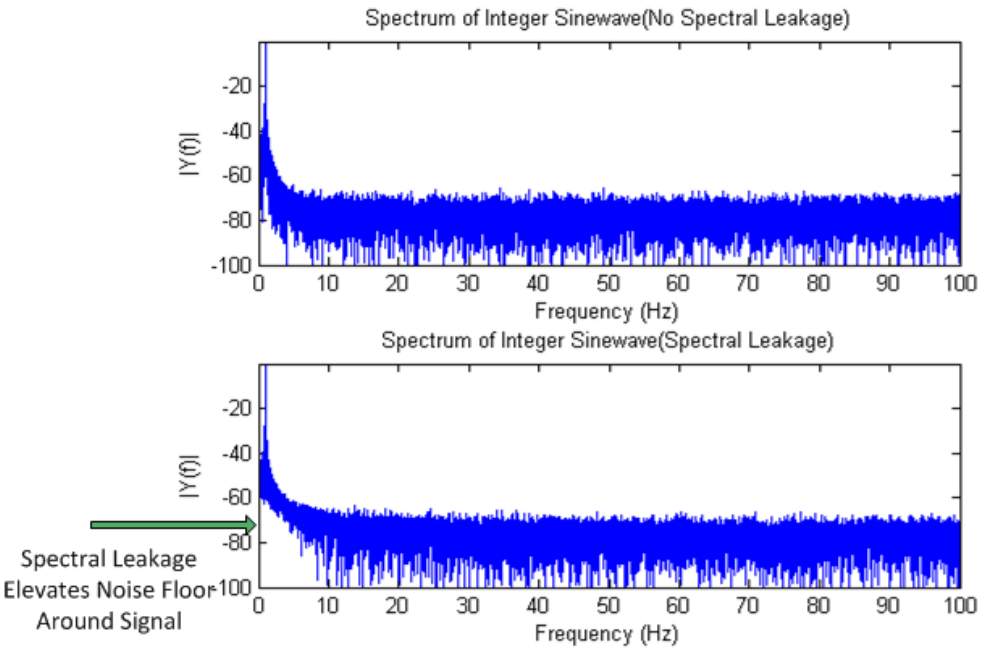


Figure 121: Effects of Spectral Leakage on a Signal's FFT

One solution devised to alleviate this inevitable condition is to run the sampled waveform through a windowing function. A windowing function is any function that can be multiplied by a sampled waveform to reduce the discontinuities produced at the end of the sampled waveform. Generally a windowing function smoothly reduces the ends of the signal to zero while leaving it wholly intact in the center of the window.

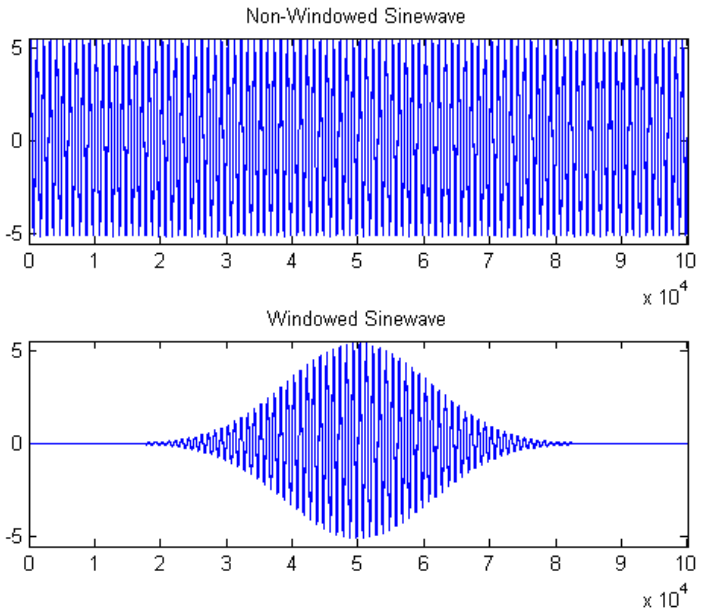


Figure 122: Non-Windowed Vs. Windowed Sine Wave

Windowing a signal has a profound effect on the frequency domain graph, eliminating the spectral leakage seen in the frequency domain of a non-windowed signal. This effect has a tradeoff though as apply a windowing function lowers the energy found in the fundamental frequency. This can lead to lower readings in dynamic parameters such as SNR and SINAD if not compensated for [**74**].

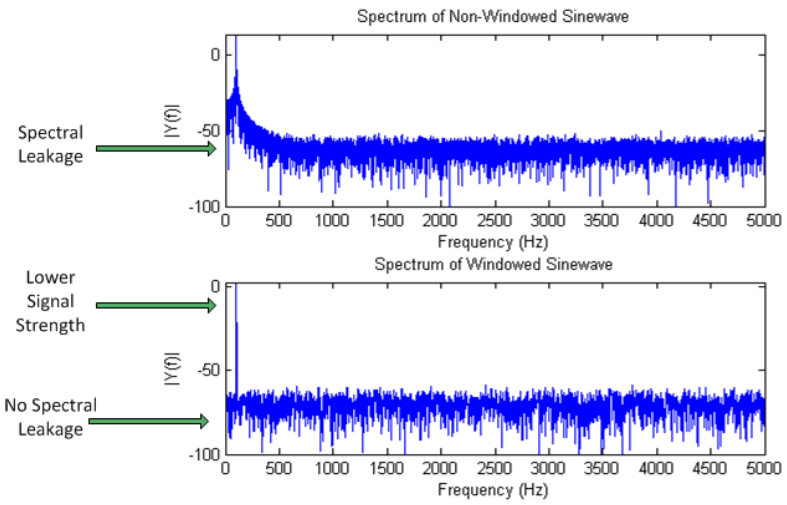


Figure 123: Effect of Windowing a Signal on the FFT

It is currently unknown whether there is any compensation being made in the LabVIEW FFT module used in Analog Devices' evaluation software. If this compensation is not being made SNR and SINAD could be falsely reading 2 to 3dB low. Of course, this improvement hinges on several assumptions. First, someone with a good knowledge of the FFT would need to work through this code to determine if there is any compensation for the windowing taking place in the existing libraries. This would also be contingent on whether windowing is used when the datasheet specifications are gathered; the applications team should endeavor to match the component qualification procedure as closely as possible.

Lastly a continuation of the high AC performance *CftL* detailed in Section 5.4 Testing Results of the High AC Performance *CftL* should be pursued. Time and component constraints left the results falling short of the envisioned goal. It is the belief of this group that the results gathered can be improved upon by investigating the effect of the reference buffer as well as additional ways to reduce noise produced by the reference itself.

Appendix A: Full Results Data

PERFORMANCE OF ADA4841 LOW POWER BOARDS

Driver	Power	Reference	Buffer	f_S [Hz]	f_{IN} [Hz]	SNR [dB]	SINAD [dB]	THD [dB]
ADA4841	3.5V to 0V	ADR291	AD8032	200000	5000	81.652	81.570	-98.232
					10000	81.516	81.439	-98.340
					20000	81.931	81.832	-98.051
				400000	5000	81.603	81.525	-98.318
					10000	81.593	81.526	-98.838
					20000	82.012	81.905	-97.690
				600000	5000	81.648	81.573	-98.514
					10000	81.591	81.528	-99.081
					20000	81.988	81.884	-97.733
				800000	5000	81.730	81.657	-98.637
					10000	81.711	81.650	-99.258
					20000	82.106	82.017	-98.395
				1000000	5000	81.683	81.591	-97.701
					10000	81.700	81.633	-98.961
					20000	82.118	82.010	-97.672
ADA4841	3.5V to 0V	ADR291	None	200000	5000	82.647	63.234	-63.298
					10000	82.906	68.782	-68.965
					20000	83.014	73.044	-73.530
				400000	5000	82.781	63.228	-63.353
					10000	82.966	68.777	-68.963
					20000	83.077	73.046	-73.539
				600000	5000	82.750	63.216	-63.286
					10000	82.934	68.778	-68.967
					20000	83.076	73.042	-73.558
				800000	5000	82.733	63.209	-63.270
					10000	82.944	68.773	-69.025
					20000	83.027	73.035	-73.544
				1000000	5000	82.762	63.196	-63.257

					10000	81.522	68.711	-68.954
					20000	83.000	73.015	-73.549
ADA4841	3.5V to 0V	ADR441	AD8032	200000	5000	82.573	82.309	-94.437
					10000	83.346	83.190	-97.414
					20000	83.282	83.132	-97.611
				400000	5000	82.551	82.304	-94.668
					10000	83.302	83.150	-97.449
					20000	83.331	83.186	-97.752
				600000	5000	82.581	82.338	-94.796
					10000	83.341	83.199	-97.768
					20000	83.292	83.158	-98.023
				800000	5000	82.464	82.225	-94.716
					10000	83.372	83.234	-97.880
					20000	83.018	82.898	-98.161
				1000000	5000	82.601	82.349	-94.623
					10000	83.140	83.031	-98.696
					20000	83.405	83.256	-97.677
ADA4841	3.5V to 0V	ADR441	None	200000	5000	83.116	78.936	-81.032
					10000	83.360	74.640	-75.277
					20000	83.474	73.642	-74.148
				400000	5000	83.231	78.999	-81.121
					10000	82.786	74.573	-75.330
					20000	83.600	73.671	-74.145
				600000	5000	83.281	79.028	-81.087
					10000	82.956	74.652	-75.364
					20000	83.584	73.692	-74.228
				800000	5000	83.399	79.093	-81.110
					10000	83.005	74.678	-75.449
					20000	83.649	73.722	-74.239
				1000000	5000	83.171	78.986	-81.078
					10000	82.734	74.653	-75.399
					20000	83.560	73.695	-74.245

PERFORMANCE OF AD8655 LOW POWER BOARDS

Driver	Power	Reference	Buffer	f_S [Hz]	f_{IN} [Hz]	SNR [dB]	SINAD [dB]	THD [dB]
AD8655	3V to 0V	ADR291	AD8032	200000	5000	81.116	80.639	-90.400
					10000	81.053	80.077	-87.016
					20000	81.472	78.452	-81.603
				400000	5000	81.128	80.651	-90.413

					10000	81.165	80.171	-87.058
					20000	80.631	78.168	-81.833
				600000	5000	81.161	80.686	-90.473
					10000	81.103	80.103	-86.940
					20000	80.304	78.083	-82.115
				800000	5000	81.222	80.732	-90.355
					10000	81.201	80.200	-87.060
					20000	80.472	78.185	-82.080
				1000000	5000	81.261	80.726	-89.995
					10000	81.353	80.285	-86.893
					20000	80.406	78.131	-82.050
AD8655	3V to 0V	ADR291	None	200000	5000	81.316	63.083	-63.164
					10000	81.345	67.936	-68.150
					20000	81.666	70.662	-71.045
				400000	5000	81.355	63.077	-63.219
					10000	81.369	67.937	-68.155
					20000	80.869	70.632	-71.150
				600000	5000	81.418	63.071	-63.156
					10000	81.370	67.935	-68.155
					20000	80.507	70.635	-71.166
				800000	5000	81.447	63.064	-63.139
					10000	81.359	67.938	-68.221
					20000	80.405	70.640	-71.171
				1000000	5000	81.275	63.065	-63.144
					10000	81.365	67.966	-68.178
					20000	80.424	70.700	-71.258
AD8655	3V to 0V	ADR441	AD8032	200000	5000	84.004	83.035	-90.011
					10000	84.261	82.435	-87.080
					20000	84.625	79.764	-81.577
				400000	5000	84.042	83.079	-90.092
					10000	84.289	82.438	-87.065
					20000	83.050	79.326	-81.759
				600000	5000	84.068	83.101	-90.107
					10000	84.005	82.247	-87.015
					20000	81.893	78.950	-82.083
				800000	5000	84.062	83.113	-90.159
					10000	83.995	82.251	-87.084
					20000	81.555	78.806	-82.118
				1000000	5000	84.304	83.305	-90.162
					10000	83.928	82.168	-86.952
					20000	81.496	78.732	-82.035
AD8655	3V to 0V	ADR441	None	200000	5000	82.816	78.648	-80.757

					10000	82.348	74.467	-75.249
					20000	82.824	72.665	-73.127
				400000	5000	82.823	78.666	-80.834
					10000	82.470	74.518	-75.293
					20000	81.900	72.628	-73.259
				600000	5000	82.638	78.622	-80.837
					10000	82.465	74.543	-75.324
					20000	81.425	72.608	-73.277
				800000	5000	82.548	78.609	-80.858
					10000	82.455	74.569	-75.416
					20000	81.447	72.641	-73.299
				1000000	5000	82.466	78.625	-80.944
					10000	82.453	74.625	-75.415
					20000	81.341	72.709	-73.416
AD8655	4V to -1V	ADR291	AD8032	200000	5000	81.217	81.125	-97.371
					10000	81.446	81.331	-96.719
					20000	81.387	81.141	-93.599
				400000	5000	81.243	81.157	-97.576
					10000	81.427	81.317	-96.827
					20000	81.428	81.160	-93.288
				600000	5000	81.277	81.197	-97.858
					10000	81.441	81.334	-96.944
					20000	81.421	81.156	-93.311
				800000	5000	81.317	81.238	-97.918
					10000	81.521	81.408	-96.812
					20000	81.598	81.340	-93.572
				1000000	5000	81.379	81.304	-98.229
					10000	81.677	81.582	-97.636
					20000	81.586	81.367	-94.238
AD8655	4V to -1V	ADR291	None	200000	5000	81.403	63.199	-63.281
					10000	81.629	68.314	-68.533
					20000	81.626	71.677	-72.159
				400000	5000	81.438	63.198	-63.342
					10000	81.682	68.312	-68.533
					20000	81.647	71.672	-72.220
				600000	5000	81.389	63.192	-63.280
					10000	81.688	68.296	-68.518
					20000	81.545	71.658	-72.187
				800000	5000	81.373	63.192	-63.271
					10000	81.559	68.285	-68.575
					20000	81.677	71.675	-72.179
				1000000	5000	81.329	63.193	-63.274

					10000	81.638	68.308	-68.523
					20000	81.668	71.747	-72.286
AD8655	4V to -1V	ADR441	AD8032	200000	5000	84.085	83.362	-92.032
					10000	84.482	83.767	-93.778
					20000	84.600	81.624	-86.901
				400000	5000	84.123	83.434	-92.309
					10000	84.464	83.537	-92.606
					20000	84.175	82.726	-90.362
				600000	5000	84.179	83.534	-92.739
					10000	84.268	83.089	-90.717
					20000	83.456	81.890	-88.763
				800000	5000	84.202	83.586	-92.939
					10000	84.360	83.379	-91.988
					20000	83.207	81.621	-88.228
				1000000	5000	84.351	83.738	-93.245
					10000	84.226	83.041	-90.841
					20000	82.853	81.059	-87.264
AD8655	4V to -1V	ADR441	None	200000	5000	82.956	79.158	-81.510
					10000	83.248	75.055	-75.778
					20000	83.318	73.732	-74.256
				400000	5000	82.966	79.188	-81.610
					10000	83.275	75.092	-75.822
					20000	83.373	73.763	-74.352
				600000	5000	83.033	79.241	-81.605
					10000	83.274	75.131	-75.871
					20000	83.399	73.794	-74.355
				800000	5000	82.998	79.238	-81.611
					10000	83.322	75.176	-75.977
					20000	83.480	73.818	-74.361
				1000000	5000	83.042	79.305	-81.694
					10000	83.318	75.234	-75.975
					20000	83.452	73.930	-74.516

POWER CONSUMPTION OF LOW POWER BOARDS

Driver	Reference	Buffer	f_S	Rail Current [mA]					Total Power [mW]
				-1.0V	3.0V	3.5V	4.0V	2.5V	
ADA4841	ADR291	None	1000000			3.72		1.35	16.41

			800000			3.68	1.09	15.62
			600000			3.64	0.83	14.80
			400000			3.59	0.56	13.97
			200000			3.55	0.28	13.13
			0			3.50	0.00	12.26
AD8655	ADR291	None	1000000		5.76		1.36	20.68
			800000		5.72		1.10	19.91
			600000		5.68		0.84	19.12
			400000		5.63		0.57	18.32
			200000		5.59		0.29	17.49
			0		5.54		0.00	16.63
AD8655	ADR441	None	1000000		8.42		1.36	28.65
			800000		8.38		1.10	27.88
			600000		8.34		0.84	27.10
			400000		8.30		0.57	26.30
			200000		8.26		0.29	25.49
			0		8.21		0.00	24.63
AD8655	ADR441	None	1000000	3.52		8.61	1.35	41.35
			800000	3.52		8.57	1.10	40.55
			600000	3.52		8.53	0.84	39.73
			400000	3.52		8.49	0.57	38.89
			200000	3.52		8.45	0.29	38.03
			0	3.52		8.40	0.00	37.12
AD8655	ADR441	AD8032	1000000	3.51		10.21	1.35	47.74
			800000	3.51		10.18	1.10	46.99
			600000	3.51		10.16	0.84	46.22
			400000	3.51		10.13	0.57	45.44
			200000	3.51		10.10	0.29	44.64
			0	3.51		10.07	0.00	43.79
AD8655	ADR441	AD8032	1000000		10.21		1.36	34.04
			800000		10.18		1.10	33.31
			600000		10.16		0.84	32.57
			400000		10.13		0.57	31.81
			200000		10.11		0.29	31.03
			0		10.07		0.00	30.22
ADA4841	ADR441	AD8032	1000000			8.00	1.35	31.38
			800000			7.97	1.09	30.63
			600000			7.94	0.83	29.88
			400000			7.92	0.56	29.11
			200000			7.89	0.28	28.32
			0			7.83	0.00	27.42
ADA4841	ADR441	None	1000000			6.38	1.35	25.72

			800000	6.34	1.09	24.94
			600000	6.31	0.83	24.16
			400000	6.27	0.56	23.35
			200000	6.24	0.28	22.53
			0	6.20	0.00	21.70
ADA4841	ADR291	AD8032	1000000	5.01	1.35	20.92
			800000	4.98	1.10	20.17
			600000	4.95	0.83	19.41
			400000	4.92	0.56	18.63
			200000	4.90	0.29	17.85
			0	4.87	0.00	17.03
AD8655	ADR291	AD8032	1000000	7.25	1.36	25.17
			800000	7.22	1.10	24.43
			600000	7.19	0.84	23.68
			400000	7.17	0.57	22.92
			200000	7.14	0.29	22.14
			0	7.20	0.00	21.61

PERFORMANCE OF SPORT AND SPI ACROSS F_S AND F_{IN}

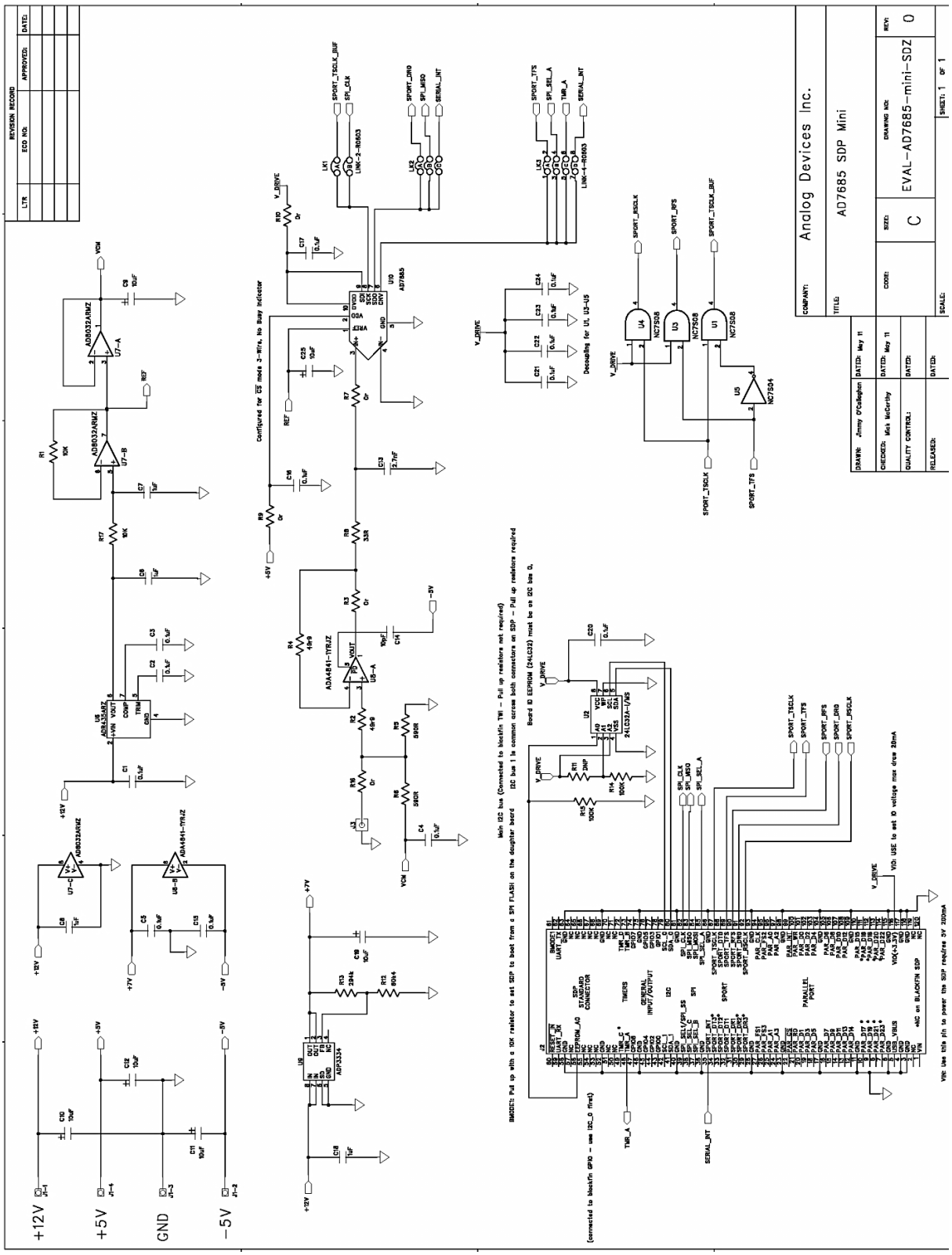
		SPORT			SPI		
f_S [kSps]	f_{IN} [kHz]	SNR [dB]	SINAD [dB]	THD [dB]	SNR [dB]	SINAD [dB]	THD [dB]
857.1	6	89.681	89.441	-101.971	67.713	67.706	-91.275
857.1	8	89.800	89.606	-102.986	67.684	67.683	-92.546
857.1	10	90.351	90.128	-102.990	67.603	67.591	-90.231
857.1	12	90.231	89.984	-102.393	67.602	67.592	-90.607
857.1	14	90.290	90.026	-102.231	67.666	67.655	-90.135
857.1	16	90.309	90.023	-101.827	67.590	67.588	-92.038
857.1	18	90.320	90.000	-101.404	67.589	67.581	-91.066
857.1	20	90.251	89.919	-101.133	67.561	67.557	-92.240
857.1	22	89.524	89.243	-101.153	67.556	67.548	-90.957
857.1	24	89.551	89.265	-101.150	67.574	67.574	-92.431
857.1	26	89.619	89.309	-100.839	67.546	67.530	-89.515
857.1	28	89.493	89.190	-100.818	67.551	67.536	-89.811
857.1	30	89.313	89.023	-100.813	67.549	67.545	-91.595
857.1	32	89.589	89.254	-100.467	67.565	67.526	-87.941
857.1	34	89.307	88.993	-100.486	67.508	67.504	-91.369
857.1	36	89.240	88.927	-100.375	67.500	67.494	-91.208

857.1	38	88.892	88.591	-100.234	67.513	67.511	-92.064
857.1	40	89.360	89.024	-100.210	67.484	67.480	-91.457
857.1	45	89.164	88.801	-99.678	67.466	67.460	-91.153
857.1	50	88.762	88.425	-99.606	67.489	67.486	-91.893
857.1	55	88.628	88.289	-99.461	67.471	67.466	-91.134
857.1	60	88.670	88.279	-98.895	67.435	67.428	-90.828
857.1	70	88.223	87.838	-98.508	67.466	67.443	-88.775
857.1	80	87.979	87.547	-97.812	67.452	67.451	-92.336
857.1	90	87.649	87.213	-97.378	67.452	67.446	-91.143
857.1	100	87.225	86.801	-97.066	67.421	67.405	-89.983
500.0	6	89.669	89.442	-102.203	89.651	89.042	-97.834
500.0	8	89.767	89.567	-102.844	89.812	89.457	-100.434
500.0	10	90.270	90.047	-102.886	90.316	90.055	-102.244
500.0	12	90.218	89.965	-102.276	90.253	90.056	-103.420
500.0	14	90.228	89.950	-101.872	90.259	90.088	-104.053
500.0	16	90.189	89.893	-101.590	90.218	90.051	-104.043
500.0	18	90.198	89.897	-101.501	90.199	90.035	-104.115
500.0	20	90.194	89.875	-101.263	90.026	89.855	-103.817
500.0	22	89.197	88.959	-101.527	89.077	88.926	-103.413
500.0	24	89.190	88.937	-101.257	89.122	88.972	-103.398
500.0	26	89.397	89.104	-100.841	89.198	89.041	-103.378
500.0	28	89.149	88.865	-100.745	89.129	88.975	-103.370
500.0	30	88.750	88.493	-100.802	88.870	88.706	-102.822
500.0	32	89.280	88.969	-100.474	89.263	89.083	-102.822
500.0	34	88.928	88.643	-100.550	88.835	88.669	-102.745
500.0	36	88.879	88.592	-100.440	88.767	88.584	-102.236
500.0	38	88.695	88.418	-100.404	88.498	88.326	-102.235
500.0	40	88.775	88.483	-100.257	88.859	88.664	-102.062
500.0	45	88.578	88.264	-99.744	88.684	88.504	-102.248
500.0	50	88.087	87.792	-99.593	88.234	88.044	-101.579
500.0	55	88.127	87.804	-99.210	88.044	87.845	-101.199
500.0	60	88.087	87.756	-99.078	87.952	87.753	-101.161
500.0	70	87.594	87.268	-98.633	87.297	87.106	-100.710
500.0	80	87.399	87.022	-97.862	87.349	87.142	-100.326
500.0	90	86.882	86.522	-97.540	86.886	86.688	-100.083
500.0	100	86.771	86.023	-94.881	86.413	86.173	-99.049
250.0	6	89.643	89.126	-98.588	89.661	89.282	-99.964
250.0	8	89.743	89.391	-100.388	89.780	89.572	-102.705
250.0	10	89.405	89.069	-100.718	90.170	90.003	-104.003
250.0	12	90.094	89.777	-101.225	90.189	90.036	-104.402
250.0	14	90.014	89.723	-101.525	90.159	90.024	-104.866
250.0	16	90.033	89.733	-101.348	90.124	89.968	-104.252

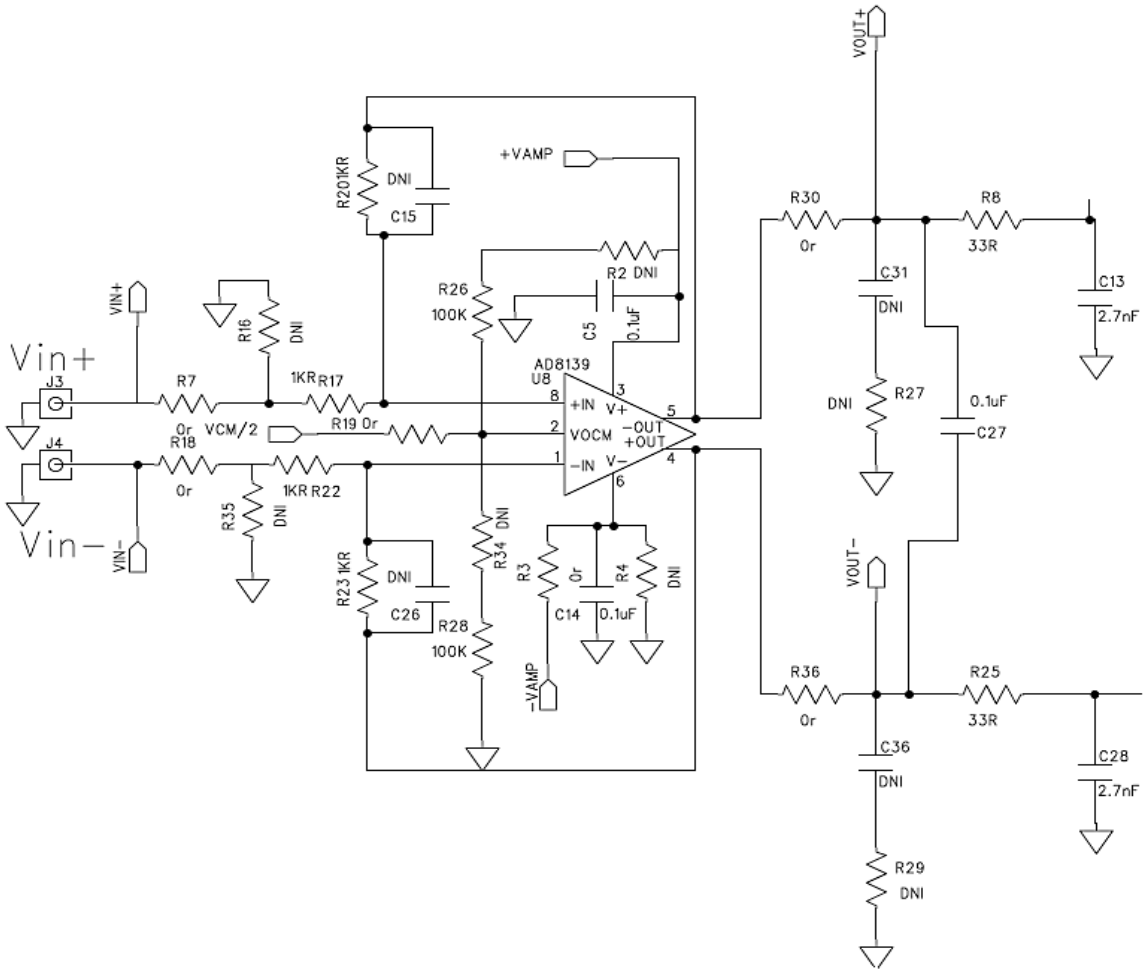
250.0	18	89.921	89.610	-101.100	90.087	89.943	-104.594
250.0	20	89.963	89.669	-101.385	89.999	89.852	-104.414
250.0	22	88.512	88.283	-101.049	88.529	88.421	-104.180
250.0	24	88.178	87.960	-100.994	88.350	88.233	-103.707
250.0	26	88.557	88.328	-101.105	88.388	88.268	-103.693
250.0	28	88.323	88.096	-100.890	88.056	87.932	-103.237
250.0	30	87.976	87.747	-100.527	88.026	87.894	-102.987
250.0	32	88.396	88.160	-100.820	88.700	88.561	-103.340
250.0	34	87.950	87.715	-100.400	88.079	87.938	-102.661
250.0	36	87.843	87.606	-100.303	87.842	87.698	-102.419
250.0	38	87.218	87.010	-100.226	87.411	87.283	-102.501
250.0	40	87.915	87.671	-100.262	87.954	87.804	-102.340
250.0	45	87.589	87.359	-100.154	87.837	87.691	-102.354
250.0	50	88.133	86.673	-93.015	86.926	86.612	-99.096
250.0	55	86.478	86.273	-99.642	86.902	86.751	-101.296
250.0	60	86.665	86.447	-99.490	86.859	86.709	-101.344
250.0	70	86.078	85.875	-99.289	86.143	85.995	-100.663
250.0	80	85.858	85.658	-99.148	85.665	85.528	-100.518
250.0	90	85.456	85.263	-98.871	85.062	84.933	-100.134
250.0	100	86.178	84.463	-90.320	84.985	84.776	-98.694

Appendix B: Schematics

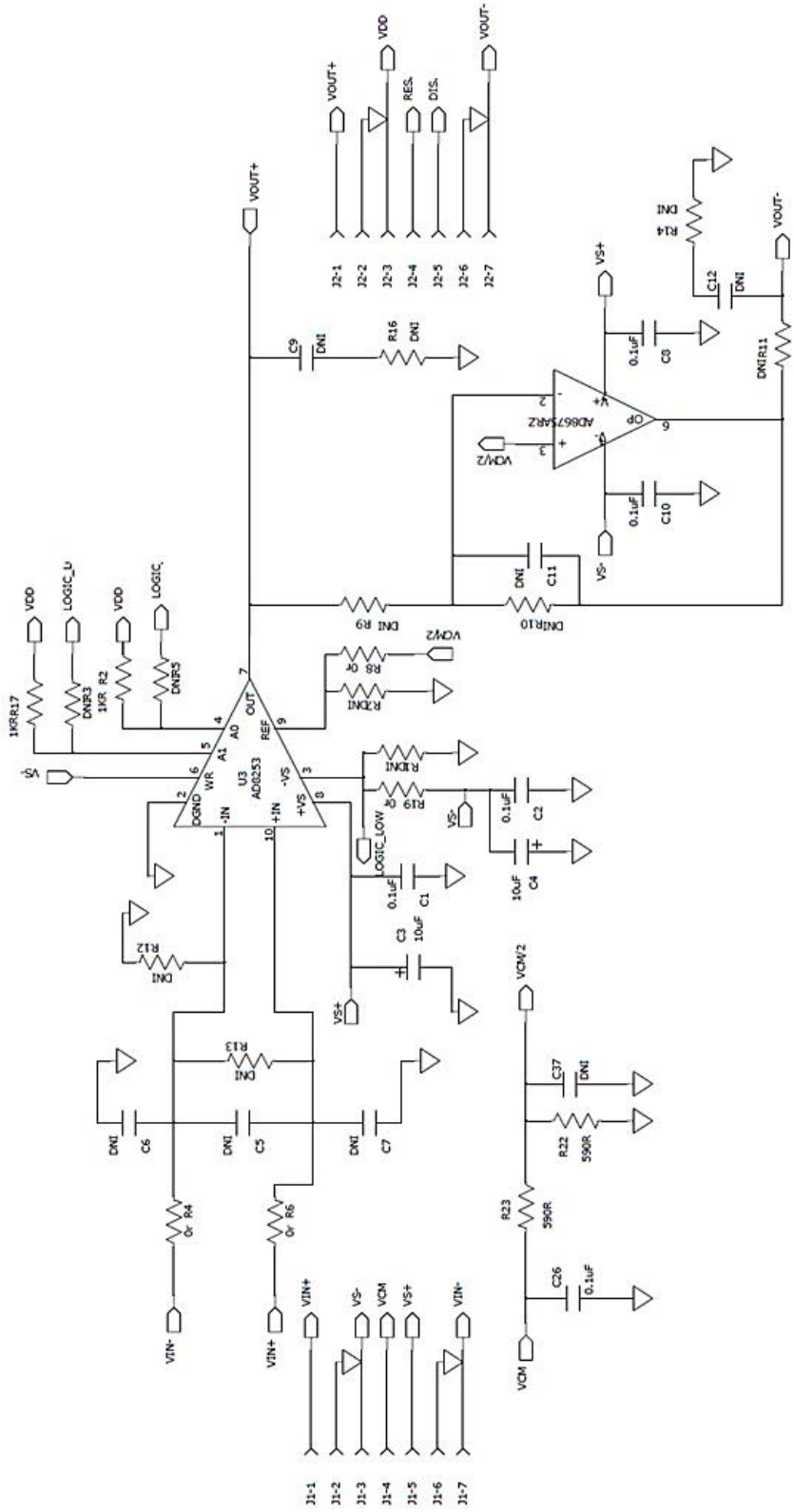
ORIGINAL DAUGHTER CARD SCHEMATIC



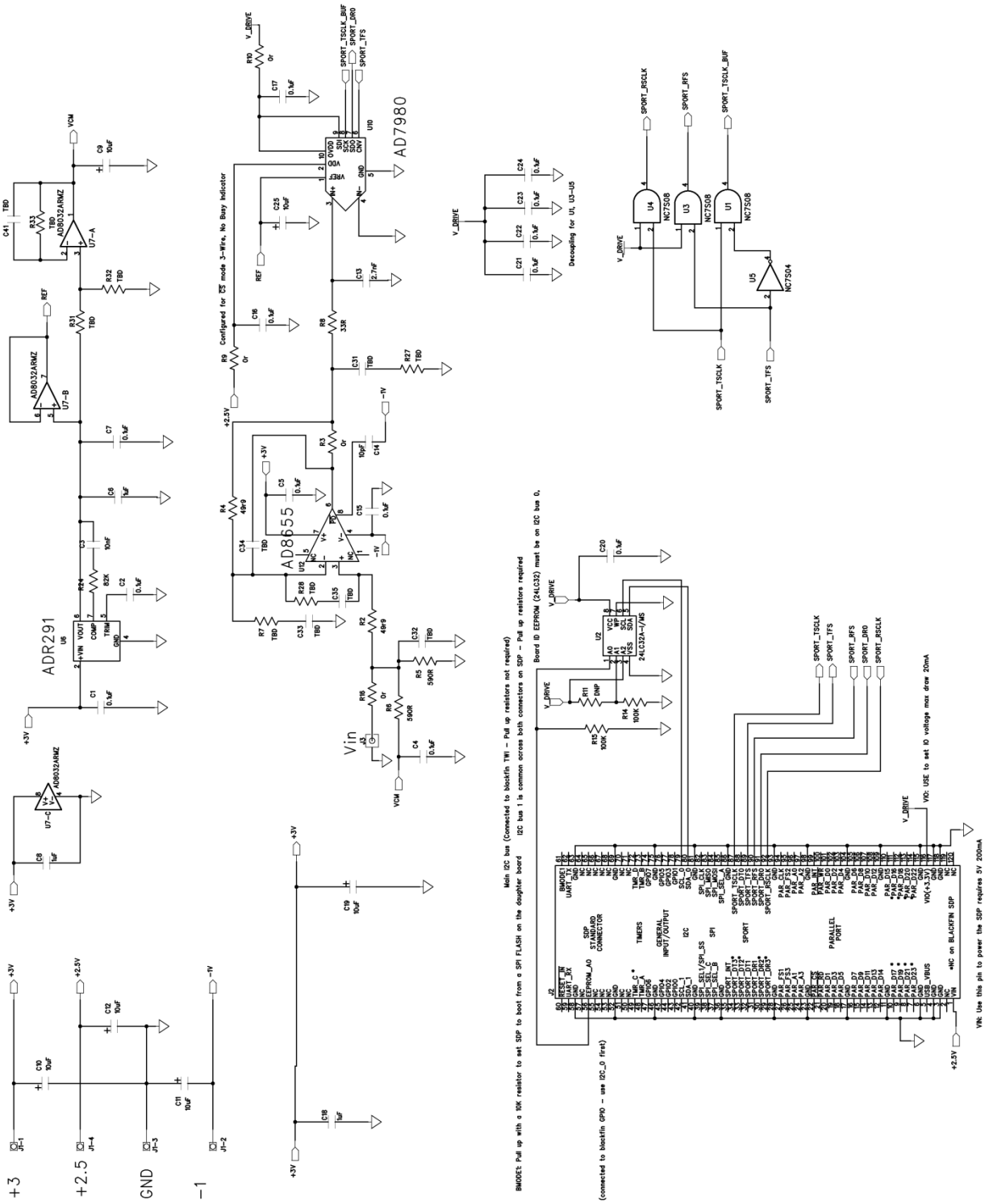
DIFFERENTIAL AMPLIFIER SCHEMATIC



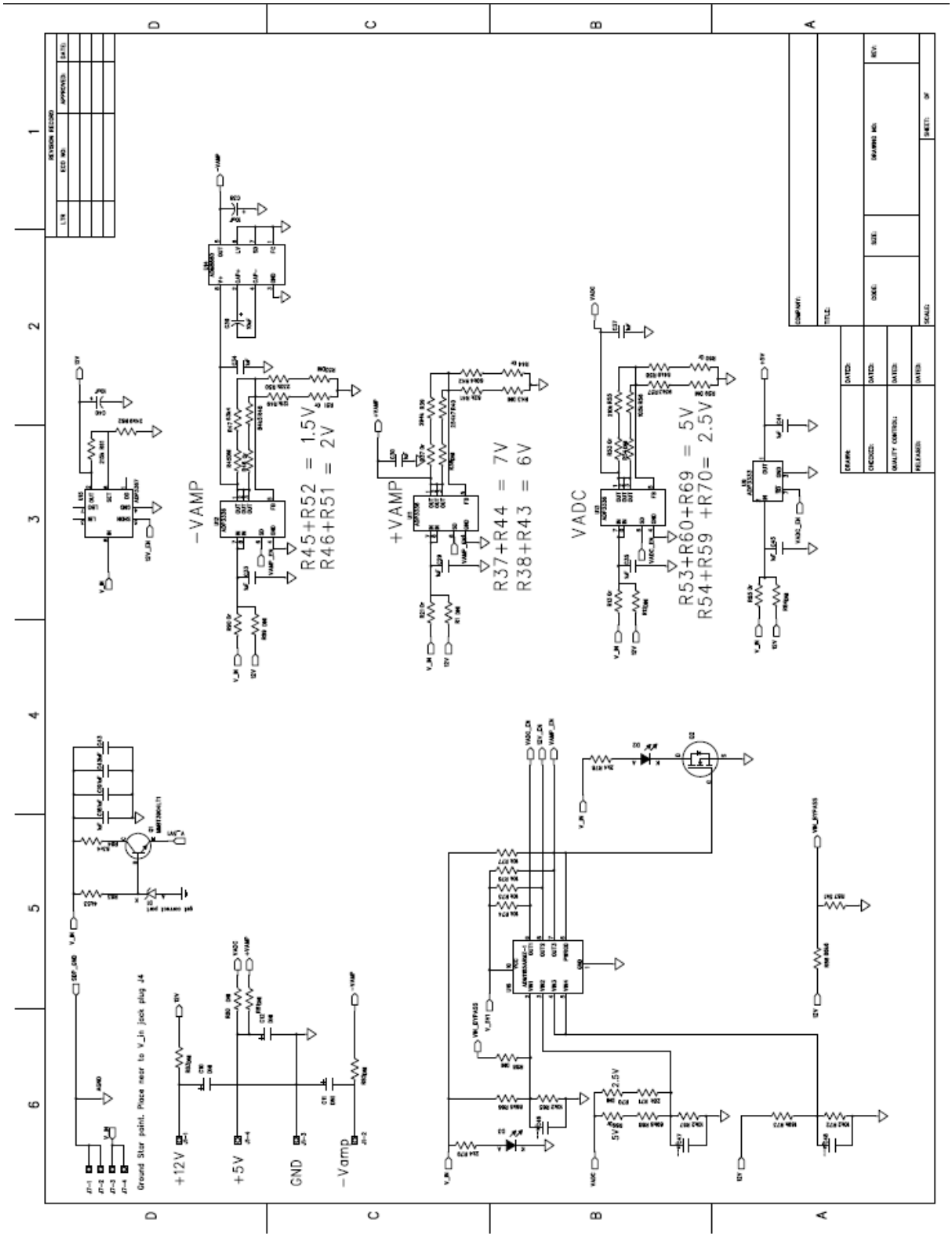
INSTRUMENTATION AMPLIFIER SURFBOARD SCHEMATIC



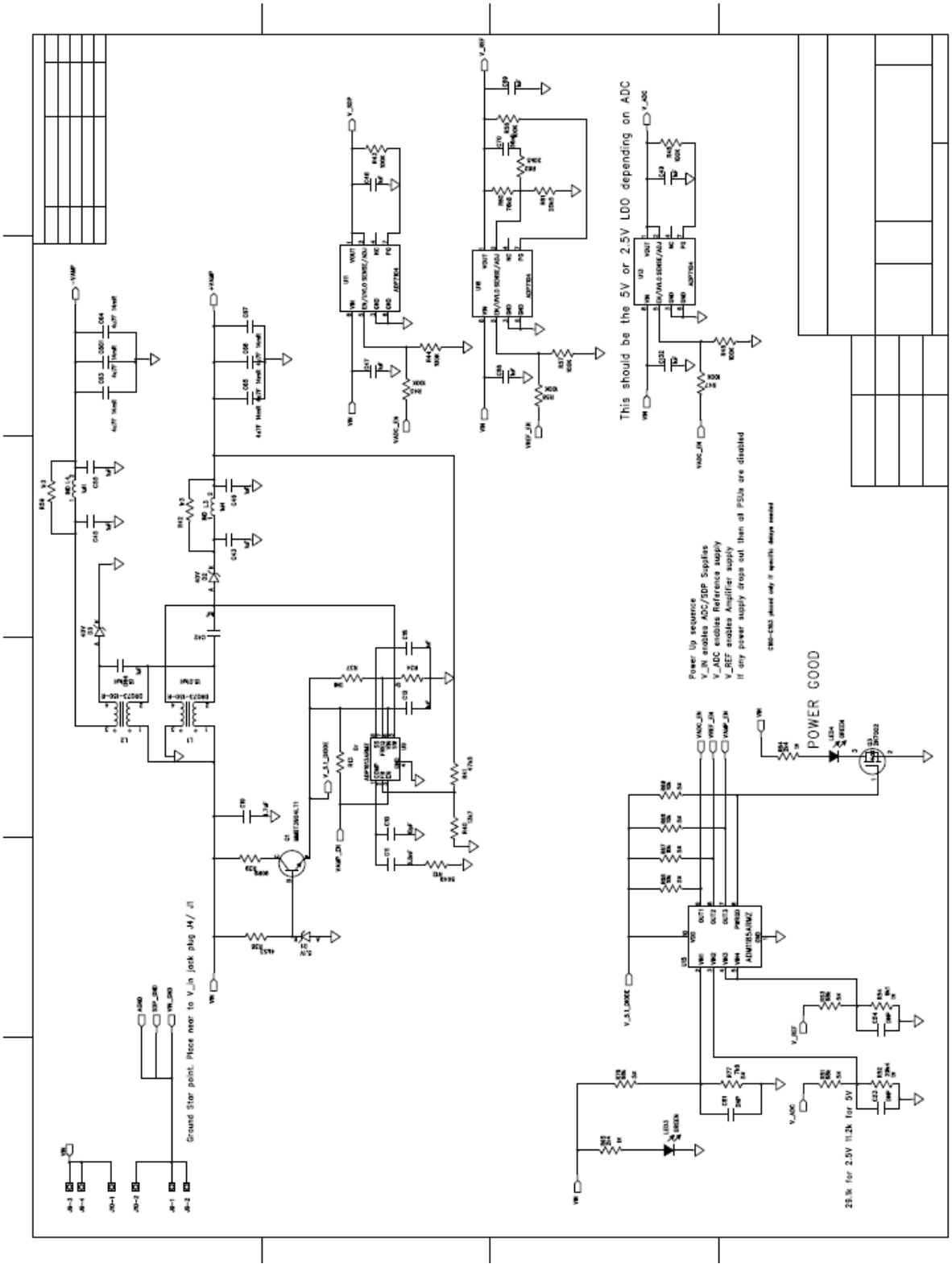
LOW POWER AD7980 SCHEMATIC



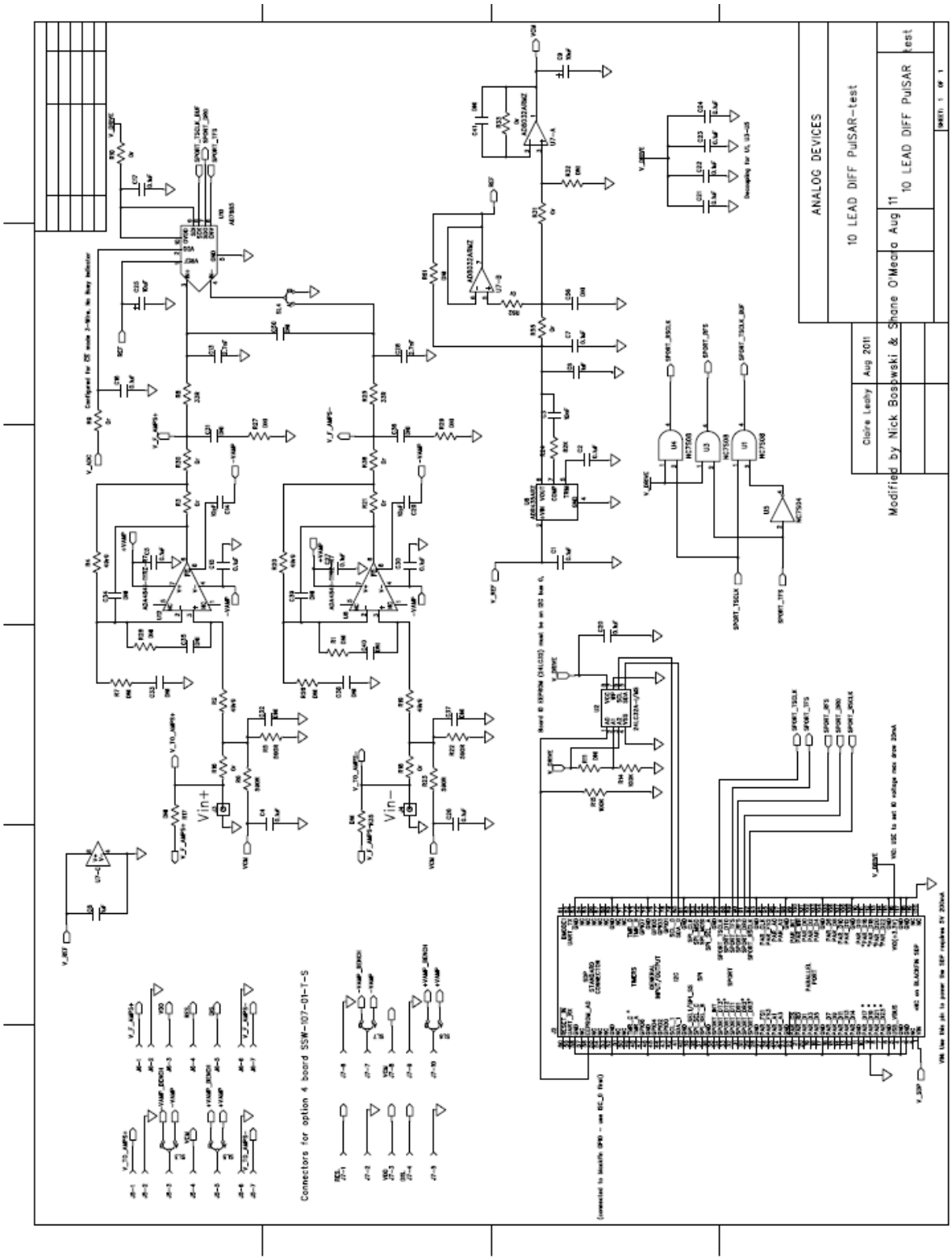
POWER SUPPLY REVISION ONE

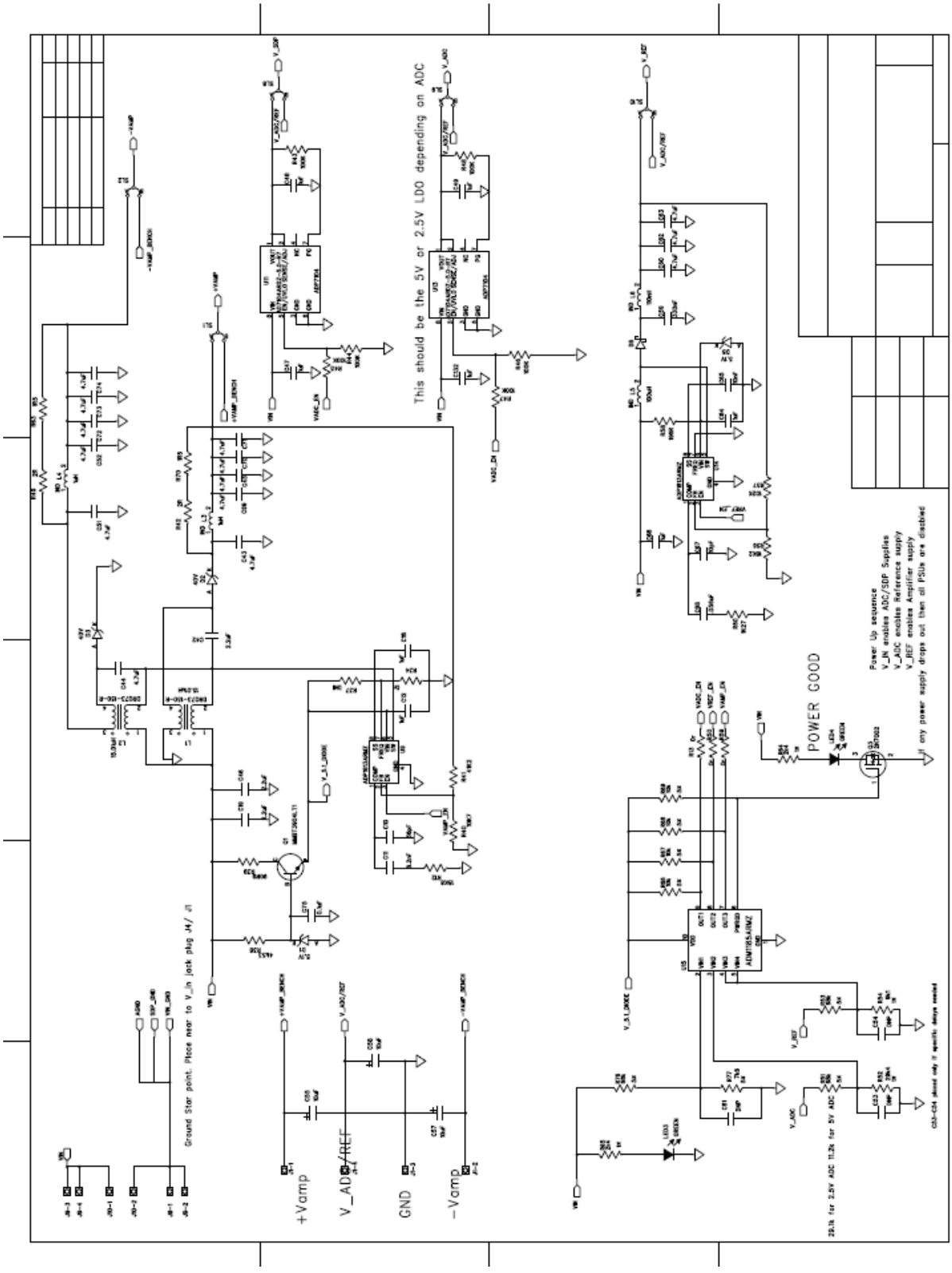


POWER SUPPLY REVISION TWO



POWER SUPPLY FINAL REVISION




This should be the 5V or 2.5V LDO depending on ADC
POWER GOOD
Power Up sequence
V_IN enables ADC/SDP Supplies
V_ADC enables Reference supply
V_REF enables Amplifier supply
If any power supply drops out then all PSUs are disabled
Ground Star point. Place near to V_in jack plug J4/ J1
+Vamp
V_ADC/REF
GND
-Vamp

Appendix C: MATLAB Code

SARCONVERGENCE.M (FIGURE 10)

```
N = 4;
v_code  = (bin2dec('0101')/(2^N-1)).*ones(1,100*N);
tvec = linspace(0,1,N*100);
sar = ones(1,800);
lastguess = 0;
for i=1:N
    v_bit = lastguess + 1/(2^i);
    if i==1
        sar = [v_bit.*ones(1,100), sar(101:100*N)];
    else
        if i==N
            sar = [sar(1:100*(N-1)), v_bit.*ones(1,100)];
        else
            sar = [sar(1:(100*(i-1))), v_bit.*ones(1,100),
                   sar(100*i+1:100*N)];
        end
    end
    if v_bit < v_code
       lastguess = v_bit;
    end
end
plot(tvec, sar, tvec, v_code);
axis([0 1 0 1]);
xlabel('Fraction of Total Acquisition Time, t_{ACQ}');
ylabel('Fraction of Full Scale Range, V_{FSR}');
```

ANALOGINPUTS.M (FIGURE 12)

```
N = 4;
numPts = 100*2^N;
idealIn = linspace(0,1,numPts);
idealOut = linspace(0, 2^N, numPts);
widths = (1/2^N).*ones(1,2^N);
widths = widths + 0.05*randn(size(widths));
```

```
widths = (1/sum(widths)).*widths;
realOut = (2^N-1).*ones(1,numPts);
begin = 1;
for i=1:2^N
    stop = floor(widths(i)*100*2^N)+begin-1;
    for j=begin:stop
       realOut(j) = i-1;
    end
    begin = stop+1;
end
figure(1);
plot(idealIn,realOut, 'k', 'LineWidth', 2);
axis([0 1 0 16]);
xlabel('Input Voltage as Fraction of FSR');
ylabel('Output Code');
```

GENERATEFFT.M (FIGURE 15 AND FIGURE 17)

```
Fs    = 1e6;
Fin   = 50e3;
tvec  = 0:1/Fs:307/Fin-1/Fs;

% Signal and its harmonics. Amplitudes are merely relative.
xfund = 1.00*sin(2*pi*Fin*tvec);
x2nd  = 0.0003*sin(2*pi*Fin*2*tvec);
x3rd  = 0.0008*sin(2*pi*Fin*3*tvec);
x4th  = 0.00015*sin(2*pi*Fin*4*tvec);
x5th  = 0.00025*sin(2*pi*Fin*5*tvec);

% Each decimal place zero moves noise floor down 20dB
noise = 0.001*randn(size(tvec));
x     = xfund+x2nd+x3rd+x4th+x5th+noise;
X     = abs(fft(x));
Xnorm = X ./ max(X);
dBFs  = 25; % Signal dB below full scale.
XdB   = 20*log10(Xnorm)-dBFs;
fvec  = Fs*(0:length(X)/2)/(length(X)*1000);

figure(1);
plot(Fs*tvec(1:50),x(1:50),Fs*tvec(1:50),xfund(1:50));
title('Signal with Heavy Noise and Harmonics');
xlabel('Time (usec)');
ylabel('Signal Amplitude (V)');

figure(2);
plot(fvec,XdB(1:length(XdB)/2+1),'k');
xlabel('Frequency [kHz]');
ylabel('Spectral Amplitude [dB]');
axis([0 max(fvec) -160 0]);
```

DNLTRANSFER.M (FIGURE 18)

```
N = 4;
numPts = 100*2^N;
idealIn = linspace(0,1,numPts);
widths = (1/2^N).*ones(1,2^N);
widths = widths + 0.05*randn(size(widths));
widths = (1/sum(widths)).*widths;
realOut = (2^N-1).*ones(1,numPts);
begin = 1;
for i=1:2^N
    stop = floor(widths(i)*100*2^N)+begin-1;
    for j=begin:stop
       realOut(j) = i-1;
    end
    begin = stop+1;
end
figure(1);
plot(idealIn,realOut, 'k', 'LineWidth', 2);
axis([0 1 0 16]);
xlabel('Input Voltage as Fraction of FSR');
ylabel('Output Code');
```

SINEPDFANDCODEDIST.M (FIGURE 19)

```
A = 1;
N = 3;
V = linspace(-A,A,100*2^N);
P = 1./(pi*sqrt(A^2 - V.^2)); % Probability function
codeP = 100.*ones(1, 100*2^N);
for i=1:2^N-2
    begin = 1+i*100;
    stop  = (i+1)*100;
    for j=begin:stop
        codeP(j) = sum(P(begin:stop));
    end
end
codeP = codeP./100;
figure(1);
plot(V, P, '-k', V, codeP, '-r', 'LineWidth', 2);
axis([-A +A 0 1.1]);
xlabel('Input Voltage from -A to +A');
ylabel('Probability of Occurrence');
```

NOISYSINEPDF.M (FIGURE 20)

```
A = 1;
N = 8;
V = linspace(-A,A,100*2^N);
P = 1./(pi*sqrt(A^2 - V.^2)); % Probability function
Pn = P + .3*randn(size(P));
codeP = 100.*ones(1, 100*2^N);
for i=1:2^N-2
    begin = 1+i*100;
    stop  = (i+1)*100;
    for j=begin:stop
        codeP(j) = sum(Pn(begin:stop));
    end
end
codeP = codeP./100;
figure(1);
plot(0:0.01:2^N-0.01, codeP, '-k', 'LineWidth', 2);
axis([0 2^N 0 1.1]);
xlabel('Output Code');
ylabel('Probability of Occurrence');
```

APERTURE.M (FIGURE 33)

```
fsin = 2e6;
fsq  = 5e6;
t    = linspace(0,1/fsin,10000);
vsin = 0.5 .* sin(2*pi*fsin*t)+0.6;
vsq  = 0.5 .* square(2*pi*fsq*t)-0.6;
plot(t, vsin, '-k', t, vsq, '-b');
axis([0 1/fsin -1.3 1.3]);
legend('Input Signal', 'Clock Signal')
set(gca, 'XTickLabelMode', 'Manual');
set(gca, 'XTick', []);
set(gca, 'YTickLabelMode', 'Manual');
set(gca, 'YTick', []);
```

JITTERLIMITEDSNR.M (FIGURE 34)

```
tj = [0.1e-12, 1e-12, 10e-12, 100e-12, 1e-9, 10e-9];
f = logspace(3, 6, 10000);
figure(1);
for i=1:6
   snrline = 20*log10(1./(2*pi*f*tj(i)));
```

```
    semilogx(f,snrline, '-k');
    hold on;
end
xlabel('Input Frequency [Hz]');
ylabel('Maximum SNR [dB]');
```

EQUIVALENTDRIVERLOAD.M (FIGURE 62, FIGURE 63, AND FIGURE 64)

```
R_ADC = 400;
C_ADC = 30E-12;
R_IN = [12, 22, 33, 50];
C_IN = 2.7E-9;
f = logspace(3,5,10000);
w = 2*pi*f;
color = 'rgbk';
for i=1:4
    T_ADC = R_ADC.*C_ADC;
    RS = R_IN;
    RP = (1 + (w.^2).*(T_ADC^2)) ./ ((w.^2).*T_ADC.*C_ADC);
    CP = ((w.^2).*(T_ADC^2).*C_IN + C_IN + C_ADC) ./ (1 + (w.^2).*(T_ADC^2));
    RL = (RS(i)^2 + 2.*RS(i).*RP + RP.^2 +
         (w.^2).*(RS(i).^2).*(RP.^2).*(CP.^2)) ./ (RS(i) + RP +
         (w.^2).*(CP.^2).*(RP.^2).*RS(i));
    CL = ((RP.^2).*CP) ./ (RS(i)^2 + 2.*RS(i).*RP + RP.^2 +
         (w.^2).*(RS(i)^2).*(RP.^2).*(CP.^2));
    figure(1);
    loglog(f, RL, color(i), 'Linewidth', 2);
    xlabel('Frequency [Hz]');
    ylabel('Equivalent Load Resistance [\Omega]');
    hold all;
    figure(2);
    semilogx(f, CL, color(i), 'Linewidth', 2);
    axis([1e3 1e5 2.72e-9 2.7305e-9]);
    xlabel('Frequency [Hz]');
    ylabel('Equivalent Load Capacitance [F]');
    grid on;
    hold on;
end
figure(1);
legend('12\Omega', '22\Omega', '33\Omega', '50\Omega', 'Location',
   'SouthWest');
figure(2);
legend('12\Omega', '22\Omega', '33\Omega', '50\Omega', 'Location',
   'SouthWest');
```

SPORTVSSPINORMALITY.M (FIGURE 95 AND FIGURE 96)

```
snrall = [0.0180, -0.0442, -0.0463, -0.0347, -0.0303, -0.0296, -0.0007,
      0.1680, 0.1196, 0.0677, 0.1999, 0.0209, -0.1201, 0.0174, 0.0930,
      0.1119, 0.1967, -0.0838, -0.1063, -0.1472, 0.0823, 0.1350, 0.2973,
      0.0493, -0.0045, 0.3577, -0.0176, -0.0367, -0.7647, -0.0956, -0.1459, -
      0.0907, -0.1660, -0.0357, -0.0176, -0.1716, 0.1684, 0.2664, -0.0493, -
      0.3035, -0.1290, 0.0008, -0.1934, -0.0392, -0.2486, 1.2063, -0.4243, -
      0.1933, -0.0657, 0.1931, 0.3933, 1.1927];
sinadall = [0.4001, 0.1103, -0.0082, -0.0912, -0.1381, -0.1585, -0.1374,
      0.0201, 0.0325, -0.0352, 0.0631, -0.1100, -0.2126, -0.1149, -0.0259,
      0.0072, 0.0924, -0.1808, -0.2408, -0.2523, -0.0408, 0.0026, 0.1622, -
      0.1206, -0.1662, -0.1493, -0.1561, -0.1806, -0.9336, -0.2590, -0.3011,
      -0.2350, -0.3331, -0.1839, -0.1383, -0.2728, 0.0598, 0.1637, -0.1469, -
      0.4010, -0.2223, -0.0921, -0.2729, -0.1335, -0.3315, 0.0613, -0.4779, -
      0.2616, -0.1192, 0.1302, 0.3305, -0.3130];
thdall = [-4.3689, -2.4101, -0.6422, 1.1436, 2.1812, 2.4533, 2.6138, 2.5541,
      1.8861, 2.1415, 2.5363, 2.6246, 2.0201, 2.3476, 2.1951, 1.7959, 1.8309,
      1.8047, 2.5043, 1.9851, 1.9889, 2.0823, 2.0779, 2.4641, 2.5432, 4.1679,
      1.3762, 2.3168, 3.2851, 3.1770, 3.3410, 2.9043, 3.4947, 3.0292,
      3.1303, 2.7126, 2.5887, 2.3470, 2.4599, 2.5196, 2.2607, 2.1152, 2.2757,
      2.0783, 2.2000, 6.0813, 1.6544, 1.8547, 1.3740, 1.3702, 1.2627,
      8.3731];
[hsnrall,ksnrall] = testnormality(snrall,  0.05,'SNR 250kSps and 500kSps');
[hsndall,ksndall] = testnormality(sinadall,0.05,'SINAD 250kSps and 500kSps');
[hthdall,kthdall] = testnormality(thdall,  0.05,'THD 250kSps and 500kSps');
```

TESTNORMALITY.M (FIGURE 95 AND FIGURE 96)

```
function [h, p, k, c] = testnormality(datain, significance,titletext)

scaled = (datain./std(datain))-mean(datain./std(datain));
[h,p,k,c] = kstest(scaled,[],significance,0);
std_norm = -3:0.1:3;
figure;
Emp = cdfplot(scaled);
hold on;
Std = plot(std_norm, normcdf(std_norm), 'r-');
set(Emp,'LineWidth',2);
set(Std,'LineWidth',2);
legend([Emp Std],'Empirical','Standard Normal','Location','NW');
title(titletext);
xlabel('Normalized Standard Deviations');
ylabel('Cumulative Probability');
```

BOOST.M(FIGURE 26 AND FIGURE 27)

```
function [] = Boost()
cycles =1.5;
F_PWM = 1e6;
duty_cycle = .2;
t = 0:1/(100*F_PWM):(cycles/F_PWM)-1/(100*F_PWM);
L = 15e-6;
current = zeros(1,length(t));
VPWM = .5*sin(2*pi*F_PWM*t)+.5;
V_Out(1:length(t)) = 1/(1-duty_cycle);
%figure(2), plot(t,V_Out);
for i =1:length(VPWM)
    if(mod(i,100)<duty_cycle*100)
        VPWM(i) = 1;
    else
        VPWM(i) = 0;
    end
end
figure(1),subplot(4,1,1), plot(t*1e6,VPWM), axis([ 0 max(t)*1e6 -.1 1.1])
%title('V_P_W_M as a Function of Time')
%xlabel('Time (\mus)')
ylabel('V_P_W_M(V)');
V_Ind = VPWM/(L*F_PWM);
for i =1:length(t)
    if(VPWM(i) == 0)
        V_Ind(i) = (-1*V_Out(i)+1)/(L*F_PWM);
    end
current(i) = sum(V_Ind(1:i));
end
figure(1),subplot(4,1,3),plot(t*1e6,current), axis([ 0 max(t)*1e6 -.25
max(current)+.25]);
%title('I_{IND} as a Function of Time')
%xlabel('Time (\mus)')
ylabel('I_{IND} (A)');
figure(1),subplot(4,1,2),plot(t*1e6,V_Ind*(L*F_PWM)),axis([ 0 max(t)*1e6
min(V_Ind)*(L*F_PWM)-.1 1.1]);
%title('V_I_N_D as a Function of Time')
%xlabel('Time (\mus)')
ylabel('V_I_N_D(V)');
figure(1),subplot(4,1,4),plot(t*1e6,V_Out),axis([ 0 max(t)*1e6 0
(V_Out(1)+.5)]);
%title('V_O_U_T as a Function of Time')
xlabel('Time (\mus)')
ylabel('V_O_U_T(V)');

d_vs_v = 0:.01:1;
V_Duty = zeros(1,length(d_vs_v));
V_Duty = 1./(1-d_vs_v);
figure(2), plot(d_vs_v,V_Duty);
title('Output Voltage Vs. Duty Cycle (1V Input)')
xlabel('Duty Cycle')
ylabel('V_O_U_T(V)');
end
```

ADC_ANALYSIS.M(USED TO COMPARE LABVIEW RESULTS)

```
function  [] = adc_analysis(x,fs)
L = length(x)          %length of input data
T = 1/fs;               %Sampling Period
t = 0:T:T*L-T;          %Time Vector
x = (10* x/(2^18))-5;   %Scale data
figure(1),plot(t,x)     %plot waveform
title('Input Waveform')
xlabel('Time')
ylabel('Amplitude')

w = blackman_harris_7(L);   %create 7 term blackman-harris window
x = x.*w;                   %Apply window
figure(4), plot(x);
%Plot resulting waveform
NFFT = 2^nextpow2(L);       %FFT formatting
y =fft(x,NFFT)/L;           %take FFT
y= 20 * log10(2*abs(y(1:NFFT/2+1)/5));  %logarithmic values
f = fs/2*linspace(0,1,NFFT/2+1);        %create frequency vector
figure(2), plot(f,y) ;                  %plot FFT
title('Single-Sided Amplitude Spectrum of y(t)')
xlabel('Frequency (Hz)')
ylabel('|Y(f)|');
b = 6;
m = find(y==max(y(6:1:length(y))));     %Find maximum location
y_n = 10.^(y/20);       %Normalize data
sig_rms = sum(y_n(m-b:1:m+b).^2)^.5; % Compute Signal RMS
noise = vertcat(y_n(6:1:m-(b+1)),y_n(m+(b+1):1:length(y_n))); % remove DC and
Signal bins
avg = mean(noise) %find average of the noise floor
harmonics_rms = [0 0 0 0 0 0]; % Initialize Harmonics vector

for i = 2:7
    harmonics_rms(i-1) = sum(y_n(i*(m-1)-2:1:i*m+3).^2)^.5; % remove
harmonics
    noise((i*m-22):1:(i*m-11)) = avg;  %replace harmonic locations with
average noise
end

scale = 1;
% 2.63 7 term blackman-harris
% 1 for no window
harmonics_rms = sum(harmonics_rms.^2)^.5;   %Compute Harmonic rms
noise_rms = (sum(noise.^2)/scale)^.5;       %Compute noise rms

THD = 20*log10(harmonics_rms/sig_rms);  %Compute THD in dB
SNR = 20* log10(sig_rms/(noise_rms));   %Compute SNR in dB
SINAD = 20*log10(sig_rms/((harmonics_rms^2+noise_rms^2)^.5)); %Compute SINAD
in dB
Fund = f(m);    %Fundamental value
%Print to File
file = fopen('analysis.txt','a');
```

```
fprintf(file, '----------------------\n');
fprintf(file, 'Computed SNR is %fdB\n', SNR);
fprintf(file, 'Computed SINAD is %fdB\n', SINAD);
fprintf(file, 'Computed THD is %fdB\n', THD);
fprintf(file, 'The Fundamental is %fHz\n',Fund);
fprintf(file, '----------------------\n\n');
fclose(file);

% Plot single-sided amplitude spectrum.
figure(2), plot(f,y) ;
title('Single-Sided Amplitude Spectrum of y(t)')
xlabel('Frequency (Hz)')
ylabel('|Y(f)|');

end
```

BLACKMAN-HARRIS.M(USED IN ADC_ANALYSIS.M)

```
function [w] = blackman_harris_7 (length)
w = zeros(length,1);
% Found these coefficients online in
% SOLOMON: USE  OF D I T  WINDOWS  IN  SIGNAL-TO-NOISE RATIO AND
% HARMONIC  DISTORTION COMPUTATIONS
% at http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=00293419
a0  =  0.271051400693424;
a1  = 0.433297939234485;
a2  =  0.218122999543110;
a3  = 0.065925446388031;
a4  =  0.010811742098371;
a5  = 0.000776584825226;
a6  =  0.000013887217352;
for i = 1:length
    w(i) = a0-a1*cos(2*pi*i/(length))...
    +a2*cos(4*pi*i/(length))-a3*cos(6*pi*i/(length))...
    +a4*cos(8*pi*i/(length))-
a5*cos(10*pi*i/(length))+a6*cos(12*pi*i/(length));
end
```

DIFF_VS_SINGLE.M(FIGURE 14)

```
function[] =diff_vssingle()
fs = 1000;
ts = 1/fs;
x = 0:ts/50:3*ts;
diff_p = cos(2*fs*pi*x);
diff_n = -1*diff_p;
noise = .5*rand(1,length(x))-.1;
```

```
diff_p = noise +diff_p;
diff_n = noise +diff_n;
single = 2*cos(2*fs*pi*x)+ noise;
diff = diff_p-diff_n;
hold all
figure(1), subplot(2,2,1),plot(x,diff_p,x,diff_n)
axis([0 max(x) -1.5 1.5])
title('Differential signal outside ADC(noisy)')
xlabel('Time')
ylabel('Magnitude(V)');
subplot(2,2,2),plot(x,single);
title('Single Ended signal outside ADC(noisy)')
xlabel('Time')
ylabel('Magnitude(V)');
axis([0 max(x) -2.5 2.5])
subplot(2,2,3),plot(x,diff)
title('Differential signal inside ADC(no noise)')
xlabel('Time')
ylabel('Magnitude(V)');
axis([0 max(x) -2.5 2.5])
subplot(2,2,4),plot(x,single);
title('Single Ended signal inside ADC(noisy)')
xlabel('Time')
ylabel('Magnitude(V)');
axis([0 max(x) -2.5 2.5])
end
```

WINDOWING.M(FIGURE 120, FIGURE 121, FIGURE 122, AND FIGURE 123)

```
function [] = windowing()
fs = 200; % sampling frequency
freq = 10; % tone frequency
clean = 0:1/(fs*10):100/freq; % make a clean cut & not vector
dirty = 0:1/(fs*10):100.37/freq;

x_c = 5*sin(2*freq*pi*clean);
x_d = 5*sin(2*freq*pi*dirty);

noise = .2*rand(1,length(x_c))-.1;
x_c = x_c+noise;
noise = .2*rand(1,length(x_d))-.1;
x_d = x_d+noise;

L_c = length(x_c);
L_d = length(x_d);


NFFT_c = 2^nextpow2(L_c);       %FFT formatting
```

```
NFFT_d = 2^nextpow2(L_d);

y_c =fft(x_c,NFFT_c)/L_c;           %take FFT
y_d =fft(x_d,NFFT_d)/L_d;

y_c= 20 * log10(2*abs(y_c(1:NFFT_c/2+1)/5));  %logarithmic values
y_d= 20 * log10(2*abs(y_d(1:NFFT_d/2+1)/5));
%y_c = abs(y_c(1:NFFT_c/2+1));
%y_d = abs(y_d(1:NFFT_d/2+1));

f_c = fs/2*linspace(0,1,NFFT_c/2+1);        %create frequency vector
f_d = fs/2*linspace(0,1,NFFT_d/2+1);

figure(1), subplot(2,1,1),plot(x_c(18000:20000)),axis([0 2000 -5.2 5.2]);
%plot FFT
title('Integer Cycles Sinewave')
figure(1), subplot(2,1,2),plot(x_d(length(x_d)-2700:...
                           length(x_d))),axis([0 2700 -5.2 5.2]);
%plot FFT
title('Non-Integer Cycles Sinewave')

figure(2), subplot(2,1,1),plot(f_c,y_c), axis([0 100 -100 max(y_c)]);
%plot FFT
title('Spectrum of Integer Sinewave(No Spectral Leakage)')
xlabel('Frequency (Hz)')
ylabel('|Y(f)|');
figure(2), subplot(2,1,2),plot(f_d,y_d),axis([0 100 -100 max(y_c)]);
%plot FFT
title('Spectrum of Integer Sinewave(Spectral Leakage)')
xlabel('Frequency (Hz)')
ylabel('|Y(f)|');

%Apply Blackman-Harris
fs = 100000;
freq = 5000;
z = 0:1/(fs*50):100/freq;
x_nw = 5*sin(2*freq*pi*z);
noise = .5*rand(1,length(x_nw))-.1;
x_nw = x_nw+noise;
h = blackman_harris_7(length(x_nw));
x_w = h.*x_nw(:);

L = length(x_nw);
NFFT = 2^nextpow2(L);       %FFT formatting

y_w =fft(x_w,NFFT)/L;           %take FFT
y_nw =fft(x_nw,NFFT)/L;

%y_w = abs(y_w(1:NFFT/2+1));
%y_nw = abs(y_nw(1:NFFT/2+1));
y_w= 20 * log10(2*abs(y_w(1:NFFT/2+1)));  %logarithmic values
y_nw= 20 * log10(2*abs(y_nw(1:NFFT/2+1)));
```

```
f_w = fs/2*linspace(0,1,NFFT/2+1);        %create frequency vector
f_nw = fs/2*linspace(0,1,NFFT/2+1);

figure(3), subplot(2,1,1),plot(x_nw), axis([0 length(x_nw) -5.5 5.5]);
%plot FFT
title('Non-Windowed Sinewave')
figure(3), subplot(2,1,2),plot(x_w), axis([0 length(x_w) -5.5 5.5]);
%plot FFT
title('Windowed Sinewave')

figure(4), subplot(2,1,1),plot(f_nw,y_nw),axis([0 5000 -100 max(y_nw)]);
%plot FFT
title('Spectrum of Non-Windowed Sinewave')
xlabel('Frequency (Hz)')
ylabel('|Y(f)|');
figure(4), subplot(2,1,2),plot(f_w,y_w),axis([0 5000 -100 max(y_w)]);
%plot FFT
title('Spectrum of Windowed Sinewave')
xlabel('Frequency (Hz)')
ylabel('|Y(f)|');
end
```

Appendix D: Power Supply Analysis

Output Analysis							
Desc.	Part	Value	Unit	Accuracy	Worst Case(low)	Worst Case(High)	Unit
Voltage Monitor	ADM1185	0.6	V	0.008	0.595	0.605	V
Res. 7V comp	R76	68000	Ω	0.05	64600	71400	Ω
Res. 7V comp	R77	7600	Ω	0.05	7220	7980	Ω
Res. V_ADC Comp	R51	68000	Ω	0.05	64600	71400	Ω
Res. V_ADC Comp(5V)	R52	11200	Ω	0.01	11088	11312	Ω
Res. V_ADC Comp(2.5V)	R52	29400	Ω	0.01	29106	29694	Ω
Res V_REF Comp	R53	68000	Ω	0.05	64600	71400	Ω
Res V_REF Comp	R54	9100	Ω	0.01	9009	9191	Ω
Res V_REF LDO	R60	76800	Ω	0.01	76032	77568	Ω
Res V_REF LDO	R61	20500	Ω	0.01	20295	20705	Ω
SDP Voltage	ADP7104	5	V	0.03	4.850	5.150	V
ADC Voltage(5V)	ADP7104	5	V	0.03	4.850	5.150	V
ADC Voltage(2.5V)	ADP7104	2.5	V	0.03	2.425	2.575	V
Amplifer Voltage	ADP1613	5.5	V	0.017	5.404	5.596	V

Scenario	Value	unit	Scenario	Value	unit
Typical 7V turnon	5.968421053	V	Typical Amplifer Voltage	11.0	V
Worst Case (High)	6.58578615	V	Worst Case(High)	11.1922	V
Worst (Low)	5.413485714	V	Worst Case(Low)	10.8078	V
Typical ADC 5V turnon	4.242857143	V	Typical V_REF turnon	5.083516484	V
Worst case (High)	4.499345455	V	Worst case(High)	5.398086713	V
Worst case(Low)	3.99423819	V	Worst case(Low)	4.778631618	V
Typical ADC 2.5V turnon	1.987755102	V			

Worst case (High)	2.088436364	V	ADR445 Draw	3.5	mA
Worst case(Low)	1.890071691	V	ADM1185 Draw	0.00002	mA
			AD8032 Draw	0.95	mA
Typical SDP_Voltage	5	V	Draw on V_REF	4.45002	mA
Worst case(High)	5.15	V	Dropout	5	mV
Worst case(Low)	4.85	V			
Typical ADC(5V) voltage	5	V			
Worst case(High)	5.15	V			
Worst case(Low)	4.85	V			
Typical ADC(2.5V) voltage	2.5	V			
Worst case(High)	2.575	V			
Worst case(Low)	2.425	V			
Typical V_REF	5.790536585	V			
Worst case(High)	5.882870658	V			
Worst case(Low)	5.70003091	V			

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