DESIGN OF SINGLE PHASE BOOST POWER FACTOR CORRECTION CIRCUIT AND CONTROLLER APPLIED IN ELECTRIC VEHICLE CHARGING SYSTEM

by

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ABSTRACT

In this thesis, based on the existing researches on power factor correction technology, I analyze, design and study the Boost type power factor correction technology, which is applied in the in-board two-stage battery charger.

First I analyzed the basic working principle of the active power factor corrector. By comparing several different topologies of PFC converter main circuit and control methods, I specified the research object to be the average current control (ACM) boost power factor corrector.

Then I calculated and designed the PFC circuit and the ACM controller applied in the first level charging of EVs. And I run the design in Simulink and study the important features like power factor, the input current waveform and the output DC voltage and the THD and odd harmonic magnitude.

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Chapter 1: Introduction

1.1 Project Background

With the high modernization and electrification of industry, people now have a higher requirement for the power quality. For instance, personal computers, electronic devices, cell phones, they each has a basic requirement for power quality. Bad power quality may cause the electronic devices not working properly or even not working. For power quality, power factor is a significant factor, which impacts power quality directly. Small power factor will cause many negative effects, such as power grid waveform distortion and large line loss, which may reduce the service time of power devices.

As electricity gets more and more important in people's life, there are increasing number of power devices with different features. The power we get from national grid is 110V and 60 Hz. But most of the power devices require a different input from what we get from national grid, so we have to make some conversion of the voltage and current. There are 4 kinds of conversion circuits as below: AC-DC circuit, DC-DC circuit, DC-AC circuit and AC-AC circuit. AC-DC conversion circuit, which converts current to direct current, is most used in industry nowadays. And we call this kind of circuit rectifier circuit. Rectifier circuit has many applications, such as appliances like uninterrupted power supply(UPS). Rectifier circuit can act as interface circuit between power grid and power electronic devices, composing DC regulated power supply, and supplying high quality power for power electronic devices.

Power factor is a significant qualification of power system. With the wide application of power electronic in industry, switching devices are widely used in different power conversion devices. The introducing of switching devices improved the devices' efficiency of power conversion but brought problems like harmonic pollution and low power factor. In order to eliminate harmonic and improve power factor, people bring a new technology which is called power factor correction. Because people now are trying to get high quality power, power factor correction is in leading edge of power electronics research.

Power factor correction is very important because low power factor brings lots of problems to our circuits and power devices. The key point to improve the power factor of power devices is the research of topology structure of power factor correction circuit and integrated circuit of power factor correction. There are several popular chips used to achieve power factor correction, like L4981, UC3842-UC3855A series, KA7534 and TDA4814. [1]

Boost circuit is a basic DC-DC conversion circuit. Boost circuit has many advantages like continuous inductor current, less distortion of current waveform and less RFI and EMI noise, so boost circuit is widely used in different power design. But for basic boost circuit, there are some perspectives we can improve such as power factor and circuit transmission efficiency.

Because of the wide application of power electronic devices, there are reactive power and harmonics in the power grid. One of the method to solve this problem is to apply active power factor correction technique. This technique brings active switch into

conversion circuit, through the control of on and off of active switch, we can make input current follow the input voltage. So we can make a sinusoids shape input current and a power factor which approaches 1. The main research content of this paper is the design of boost power factor correction circuit and design of its control system.

1.2 Disadvantage due to Harmonic Current in Power Grid [2]

In fact, the decrease of power factor caused by harmonic current already exists for a long time. People don't pay much attention because the use of switching devices is not widely used and people know little about the disadvantage of harmonic current. Generally speaking, there are always harmonics wherever there are switching devices. The existence of harmonics will lead to decrease of power factor. In earlier years, people use thermistor and rectifier diodes a lot, so there are problems like harmonic current and low power factor in power electronic devices.

Impulse shaped AC input current waveform contains a lot of harmonic current components. These Harmonic current components will pollute power grid. Harmonics in an electric power system are a result of non-linear electric loads. It will produce current in a different frequency from its original frequency. Harmonic current has following disadvantages:

(1) The 'secondary effect' of harmonic current, which is, when harmonic current passes the loads, it will cause harmonic voltage which will distort the voltage of power grid, so there will be overcurrent or overvoltage.

(2) It will increase the extra loss of the circuit, and decrease the efficiency of the power

generation equipment and power transmission equipment.

(3) It will make power devices (such as transformer, capacitor and electric motor) work abnormally, accelerate the insulation aging and abbreviate the devices' service life.

(4) It will make relay protection, automatic devices and computer system work abnormally or even don't work.

(5) It will make measuring equipment or instrumentation not able to measure.

(6) It will interfere communication systems, decrease the transmission quality of signal, or even damage the communication devices.

So we can conclude that the existence of harmonic current pollute power grid so much and we have to take some actions to eliminate or restrain harmonic current. There are two ways to restrain harmonic current, the first is to use reactive power compensation device to produce harmonic which has the same frequency but opposite phase. The second way is to produce some devices which doesn't produce harmonic current.

1.3 PFC in EV Front-End AC-DC Converter Applied in Charger

In the EV charging system, the front-end AC-DC converter is very important and should meet the requirements of the efficiency and power density. And this thesis focuses on the AC/DC PFC boost converter component and the its controller. The system block diagram of a universal in-board two-stage battery charger in Fig.1.1 [3] [4].

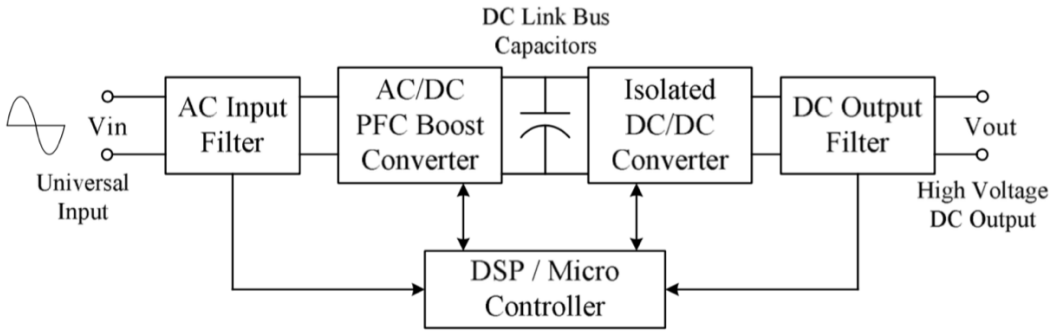


Fig.1.1 Simplified system block diagram of a universal in-board two-stage battery charger

1.4 The Main Content of the Research

a. Learn the control strategy of power factor correct circuit.

b. Learn the principle and basic control strategy of boost converter power factor correction circuit.

c. Simulate the boost converter power factor correction circuit applied in EV level 1 charger.

Chapter 2: Single Phase APFC's Main Power Topology and Its Control Strategy

The main contents of this chapter are as follows:

(1) Activate power factor correction.

(2) The main power topology structure of APFC and its modified topology structures.

(3) The typical control strategy of APFC.

(4) The advantages and disadvantages of Boost APFC.

The basic idea of PFC is using power conversion of high frequency switching mode to make the shape of input current close to sinusoidal wave. One of the popular ways is to have a value which is in proportion to the input voltage to be the reference of the current. For this way, we just assume that the harmonic of the input voltage is small and can't effect the control of harmonic current. In most cases, the correction of power factor is achieved by an an independent part which is called PFC (power factor corrector). The input of the PFC is usually power grid, and the output is usually a DC voltage. The DC voltage will be the input of DC-DC converter or DC-AC current and provides a stable output for the next converter, making the DC-DC converter or DC-AC converter becomes an optimal design.

2.1 Active Power Factor Correction(APFC)

2.1.1 The definition of AC-DC converter power factor and its relationship with harmonic waves [4]

In linear circuit, we use cosφ to express power factor, of which φ is the phase difference of sinusoidal voltage and sinusoidal current. Because diodes in the rectifier circuit is not linear, although the input voltage is sinusoidal, the rectified current is non-sinusoidal. So the power factor calculation in linear circuit is no longer valid in AC-DC converter. We use PF to express power factor here.

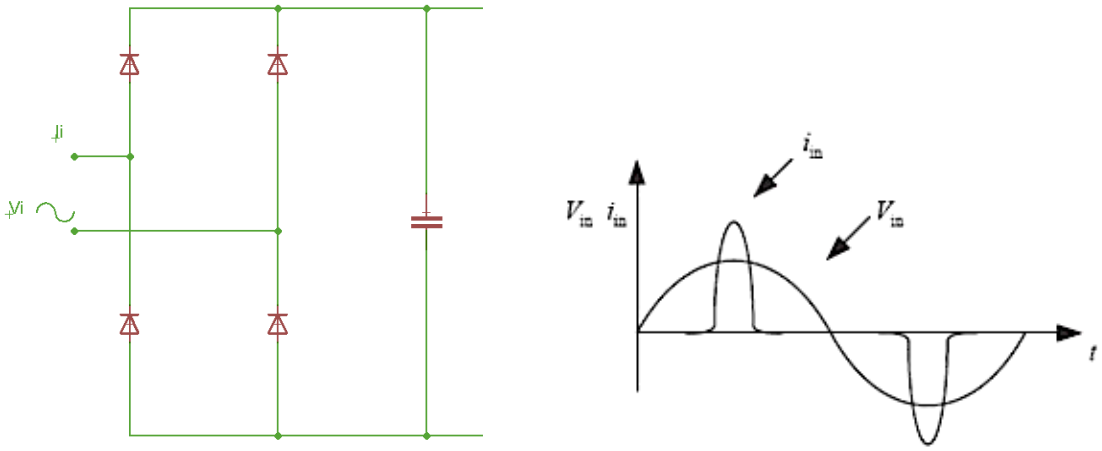


Fig.2.1 Rectifier circuit and its input voltage and current waveform

The definition is PF=active power/apparent power=P/V•I.

In the equation above, V and I here are the rms voltage and rms current.

We assume the input voltage v_i (rms value is V) is sinusoidal, and input current is not sinusoidal, the rms of current is shown as follow:

$$I = \sqrt{I_1^2 + I_2^2 + \cdots + I_n^2 + \cdots} \tag{2.1}$$

In this equation, I_1, I_2, ..., I_n are respectively the fundamental component, second harmonic, …, and N^{th} harmonic.

Because the input current has a terrible distortion and phase change, the definition of the power factor used in linear systems is not available anymore in switching power systems. We assume that i_1 lags v_i by phase α, as shown the figure below:

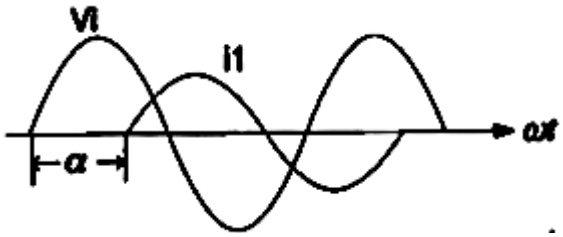


Fig.2.2 The V_i, i_l waveform

$$P = VI_1 \cos\alpha \tag{2.2}$$

$$PF = VI_1 \cos\alpha / VI = I_1 \cos\alpha / I \tag{2.3}$$

And we know that,

$$I_1/I = I_1/\sqrt{I_1^2 + I_2^2 + \cdots + I_n^2 + \cdots} \tag{2.4}$$

I_1, I_2, ..., I_n are rms value of the fundamental component, second harmonic, …, and N^{th} harmonic. The equation above describes the relative magnitude of the fundamental current, which is called distortion factor. And cosα is called displacement factor, and the power factor equals the distortion factor times the displacement factor. When α=0, PF=I_1/I.

We call the total harmonic distortion THD, so

$$THD = I_h/I_1 = \sqrt{(I_2^2 + I_3^2 + \cdots + I_n^2 + \cdots)/I_1^2} \tag{2.5}$$

I_h is the rms value of all the harmonic currents.

So we can get the equation of distortion factor:

$$I_1/I = 1/\sqrt{1 + THD^2} \tag{2.6}$$

And when α=0,

$$PF = I_1/I = 1/\sqrt{1 + THD^2} \tag{2.7}$$

2.1.2 Basic principle of APFC [5]

The circuit of APFC contains two parts, one is the main circuit and the other is the control circuit. We take boost PFC circuit as an example. From Fig.2.3 [6] we can see, the main circuit consists of a single-phase bridge rectifier and DC-DC converter. And for control circuit, we have reference voltage ($V_{o,\,ref}$), voltage error amplifier (VA), multiplier (M), current error amplifier (CA) and pulse width modulator (PWM).

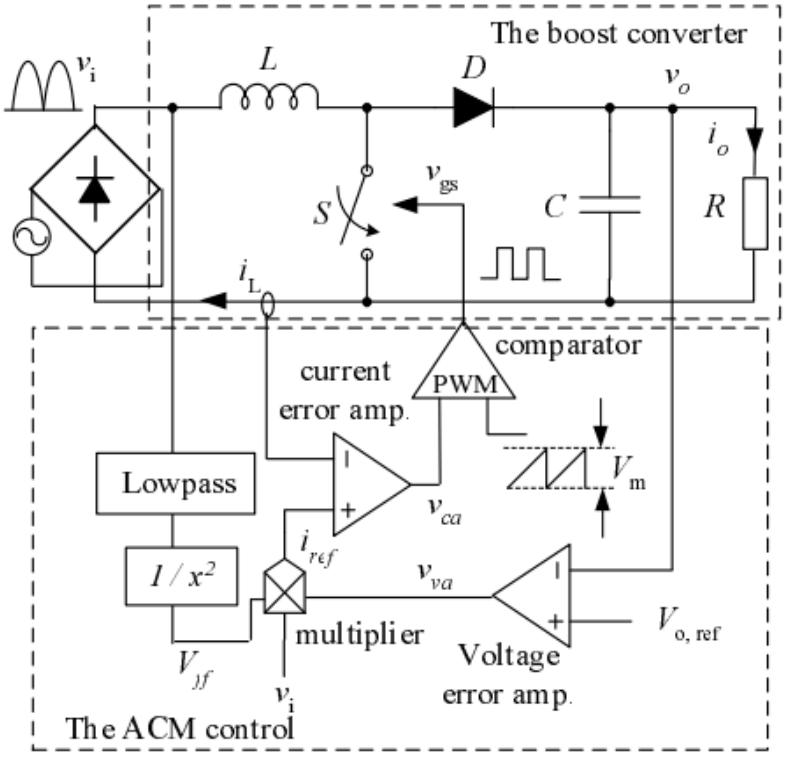


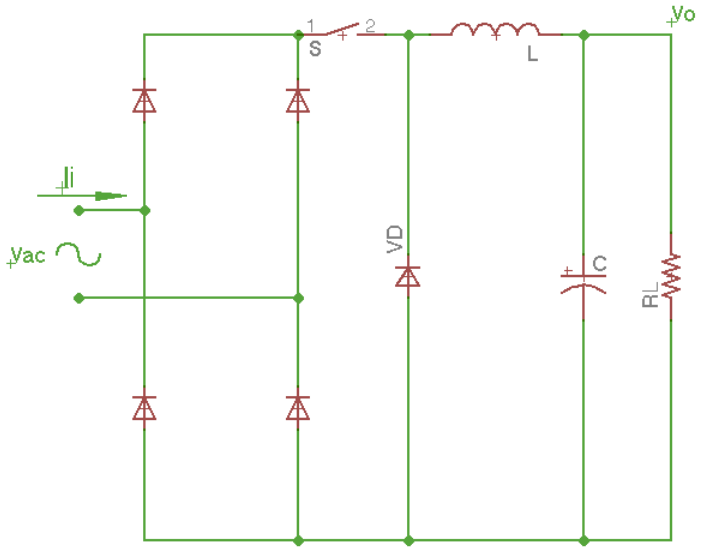
Fig.2.3 Simple schematic of the boost APFC under ACM control

Now we discuss the principle of PFC. After comparing the output voltage with the reference voltage, the result goes through the voltage error amplifier. The output of voltage error amplifier and rectified input voltage together go to multiplier and we set the output of the multiplier as the reference of current feedback control. After comparing the reference current with the input detected current, the result goes into the current error amplifier and control the on and off of the switch S. So we can make the input current and the rectifier input voltage be at almost the same phase, and there is less harmonic current, that we can increase the power factor and make the output voltage stable.

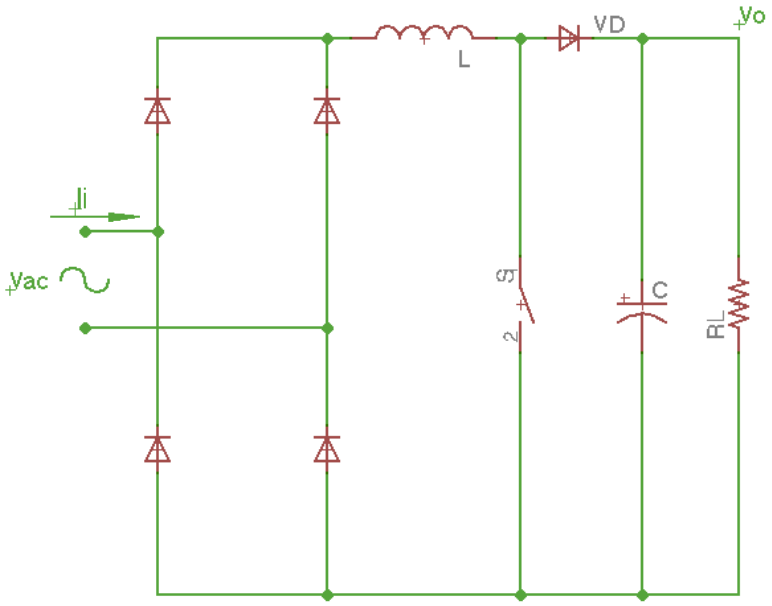
2.2 The Topology Structure of APFC

2.2.1 Several typical topologies of APFC

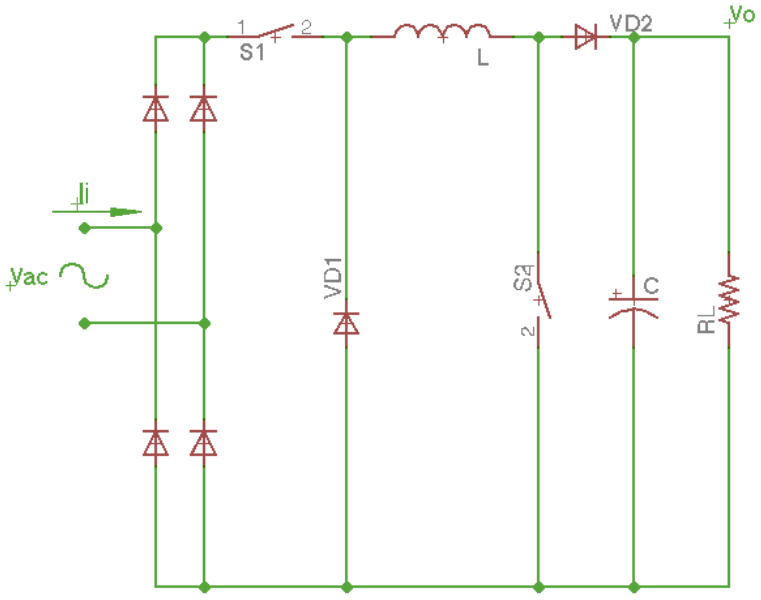
There are many kinds of topologies of APFC, the typical topologies of APFC are Boost, Buck, Boost-Buck, Ćuk and flyback converters. Boost converter is most used because it has several advantages against other APFC circuits. Boost and Buck converters have the most basic topology structures among all APFC circuits and other structures are developed from these two structures. Now we simply talk about the features of Boost, Buck, Boost-Buck and Ćuk converters.



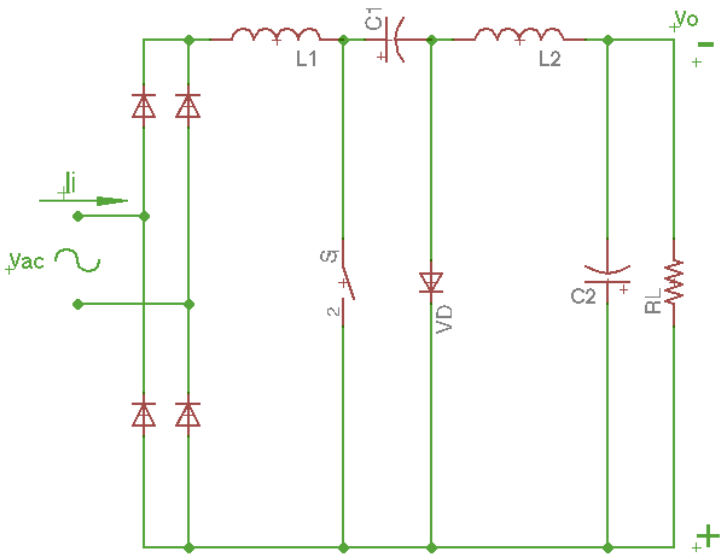
(a) Buck PFC



(b) Boost PFC



(c) Buck-boost PFC



(d) Ćuk PFC

Fig.2.4 Several topology structure of PFC

a. Buck converter:

(1) Buck converter can only buck the voltage because when the switch is on, the inductor L and conductor C are in series connection.

(2) The input current of the source is discontinuous because when the switch S is off, V_{ac} and inductor L, conductor C are insulated. So it restricts the efficiency of the converter and leads to high ripples of the input current.

(3) When switch is on, the source voltage is V_d. But when switch is off, the source voltage is 0. So when the input voltage is high, we need a specific floating drive for the switch since the source voltage is float. As a result, it makes the design of circuit more complicated.

(4) Because buck the converter can only be used to buck voltage, we cannot use it for APFC

directly, because the source voltage V_d is a half sinusoidal waveform after rectified by the full bridge rectify. So for 110VAC source, the variation range of V_d is from 0 to 155.56V. And when V_d is smaller than the output voltage Vo, the converter can't work, which restricts the increase of the power factor.

b. Boost converter:

(1) When boost converter is the main circuit of PFC, it can only boost the voltage so that this circuit is working stably. The inductor L is charged when switch S is on and when switch S is off, L is discharged.

(2) The AC input current is always the same with inductor current, so that input current is continuous. When implementing large power DC-DC converting and power factor correction, the continuous input current has its own advantage. At the same time, the ripple current is small when input current is continuous, so it reduces the processing requirements for the filter circuit.

(3) Because the source voltage of the switch is always 0, it's easy to control the switch.

c. Buck-Boost converter:

(1) When we take Buck-Boost converter as the main PFC circuit, we can either buck voltage or boost the voltage, which can get over some disadvantages of the circumstances that we have only boost converter or buck converter.

(2) The input current of the source is discontinuous, which is the same with the Buck converter because the input itself is a Buck converter. So it increased the requirements for the filter circuit.

(3) When we use Buck-Boost converter as the main PFC circuit, we need two switches

(one for drive control). so the circuit is more complicated.

d. Ćuk converter:

The main idea of Ćuk converter is to have a series connection of a Boost converter and a Buck converter.

(1) Whether the switch S is on or off, the current of inductor L1 and L2 is continuous, and the input source current is always the same with the current in the inductor L1. And this feature is the same with the Boost converter.

(2) When we increase the inductor L1 and L2, we can make ripple current very small. So we don't need extra EMI filter, and the devices can be miniaturized.

(3) Ćuk converter can either buck or boost the voltage like Buck-Boost converter.

2.2.2 Several topologies of modified single phase PFC

a. Center tapped boost inductor circuit

The center tapped boost inductor circuit is like the figure below. Through adding several coils on the magnetic ring of the boost inductor, the drain of the MOSFET is not connected to the boost diode directly. And we know that the inductor current cannot be mutated so that we can restrain the large instantaneous current caused by backward recovery of the boost diode D1. And we can restrain the overheat caused by the large opening loss. The main disadvantage of this circuit is the ripple noise of output voltage caused by the backward recovery of D1. So we have to add a LC filter at the output to eliminate the ripple.

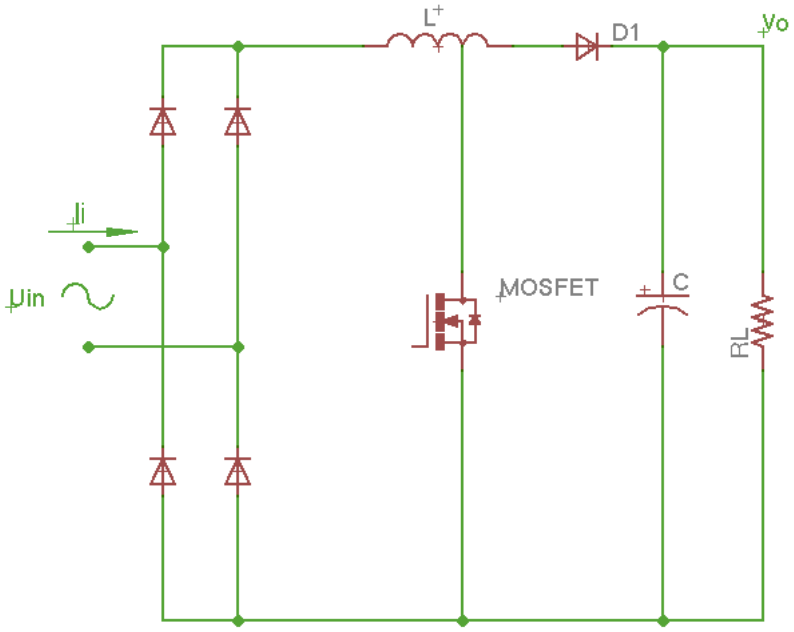


Fig.2.5 Center tapped boost inductor circuit

b. Series inductor and RCD snubber circuit and clamp circuit

As shown in Fig.2.6 and Fig.2.7, through increasing L2 we can restrain the impulse current caused by the backward recovery of D1. But when the MOSFET is cut off, we have to solve the problem of overvoltage generated by L2 on the switch.

In the upper figure, we use D2, C2 and R1 to compose RCD snubber circuit. Because capacitor voltage cannot be mutated, and we can use that to restrain the overvoltage caused on L2 by cutting off of the MOSFET. The overvoltage on the capacitor is released to the 400V output, so we can protect the switch from the overvoltage.

In the lower figure, R1, C1 and D2 composed clamp circuit. Because in PFC circuit, we tend to use a large electrolytic capacitor filter at the output, we can hold up the output

voltage at 400V. So we can use the clamp characteristics to restrain the switch voltage in the rated voltage range across the transistor switch.

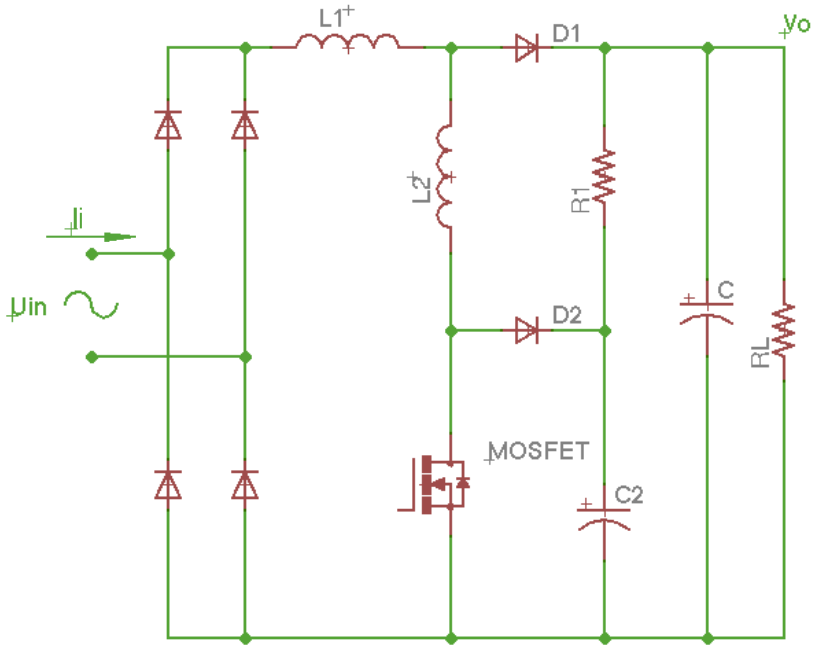


Fig.2.6 Series inductor and RCD snubber circuit

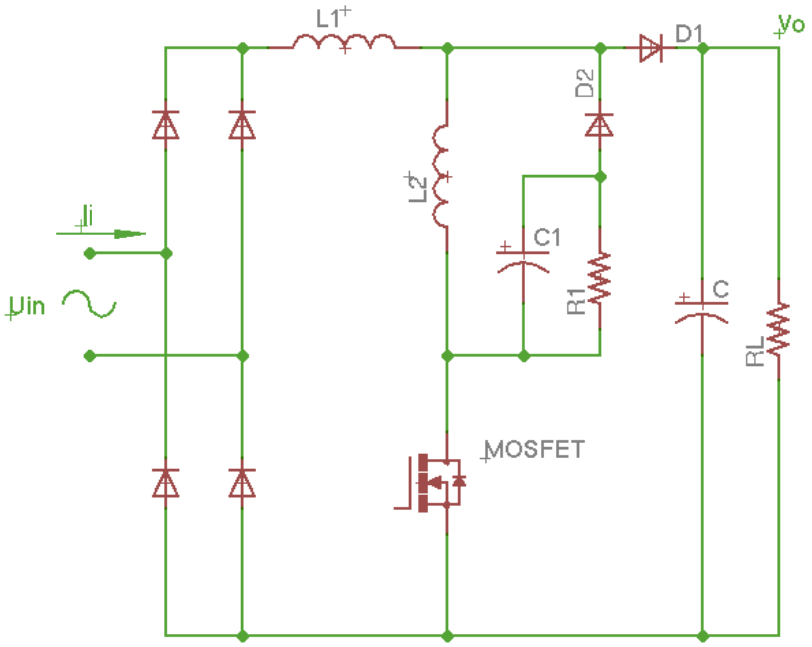


Fig.2.7 Series inductor and clamp circuit

c. Series inductor and lossless snubber circuit

In this circuit, we add C1 and D3 to be the snubber circuit of diode D1. When the switch is off, the current flow through L2 and charge the snubber capacitor C2 and the junction capacitance of switch. Because we added snubber capacitor, the rising speed of the voltage will be slowed, so that we achieve the shutdown buffer. In addition, the series connection of D2, D and D3 can restrain the impulse current of the switch.

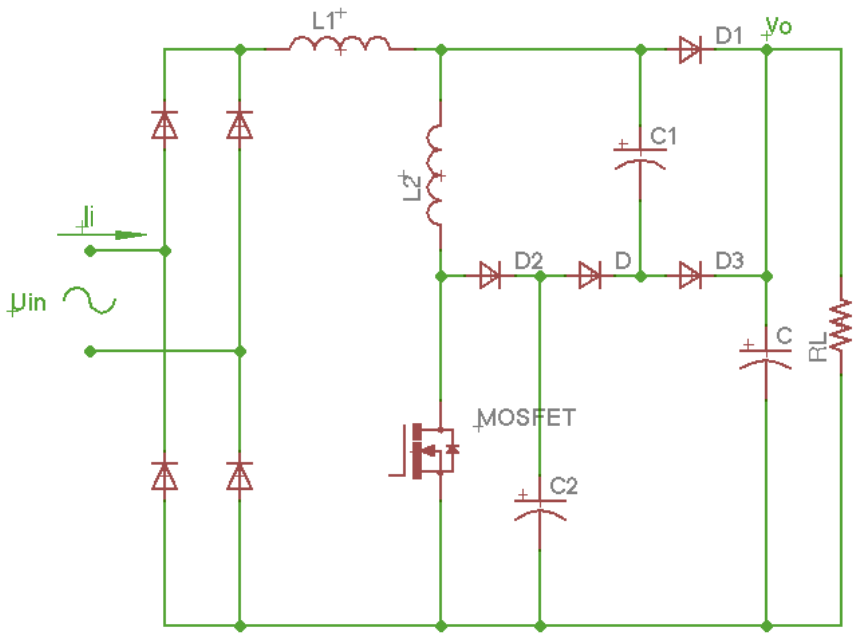


Fig.2.8 Series inductor and no loss snubber circuit

d. Series Schottky diodes circuit

In Fig.2.9, D1, D2 and D3 are all Schottky diodes. Since the backward recovery time of Schottky diode is very small (less than 10ns), we can use Schottky diode to restrain the impulse current. Schottky diode has small withstand voltage, so we just apply series structures of D1, D2 and D3. This series connection will also decrease the impulse current of the switch. But this circuit has high requirements for the withstand voltage and the consistency of the dynamic and static characteristics of Schottky diode.

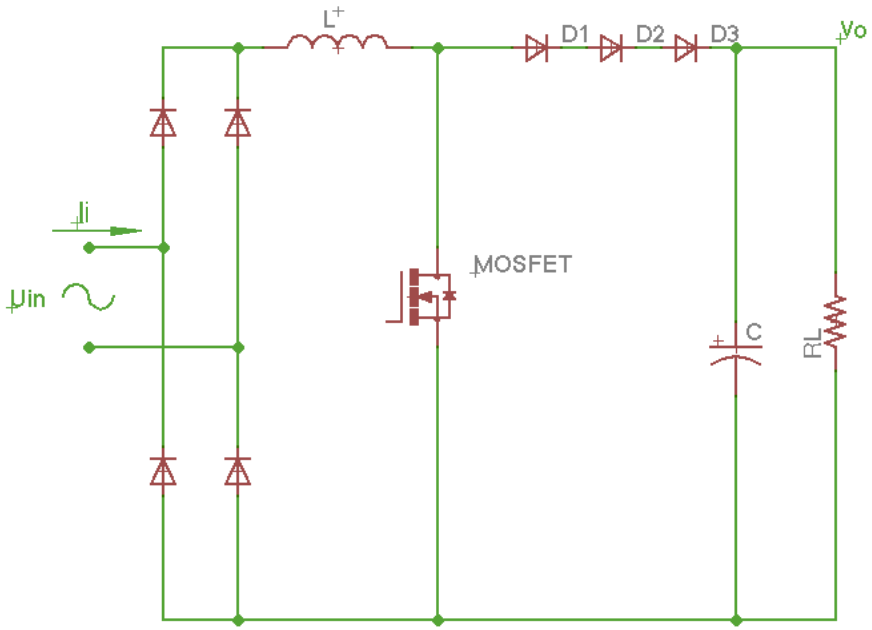


Fig.2.9 Series Schottky diode circuit

2.3 Typical Control Strategy of APFC

In practical applications, we have different control strategies for different APFC topologies. No matter what APFC topology we use, in order to achieve PFC, we have to take control of two variables:

a. Output voltage, that we have to make sure is stable DC voltage.

b. Input current, that we have to make to follow the input voltage at the same frequency and the same phase, and make the input port to be pure resistance.

Therefore, for APFC, we usually apply Voltage-Current double-loop feedback control strategy. In some cases, it will make the PFC circuit more complicated. Because Boost converter has many advantages, like it is easy to control, and it has continuous input

current and small ripple current, it is widely used in industry. So we take Boost converter as an example to analyze the control strategy.

There are two goals we need to achieve for APFC strategy, which are stabling the output voltage and realizing unit input power factor. And there are many different control schemes presented by many scholars to fulfill the different requirements in different circumstance. We can divide APFC into two types according to whether the inductance current is continuous. One is DCM (Discontinuous Conduction Mode) and the other is CCM (Continuous Conduction Mode) [7] [8]. In CCM, we can achieve PFC using multiplier. While in DCM, we realize PFC using voltage follower. Under CCM, the control strategy is furtherly divided into two methods according to whether we use the instantaneous inductor current as feedback. Direct current control adds the current feedback. And for Indirect current control, current feedback is not added.

2.3.1 Discontinuous conduction mode

We call Discontinuous Conduction Mode as Voltage-follower Control. There are two control modes, one is constant frequency mode and the other is variable frequency mode [9]. In order to get steady output voltage, we need output voltage closed loop feedback control, of which the switch is controlled by the output voltage error signal. During one switching circle, the mean value of the inductor current is in proportion to the output voltage, so that the input current follows the input voltage automatically.

a. Constant frequency mode

Fig.2.10 shows the DCM control strategy of Boost circuit. We set the frequency bandwidth of voltage regulator at 10-20Hz, so that the duty circle is steady during half of the frequency period. In constant frequency mode, the switching frequency stays constant and the inductor current is discontinuous. And the average inductor current during a switching cycle is written as below [10]:

$$I_{avg} = \frac{V_d T_{on}(T_{on}+T_{don})}{2LT_s} \tag{2.8}$$

V_d is the rectified voltage, Ton is the conducting time when the switch S is on, T_{don} is the freewheeling time of the diode VD and T_s is the switching cycle.

In the equation, we assume T_{don} is constant and we take the input port of DC-DC converter as pure resistance. So for the AC side, the voltage and the current are of the same phase. Actually, T_{don} is not constant so there is some degree of distortion of the average input current. The greater the ratio of the output voltage over the peak of the input voltage, the smaller the distortion will be [11].

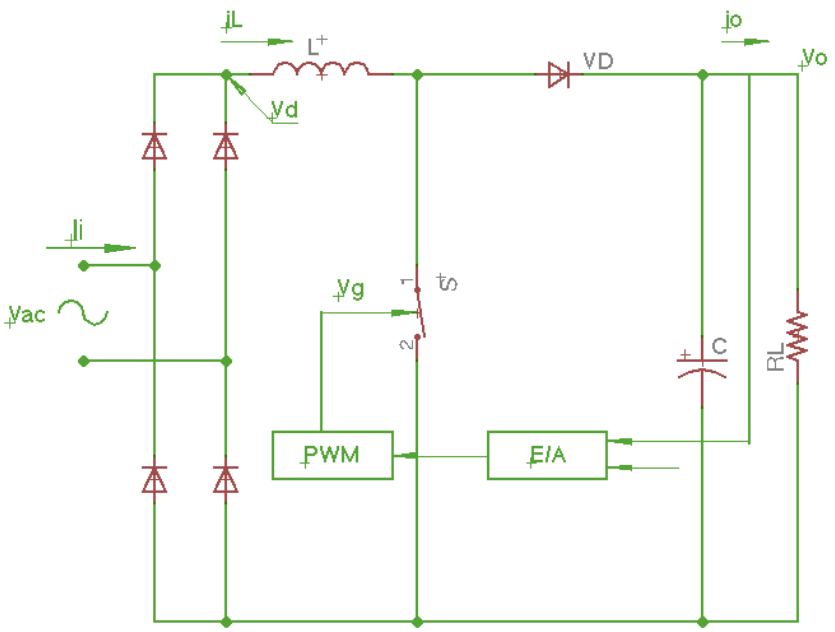


Fig.2.10 DCM mode of boost circuit

b. Variable frequency mode

In the equation (2.7), if $T_s=T_{on}+T_{don}$, the average input current is only related to the time when the switch is on. So if T_{on} is constant, there should be no distortion on input current, and this is how the variable frequency mode works. When the duty circle and the switching frequency is constant, the average input current is in proportion to the input voltage. So we don't have to regulate the current, and the average input current is following input voltage automatically.

- Advantages of DCM mode:

(1) The circuit structure is simple, and it is not necessary to add multiplier.

(2) The input current follows the input voltage automatically.

(3) The diode won't suffer the impulse current caused by backward recovery.

- Disadvantages of DCM mode:

(1) The inductor current is discontinuous so there is large ripple current, and the filter need to satisfy high requirements [12].

(2) The output contains the second harmonic, and the power devices take a little bit large current stress.

(3) The power of the single phase PFC is usually smaller than 200W.

2.3.2 Continuous conduction mode (CCM)

We can divide CCM into two control mode, one is indirect current control, and the other is direct current control.

a. Indirect current control mode

For indirect current control, it's also known as phase amplitude control. It is a control mode which is based on steady frequency. Through regulating the input voltage of the rectifier, making it at specific phase and amplitude related with source voltage, we can regulate the AC input current to be sinusoidal wave, and also at the same phase with the input voltage. The advantage of this control mode is that its structure is clean and easy to build [13]. And there are also some disadvantages of this circuit. It can't limit the current, so we have to add an overcurrent protection circuit. Furthermore, in transition from a steady state to another, there will be DC component in current wave. In addition, the dynamic response of this system is slow.

b. Direct current control mode [4] [14]

In direct current control mode, the circuit contains multipliers so it is also called multiplier approach control. The basic idea of this control mode is to feed the input voltage signal and the output voltage signal into the multiplier, and then make the output signal of multiplier as reference current signal of current controller. The current controller will control the input current to vary and follow the reference signal. The disadvantage of this circuit is that the circuit is kind of complicated compared to indirect current control. In this control mode, we sometimes need to add a current loop compensation network; the output contains second harmonic; the dynamic response is also very slow; and the nonlinear distortion of multiplier will increase the harmonic in the current. Because the input current always contains ripple of switching frequency, we have to decide which current should be the feedback. So there are three kind of control mode. The first one is peak current mode control. The second one is hysteresis current mode control and the last one is average current mode control. These three control modes are widely used in APFC.

Now we take Boost PFC circuit as an example to introduce the principle of these three control modes. And we assume they all work as CCM.

(1) Peak current mode control

Fig.2.11(a)-(b) shows the schematic diagram of peak current mode control. The switching period is T and stays constant. We multiply the input voltage signal with the feedback signal of the output voltage, and we can get a current control reference signal which is the same phase and same frequency with input voltage. When the switch is on and inductor L is getting charged, we compare the inductor current with the current

control reference signal. When the inductor current rises to the reference signal, the switch is shut down by logical control. Then the inductor starts discharging, and after a switching cycle the switch is closed again. Fig.2.11(b) shows the inductor current i_L and switch control voltage V_g.

As the peak of inductor current increased sinusoidal, the duty circle of control waveform will vary from a large value to a small one. During half of the switching cycle, the duty cycle is sometimes greater than 0.5 and sometimes smaller than 0.5. When the duty cycle is larger than 0.5, the outside interference will be amplified, and the system current is not convergent, which may lead to sub-harmonic oscillation. So it is necessary to add a slope compensation or a ramp. Under this condition, the circuit will work well and stable when the duty circle changes [4] [11].

The main problem of Peak Current Mode Control is that we are trying to control the peak of inductor current, but we cannot ensure that average input current is in proportion to input current. And in some cases, it will generate a large error, so there might be large distortion which we don't expect. On the other hand, the peak current is very sensitive to noise. So in PFC circuit, we don't tend to use peak current mode control anymore.

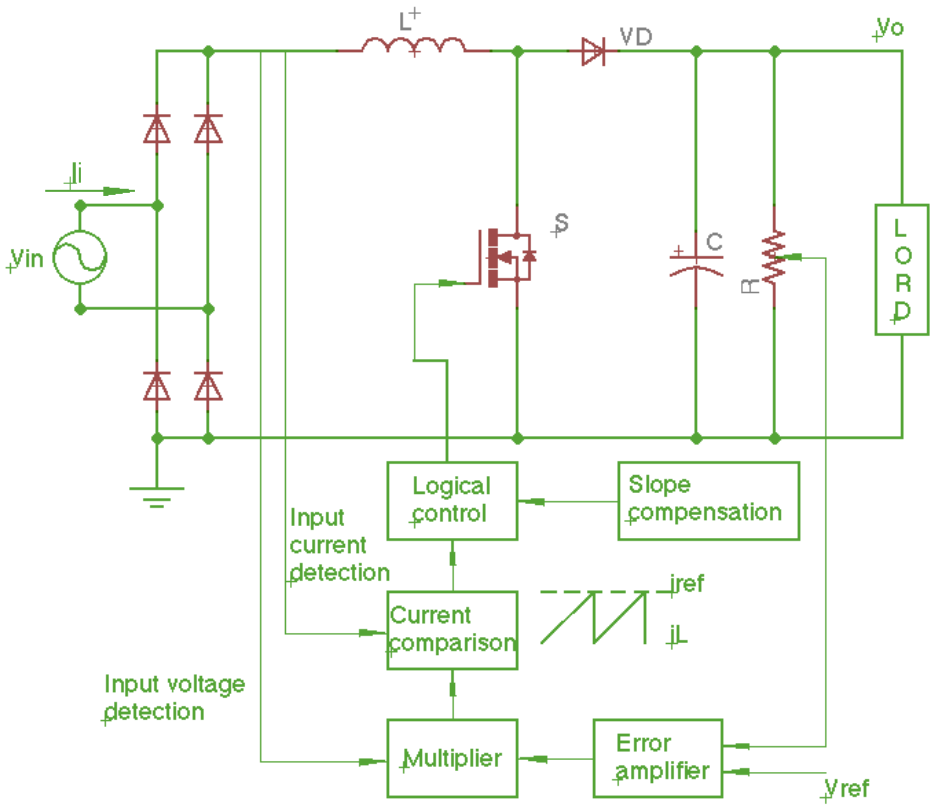


Fig.2.11(a) Peak current mode control PFC

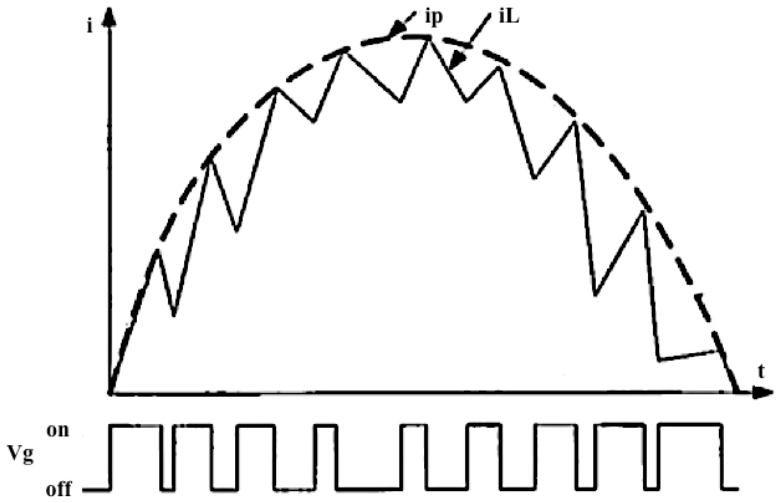


Fig.2.11(b) Peak current mode control inductor current waveform

(2) Hysteresis current control [15] [16]

Fig.2.12(a)-(b) shows the hysteresis current control Boost PFC circuit and the control waveform of switch S and inductor current i_L in half of the switching circle. Different from peak current control mode, the variable we take control in this control mode is the range of the inductor current. We multiply the input voltage signal with the feedback signal of the output voltage, then we will have two different current control reference signals which are same phase and same frequency with the input voltage. We call larger signal upper bound reference current loop signal and the smaller one lower bound reference current loop signal. We detect the inductor current and compare it with the two reference current signals. The control strategy is as follows:

- When the switch S is on, the inductor L will be charged, and the detected inductor current is compared with the upper bound reference current loop signal. And when the inductor current rises to the upper bound, the trigger logic control will cut off the switch S and the inductor starts discharging.
- When the inductor current falls to lower bound, the trigger logic control will turn on the switch and the inductor L gets charged.

In this control mode, the conducting time of switch S is constant, but the shutdown time varies. So the switching cycle is not constant. The bandwidth of hysteresis decides the size of the ripple, which can be constant or in proportion to instantaneous average current.

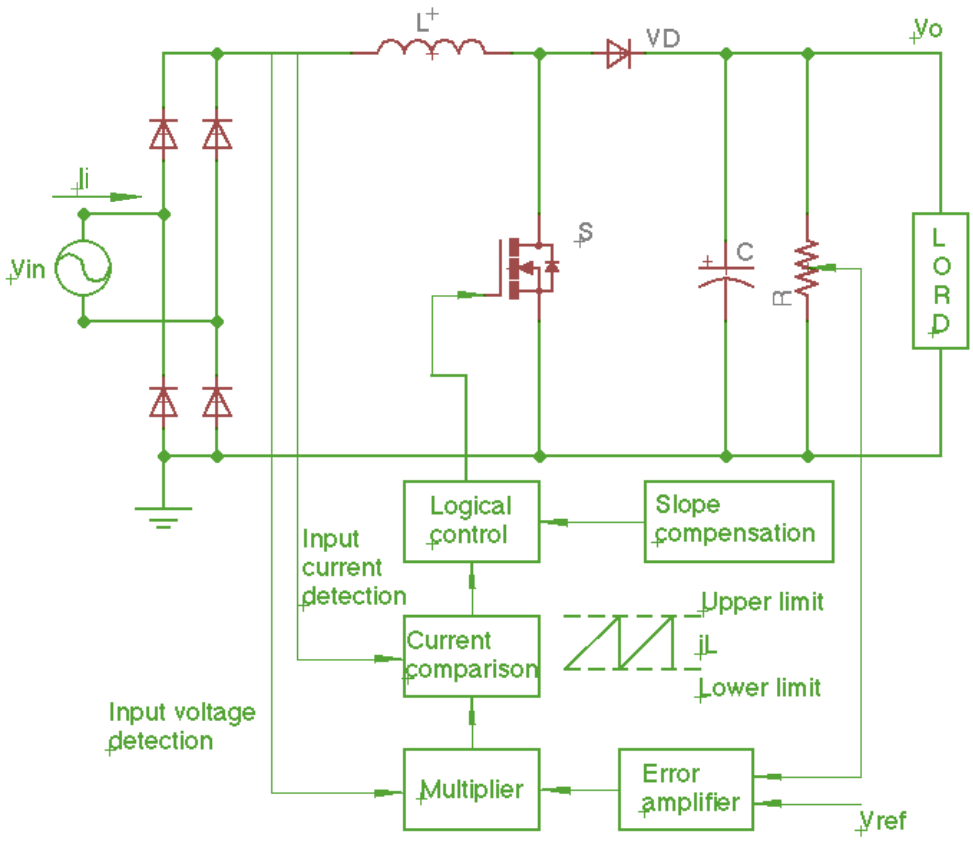


Fig.2.12(a) Hysteresis current control PFC

For Boost PFC, hysteresis current control is a simple control mode, because we have no extra modulation signal. And we can get wide current bandwidth and fast dynamic response. The disadvantage of this circuit is very obvious, that is, the load has large effects on the switch, so when we design the filter we need to consider the lowest switching frequency. Also the hysteresis bandwidth has large effect on switching frequency and system performance. Moreover, when source voltage approaches zero the difference between two reference signals is very small, so we always need some compensation for this circuit.

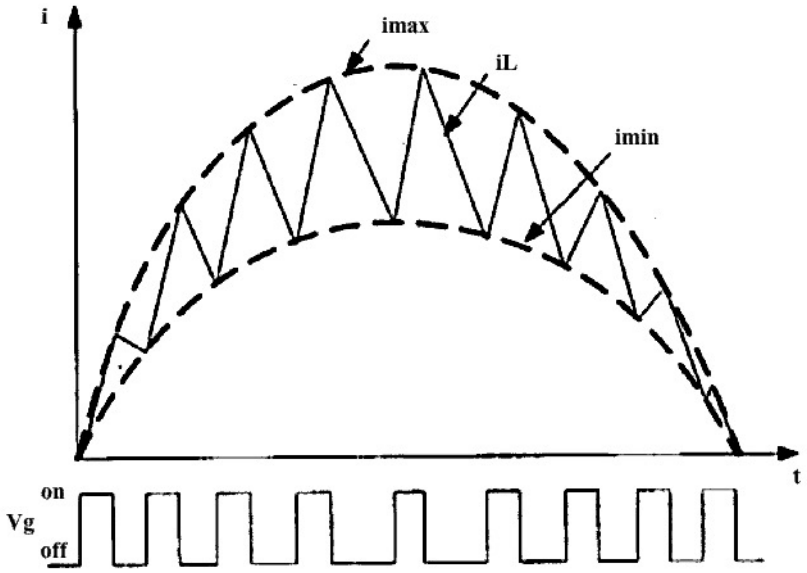


Fig.2.12(b) Hysteresis current control inductor current waveform

(3) Average current mode control

Fig.2.13(a) shows the schematic diagram of average current mode control. This kind of circuit is most widely used in PFC, and the inductor current waveform is shown in Fig.2.13(b). We multiply the rectified input voltage with amplified error signal of output voltage, and take the result as the reference signal. Through current loop regulation, we can control the average current and make it same phase with the input voltage. We detect the input current directly and then compare it with the reference current, and then the high frequency components will be average processed by the current error amplifier. Then we compare the amplified average current error with the sawtooth wave ramp and generate the switch driving signal, which decides the duty circle. So the current error will be eliminated in a fast speed [17].

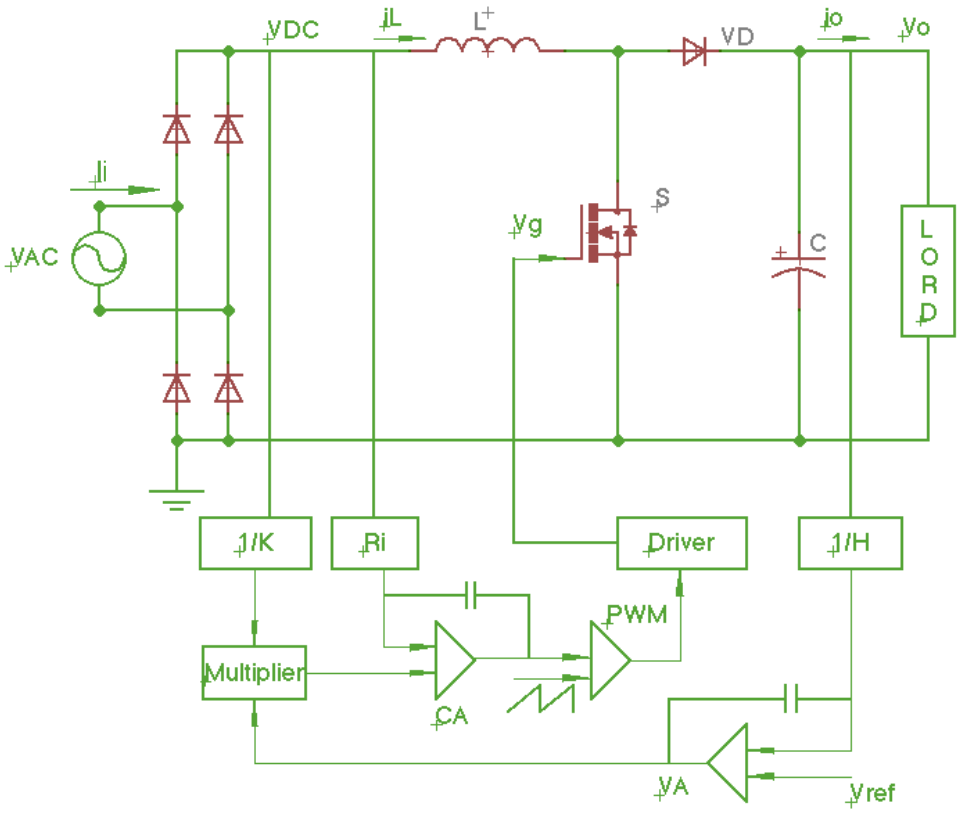


Fig.2.13(a) Average current mode control PFC

The advantage of average current mode control is that the variable is the average of input current, so the THD and EMI is small; it is not sensitive to noise; it can work under both CCM and DCM mode; and the switching frequency is constant so it is good for high power applications. And this is the most widely used control mode in PFC.

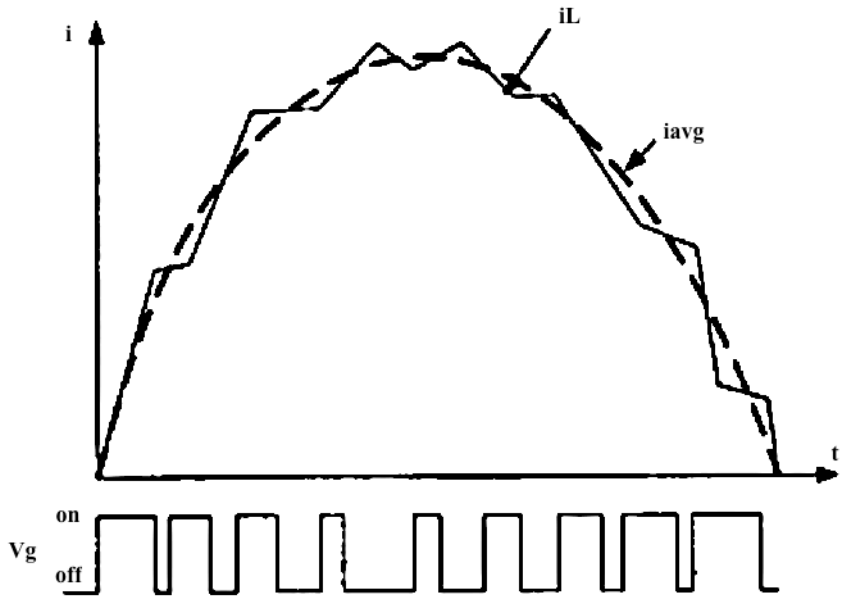


Fig.2.13(b) Average current mode control inductor current waveform

2.4 The Advantages and Disadvantages of Boost APFC

Advantages:

(1) The input current is continuous, and the EMI as well as the THD are small.

(2) It contains the input inductor, so there is less requirement for input filter. The input inductor can protect the main circuit from the high frequency transient impulse coming from power grid.

(3) The output voltage is larger than the peak of input voltage.

(4) The maximum voltage across the transistor switch S is smaller than the output voltage.

(5) It's easy to control the switch and the potential of the source is zero.

(6) It can work properly under a wide range of voltage and frequency.

Disadvantages:

(1) There is no insulation between the input and the output.

(2) If there is stray inductance in the loop composed by the switch S, diode D and the output capacitor C, there will be an overvoltage in the condition of 25-100KHz PWM frequency. So it is not safe for switch S.

Normally, boost APFC circuit is used for hundreds of watts to several kilowatts.

2.5 Summary

- In this chapter, the definition of power factor and the relationship between power factor and harmonic are described.
- Several common APFC main circuit topologies are listed, and their characteristics are compared and analyzed.
- The main circuit topology of several improved single-phase power factor correction is introduced, and the function of the circuit is analyzed.
- In this chapter, the control method of power factor correction technology is analyzed in detail, the principle of work is analyzed, and the advantages and disadvantages of each method and its application are pointed out.
- In the end, the advantages of APFC type Boost circuit are summarized.

Chapter 3: Design and simulation of the PFC boost converter

The design is based on the two-stage level 1 charging system in electric and hybrid electric vehicles. And the PFC circuit in the system is to correct the power factor and stabilize the voltage to the DC/DC stage. And the load is set as an equivalent resistor in this design. And there are several PFC topologies used in the market these days, but this design is based on conventional PFC circuit. And the main circuit is shown in Fig.3.1.

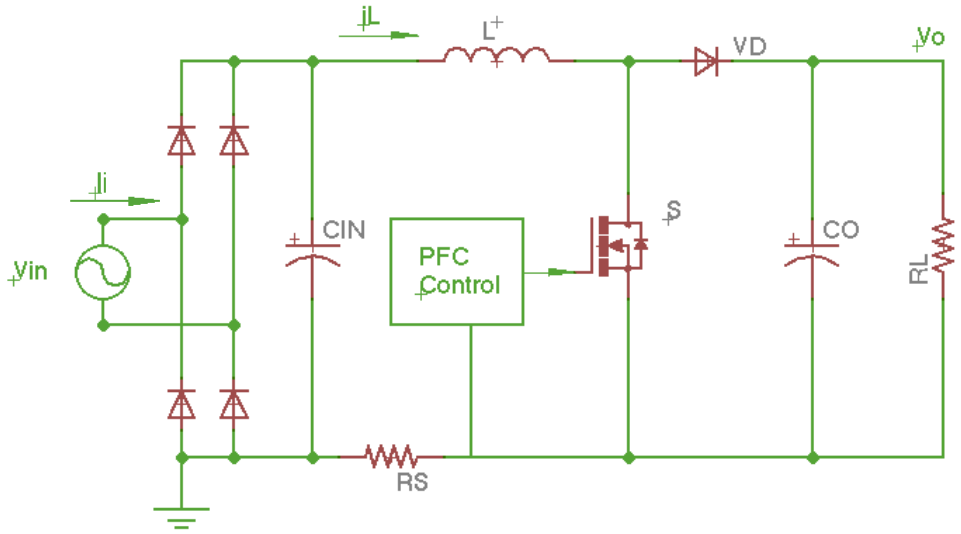


Fig.3.1 Conventional boost PFC circuit

3.1 System Main Circuit Design

3.1.1 Specifications

Determine the Operating Requirements for the Active Power Factor Corrector.

a. Rated output power P_o: 1.5kW

b. AC input voltage range: 85-140VAC

c. Grid frequency range: 60±1Hz

d. Output DC voltage U_o: 400V

e. Switch frequency f_{sw}: 50kHz

f. Efficiency η: >94%

3.1.2 Input filter capacitor selection [18]

The input filter capacitor is required to withstand input transient voltage as well as the superposition of the ripple voltage. The maximum high frequency ripple voltage ratio $r=\Delta V_L/V_L\approx0.02\sim0.08$, when considering the worst condition is the minimum input voltage. ΔV_L is the ripple voltage across the inductor, and V_L is the inductor voltage.

The formula for calculating the input filter capacitor is:

$$C_{in} \geq \frac{I_{rms}\bullet K_r}{V_{rms(min)}\bullet r\bullet \omega_s} \tag{3.1}$$

K_r is the ripple current coefficient, f_s is the switch frequency and $\omega_s=2\pi f_s$, $V_{rms(min)}$ is the minimum input voltage, I_{rms} is the rms value of the input current. Set Kr=0.2, r=0.05, f_s=50kHz, and we can get $C_{in}\geq2.64\mu F$. We select 3μF as the input filter capacitor.

3.1.3 Boost inductor selection [1]

The inductor is composed of a winding and a magnetic core, which plays the role of energy transfer, storage and filtering, and determines the magnitude of the high frequency ripple in the input current. The design of the inductor is crucial to the performance,

efficiency and function of the circuit, and whether the effect of the inductor can be satisfied.

When it is the minimum input current, current ripple is the maximum. In order to guarantee that the input current ripple meets the requirement in that situation, we need to calculate the inductor when the it is the minimum input voltage [19] [20].

$$L\frac{\Delta I_L}{DT_s} = V_{in} \tag{3.2}$$

$$L = \frac{V_{in}DT_s}{\Delta I_L} = \frac{V_{in}D}{f_s\Delta I_L} \tag{3.3}$$

In equations (3.2) and (3.3), L is the inductance, ΔI_L is the inductor ripple current, T_s is the switching period and D is the duty cycle.

a. Calculate the peak of the maximum input current:

$$I_{PK} = \frac{\sqrt{2}P_{in}}{V_{in(min)}} = \frac{\sqrt{2}\times 1500}{85} = 24.96(A) \tag{3.4}$$

In equation (3.4), P_{in} is the input power.

b. The maximum inductor current ripple ΔI_L allowed is normally set as 20% of the maximum peak inductor current:

$$\Delta I_L = 0.2I_{PK} = 0.2\times 24.96 = 5(A) \tag{3.5}$$

c. Calculate the duty cycle when the inductor current gets to the maximum peak. When the input voltage reaches the peak, the input current reaches the peak with the maximum ripple current. Therefore, we should calculate the duty cycle when it is the minimum input voltage:

$$D = \frac{V_o - \sqrt{2}V_{in(min)}}{V_o} = \frac{400 - \sqrt{2}\times 85}{400} = 0.7 \quad (3.6)$$

In equation (3.6), V_o is the output DC voltage.

d. At last, we can calculate the value of the boost inductor combining equation (3.3), (3.5) and (3.6):

$$L = \frac{\sqrt{2}V_{in(min)} \cdot D}{f_s \cdot \Delta I_L} = \frac{\sqrt{2}\times 85\times 0.7}{50\times 10^3 \times 5} = 0.44(mH) \quad (3.7)$$

3.1.4 Output capacitor selection

When selecting the output capacitor, the second harmonic current, the switching frequency ripple current, the DC output voltage, the output voltage ripple [21], and the hold-up time are considered. The total current through the output capacitor is the second harmonic of line current and the rms value of switching frequency ripple current. Usually we choose aluminum electrolytic capacitors that have long life, low leakage resistance, ability to resist large ripple current and work in a wide range.

There are two ways to design the output capacitance. The first one is to meet the requirement of the output ripple voltage, and the second one is to satisfy the hold-up time. In this design, we directly use the second method. And we set the hold-up time as 35ms and minimum output DC voltage as 350V [22].

$$C_o = \frac{2P_o \bullet \Delta t}{U_o^2 - U_{o(min)}^2} = \frac{2\times 1500\times 35\times 10^{-3}}{400^2 - 350^2} = 2.8(mF) \quad (3.8)$$

In equation (3.8), P_o is the output power, Δt is the hold-up time, $U_{o(min)}$ is the minimum output DC voltage.

3.1.5 Current sensing resistor selection

Normally there are two methods to sense the current, connecting a resistor in series in the line or using current transformer. Using sensing resistor will be cheaper than the other method, and it is mainly applied in low power and low current situations. So in this design, we use sensing resistor to detect the input current. The voltage across the sensing resistor will be modulated by the current loop and force the input current to be sinusoidal.

The dissipation power on sensing resistor should be below 10W, we set the power as 5W [18].

$$R_S = \frac{P_S}{I_{R(RMS)}^2} = \frac{P_S}{(I_{PK}/\sqrt{2})^2} = \frac{5}{(24.96/\sqrt{2})^2} = 0.016(\Omega) \quad (3.9)$$

In equation (3.9), P_s is the power dissipated on the sensing resistor, and $I_{R(RMS)}$ is the rms value of the current through the sensing resistor. For convenience, we select R_s to be 0.02Ω [22].

3.1.6 Power switch transistor and diodes selection [18]

When the switch transistor turns on, the diode reverse cutoff and the current flowing through the transistor is the inductor current, and the reverse voltage across the diode is output voltage. When the switch transistor turns off, the diode conducts forward. The voltage across the switch transistor is the output voltage, and the current flowing through the diode is the inductor current.

So, when selecting power switch transistor and diodes, the rated voltage must be greater than the output voltage, and the rated current must be greater than the maximum inductor current. We take the safety margin of voltage and current to be 1.2 and 1.5.

$$V_{rated} \geq 1.2V_o = 1.2\times400 = 480(V) \tag{3.10}$$

$$I_{rated} \geq 1.5I_{L(max)} = 1.5I_{PK} = 1.5\times24.96 = 37.44(A) \tag{3.11}$$

3.2 APFC Control Circuit Design

PFC circuit has the both the function of rectification and voltage stabilization, that is, the rectification requires the input power factor to be 1, and the voltage stabilization requires stable output voltage. Therefore, PFC circuit must be applied voltage feedback and current feedback simultaneously to form a dual loop control system. The outer loop is to keep the output voltage stable, and the inner loop shape the input current to make it a standard sinusoidal waveform with the same phase of the input voltage.

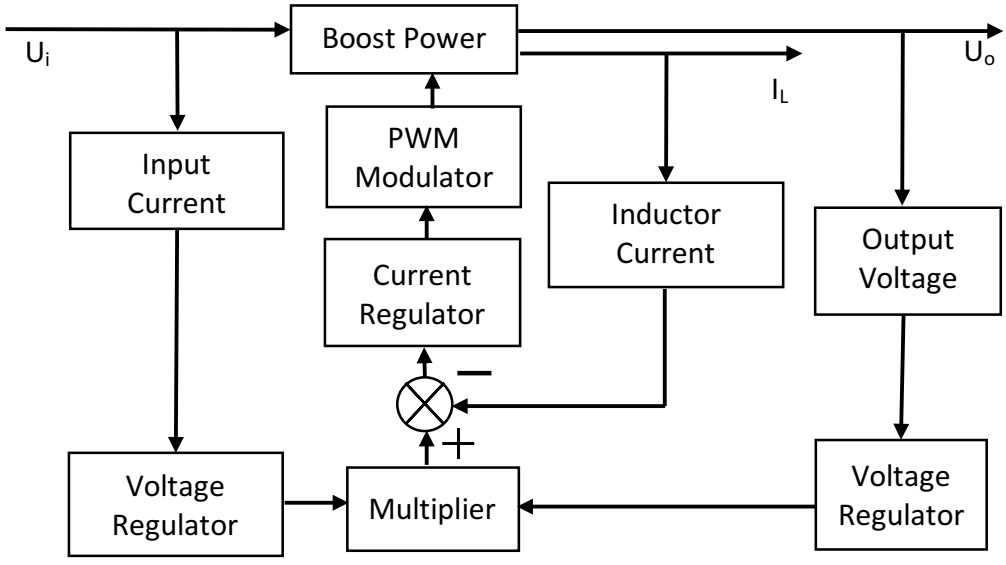


Fig.3.2 Control structure block diagram of PFC circuit

According to the above ideas, the control circuit of PFC can be drawn, and the control structure diagram is shown in Fig.3.2. In the figure, the boost power level represents the main circuit boost converter of PFC, of which the power device is controlled by the output signal conduction ratio (D) of the current controller, and operates in switch mode and achieve input current shaping and output voltage stabling.

Voltage regulator is used to improve the dynamic characteristics of the PFC output voltage. Its output signal U_e is multiplied by the instantaneously detected input voltage signal in the multiplier, and then divided by square of the input voltage rms value, then we constitute the reference current signal. After that, the reference current is compared with the instantaneously detected input current signal, and the result is processed by the PWM technology to achieve input current control to drive the switch.

3.2.1 Current control loop design for PFC circuit [1]

Current loop is the inner loop, which modulates the duty cycle of the power switch transistor, and force the input current to track the input voltage waveform. Because the input voltage is full-wave rectified waveform and contains rich harmonics, the current control loop must have enough bandwidth. While designing current control loop, we suppose the output voltage fully tracks the reference voltage, which is a constant value.

We can draw the ACM controlled current control loop as Fig.3.3. It consists of the current error amplifier, the pulse width modulator (PWM) and the power stage. In this figure, $G_{CEA}(s)$ represents the transfer function of the current error amplifier; $G_{PWM}(s)$ represents the transfer function of the pulse width modulator; and $G_P(s)$ represents the transfer function that the voltage across the sensing resistor R_s is controlled by the duty cycle D.

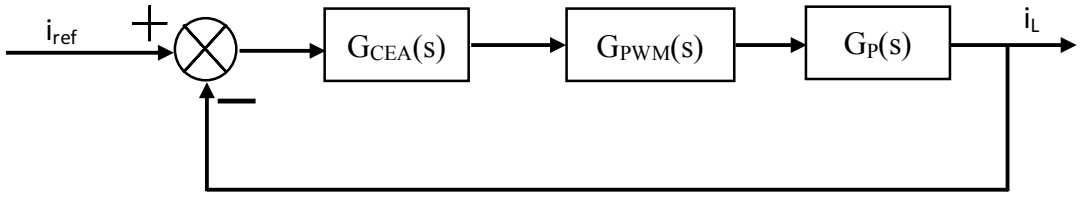


Fig.3.3 Current control loop structure

a. Power stage

In one switch cycle, the inductor voltage is:

$$L\frac{di_L}{dt} = U_i,\ switch\ on \tag{3.12}$$

$$L\frac{di_L}{dt} = U_i - U_o,\ switch\ off \tag{3.13}$$

According to the state space averaging technic, we can get:

$$I_L(s) = \frac{V_o \bullet D(s)}{S \bullet L} \tag{3.14}$$

And we can calculate the power stage transfer function:

$$G_P(s) = \frac{V_S(s)}{D(s)} = \frac{R_S \bullet I_L(s)}{D(s)} = \frac{R_S \bullet V_o}{s \bullet L} \tag{3.15}$$

b. Pulse width modulator

The principle of the PWM generator is shown as Fig.3.4.

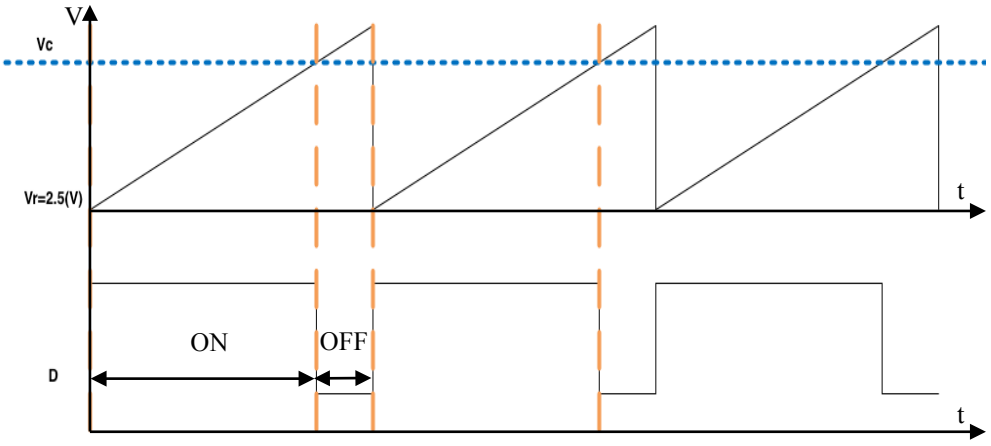


Fig.3.4 Pulse width modulator

The peak-peak voltage V_r of the sawtooth signal is set as 2.5V [23]. And the duty cycle is get from the calculation of V_r minus the output signal of the current error amplifier V_c. So we can get the transfer function:

$$G_{PWM}(s) = \frac{\Delta D}{\Delta V_c} = \frac{1}{V_r} \tag{3.16}$$

c. Current error amplifier

We use a PI controller to achieve the function of the current error amplifier [24]:

$$G_{CEA}(s) = k_{pc} + \frac{k_{ic}}{s} \tag{3.17}$$

So the open loop transfer function of the current loop is:

$$G_i(s) = G_{CEA}(s) \bullet G_{PWM}(s) \bullet G_P(s) \tag{3.18}$$

In order to give the current loop enough bandwidth to track the reference current, the open loop crossover frequency of the current loop is set 5kHz. And to make the system stable and have a proper respond speed, the phase margin is set 45˚ [25]. So we could write the two functions as below:

$$|\mathrm{G_i(s)}| = |\mathrm{G_{CEA}(s) \bullet G_{PWM}(s) \bullet G_P(s)}| = 1 \tag{3.19}$$

$$\angle G_i(s) = -180^\circ + 45^\circ \tag{3.20}$$

So we can calculate the parameters of the current loop PI controller, k_{pc}=2.16 and k_{ic}=6.79×10^4. And we can write the transfer function of the current error amplifier and the current control loop:

$$G_{CEA}(s) = 2.16 + \frac{6.79\times10^4}{s} \tag{3.21}$$

$$G_i(s) = \frac{R_s \bullet V_o}{s \bullet L \bullet V_r}\left(k_{pc} + \frac{k_{ic}}{s}\right) = \frac{0.02\times400}{s\times0.44\times10^{-3}\times2.5}\left(2.16 + \frac{6.79\times10^4}{s}\right) = \frac{17.28s+5.432\times10^5}{0.0011s^2} \tag{3.22}$$

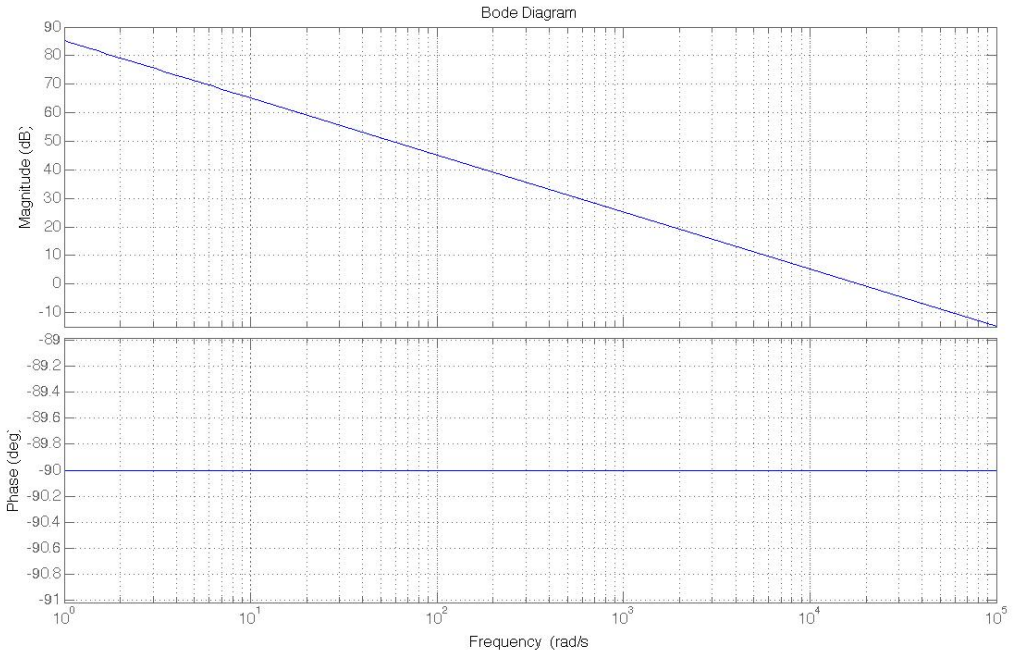


Fig.3.5 Bode diagram of the power stage

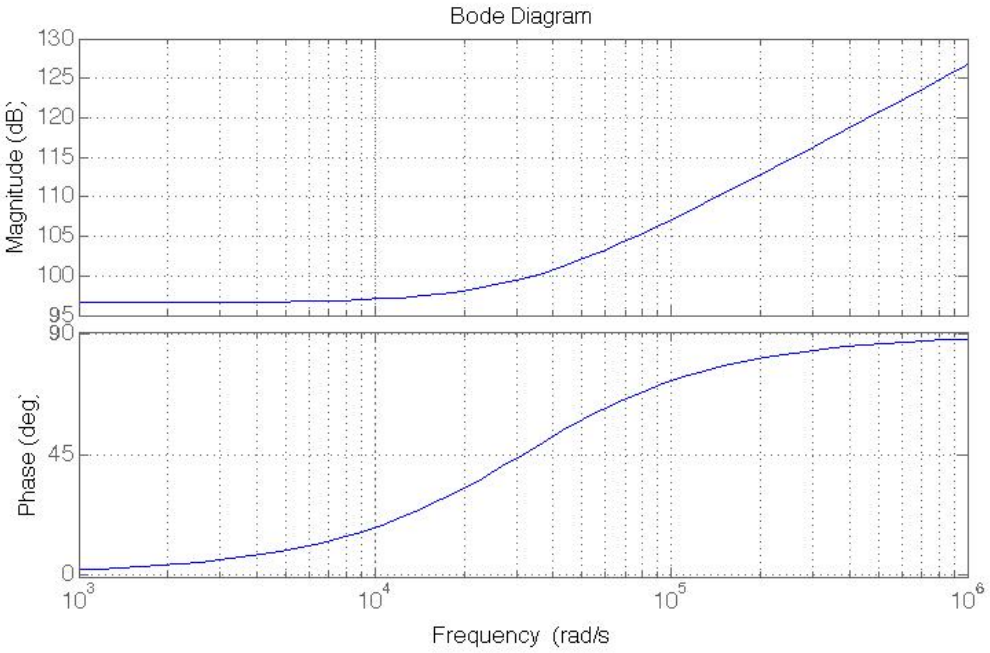


Fig.3.6 Bode diagram of the current error amplifier

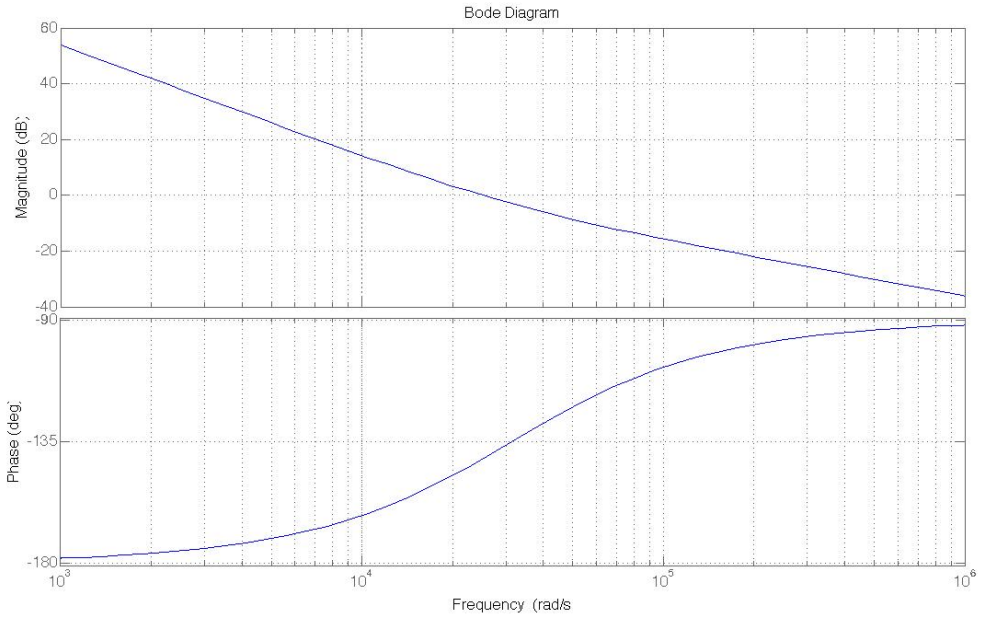


Fig.3.7 Bode diagram of the current open loop

From the simulation of MATLAB in Fig.3.5-3.7, we can see that when the $|G_p(s)|=1$, the crossover frequency of the power stage is around 2.86KHz. So the bandwidth of the power stage is too small and needs to be compensated, and it should be improved to around 5KHz. And after the signal going through the current error amplifier as designed, the magnitude of the current open loop $|G_i(s)|=1$ at 4.8KHz. So the design meets the requirement of the compensation and keeps the system stable.

3.2.2 Voltage control loop design for PFC circuit [1]

Voltage control loop is the outer loop, which provides the reference current signal for the inner current control loop, and stable the output DC voltage of the PFC system by modulate the magnitude of the reference current signal. In the study of the voltage control loop, we could ignore the input voltage ripple in one switch cycle because the speed of the outer loop is much slower than the inner loop. And to simplify the analysis, we suppose that inductor current fully tracts the reference current, that is the inner closed current control loop is ideal, and also we suppose the output power is constant and the input average power equals the output average power.

The voltage control loop can be drawn as Fig.3.8, and it includes the voltage error amplifier, the closed current control loop and the boost stage. In the figure below, $G_{VEA}(s)$ represents the transfer function of the voltage error amplifier; the constant 1 represents the inner closed current control loop; and $G_{bst}(s)$ represents the transfer function of the boost stage.

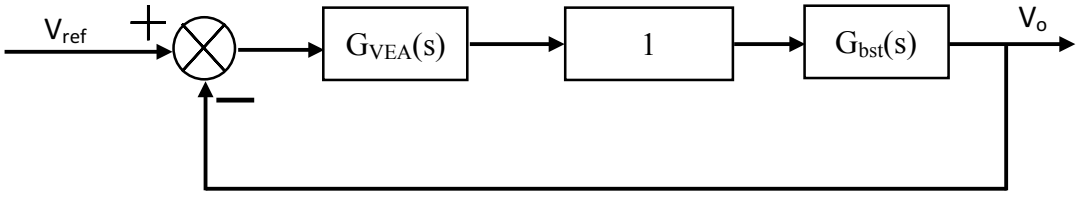


Fig.3.8 Voltage control loop structure

a. Boost stage

The function of the i_{ref} can be write as below [25]:

$$i_{ref} = \frac{K_m \bullet K_{in} \bullet V_v \bullet |v_i|}{V_{ff}^2} = \sqrt{2}\frac{K_m \bullet K_{in} \bullet V_v \bullet V_{i(rms)} \bullet |sin\omega t|}{V_{ff}^2} \quad (3.23)$$

In the function, K_m is the current control loop coefficient and equals to constant 1; K_{in} is the input voltage sampling coefficient and is set 1/80 [23]; $V_{i(rms)}$ is the rms value of the input voltage; V_v is the output signal of the voltage error amplifier; V_{ff} is the feedforward voltage, and the denominator V_{ff}^2 of the equation makes the input power not vary with the change of the input voltage.

And we also have the equation of the inductor current i_L:

$$i_L = \sqrt{2}\frac{K_i \bullet P_i \bullet |sin\omega t|}{V_{i(rms)}} \quad (3.24)$$

K_i is the input current sampling coefficient; P_i is the input average power. And then we have:

$$P_i = P_o = V_o \bullet I_o \quad (3.25)$$

P_o is the output average power; V_o and I_o are the steady state components of the output voltage and current.

Then according to the equations above, we have:

$$V_o \bullet I_o = \frac{K_m \bullet K_{in} \bullet V_v}{K_i} \left(\frac{V_{i(rms)}}{V_{ff}}\right)^2 = K_{bst} \bullet V_v \tag{3.26}$$

$$K_{bst} = \frac{K_m \bullet K_{in}}{K_i} \left(\frac{V_{i(rms)}}{V_{ff}}\right)^2 \tag{3.27}$$

K_{bst} is a constant, and V_o, I_o and V_v are DC operating points of the voltage loop.

Considering the output of the PFC circuit, we have:

$$i_o = \frac{P_o}{u_o} + C\frac{du_o}{dt} \tag{3.28}$$

Because P_o is assumed constant, we solve the equation in small-signal analysis method:

$$\frac{K_{bst} \bullet \tilde{u}_v}{V_o} = C\frac{d\tilde{u}_o}{dt} \tag{3.29}$$

In the equation above, $\tilde{u}_o$ and $\tilde{u}_v$ are small-signal perturbations. So using Laplace transformation we can get the transfer function of the voltage control boost stage:

$$G_{bst}(s) = \frac{\tilde{u}_o}{\tilde{u}_v} = \frac{K_{bst}}{C \bullet V_o \bullet s} \tag{3.30}$$

b. Voltage error amplifier

The input frequency of the system is 60Hz, so the second harmonic output voltage ripple is at 120Hz. In order to restrain the affection of the second harmonic output voltage ripple to the current control loop, the voltage open loop crossover frequency is normally set 1/10 of the second harmonic frequency. So in this design, the crossover frequency is set 12Hz.

And the transfer function of the voltage error amplifier is written as [18]:

$$G_{VEA} = \frac{k_v}{1 + {}^{s}/_{\omega_{cv}}} \tag{3.31}$$

So the open loop transfer function of the voltage loop is:

$$G_v(s) = K_{vs} \bullet G_{VEA}(s) \bullet G_{bst}(s) \tag{3.32}$$

K_{vs} is the output voltage sampling coefficient and is set 1/80 [23].

Also to make the system stable and well responded, the phase margin of the open voltage loop is set 45˚ [25]. Therefore, we can get:

$$|G_v(s)| = |K_{vs} \bullet G_{VEA}(s) \bullet G_{bst}(s)| = 1 \tag{3.33}$$

$$\angle G_v(s) = -180^\circ + 45^\circ \tag{3.34}$$

Then we calculate the parameters of the voltage error amplifier, and get k_v=2.8149 and ω_{cv}=75.4 rad/s. After calculation we also get $K_{bst}=\frac{1/80}{0.02}(\sqrt{2}\pi/4)^2$=4840. And we can write the transfer function of the voltage error amplifier and the voltage control loop:

$$G_{VEA} = \frac{2.8149}{1+{}^{s}/_{75.4}} \tag{3.35}$$

$$G_v(s) = \frac{1}{80} \bullet \frac{k_v}{1+{}^{s}/_{\omega_{cv}}} \bullet \frac{K_{bst}}{C \bullet V_o \bullet s} = \frac{1}{80} \bullet \frac{2.8149}{1+{}^{s}/_{75.4}} \bullet \frac{4840}{2.8\times10^{-3}\times400s} = \frac{1.36\times10^4}{89.6s+1.188s^2} \tag{3.36}$$

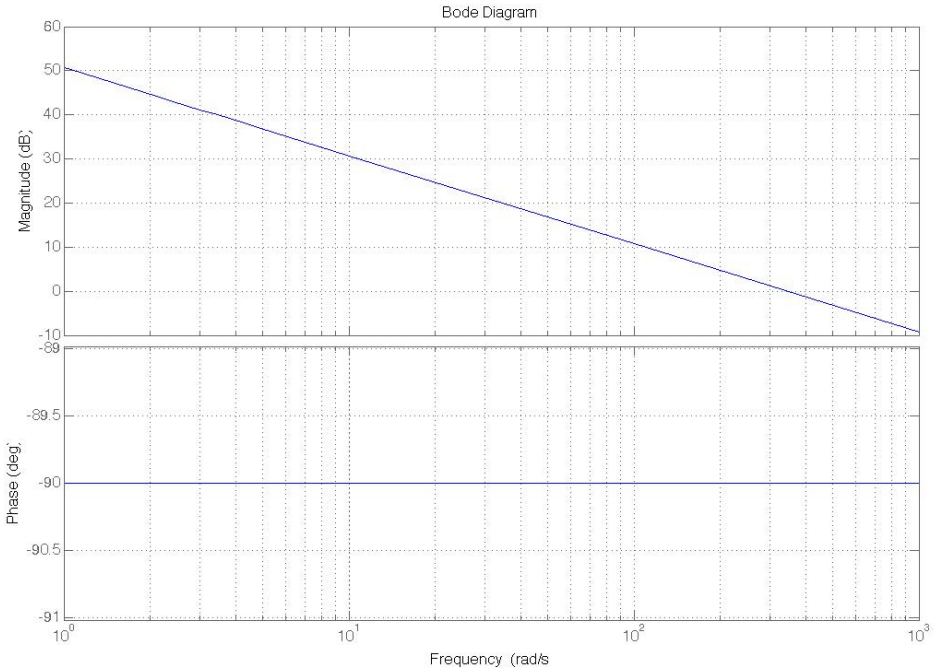


Fig.3.9 Bode diagram of the boost stage

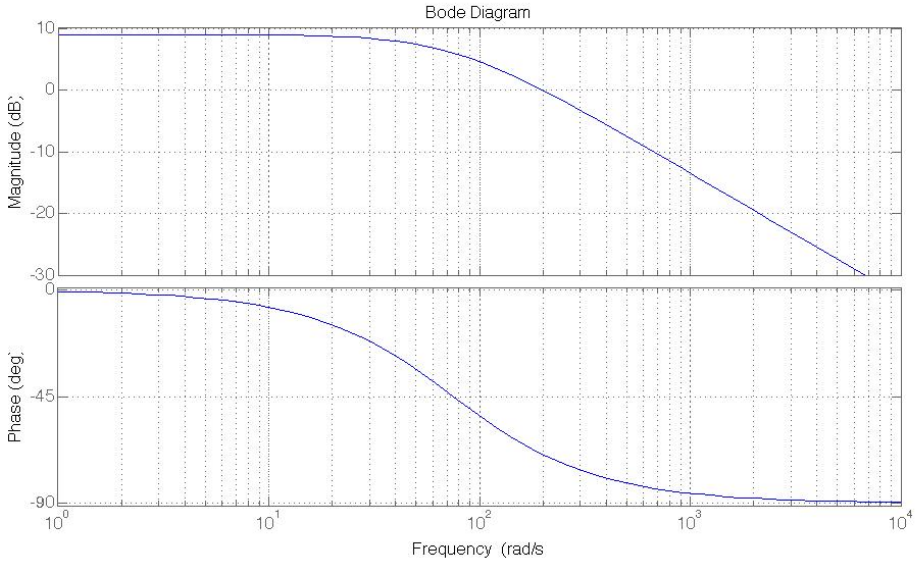


Fig.3.10 Bode diagram of the voltage error amplifier

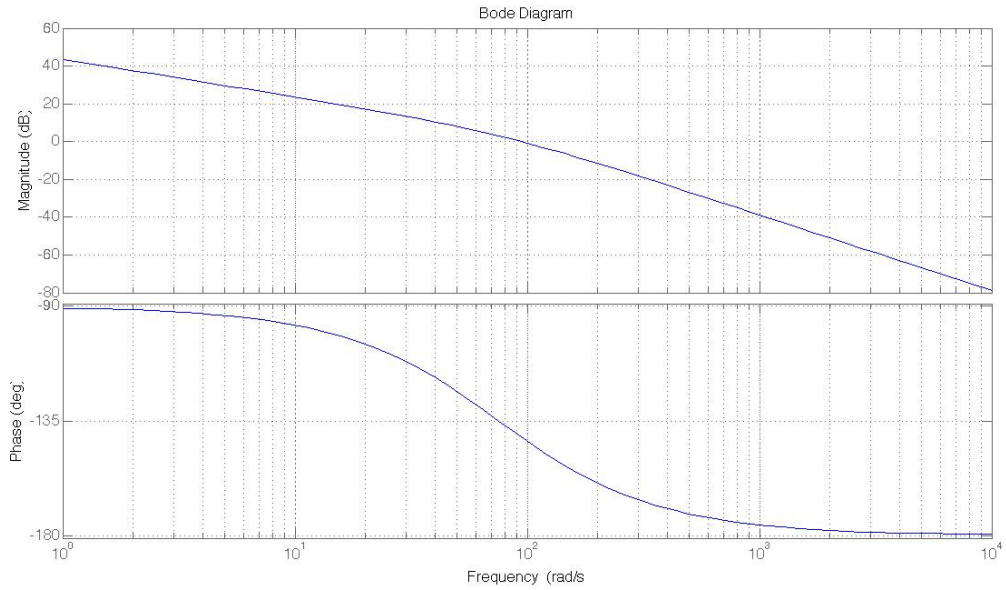


Fig.3.11 Bode diagram of the voltage open loop

According to the simulation results of MATLAB in Fig.3.9-3.11, we can get that when the $|G_{bst}(s)|=1$, the crossover frequency of the boost stage is around 340Hz. So the bandwidth of the voltage loop is too large and needs to be compensated, and it should be improved to around 12Hz. Then taking the designed current error amplifier into the voltage loop, the magnitude of the voltage open loop $|G_v(s)|=1$ at around 13Hz. So the design meets the requirement of the compensation and stabilizes the system.

3.3 System Simulation and Results Analysis

According to the calculations above, I use Simulink to build the circuit and run the simulation. The circuit consists of an internal current loop and an external voltage loop, and the two loops are connected together by a multiplier. There are two input ports of the

multiplier. One is the AC sinusoidal half wave signal, which is the rectified given AC sinusoidal wave signal; the other one is the difference of the output DC bus sampling voltage and the reference voltage, and the difference will go through a first order process and the amplitude will be limited. The output of the multiplier is also an AC sinusoidal half wave signal, whose amplitude is regulated by the output DC bus voltage. The multiplier output works as the reference value of the current loop, and it is compared with the inductor sampling current and outputs the result to the PI controller and get adjusted, and at last PWM drive signal can be generated and control the operation of the MOSFET.

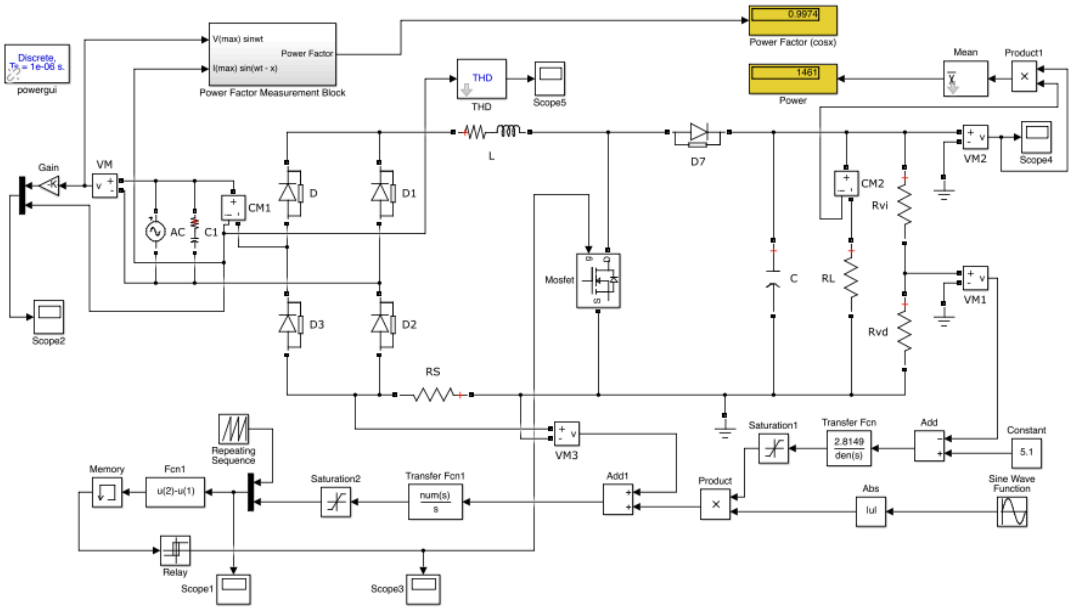


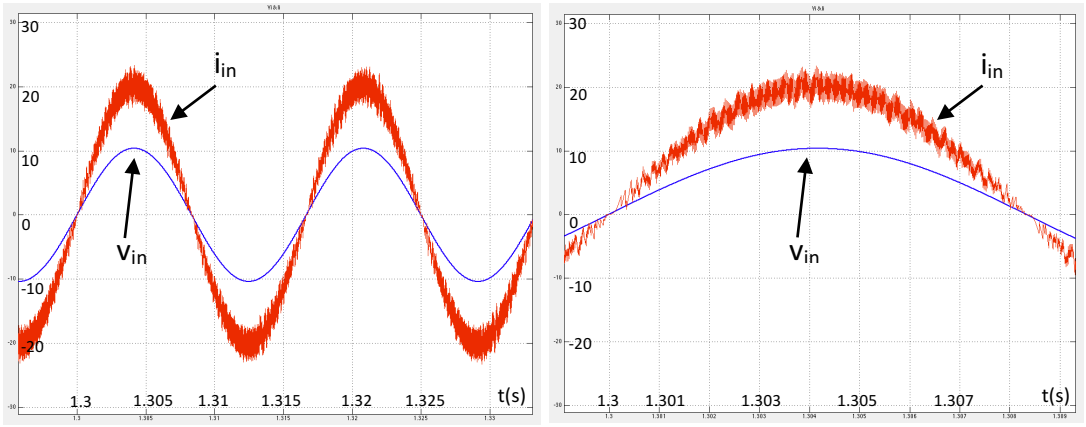
Fig.3.12 APFC simulation mode schematic in Simulink

The parameters applied in the simulation: input AC voltage is 110V/60Hz, the boost inductor L=0.44mH, the output filter capacitor C=2.8mF, and the load resistor R_L=106Ω.

Fig.3.13 shows the contrast diagram of the input AC current and the input AC voltage waveforms. The input voltage signal is scaled by 1/15 so that it is easier to compare. From the figure we can obvious see that the input current waveform is standard sinusoidal waveform and is nearly the same phase with the input voltage waveform. The input current peak value is around 20A, and the current ripple peak-to-peak value is below 5A, which satisfy the design objective.

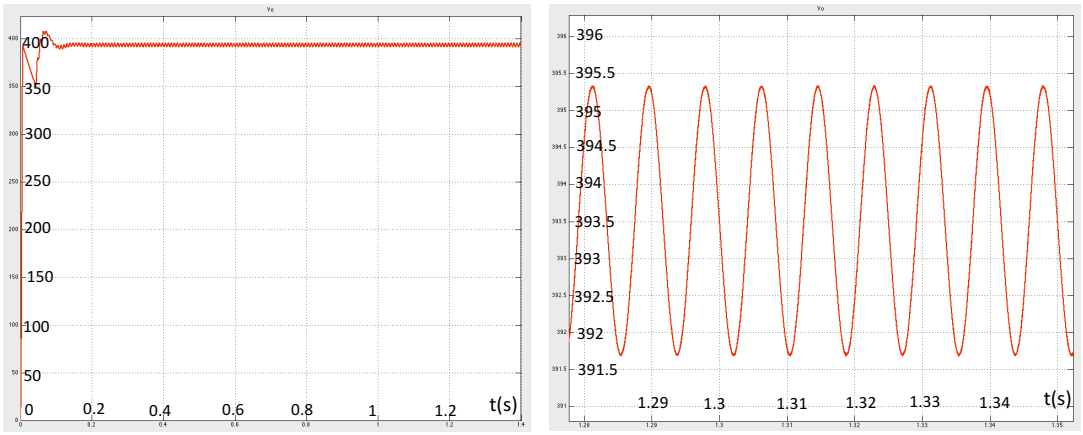
Fig.3.14 shows the output DC voltage waveform. The average value of the output voltage is about 393.5V, and the voltage ripple peak-to-peak value is below 4V, which meets the requirements of the design.

Through the output power calculating component that I designed in the Simulink, it is shown that the output power is 1461W, which is very close to the design goal. And through the power factor calculating component that I designed in the Simulink, the power factor is shown as 99.74%, which means the PFC circuit greatly improves the power factor of the boost circuit. The frequency spectrum diagram is shown in Fig.3.15, and the THD of the input current is 7.05%, which is largely reduced.



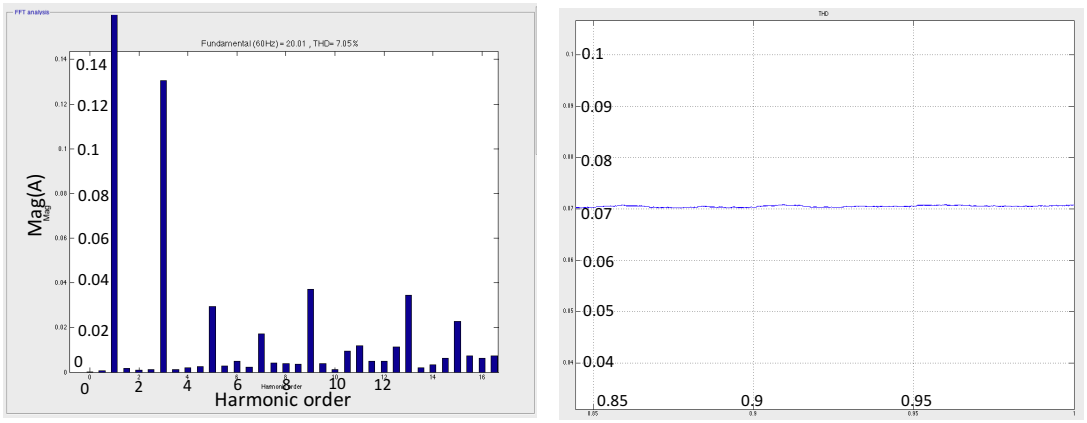
(a) (b)

Fig.3.13 Input current and input voltage waves



(a) (b)

Fig.3.14 Output DC voltage wave



(a) (b)

Fig.3.15 Diagram of the input current (a) frequency spectrum, (b) THD

Fig.3.16-3.19 shows the input voltage and input current waveforms and frequency spectrum of a group of different input voltage. Through the figures we can see that the input current waveforms are standard sinusoidal waveforms and are strictly the same phase with the input voltage waves.

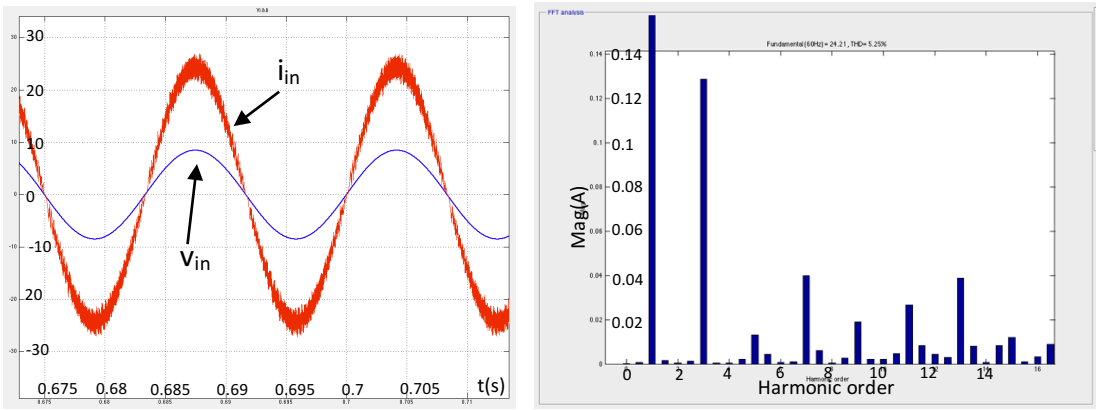


Fig.3.16 When the input voltage is 90V, the diagram of (a) the input voltage and current (b) frequency spectrum

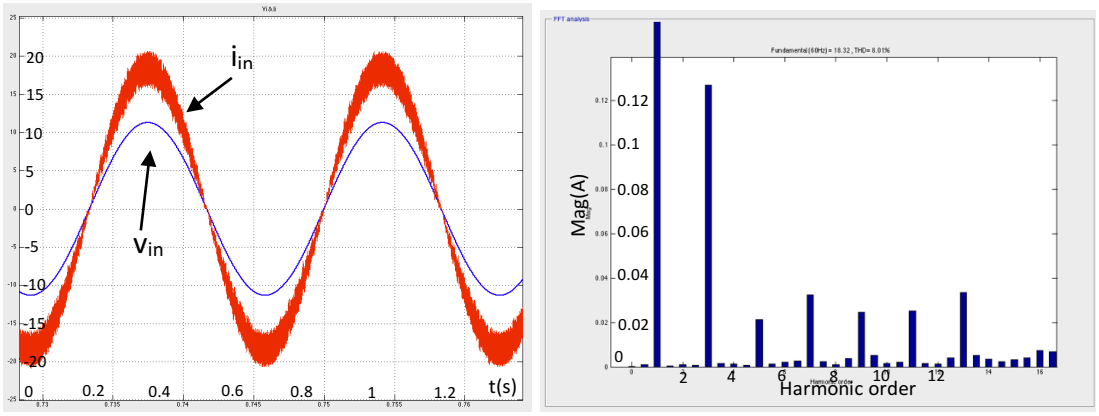


Fig.3.17 When the input voltage is 120V, the diagram of (a) the input voltage and current (b) frequency spectrum

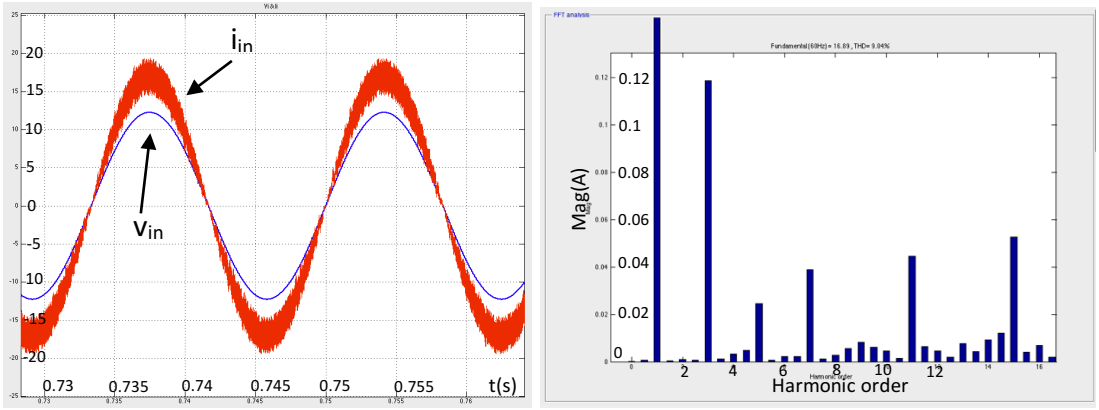


Fig.3.18 When the input voltage is 130V, the diagram of (a) the input voltage and current (b) frequency spectrum

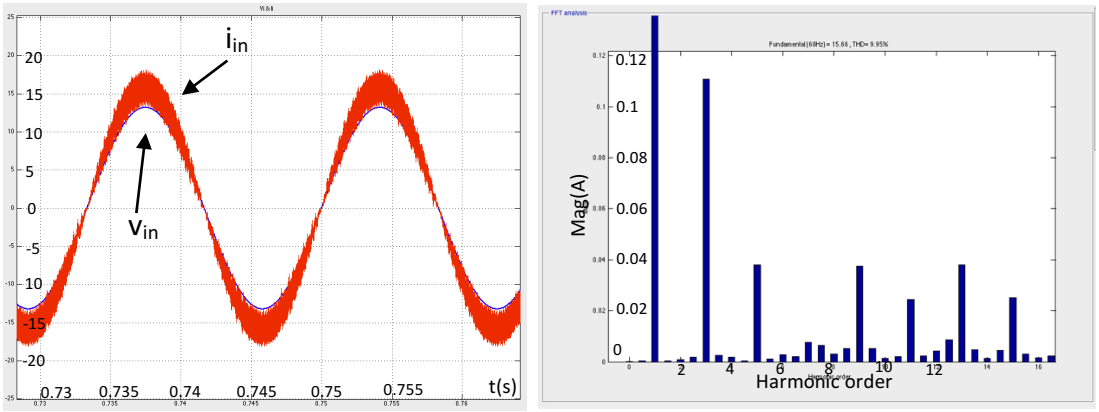


Fig.3.19 When the input voltage is 140V, the diagram of (a) the input voltage and current (b) frequency spectrum

Table 3.1-3.4 shows the output DC voltage, PF value and harmonic currents in the range of AC input voltage at 1500W as well as in 110VAC input voltage at different input power. We can see that when the input power is too small (below 1kW), the THD is too large and the system is not working in the perfect status. And in other conditions, the magnitude of the harmonic currents satisfies the requirement. And the result of the power factor correction is pretty good.

Table 3.1: Output DC voltage and PF value in the range of AC input voltage at 1500W

Input voltage (V)	Input current (A)	Output DC voltage (V)	Power Factor (%)	Input power (W)
90	17.38	393.5	99.66	1460

110	14.15	393.5	99.74	1461
120	12.96	393.6	99.67	1462
130	11.94	393.5	99.58	1461
140	11.08	393.5	99.48	1461

Table 3.2: Odd harmonic current values in the range of AC input voltage at 1500W

Input current (A)	3^{rd} harmonic component (A)	5^{th} harmonic component (A)	7^{th} harmonic component (A)	9^{th} harmonic component (A)	THD (%)
17.38	0.13	0.01	0.04	0.02	5.25
14.15	0.13	0.03	0.02	0.04	7.05
12.96	0.13	0.02	0.03	0.02	8.01
11.94	0.12	0.02	0.04	0.01	9.04
11.08	0.11	0.04	0.01	0.04	9.95

Table 3.3: Output DC voltage and PF value in 110VAC input voltage at different input power

Input voltage (V)	Input current (A)	Output DC voltage (V)	Power Factor (%)	Input power (W)
110	5.21	402	98.13	506.71
110	7.04	400.7	98.96	702.8
110	9.72	398	99.46	990.03
110	14.15	393.5	99.74	1461
110	16.6	391	99.81	1720
110	18.25	389.2	99.84	1895
110	22.29	385.3	99.89	2318
110	26.19	381.2	99.92	2725

Table 3.4: Odd harmonic current values in 110VAC input voltage at different input power

Input current (A)	3rd harmonic component (A)	5th harmonic component (A)	7th harmonic component (A)	9th harmonic component (A)	THD (%)
5.21	0.07	0.04	0.03	0.04	19.33
7.04	0.07	0.03	0.02	0.03	14.30
9.72	0.1	0.03	0.02	0.03	10.28
14.15	0.13	0.03	0.02	0.04	7.05
16.6	0.15	0.03	0.02	0.04	6.00
18.25	0.17	0.04	0.02	0.04	5.45
22.29	0.2	0.03	0.02	0.05	4.49
26.19	0.23	0.04	0.02	0.05	3.88

3.4 Summary

The boost PFC circuit can work properly for the first level charging of electric vehicle. It can operate in a range of input voltage and input power. And it achieves the shaping of the input current waveform and stabilizing the output voltage. The input voltage range is 85-140 VAC, the input power range is 1-3kW, the power factor stays more than 99%, and THD stays below 10%.

Conclusion

The power factor and harmonic pollution influence to the grid from the power electronic devices is an increasingly prominent problem. For the research and design of power electronic devices, it has been more and more focused on the whole operation characteristics of the system other than only considering the output characteristics of the system. To build the PFC circuit in EV charging system, not only we need to consider the output voltage, current features and adaptability to load, but also we should take into account the input features to reduce adverse effects.

In my design, the PFC circuit is applied in EV first level two-stage charging system, which is mostly operated in the common house hold circuit. Therefore, I set the rated output power 1.5kW, output DC voltage around 400V, frequency 60±1Hz. And also I set AC input voltage range 85-140VAC, and the available output power range around 1-3kW. First I calculated and designed the main circuit of the PFC system, which will meet the requirements of the input and output voltage as well as output power. After that I successively designed the inner current control loop and the outer voltage control loop. To complete the design of the dual-loop controller, I calculated the transfer functions of each loop and discussed the magnitude of the open loop transfer function and the phase margin of each loop. Then, I run the complete system in Simulink and got figures and data of some signals and do the comparison and analysis. Finally, through the research of the results of the simulation, I verified that this PFC system works in the specified conditions properly. In the results, we can see that under the first level charging

specifications, the PFC system will offer more than 99% PF for the circuit, and reduce the THD to less than 10%. It totally achieves the goal of rectifying, high input power factor, boosting voltage, stabilizing the output voltage and small ripples. Therefore, this design could be applied in the EV first level charging.

Still, there are things to be improved. Adding soft switch technology will do good to this PFC system, which can make it a very simple, efficient, high efficiency, high reliability way to achieve the transformation of electrical energy.

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