Project Number: EXC 0801

# INTERFACE BOARD DESIGN FOR PHASED ARRAY RADAR FRONT-END HARDWARE

A Major Qualifying Project Report:

submitted to the Faculty

of the


WORCESTER POLYTECHNIC INSTITUTE

in partial fulfillment of the requirements for the

Degree of Bachelor of Science

by

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Date: October 16, 2008

Approved by:

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# Abstract

The Multifunction Phased Array Radar (MPAR) project at Lincoln Laboratory is currently in its pre-prototype hardware design phase. Delivery of the first radar panel is expected in spring 2009 and therefore methods of testing the panel functionality are now being developed. A FPGA based evaluation board will be controlled with LabVIEW software to test this front end hardware of the radar. However, the output specifications of the FPGA do not match the input specifications of the radar panel, and the need for an interface becomes apparent. The focus of this project was to develop an interface board which facilitates the communication of digital signals between the FPGA and the radar panel. The interface board developed in this project has the responsibility of terminating and level shifting the digital signals at the input, buffering each of the outputs, and fanning-out a number of the digital signals.

To test the functionality of the design, a Printed Circuit Board (PCB) was developed from the design schematics. Hardware tests on this PCB showed that the interface board was successful at level shifting and fell within the differential propagation time constraints. However, the tests also concluded that there exists too much ringing on the output waveforms for the signals to be usable under MPAR. Suggestions are provided to correct this issue.

Speculating into the future of the MPAR project, the panel testing system will be replaced with a FPGA control by the phased array radars main computer. The integration of this FPGA onto the interface board has been a topic of discussion. A system level diagram has been presented showing the essential components required to amalgamate the FGPA and interface designs.

## Statement of Authorship

This project was completed by Boris Svirchuk and Calvin Goodrich of the WPI class of 2009.

Coming into Lincoln Laboratory, a project had not yet been finalized to begin working. Until a project was found, Boris and Calvin both took the responsibility of writing the project's background and introduction sections. However, as the project unfolded, Calvin took the bulk of the responsibility of writing and editing the report, while Boris took the bulk of the responsibility of developing the schematics, and ultimately bringing the PCB to realization. Every technical decision made in the project was discussed and approved by both partners.

Boris and Calvin each contributed to the population of the PCB, learning new techniques to solder surface mount ICs. Boris brought the PCB into Lincoln Laboratory to run tests, providing Calvin with a plethora of oscilloscope images needed to complete the rest of the sections of the report. Near the end of the project timeline, Boris and Calvin each contributed to the final presentation.

Both partners have evaluated their contributions to this project and feel that each partner played near an equal role in completing this project.

## Acknowledgments

We would like to extend our gratitude to our MIT Lincoln Laboratory Group 105 advisors Sean Duffy and Sean Tobin, as well as our WPI advisor Edward Clancy for their support and guidance which has made the completion of this project possible.

Appreciation is extended to Group 43 leader Mark Weber and Groups 43 advisors John Cho, Robert Frankel and William Pughe for finding us a remarkable project, expressing interest, and providing assistance throughout our entire time working in MIT Lincoln Laboratory.

A thank you is also extended to Patrick Morison, of the WPI-ECE Shop, for his help with populating the PCB, minimizing the time spent assembling the PCB and all of the surface mount ICs.

Finally, we would like to thank MIT Lincoln Laboratory for providing us this incredible opportunity by allowing us to work on its premises, and permitting us to use the MIT Lincoln Laboratory equipment.

# Executive Summary

## *Introduction*

Lincoln Laboratory, affiliated with Massachusetts Institute of Technology, has been involved with the Federal Aviation Administration on a project intending to replace multiple currently used civilian radar systems with a single network of next generation phased array radars. The project, named Multifunction Phased Array Radar or MPAR, highlights the advantages of phased array technology over dish antenna technology, and its ability to perform multiple radar functions simultaneously. The project is currently in its pre-prototyping hardware design phase with preliminary hardware deliveries planned for spring 2009.

Phased array radar is made up of multiple faces comprised of many Transmit/Receive (T/R) modules, each of which is a directive antenna. The MPAR project predicts the use of around twenty-thousand T/R modules per face. Each face will be assembled from panels of sixty-four T/R modules. To test the functionality of the radar array, an FPGA based test system is being developed to test the sixty-four T/R module panel. Due to manufacturing limitations of the T/R modules, an interface board is required to appropriately translate and route control and data signals from the test-bed FPGA and potentially any upstream hardware to the radar panel. The design of the interface board is the project discussed in this report.

The interface board will be implemented for use with a single radar panel, however to design and test the interface board a second design was implemented for a single T/R module. This approach shows the scalable modularity of phased array, as proving the interface board concept for a single T/R module, the module design, would prove the concept for the radar panel, the panel design, as well. To prove the concept of the single T/R module interface board design, the schematic design was developed into a PCB and tested under various conditions.

## *Hardware Design*

The specifications for the radar panel are not explicitly known, as the overall radar design is still evolving. However, requirements were provided to begin the design process. The interface board will accept multiple 20MHz digital signals (data and control lines) from the output of the upstream FPGA over a cable, which needs to be terminated. These digital TTL logic based signal need to be level shifted on the interface board to comply with the digital voltage levels of the T/R modules. Also, each control signal needs to be fanned-out to eight individual lines and all of the signals require the use of a buffer to provide current to be able to drive the output through another cable. The last requirement was a differential propagation time of 50ns through the various paths of the interface board.

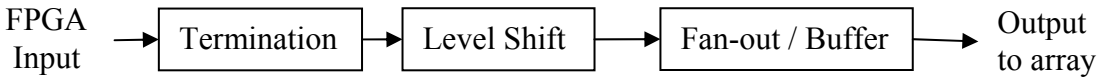


**Figure 1: The Approach to the Design of the Interface Board.**

The design was broken down into three separate functional blocks; the first of which is termination. The length of the cable connecting the FPGA to the interface board was projected at being somewhere between one and three meters in length. To prevent reflections in the cable, which ultimately degrade signal quality, a Thevenin termination was included on the interface board to match the cable's characteristic impedance of $90\,\Omega$. The two resistor approach, accounting for real impedance only, was realized with network resistors to save space on the PCB; each input requires a pair of the resistors. The network resistor values selected for termination are $R_1 = 220\Omega$ and $R_2 = 150\Omega$.

The T/R modules utilize shifted digital logic voltage levels. The FPGA outputs digital signals at 0V and +5V, logical 0 and 1 respectively. The T/R modules utilize -5V and 0V. To

translate the voltage levels, a quad-channel level shifting IC was selected. Designated SWD-119, this surface mount device is efficient at providing the required functionality; however, it fails at providing enough current at its output, requiring the use of buffers at the next functional block.

The panel design requires that each of its input control lines be fanned-out to eight individual lines on the output. The current needed to drive each signal to the T/R module was not explicitly specified during the design, but rather a broad range of 5mA -25mA; therefore an octal buffer with a high output current drive was selected. The SN74ABT244A octal buffer provides 64mA and -32mA, during low and high states respectively. Using the octal buffer provides an efficient way to fan-out the control lines, while keeping the layout of the design simple.

## *Hardware Realization and Testing*

Multisim was used to develop the schematic deliverables. The schematic, for the single T/R module design, was imported into Ultiboard to create a PCB layout, which can be observed as a 3-D model in Figure 2. Tests included variable input frequencies, two separate output locations from the PCB, variable output cable lengths, and evaluation sof differential propagation delay output cable termination.

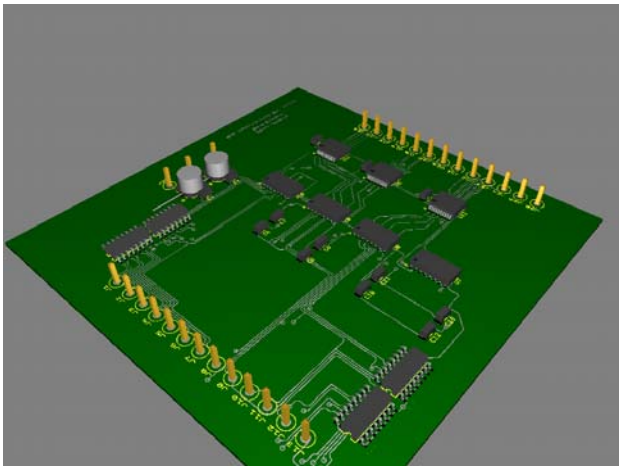

**Figure 2: 3-D Representation of the Module PCB Design**

## *Results*

Schematics for both the module and panel design were developed. The testing produced a number of images taken directly from the oscilloscope showing the behavior of the output waveform under a variety of different configurations. From these oscilloscope images, conclusions were drawn about the interface board module design.

## *Discussion*

From the oscilloscope images, the level shifting functionality of the SWD-119 IC was proved valid. However the output of the IC shows an unexpected inversion. The IC which was provided is a new revision of the SWD-119, which exhibits an inverted behavior from the truth table in the current SWD-119 datasheet. Also, the differential propagation delay, seen on the output of multiple traces, was far within specification.

The output of the interface board, a 20MHz square wave driving a three meter terminated cable, proves that the design of the interface board needs to be improved to be a valid design for MPAR. The output of a 1MHz signal through the interface board shows a ringing of 200ns in duration and 1V in amplitude. This ringing is the main cause for severe distortion of the 20MHz output signal.

Four methods have been proposed as revisions to the interface design, which would help reduce the output ringing. The first involves redesigning the PCB, using shorter traces and wider traces could improve signal integrity. The second considers the termination of the output signal, suggesting the use of different techniques to account for complex impedances. The third proposed method was researching into a better IC buffer, which may help reduce the output ringing directly, as the output of the SWD-119 IC shows. Finally, minimizing output cable length and quality would greatly increase signal integrity.

### *Future Development*

The FPGA based test-bed will remain in place of the beam steering subsystem during all preliminary hardware tests. However, looking into the future, the beam steering subsystem will be comprised of a FPGA as well. A system level investigation into the necessary steps needed to integrate the FPGA onto the interface board was completed.

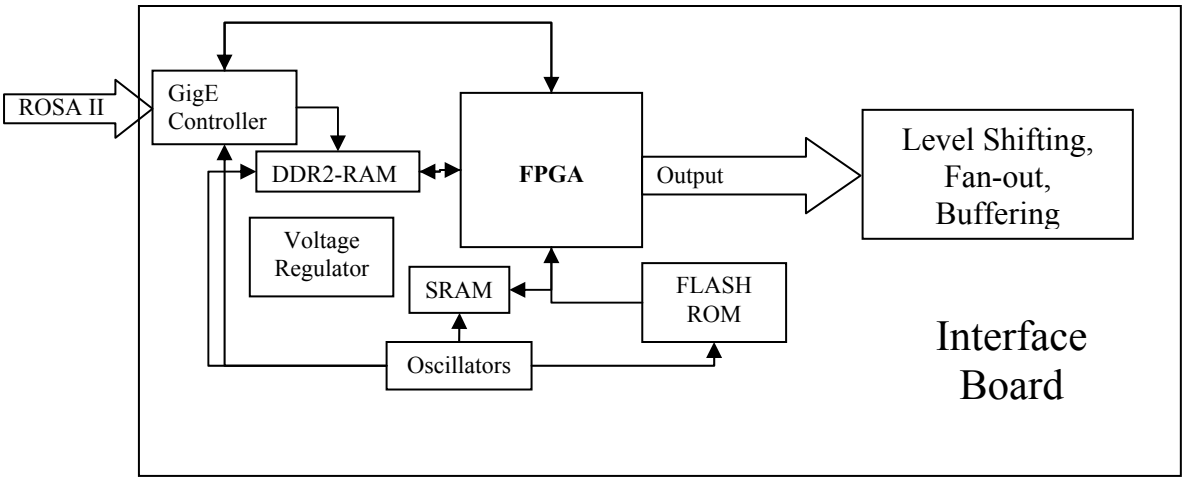


**Figure 3: System Level Block Diagram of the Necessary Components to Isolate a FPGA**
**The block diagram above shows all necessary components for FPGA operation specified by the MPAR project. The interactions of the components are designated by arrows.**

This exercise required the extraction of information from various source including presentation slides, datasheets and even other Lincoln Laboratory staff. As it turns out, another group at Lincoln Laboratory has already taken the steps required to develop a FPGA based system, and offers a semi-customizable hardware solution utilizing the barebones essentials needed to operate the FPGA. The effort of researching into the required essentials to operate an FPGA yielded a system level block diagram of the necessary components, shown in Figure 3. In conclusion, to integrate the FPGA onto the interface board would require only a handful of extra components and would greatly reduce the amount of overhead hardware.

# Table of Contents

# 1.0 – Introduction

In the past few years at Lincoln Laboratory, a research laboratory affiliated with the Massachusetts Institute of Technology, there has been a Federal Aviation Administration (FAA) sponsored project known as Multifunction Phased Array Radar (MPAR). This project highlights developing a new radar platform using phased array technology to perform multiple existing radar functions such as the monitoring of aircraft traffic and weather sensing. The idea is to replace the aging civilian radar networks currently deployed around the country with a single state-of-the-art network.

In the past, phased array radars have been too expensive for civilian use and therefore have only been used in military applications. For the MPAR to be an economically feasible alternative, it must be built at a dramatically lower cost than today's military phased array systems. Work completed at Lincoln Laboratory shows that this may indeed be possible. The MPAR project is currently in its pre-prototype hardware design phase with a delivery of the RF front end panel planned for spring 2009.

Our project targets preliminary development of the communication to the front end hardware of the radar array, the Transmit/Receive (T/R) module. The MPAR will utilize 20,000 T/R modules in an array, all of which will be controlled by a beam steering subsystem. Due to manufacturing limitations, the radar array utilizes different hardware logic voltages than the upstream hardware. Our project is to design an interface board, placed directly between the subsystem and the radar array, see Figure 4, which will translate and fan-out control signals sent by the beam steering subsystem.

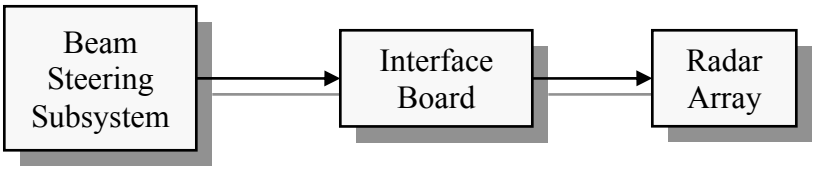


**Figure 4: Block Diagram of Where the Interface Board is Physically Located**
**The interface board in this design will be situated between the beam steering subsystem and the front-end of the radar hardware.**

In early hardware tests the prototyping array will utilize only 64 T/R modules and a National Instruments (NI) PXI-7851R Multifunction DAQ, which employs a Xilinx Virtex-5 LX30 FPGA, will take the place of the beam steering subsystem. The FPGA will be controlled with LabVIEW and will connect to the interface board using standardized VHDCI connectors. The interface board being developed in this project will, at first, be used for testing of the 64 T/R module array.

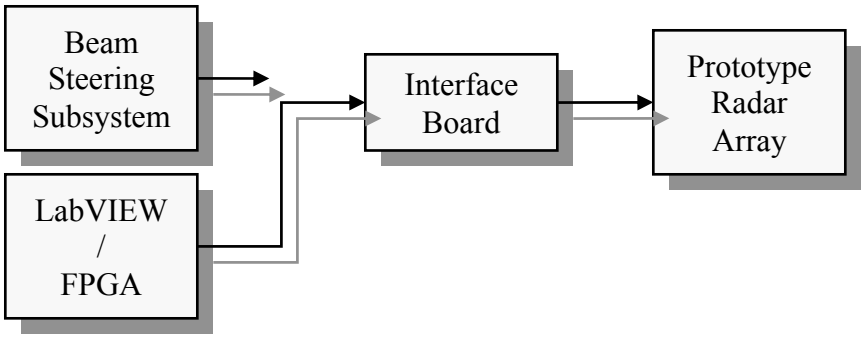


**Figure 5: Early Testing Setup**
**During the early prototyping stages, the beam steering subsystem is replaced with a NI PXI-7851R Virtex-5 LX30 FPGA which will be control using LabVIEW software.**

The interface board will have a large number of inputs and outputs to be able to control each of the 64 T/R modules independently. To design the interface board within the nine weeks of allotted time, the design and testing of a hardware interface board developed for an individual T/R module will be completed first. Once it is found that the design is effective and it resolves all communication problems, a design will be developed which will encompass all I/Os.

After the prototyping array's functionality is verified, the beam steering subsystem will replace LabVIEW and the PXI-7851R, the testing hardware. The beam steering subsystem has been determined to be kept a FPGA based system; however Lincoln Laboratory wants to reduce the amount of overhead hardware needed to use the FPGA. Therefore, the FPGA will be integrated onto the interface board. A system level block diagram has been developed to show the essential components needed to utilize the Xilinx Virtex-5 LX30 FPGA on the interface board.

There are four goals which have been agreed upon to be deliverables by the end of the project. The first is a schematic design of the interface board for a single T/R module. The second is a hardware interface board developed by the schematics of the single T/R module design; accompanying the hardware will be test data which evaluates the functionality of the design. The third is a schematic design of the interface board which will be used to control the 64 T/R modules of the prototype radar array. The last deliverable is a system level block diagram presenting the essential hardware component s needed to integrate the FPGA onto the interface board in design. This design will be used by Lincoln Laboratory to test preliminary radar hardware.

# 2.0 – Background / Literature Review

## *2.1 – History*

Knowledge about the electromagnetic spectrum was extremely limited before the late 1800's. Heinrich Hertz, a German physicist, between 1886 and 1890 pioneered research in the field of electromagnetism and was the first person to demonstrate the generation and detection of radio waves. Hertz continued his scientific research in the UHF and VHF portions of the spectrum, never pursuing possible applications of his work [Bryant, 1994, p.1]. However, Hertz's research did inspire others to develop uses for the electromagnetic spectrum early on, such as wireless telegraphy, diathermy, radio communications and broadcasting, and radio direction finding [Bryant, 1994, p.3].

The first individual to submit a patent describing a radar-type device was a German engineer named Christian Hulsmeyer. The patent was submitted to the British patent office June 10, 1904 and was titled, "Hertzian-wave projecting and receiving apparatus adapted to indicate or give warning of the presence of a metallic body, such as a ship or train, in the line of such waves [Burns, 1988, p.2]." The research for this device, performed in Dussledorf, Germany, led to a less than ideal product; however, it was able to detect targets at roughly 3000m. [Burns, 1988, p.6]

The development of radar was quite during the early 1900's. It wasn't until the 1930's, when political stress began mounting in Europe, that the need for radar became more apparent. The Committee for the Scientific Study of Air Defense was formed in Great Britain in 1934 and the National Defense Research Committee (NDRC), later to be renamed the Office of Scientific Research and Development (OSRD), was formed in the United States in 1940 to consider how scientific and technological advances could be used to change warfare. By the mid 1930's the

development of basic radar was already in progress by several countries; of these countries, the United States, the United Kingdom, and Germany had major technological and operational impact. [Bryant, 1994, p.3]

In the early 1930's, the United States was underfunded for radar research, as there was a lack of communication within the higher levels of government. However, during the mid-1930's research had begun on developing pulsed radar, where pulses of electromagnetic energy are transmitted and received. This research took place at two separate facilities in the United States, the Naval Research Laboratory (NRL) in Washington, D.C. and in Signal Corps' laboratory in Fort Monmouth, New Jersey [Bryant, 1994, p.5]. In the second half of the decade, United States research provided three technological developments which extended the usable portion of the electromagnetic spectrum; these were, "…the resonant cavity circuit, the klystron electron tube, and coaxial and waveguide transmission lines and components" [Bryant, 1994, p.4].

During 1940, Great Britain required more engineering and manufacturing resources to effectively further the research and development of their radar program. [Bryant 7].Therefore, the British Scientific Mission to the United States and Canada was developed and held. During this conference, Great Britain transplanted their radar development program to the United States. Schematics, equipment, operation manuals, and new research results were brought over by Great Britain in hopes of the Unites States and Canada helping with their war effort. In direct response to this conference, the Massachusetts Institute of Technology (MIT) Radiation Laboratory was created to help further the advancement of radar. [Bryant 9]

By mid-1940, American industries were converting and expanding to supply Great Britain with wartime supplies. Radar had evolved into many applications during WWII such as, "…waning, gun laying, airborne interception (AI), ground control of intercept (GCI), air to

surface vessel (ASV), ground control of approach (GCA), blind bombing, navigation, fire-control, and weather monitoring" [Bryant 9].When WWII ended, there was a buildup of wartime resources; an oversized labor force, reinforced with strong industrial resources, was met with a large demand for new consumer products and commercial exploitations of the new technologies. These factors marked the beginning of many civilian based radar applications. [Bryant 13]

In the U.S., the OSRD shut down and closed its laboratories, and most of its scientists returned to universities. There was major funding to these universities which led to the U.S. becoming the leader in scientific research. The abundant funding led to the founding of laboratories patterned after the MIT Radiation Laboratory, which include Lincoln Labs, labs at Columbia, Caltech, and the Universities of Michigan and Illinois. [Bryant, 1994, p.13]

During the 1950's, radar experienced a complete overhaul. A second generation of radar was in development, employing new technologies made possible by the engineering and scientific advances of the previous decade. These new technologies, including the transistor, digital computer and advances in circuit manufacturing, led to lighter, smaller and more energy efficient electronics. [Bryant 14]

Radar can be categorized into three generations. The first generation was limited to obtaining information about its target's position. Range was found by measuring the time of travel for a transmitted pulse, and direction was determined from the angular direction of the antenna. The second generation of radars, the types developed in the 1950's, utilize both signal amplitude and phase of the received pulses to increase resolution while maintaining moderate pulse length and peak transmitted power. These analog radar systems can locate remote objects, and detect and measure motion, allowing the tracking of objects and the ability to distinguish

targets from severe background clutter, the reflections of nearby trees and buildings which can falsify readings. [Bryant 15]

The third generation of radar systems came about during the 1960's when analog systems began evolving toward digital systems. Upgrading to digital systems meant reduced costs and maintenance. Digital systems also provided, "Mathematical enhancement of weak or cluttered signals [enabling] better detection and tracking abilities" [Bryant, 17].

## *2.2 – Current Types of Radar*

The current civilian radar systems in place around the country are diverse. There are primarily four types of radar systems, each with their own function. Working together, these systems provide information about weather and aircraft across the entire country.

| Radar Type | Primary Function | Model Names | Number in Use |
|---|---|---|---|
| NEXRAD | National Weather | WSR-88D | 156 |
| TWDR | Terminal Weather | TDWR | 45 |
| ARSR | National Aircraft Surveillance | ARSR-4, ARSR-1, ARSR-2 | 101 |
| ASR | Terminal Aircraft Surveillance | ASR-9, ASR-11 | 233 |

**Table 1: Currently Used Civilian Radar Systems**
**There are currently four types of civilian radar in use around the country. Next-Generation Weather Radar or NEXRAD is used for national scale weather surveillance, assisting the Terminal Doppler Weather Radar (TDWR) which monitors weather in and around airport terminal areas. The Air Route Surveillance Radar (ARSR) provides national scale aircraft surveillance, assisting the Airport Surveillance Radar (ASR) which monitors approaching aircraft near airports.**

Next-Generation Weather Radar (NEXRAD), or the WSR-88D, was designed in the 1980's by Unisys Corp, under the direction of the National Severe Storms Laboratory [Weber et al 2007]. This weather sensing system was designed for use by the National Weather Service (NWS), the Department of Defense (DoD), and the Federal Aviation Administration (FAA) for general meteorological use. NEXRAD was considered a significant upgrade to the WSR-57 and WSR-74 radars it replaced which provided limited information about the weather [Rinehart 184]. With 156 systems spread out in a gridded fashion around the country today, NEXRAD boast impressive nationwide coverage and is accessible by, "… essentially all operational weather personnel dealing with public and aviation weather services [Weber et al 2007]."

Terminal Doppler Weather Radar (TDWR) was developed as a supplemental system for sensing weather in the vicinity of airport terminals. The FAA realized the need for this additional

radar system after numerous aircraft accidents occurred in airport terminal areas in the late 1980's. TDWR was manufactured by Raytheon under strict specifications from the FAA, Lincoln Laboratory and the National Center for Atmospheric Research [Weber et al 2007]. There are many benefits to using TDWR around airports. The radar employs advanced filtering algorithms which significantly reduce ground clutter, providing more accurate forecasting and current weather information. TDWR also recognizes microbursts, invisible strong gusts of wind which make taking off and landing dangerous [Rinehart p.185-186]. After deployment in 1993, TDWR became popular among major airport terminals. Currently there are forty-five in use by Air Traffic Control (ATC) around the country.

Air Route Surveillance Radar (ARSR), most currently the ARSR-4, provides national-scale aircraft surveillance. The coverage is accomplished with a grid of 101 ARSR located around the country. The ARSR-1 and ARSR-2, which are currently in use, date back to the 1960s and require constant maintenance. The Department of Defense (DoD) and Department of Homeland Security (DHS) recently assumed control of updating these systems to the ARSR-4.

Airport Surveillance Radar (ASR), currently with models ASR-9 and ASR-11, are located at 233 different airports. ASR provides ATC with information about approaching aircraft, allowing ATC to appropriately schedule landings and takeoffs. Thirty-four of the ASR-9 systems across the country also assist in weather forecasting and provide information about wind shear and near-future storm locations. These systems are remotely operated by the United States Government, providing the information to ATC for the above stated purposes.

## *2.3 – How Radar Works*

Radar, as it exists today, is divided between two physical designs; dish radar and phased array radar. In this section, information about how both of these systems work will be presented so as to provide a background of current and future radar technologies.

### 2.3.1 – Radar as a System

Figure 6 below shows the basic idea of how radar operates. The antenna propagates electromagnetic energy in the form of pulses out from the reflector in a beam pattern. These waves propagate through the atmosphere indefinitely. Most of the energy is scattered by atmospheric impurities, however a very small amount is reflected directly back to the antenna from the target of interest, weather or aircraft. These echoes relay information about target size, location, speed, direction, and in some cases advanced images of the aircraft. Primary radar systems operate as mentioned above, without an active response from the target. Secondary radar systems also exist; requiring the target to respond to a radar pulse using a transponder. The transponder facilitates the radar in detecting the target by increasing effective detection range. The transponder replies with its own coded electromagnetic pulses, providing more energy at the radar than would be received by an echo. The MPAR project deals with primary radar only.

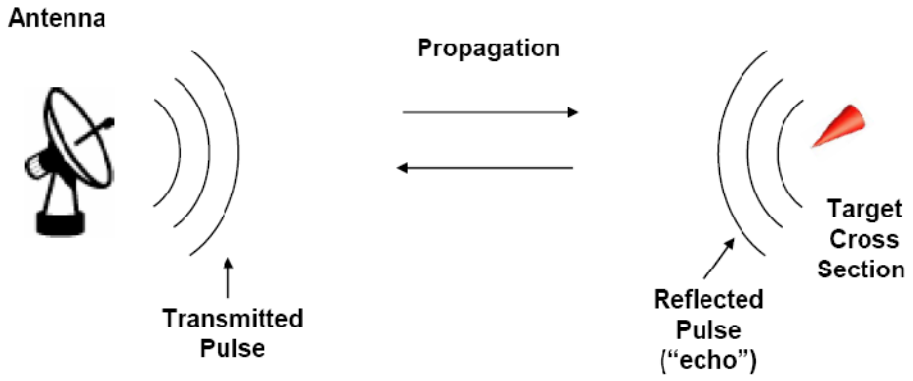


**Figure 6: How Radar Works [Noiseux, 2006]**

### 2.3.2 – Dish Radar

Dish radar is composed of a transmitter, an antenna, a Transmit/Receive switch, receiver, a signal processor, main computer and a display. The following paragraphs will explain each of these components in detail. Figure 7 is a simplified block diagram of a basic dish radar system.

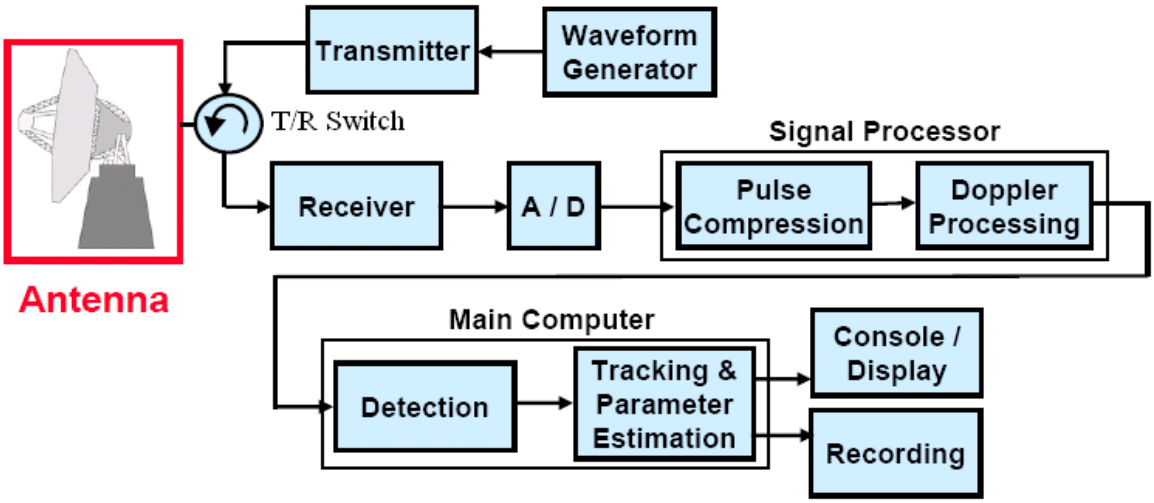


**Figure 7: Radar Subsystems**
**There are many subsystems which give dish, and phased array, radar their functionality, although the only piece which can be seen is usually the antenna. [Noiseux, 2006]**

On the transmission side of the radar system there is a waveform generator and a transmitter. The waveform generator is used to create the pulses which will be sent out from the radar, but at a much lower power level. It is the transmitter which amplifies these pulses, providing the energy needed to propagate the pulses through the atmosphere. The transmitter is the source of electromagnetic radiation radiated by the radar. Over the course of radar's history, several kinds have been developed. The most notable are the magnetron, the Klystron and solid-state transmitters [Rinehart 12].

The antenna includes the reflector, or dish, and feedhorn. The electromagnetic energy is fed from the feedhorn into the reflector. The reflector is used to direct the propagation of the electromagnetic energy from the radar, in the form of a beam, into the desired location in the sky.

A dish antenna requires mechanical movement to change the pointing direction of the antenna. The sky is referenced as elevation-azimuth space, where elevation is the angle from the horizon to the radar direction and azimuth is the angle left or right from a reference direction. The reflector also can be used on the receiving end as a collector. Radars which use the antenna for both transmitting and receiving are called monostatic, as drawn in Figure 7 above [Rinehart 7].

One important characteristic of the antenna is the antenna gain, which quantifies how much the antenna concentrates the radar beam in the specified direction. As antenna gain increases, the main lobe beam becomes smaller in diameter, and as a result the angular resolution increases [Rinehart 14]. The size and shape of the antenna directly influence the antenna gain, with its equation given as:

$$G = \frac{4\pi * A_e}{\lambda^2} \quad \textbf{Equation 1}$$

where $A_e$ = effective area of the antenna and $\lambda$ = wavelength of the propagated electromagnetic energy [Kingsley 9]. Therefore, the antenna gain increases linearly as the area of the antenna increases. Different shaped antennas also provide different areas and therefore different antenna gains.

One of the most important modules of monostatic radar is the Transmit/Receive (T/R) switch. This switch is synchronized with the transmitting of the high energy outputs and receiving low energy inputs. The switch protects the receiver by appropriately isolating the receiver input from the transmitter output. Without this piece of hardware, bistatic radar, where the transmitter and receiver are two separate antennae, would be more popular [Rinehart 23].

Once a low level signal is collected, it is passed down to the receiver. The receiver detects and amplifies weak signals so that they can be analyzed for pertinent information. Receivers used for radar applications are of very high quality as they amplify extremely weak

signals and any significant addition of noise would be detrimental to the understanding of the information [Rinehart 24]. From the receiver, the signal is passed through to a signal processor.

The signal processor conditions the signals to be more accurately understood by the main computer. Here is where, most notably, ground clutter suppression and Doppler algorithms are applied. Ground clutter is the echo, or reflection, of unwanted nearby objects, in relation to the radar, such as trees or buildings, which significantly distort received data. Doppler algorithms provide information about target line-of-sight velocity.

As a last step before displaying the information for human interpretation, the main computer is in control of detection and tracking. With help from range and Doppler information the radar can detect an object and can correctly track its trajectory throughout range-elevation-azimuth space. These two functions are essential when tracking fast moving targets such as aircraft.

### 2.3.3 – Phased Array Radars

Phased array radar was developed shortly after dish radar, and was considered a breakthrough in radar technology. Phased array radar is composed of many of the same components as used in dish radar. However, what separates the phased array radar from dish radar is its antenna. Its beam steering control technique is far superior to the dish radar's mechanical scan strategy. Fundamentally, phased array radar uses a directive antenna, which consists of numerous discrete antennas also known as the Transmit/Receive (T/R) elements. Thousands of these T/R elements are able to create single or multiple scan beams in any desired direction, and more importantly they can change the direction of the beam at a much greater rate than dish radar. [Skolnik 559-560]

As explained in the previous section, dish radar performs a scan by mechanically moving the antenna to change beam direction. The phased array technology allows the beam to be steered electronically, thus eliminating any mechanical parts used for steering the radar. Absence of the mechanical parts increases the scan speed of the radar, and reduces maintenance costs that are related to constant mechanical wear of the dish radars. Phased array radars are able to electronically scan because every element in the array is able to transmit and receive individually using precisely-controlled time differences or phase variances. The desired effect is to have all of the elements', "… interfere constructively [add] in desired directions, and interfere destructively [cancel] in the remaining space. [Evans 2006]"

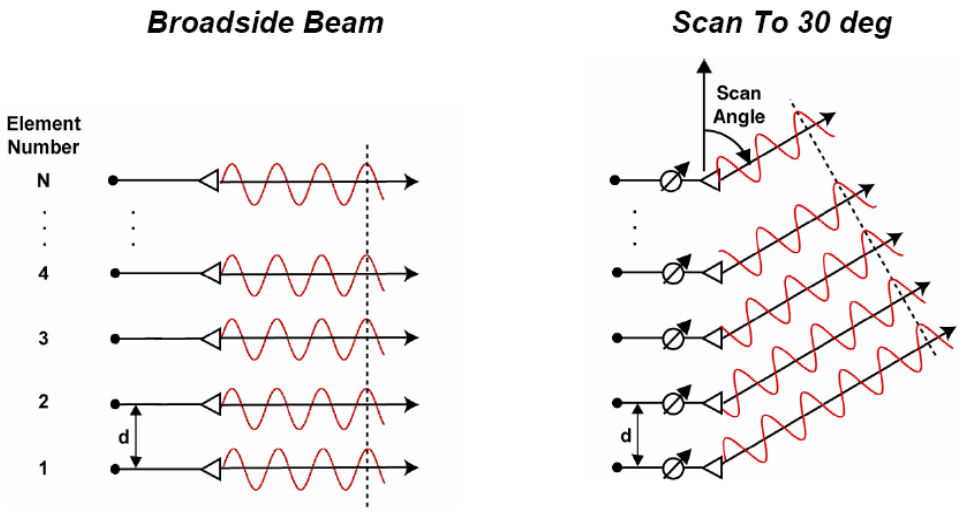


**Figure 8: Phased Array Radar Directional Capability**
**Each element radiates energy in many directions. The energy needs to be phase shifted at each T/R module so that constructive interference occurs at the desired angle.**
**[Evans, 2006]**

On the left side of the Figure 8, all of the elements propagate energy at the same instance, thus the waves interfere constructively at broadside, or 0 degrees, and interfere destructively everywhere else. The innovation of phased array technology becomes apparent when the desired scan angle is different from broadside. On the right side of the Figure 8, it can be seen that every wave interferes constructively at the 30 degree scan angle. Constructive interference is

accomplished by phase shifting the signal at every T/R module in the array, thus every element transmits at a different time and the signal interferes constructively at the desired angle only. Figure 14 below shows how the two different beam patterns appear on the Response vs. Direction (signal strength vs. scan angle) graph. In actuality, these patterns are three-dimensional; what is shown in the figure below is a two-dimensional slice of the pattern. The graph on the left shows a scan at broadside, while the graph on the right shows a scan at 30 degrees.

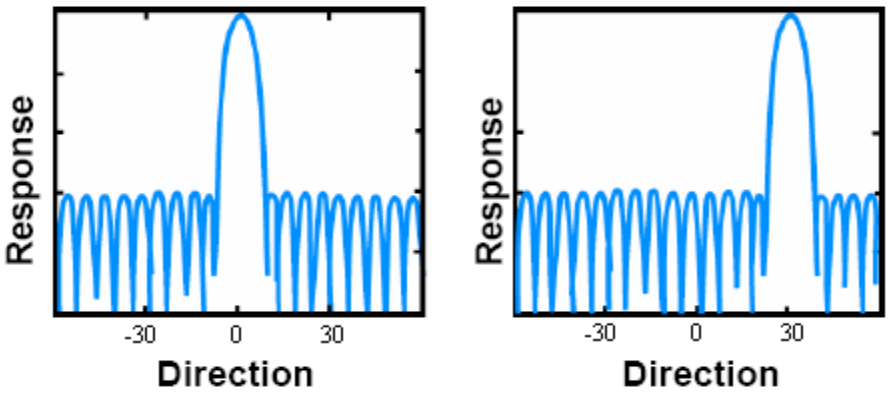


**Figure 9: Scan Angle and Response [Evans, 2006]**
**This graphic shows the intensity, or response, of a phased array radar at two different scan angles.**

Ideally, the beam patterns would exhibit infinite response at the desired angle or range of angles, and zero response everywhere else. The patterns shown above are, as is the always case, not ideal and exhibit non-zero response at angles outside the target angle, known as side lobes. This effect can be reduced significantly by creating a phased array panel with a large number of elements. The number of elements in the array is inversely proportional to the width of the beam in the desired direction. Thus, as the number of elements increases, the beam width decreases. An important characteristic of a phased array is that the beam width defines the angular

resolution of the radar; meaning that as the number of elements increases, so does the overall resolution of the radar. [Evans 2006].

Even though phased array radar was developed shortly after dish radars, phased array technology has rarely been utilized for civilian applications. Due to the historically high cost of creating the individual T/R elements, the technology has been primarily used in military applications where high resolution and scan rates are significantly more important than at civilian airports. [Weber et al 2007].

## *2.4 – Lincoln Laboratory Projects*

### 2.4.1 – Radar Open Systems Architecture (ROSA)

Current radar systems are most often custom made and contain proprietary hardware and software components, presenting an inconvenience for the operator, due to forced dependency on the manufacturer for maintenance, as well as difficult communication between the different types of radars. One of the ways to fix this problem is to create an Open System Architecture that would be compatible with all radar, greatly facilitating the user-radar interaction with different types of radars, as well as the radar-to-radar interaction [MPAR-ROSA WPI MQP 2008].

The development of ROSA was initiated by MIT Lincoln Laboratory in an effort to shift away from the inefficient traditional radar-specific architectures developed by private companies. Lincoln Laboratory's ROSA consists of separate building blocks, each of which is responsible for different elements of radar, i.e. antenna, transmitter or timing. The uniqueness of these components is in their design, which is intended to be compatible with different hardware and interfaces.

There are numerous benefits to ROSA, which include: reducing the operation and maintenance costs, more efficient use of resources, simpler communication with other radars, and most importantly, simplified modification of independent components. Because ROSA is an "open" architecture, any user has access to modify certain components to increase the overall functionality, without having to report technical difficulties to the company that developed the radar.

ROSA II is the second generation architecture that is currently being developed by MIT Lincoln Laboratory, expanding the capabilities of the ROSA, which was only designed for dish radars application. Other than numerous functionality improvements, ROSA II software

development includes the phased array radar technology. Because, in the past, the phased array radars were not considered for civilian use, the implementation of the phased array technology into ROSA seemed unnecessary. However, the current development of MPAR sparked the software upgrade. Figure 10 below is the basic ROSA II system block diagram for phased array radar.

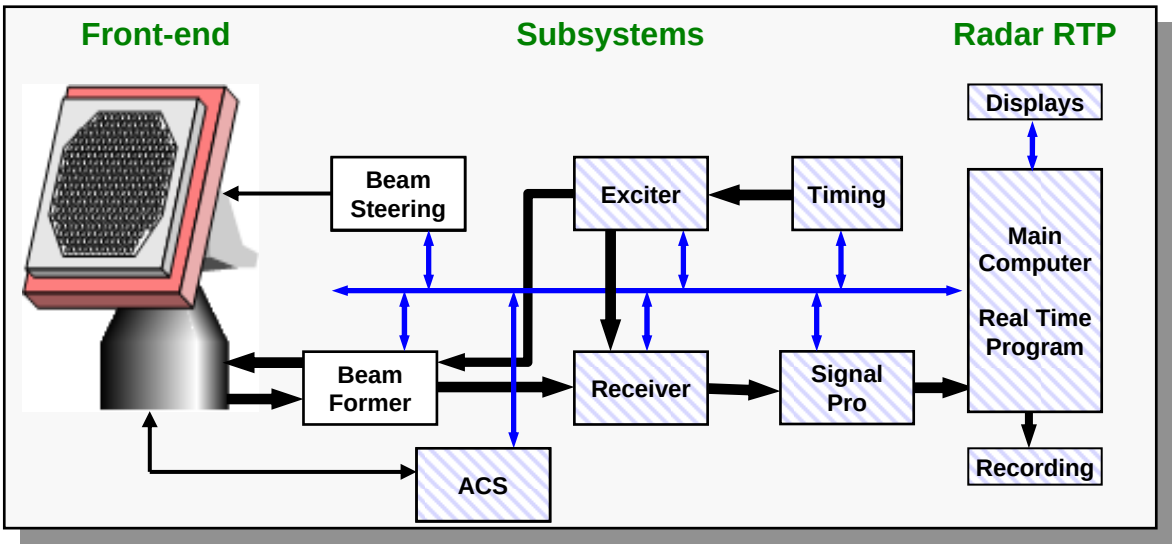


**Figure 10: ROSA Subsystems**
**The projected structure of ROSA II and its subsystems (stripped). The Beam Steering and Beam Former subsystems are front-end hardware. [MPAR-ROSA WPI MQP, 2008]**

Every arrow in Figure 10 represents messages that are being sent between the different subsystems, the front-end hardware, and the main computer. It is intended for ROSA II to be fully compatible with MPAR once the radar is built, thus eliminating any custom made architecture specifically produced for MPAR.

### 2.4.2 – Multifunction Phased Array Radar (MPAR)

As previously stated, there are multiple types of radars currently being used to survey the sky. Current U.S. surveillance networks consist of four types of radars: NEXRAD to predict general weather conditions and TDWR to assist NEXRAD in scanning for weather around airport terminals, ARSR to scan for long-range aircraft, and ASR to scan for short-range aircraft. These radars have been heavily relied on; some have been extensively used for more than 40 years, and thus are in need of constant repairs. Incremental repairs have been less costly than completely replacing the whole system. However, there comes a point when the maintenance becomes inefficient and a new technology needs to be implemented in the current infrastructure. Phased array radars are a new technology to be introduced in civilian applications. This technology was never previously considered for use in common surveillance applications, such as commercial airplane tracking or weather sensing, because of the high cost associated with phased array radars [Weber et. al 2007].

MPAR is currently being developed at MIT Lincoln Laboratory with the goal of replacing the current network of civilian surveillance radars with a single "multifunction" radar. The phased array technology allows a single radar to have multifunction capability by performing aircraft and weather scans. Also, phased array technology allows the transmit beam to be "spoiled". In brief, this technique, named beam spoiling, works as follows: at low elevation angles, the beam is pointed at the horizon and the distance to the sky ceiling is immense. When the elevation angles increase, the distance to the same sky ceiling becomes exponentially shorter. At these shorter distances the transmit power needed to attain the same resolution as at the large distances becomes much less. Thus, the technique of beam spoiling is the disbursement of beam energy over a larger area in the sky as the elevation angle increases, achieving the same resolution with a faster scan time [Weber et. al 2007].

The "scan strategy" for MPAR has not yet been finalized and has been revised numerous times. The scan strategy refers to how the array will be utilized to perform the different types of scans, as each scan requires different scanning parameters. MPAR's technology allows flexibility in scan patterns by allowing the user to control completely independent beams to perform different tasks. The original scan strategy chose to utilize the independent beams to perform different aircraft and weather scans simultaneously, which later on proved not to be the most efficient way to perform the tasks.

The current scan strategy tries to interlace the scans. MPAR will output updated information every four seconds. A complete Aircraft Scan takes approximately 3.44 seconds. The remaining time, 0.56 seconds, is then used to perform small portions of the Wind Shear Scan and the 3D Weather Volume Scan. Table 2 below shows approximate timings for scan update periods [MPAR-ROSA WPI MQP 2008 Kickoff].

| Function | Scan Update Period (sec) |
|---|---|
| **Aircraft "Track While Scan"** | **4.0** |
| **Rapid Update Weather Volume Scan** | **4.0** |
| **Wind Shear Scans** | **60** |
| **3-D Weather Volume Scan** | **120** |

**Table 2: Scan Types and Update Speeds for MPAR**

"Track While Scan" or TWS is a concept that does not simply scan for objects, but also keeps track of the old positions of already identified targets, thus tracking objects while scanning the airspace. Due to MPAR's flexibility, it is possible to devote full or partial resources strictly to tracking an object; however, the resources would only be utilized in special circumstances. The

data from an Aircraft Scan can also be analyzed for weather data, and thus allows a Rapid Update Weather Volume Scan (RUWVS) which gives a rough weather update every four seconds. The most important scan for a terminal weather radar is the Wind Shear Scan, which is extremely important for the safe approach or departure of an airplane. The Wind Shear Scan is outputted every 60.0 seconds or every 15 aircraft scans. The 3-D Weather Volume Scan, which is a detailed weather scan, is outputted every 120 seconds or every 30 aircraft scans. The Wind Shear Scan is a continuation of the 3D Weather Volume Scan, without repetitively scanning the same elevations in high-resolution. This scan strategy has been selected for its ability to match, and possibly exceed, current update times [MPAR-ROSA WPI MQP 2008 Kickoff].

The full scale MPAR is designed to have four faces to fully cover the sky. Each face would have 20,000 T/R modules, allowing the radar to achieve a 1° pencil beam, which is even thinner at broadside. Such immense numbers of elements allows MPAR to achieve the same type of resolution as today's weather radars. Figure 11, below, shows future concepts of the MPAR.

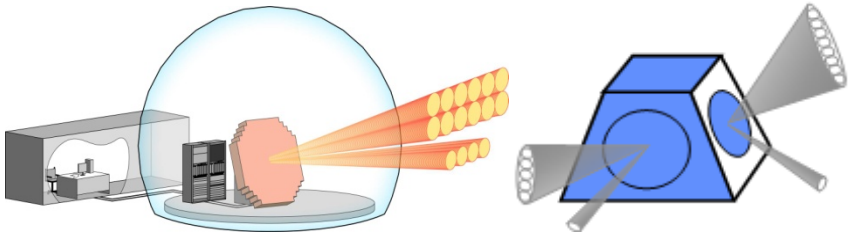

**Figure 11: Future Concepts of MPAR [MPAR-ROSA WPI MQP, 2008]**

The exact shape of the face is not yet final, but one of the greatest strengths of this radar is it scalability, meaning it can assume different shapes with different amount of elements per face [MPAR-ROSA WPI MQP 2008 Kickoff].

As an example showing scalability, the first prototype of MPAR will be the Terminal MPAR or TMPAR. TMPAR is a smaller version of MPAR, which will have only around 5,000

T/R modules per face instead of 20,000. Reducing element count significantly reduces the resolution, but it will have the same functionality as MPAR. There are multiple reasons to pursue the development of the TMPAR first. It is cheaper to build a TMPAR prototype, yet it will still confirm the functionality of MPAR. Also, TMPAR is targeted towards smaller airports that control much less air traffic than major airports and do not need as high resolution as the full-scale version [MPAR-ROSA WPI MQP 2008 Kickoff].

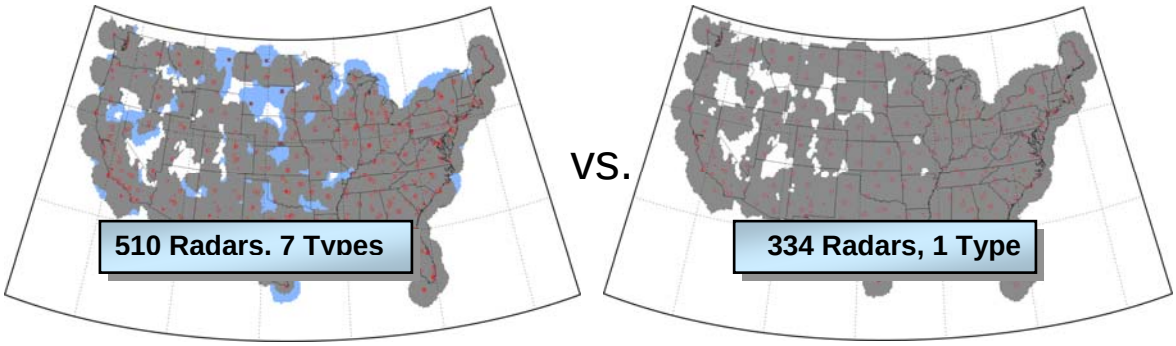


**Figure 12: Current Coverage and Future Coverage**
**The left graphic shows the current radar coverage of the United State. The right graphic shows the projected coverage using MPAR. [MPAR-ROSA WPI MQP, 2008]**

As mentioned before, the current radar network coverage includes four general types of radars: NEXRAD, TDWR, ARSR, and ASR. There are, however, seven models of radars in use. There are ASR-9 and ASR-11 radars currently in use, as well as ARSR-1/2, ARSR-3 and ARSR-4. Today's radar network coverage consists of 510 radars, which are made up from these seven different types of radars. The same radar network coverage could be achieved with 334 MPARs, where half of these would be TMPAR. Figure 12 shows the coverage that could be achieved with MPAR versus the current coverage. There would be one type of radar instead of seven, requiring less radar types to maintain, and simplifying communication between radars [Weber et. al 2007].

## *2.5 – Relative Hardware Specific to the Interface Board Design*

As mentioned before, the interface board is situated between the beam steering subsystem and the T/R modules of the phased array. This section will briefly describe the two pieces of hardware located directly on either side of the interface board.

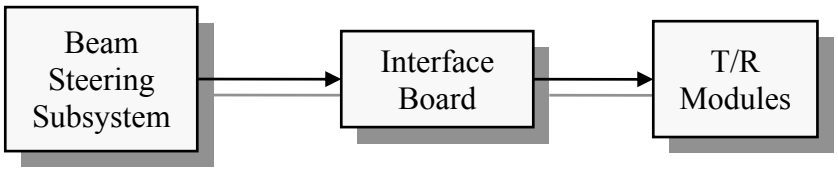


**Figure 13: Block Diagram of Where the Interface Board is physically Located**
**The interface board in this design will be situated between the beam steering subsystem and the front-end of the radar hardware.**

### 2.5.1 –The T/R Module

As stated before, the T/R module is the one of the most important pieces of radar hardware; this is especially true in phased array radar where the T/R module is also the antenna; in fact, each T/R module has two independent antennas. The T/R module is functionally responsible for changing the scan angle of the radar. Changing the scan angle is accomplished by phasing and attenuating or amplifying the modules, which electronically changes the direction in which the antenna is looking. The data and control lines, shown in Figure 14, route the phase and attenuation information from the beam steering subsystem to the T/R module, where sub-circuits read in the "directions" and appropriately adjust the information being passed to and from the antenna.

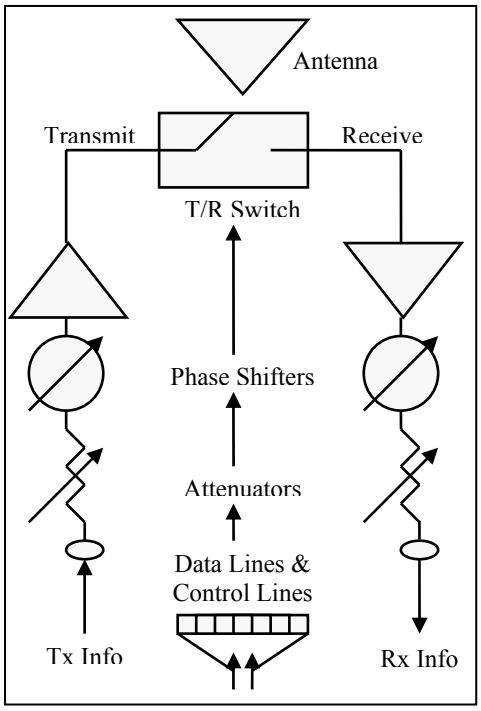


**Figure 14: Basic Block Diagram of a T/R Module**
**This generic diagram is the basic driving force behind the Transmit/Receive module. The module itself is the antenna. It is also responsible for phasing and attenuating or amplifying the received and transmitted signals through the use of data and control lines.**

There are many additional sub-circuits inside of the T/R module design for MPAR. The functionality of these sub-circuits has not been made fully available to the public domain, and therefore cannot be explained in detail. However, inferring from the pin-out of the interface board, see Section 3.2.1, there are a series of switches. These switches are simply implemented to control the on and off state of the module as a whole, which antenna is being used, and which mode the module is in. There are clock and load controls which are used to synchronize the radar array with the beam steering subsystem.

The T/R modules are being designed external to Lincoln Laboratory, at MA/COM. During the design process, there was a consensus to use Gallium Arsenic (GaAs) devices internal to the T/R module. GaAs devices' fast switching times makes them ideal for radar applications.

The only downfall to using GaAs devices is the requirement for negative logic, -5V low and 0V high, resulting in the T/R modules using level shifted digital logic voltages.

### 2.5.2 – Beam Steering Subsystem

The beam steering subsystem will be developed from a Xilinx Virtex-5 FPGA. The Virtex-5 was chosen, over previous versions, because of its support for Gigabit Ethernet, among other advantages. This interface is important to the selection of the FPGA because it is projected to be the standardized connection type for ROSA II and its control messages. The FPGA receives the UCM from the phased array radar's main computer. The job of the FPGA is to control the T/R module's status using the information provided from the main computer. The FPGA does not support negative logic voltages, and therefore it become immediately apparent the need for some sort of interface board.

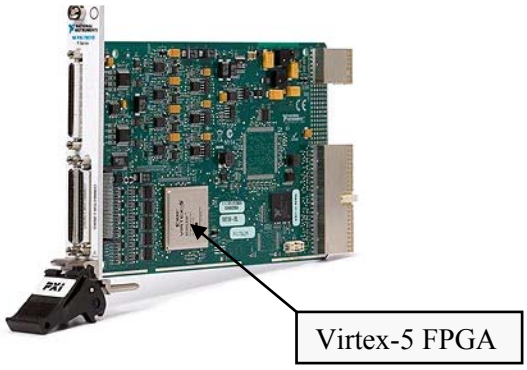


**Figure 15: The NI PXI-7851R Containing the Virtex-5 LX30 FPGA**

In the early testing stages, a National Instruments (NI) PXI-7851R evaluation board, containing a Virtex-5 LX30 FPGA, will replace the beam steering subsystem. Instead of receiving UCM messages from the radars main computer, LabVIEW software will be used to create equivalent commands to control the FPGA.

# 3.0 – Methods

The overall goal of the project was to design an interface board which facilitates communication between the beam steering FPGA and the front end hardware of the radar array, as shown in Figure 16. The first array being developed in the MPAR project will contain only sixty-four T/R modules. This down scaled panel is a cost efficient way of prototyping and will provide the same functionality as the full-scale array; allowing functionality testing on all aspects of the radar design.

The modularization of the array extends to the T/R module level. The design of the interface board will take advantage of this fact; as it will be designed for a single T/R module first and will be realized in hardware. Because the array takes a modular design, once the functionality of the hardware for a single T/R module is verified, verification of the entire array is also verified. To help differentiate between the different sizes of hardware; *array* will refer to the full-scale MPAR, *panel* will refer to the prototyping array, and *module* will refer to the single T/R module; as seen below.

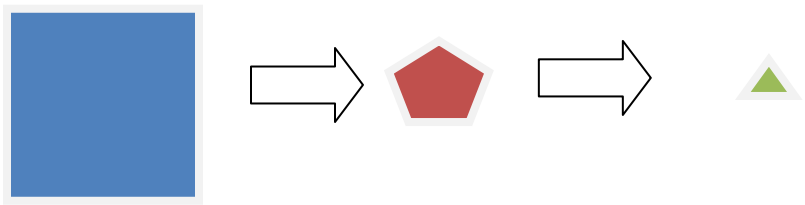


**Figure 16: Modularization of MPAR**

There are three goals for this project. First, the interface board will be designed on Multisim for a module. Second, the module design will be realized in hardware and will be tested for functionality and timing. Finally, the interface board will be redesigned, on Multisim, to

account for the panel's larger number of I/Os, the panel design. Additionally, research will be conducted on how to, in the future of the MPAR project, integrate the beam steering FPGA on the interface board to make the system less dependent on external hardware.

## *3.1 – Requirements*

Most of the specifications for the interface board are vague at this point in time in the design cycle for MPAR. Without existing hardware on either side of the interface board it is difficult to provide accurate specifications. Instead, "guidelines" were provided by the lead engineers at Lincoln Laboratory to help initiate the design. The design of the interface board was given four major requirements; reflection reduction, level shifting, fan-out, and minimizing differential propagation delays.

### 3.1.1 – Reflection Reduction

When driving a high frequency digital signal through a long cable, transmission effects need to be considered. The most detrimental effect to digital signals is reflections in the line caused by an impedance mismatch. These reflections can cause false triggering in clock lines and erroneous bits on data lines.

To correct these issues, impedance matching at the end of the wire was needed, accomplished using a technique known as termination. The termination portion of the circuit matched this impedance to prevent echoing on the cable. The characteristic impedance specification of the one to three meter cable connecting the PXI-7851R to the interface board is 90Ω.

### 3.1.2 – Level Shifting

The beam steering FPGA and the T/R modules use different digital logic voltage levels. The FGPA utilizes TTL logic; 0V for a logic 0 and +5V for a logic 1. The T/R modules use

negative logic; -5V for a logic 0 and 0V for a logic 1. The level shifting portion of the system translates the FPGA's digital voltage levels to be "readable" by the T/R module.

### 3.1.3 – Fan-out

The next portion of the system is in control of fanning-out the control lines and buffering them to make sure enough current is available to drive the signal through the cable connecting the interface board to the T/R modules. There are no precise specifications, yet, as to how much current is needed on the output. Instead, a range of possible current requirements per line has been provided as between 5mA and 25mA.

### 3.1.4 – Minimizing Differential Propagation Delay

True propagation delay was not considered in this design; the only requirement was to try to keep is as low as possible. The more important timing design consideration is differential propagation delay. It was expected that all of the signal paths have approximately the same delay in regards to each other; in other words it was expected that all information arrive at the outputs together. The specification provided by the lead engineers was that all data arrive within 50ns of each other at the outputs. Shorter differential propagation times are, of course, better.

## *3.2 – Approach to Design*

The approach to satisfy each of the aforementioned requirements is explained in this section. Figure 17 shows the sequence of steps taken to fulfill the requirements. In addition to the requirements from the Lincoln Laboratory advisors, other design considerations have been developed and included in their own segment at the end of this section. To begin describing the design process, a description of the pin-out is included to clarify between the two designs that are being developed.

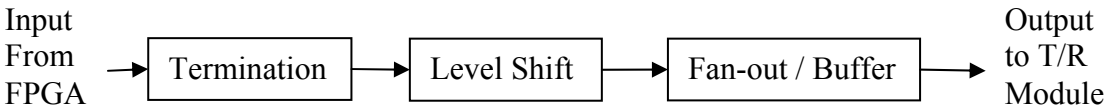


**Figure 17: Top-Level Progression Diagram**

### 3.2.1 – Pin-Out Description

The interface board is used to manipulate data and control lines passing digital signals. The number of lines differs dramatically between the module and panel designs. Table 3 shows the pin-out for the interface board panel design. Notice how each of the control lines must fan-out to eight separate lines on the output of the panel design; these are then fanned-out again on the panel to account for the sixty-four T/R modules.

Table 4 shows the reduced number of I/Os for the module design; the main reason why the module design is the only design to be realized in hardware in this project. The use of only a single data line contributes to the low input pin count. The module design, as stated before, accounts for only a single T/R module; therefore this design does not require fan-out of the control lines on the output, as does the panel design.

| INPUTS | | | OUTPUTS | | |
|---|---|---|---|---|---|
| **Function** | **Number Of Pins** | **Description** | **Function** | **Number of Pins** | **Description** |
| DGND | 52 | Ref Phase | DGND | ? | Ref Phase |
| Data In | 64 | Ref Phase | Data Out | 64 | Ref Phase |
| Clock | 1 | Data Shifts on Rising Edge | Clock | 8 | Data Shifts on Rising Edge |
| Load | 1 | Loads Information | Load | 8 | Load Information |
| Tx_Data State | 1 | Part of TX Control | Tx_Data_State | 8 | Part of TX Control |
| Sngl_Dual | 1 | Part of TX Control | Sngl_Dual | 8 | Part of TX Control |
| Xover-switch1 | 1 | Crossover Control 1 | Xover-switch1 | 8 | Crossover Control 1 |
| Xover-switch2 | 1 | Crossover Control 2 | Xover-switch2 | 8 | Crossover Control 2 |
| Tx1 pwr on/off | 1 | Power Switch 1 | Tx1 pwr on/off | 8 | Power Switch 1 |
| Tx2 pwr on/off | 1 | Power Switch 2 | Tx2 pwr on/off | 8 | Power Switch 2 |
| TRswitch1 | 1 | T/R Switch Control | TRswitch1 | 8 | T/R Switch Control |
| TRswitch2 | 1 | T/R Switch Control | TRswitch2 | 8 | T/R Switch Control |
| TOTAL PINS | 126 | | | 144+ | |

**Table 3: Interface Board Pin-Out for Panel Design**

**There are a large number of DGNDs on the input of the panel design because of the standardized connection from the NI PXI-7851R. In actuality, there are only seventy-six lines which are of concern on the input. The output connector has yet to determined, therefore the number of grounds being passed to the T/R module is undefined. Each of the control lines is fanned-out to eight separate lines.**

| INPUTS | | | OUTPUTS | | |
|---|---|---|---|---|---|
| **Function** | **Number Of Pins** | **Description** | **Function** | **Number of Pins** | **Description** |
| Data In | 1 | Ref Phase | Data Out | 1 | Ref Phase |
| Clock | 1 | Data Shifts on Rising Edge | Clock | 1 | Data Shifts on Rising Edge |
| Load | 1 | Loads Information | Load | 1 | Loads Information |
| Tx_Data State | 1 | Part of TX Control | Tx_Data_State | 1 | Part of TX Control |
| Sngl_Dual | 1 | Part of TX Control | Sngl_Dual | 1 | Part of TX Control |
| Xover-switch1 | 1 | Crossover Control 1 | Xover-switch1 | 1 | Crossover Control 1 |
| Xover-switch2 | 1 | Crossover Control 2 | Xover-switch2 | 1 | Crossover Control 2 |
| Tx1 pwr on/off | 1 | Power Switch 1 | Tx1 pwr on/off | 1 | Power Switch 1 |
| Tx2 pwr on/off | 1 | Power Switch 2 | Tx2 pwr on/off | 1 | Power Switch 2 |
| TRswitch1 | 1 | T/R Switch Control | TRswitch1 | 1 | T/R Switch Control |
| TRswitch2 | 1 | T/R Switch Control | TRswitch2 | 1 | T/R Switch Control |
| TOTAL PINS | 11 | | | 11 | |

**Table 4: Interface Board Pin-Out for Module Design**

**The module design, for a single T/R module, omits DGND inputs sixty-three of the data lines. Also, the fan-out of the control lines is omitted. This proof of concept design will be realized in hardware.**

The names of the pins have been taken from a document internal to Lincoln Laboratory outlining the basic parameters of the T/R module. As stated when describing the T/R module in Section 2.5.1, the functionality of these pins has not been made available to the public domain. However, observation of the tables above shows that they can be grouped into several categories. The data lines contain information about phase and attenuation for each T/R module. There are a series of switches which are used to select which antenna is being used or if the module is on or off. The clock and strobe lines are used to synchronize the T/R modules of the array to the beam steering system. Besides this brief contemplation of their functionality, the underlying contents of the digital information being passed through the interface board are irrelevant to the design, as long as their requirements are met.

### 3.2.2 – Termination

There are five approaches to termination as described in an article written by John Nemec [Nemec, 2007]. These techniques are named: parallel termination, Thevenin termination, series termination, AC termination and Schottky-Diode termination. After conferring with the Lincoln Laboratory lead engineers, Thevenin termination was considered most applicable to this design.

Thevenin termination possesses benefits for digital signals. This two resistor design, shown in Figure 18, is effective at eliminating the reflections of mismatched impedances, while maintaining signal integrity by improving the noise margin of the system. Resistors R1 and R2 are pull-up and pull-down resistors, respectively, assisting the FPGA in providing current to the load during both logic states.

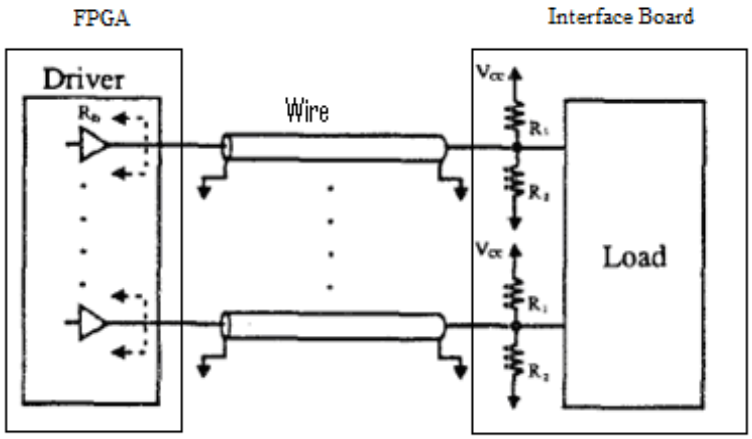


**Figure 18: Thevenin Termination**
**The location of the termination resistors is on the input of the interface board.**
**(Modified from [Nemec, 2007])**

Nemec [Nemec, 2007] describes how to determine optimal values for the pull up and pull down resistors, whose parallel equivalence matches the characteristic impedance of the transmission cable. The first step is determining a Thevenin voltage ($V_{TH}$), which is dependent on the driving characteristics of the FPGA evaluation board.

$$V_{TH} = V_{OH(MIN)} - I_{OH(MAX)}\left(R_D + Z_0\right) \qquad \textbf{Equation 2}$$

In this equation $V_{OH}$ is the physical voltage corresponding to the high logic output, $I_{OH}$ is the physical output current corresponding to the high logic output, and $R_D$ is the output impedance; all of the PXI-7851R. This information can be found on the PXI-7851R datasheet, see Appendix 9.2.1. $Z_0$ is the characteristic impedance of the transmission line, which was given as $90\Omega$ by the Lincoln Laboratory lead engineers. Substituting values:

$$V_{TH} = 2.4 - 0.004\left(0.5 + 90\right) = 2.038V$$

Now that the Thevenin voltage has been determined, the resistor values can be found directly with the following equations:

$$R_1 = \frac{Z_0 * V_{CC}}{V_{TH}}$$ **Equation 3** $$R_2 = \frac{Z_0 * V_{CC}}{V_{CC} - V_{TH}}$$ **Equation 4**

$V_{CC}$ is +5V. All of the other values are known at this point. Substituting values:

$$R_1 = \frac{90 * 5}{2.038} = 220.8\Omega \qquad R_2 = \frac{90 * 5}{5 - 2.038} = 151.9\Omega$$

The parallel equivalence of these resistor values is 89.9 Ohms, matching the characteristic impedance of the cable. In this configuration, it is expected that the reflections in the cable are minimized. Each input will need these termination resistors; therefore the number of resistors on the interface board will be numerous in both the panel and module designs. To save space and simplify PCB layout, surface mount network resistors were used. The closest network resistor values found were 150 Ohms and 220 Ohms at a 2% tolerance. The parallel equivalence of these values is 89.1 Ohms. Accounting for worst case, where both resistors exhibit maximum tolerance in the same direction, the range of parallel equivalences cover 88.3 Ohms – 90.08 Ohms.

An undesired characteristic of the Thevenin termination approach is leakage current; the flow of current from the voltage rail to ground through the resistors. With this design there is a 13.5mA leakage current per termination [5V / (150Ω +220Ω)]; or close to 1A leakage current taking into account all seventy-six terminations of the panel design. As there are no power usage specifications, this amount of power leakage is acceptable.

The network resistor's manufacturer numbers are 767163150-ND and 767163220-ND, 150Ω and 220Ω respectively. These are 16-pin surface mount, isolated network resistors; meaning that each set of pins designates separate resistor.

### 3.2.3 – Changing Logic Levels

One of the most important tasks of this design is the translation of logic level voltages. As stated before, the FPGA supports normal logic; that is, a low-logic state is 0V and a high-logic state is 5V. The T/R modules require the use of "negative logic," where a low-logic state is -5V and a high-logic state is 0V. The change in logic is not  a negation as one might think; it is a level shift. To accomplish this task, the SWD-119 digital IC has been selected, see Appendix 9.2.2.

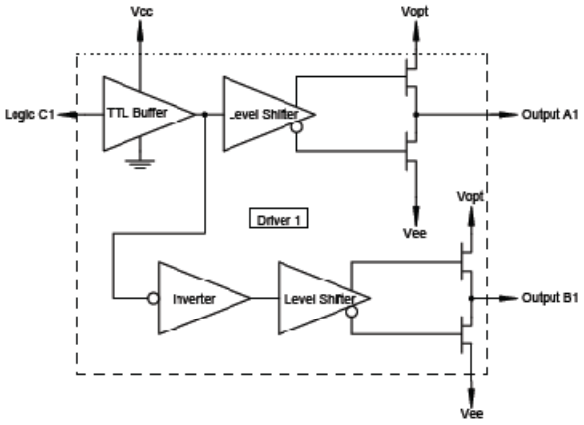


**Figure 19: One Channel of the SWD-119**
**The SWD-119 is a quad driver for Gallium Arsenic (GaAs) devices. Its functionality is to output either $V_{OPT}$ or $V_{EE}$ depending on the input logic state. This is accomplished using a pair of BJTs. Because these two voltages are user selectable, this device can be used in the design as a level shifter.**

The SWD-119 is a 16-pin surface mount, quad channel device. For each input, C, there is a pair of outputs, A and B; which are logic inverses of each other. For this design, only output A is used. Depending on the input logic state, $V_{OPT}$ and $V_{EE}$ are seen on the output, and thus define the output logic level voltages. When $V_{OPT}$ is connected to 0V and $V_{EE}$ is connected to -5V, the input logic to this device will be shifted to the required voltage levels. Therefore, when the input logic is high, the output logic voltage level is 0V, and when the input logic is low, the output logic voltage level is -5V.

### 3.2.4 – Buffering

While the idea of buffering is simple, it can prove difficult to find the type of buffer needed for a specific application. Buffers have been implemented in all logic families, diversifying their characteristics. Functionally, an octal buffer is preferred because, in the full design, each of the control lines is being fanned out to eight separate lines, suggesting in the full design the use of eight octal buffers for the sixty-four data lines and ten octal buffers for the control lines, one buffer for each input control line; minimizing complexity of the design and the PCB layout.

The digital signals will already have been converted to "negative" logic when they are inputted into the buffers. Therefore, the buffers need to operate at a shifted voltage themselves. The high-logic output voltage is still greater than the low-logic output voltage; which allows us to shift the GND and VCC pins of the buffer to -5V and 0V, respectively. This approach, still having a positive potential from GND to VCC, allows the buffer to act normally while buffering the shifted voltage level digital signals.

There were two main considerations when choosing the buffer to use; minimizing differential propagation delay and providing sufficient current. Table 5, below, shows a selection of surface mount octal buffers and their different specifications. Current drive refers to the output current; $I_{OH}$ refers to current output during the high logic state, and $I_{OL}$ refers to the current output during the low logic state. The value listed under differential transition speed is the worst-case difference in switching times of the buffer,  found by taking the difference between the maximum delay and the minimum delay.

| Part Number | Logic Family | Current Drive | Differential Transition Speed (MAX – MIN) | Cost ($US) \| Quantity |
|---|---|---|---|---|
| SN74ABT244A | BiCMOS | $I_{OH}$ = –32mA, $I_{OL}$ = 64mA | $t_{PLH}$ = 3.6ns | 0.44 \| 1ku |
| | | | $t_{PHL}$ = 3.6ns | |
| SN74F241 | TTL | $I_{OH}$ = –15mA, $I_{OL}$ = 64mA | $t_{PLH}$ = 4.5ns | 0.40 \| 1ku |
| | | | $t_{PHL}$ = 4.5ns | |
| SN74S244 | TTL | $I_{OH}$ = –15mA, $I_{OL}$ = 64mA | $t_{PLH}$ = 9.0ns | 2.20 \| 1ku |
| | | | $t_{PHL}$ = 9.0ns | |
| SN74AS244A | TTL | $I_{OH}$ = –15mA, $I_{OL}$ = 64mA | $t_{PLH}$ = 4.2ns | 2.27 \| 1ku |
| | | | $t_{PHL}$ = 4.2ns | |
| SN74AHC541 | CMOS | $I_{OH}$ = –8mA, $I_{OL}$ = 8mA | $t_{PLH}$ = 7.5ns | 0.31 \| 1ku |
| | | | $t_{PHL}$ = 7.5ns | |

**Table 5: Choices of Octal Buffers**
**The initial search of octal buffers provided this table. Listed are octal buffers from various logic families and their corresponding characteristics important to the design of the interface board.**

The first choice buffer, SN74ABT244A, is part of the BiCMOS logic family, meaning it employs both BJTs and CMOS technology. This family is known for its low current consumption and is ideal for digital logic applications. It is able to provide more current and offer a lower differential propagation delay than the others chosen. This buffer is also among the least expensive.

The SN74ABT244A, see datasheet in Appendix 9.2.3, comes in a 20-pin surface mount package. Initially, it was believed that the input and outputs of the buffer would be separate sides of the package, simplifying the PCB design. However, this is not the case with any of the octal buffers. In addition to the $V_{CC}$ and GND pins, there are two output enable (OE) pins, which each control four of the buffers. To operate this octal buffer, both of the output enables need to be tied to -5V. Four of the buffers input left to right, while the remaining four input right to left, as seen in Figure 20.

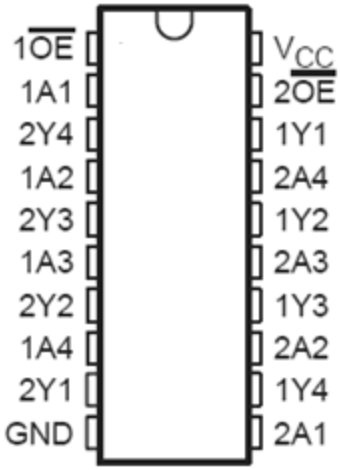


**Figure 20: Pin-Out of the SN74ABT244A Octal Buffer**
**1OE controls 1A1-1A4, and output on 1Y1-1Y4 (left to right)**
**2OE controls 2A1-2A4, and output on 2Y1-2Y4 (right to left)**

## *3.3 – Other Design Considerations*

### 3.3.1 – Connections on Interface Board Panel Design

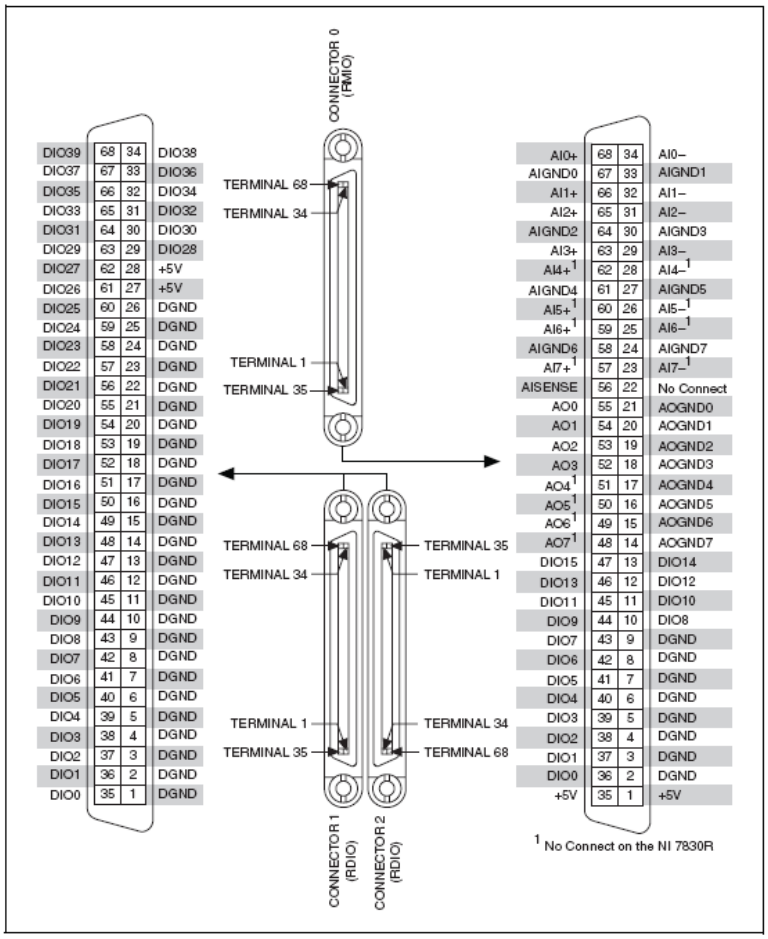


**Figure 21: NI PXI-7851R Connector Pin Assignments and Locations**
**This graphic describes the pin-out of the VHDCI connectors located on the NI PXI-7851R. The two bottom connectors are the ones which will be implemented into the design of the interface board.**

The National Instruments (NI) PXI-7851R Multifunction DAQ utilizes three 68-pin high-density VHDCI female connectors. The physical pin-out, taken from the PXI-7851R user manual, is shown above in Figure 21. Connector 1 and Connector 2 have forty digital I/Os each; enough to account for the seventy-six which will be used. Thus, Connector 0, which is mainly used for analog I/Os, will remain unused in this design. The module design will not utilize these standardized connectors, as it is a prototype used for verifying proof of concept.

| CONNECTOR 1 | | | | | |
|---|---|---|---|---|---|
| ***Description*** | ***Output*** | ***Pin #*** | ***Pin #*** | ***Output*** | ***Description*** |
| DATA_33 | DIO39 | 68 | 34 | DIO38 | DATA_34 |
| DATA_32 | DIO37 | 67 | 33 | DIO36 | DATA_35 |
| DATA_31 | DIO35 | 66 | 32 | DIO34 | DATA_36 |
| DATA_30 | DIO33 | 65 | 31 | DIO32 | DATA_37 |
| DATA_29 | DIO31 | 64 | 30 | DIO30 | DATA_38 |
| DATA_28 | DIO29 | 63 | 29 | DIO28 | DATA_39 |
| DATA_27 | DIO27 | 62 | 28 | +5V | UNUSED |
| DATA_26 | DIO26 | 61 | 27 | +5V | UNUSED |
| DATA_25 | DIO25 | 60 | 26 | DGND | GND |
| DATA_24 | DIO24 | 59 | 25 | DGND | GND |
| DATA_23 | DIO23 | 58 | 24 | DGND | GND |
| DATA_22 | DIO22 | 57 | 23 | DGND | GND |
| DATA_21 | DIO21 | 56 | 22 | DGND | GND |
| DATA_20 | DIO20 | 55 | 21 | DGND | GND |
| DATA_19 | DIO19 | 54 | 20 | DGND | GND |
| DATA_18 | DIO18 | 53 | 19 | DGND | GND |
| DATA_17 | DIO17 | 52 | 18 | DGND | GND |
| DATA_16 | DIO16 | 51 | 17 | DGND | GND |
| DATA_15 | DIO15 | 50 | 16 | DGND | GND |
| DATA_14 | DIO14 | 49 | 15 | DGND | GND |
| DATA_13 | DIO13 | 48 | 14 | DGND | GND |
| DATA_12 | DIO12 | 47 | 13 | DGND | GND |
| DATA_11 | DIO11 | 46 | 12 | DGND | GND |
| DATA_10 | DIO10 | 45 | 11 | DGND | GND |
| DATA_9 | DIO9 | 44 | 10 | DGND | GND |
| DATA_8 | DIO8 | 43 | 9 | DGND | GND |
| DATA_7 | DIO7 | 42 | 8 | DGND | GND |
| DATA_6 | DIO6 | 41 | 7 | DGND | GND |
| DATA_5 | DIO5 | 40 | 6 | DGND | GND |
| DATA_4 | DIO4 | 39 | 5 | DGND | GND |
| DATA_3 | DIO3 | 38 | 4 | DGND | GND |
| DATA_2 | DIO2 | 37 | 3 | DGND | GND |
| DATA_1 | DIO1 | 36 | 2 | DGND | GND |
| DATA_0 | DIO0 | 35 | 1 | DGND | GND |

**Table 6: Connector 1 Pin-Out and Description**

**Connector 1 is only responsible for transmitting forty of the sixty-four data lines from the PXI-7851R to the panel design.**

| CONNECTOR 2 | | | | | |
|---|---|---|---|---|---|
| ***Description*** | ***Output*** | ***Pin #*** | ***Pin #*** | ***Output*** | ***Description*** |
| DATA_63 | DIO39 | 68 | 34 | DIO38 | UNUSED |
| DATA_62 | DIO37 | 67 | 33 | DIO36 | UNUSED |
| DATA_61 | DIO35 | 66 | 32 | DIO34 | UNUSED |
| DATA_60 | DIO33 | 65 | 31 | DIO32 | UNUSED |
| DATA_59 | DIO31 | 64 | 30 | DIO30 | UNUSED |
| DATA_58 | DIO29 | 63 | 29 | DIO28 | UNUSED |
| DATA_57 | DIO27 | 62 | 28 | +5V | UNUSED |
| DATA_56 | DIO26 | 61 | 27 | +5V | UNUSED |
| DATA_55 | DIO25 | 60 | 26 | DGND | GND |
| DATA_54 | DIO24 | 59 | 25 | DGND | GND |
| DATA_53 | DIO23 | 58 | 24 | DGND | GND |
| DATA_52 | DIO22 | 57 | 23 | DGND | GND |
| DATA_51 | DIO21 | 56 | 22 | DGND | GND |
| DATA_50 | DIO20 | 55 | 21 | DGND | GND |
| DATA_49 | DIO19 | 54 | 20 | DGND | GND |
| DATA_48 | DIO18 | 53 | 19 | DGND | GND |
| DATA_47 | DIO17 | 52 | 18 | DGND | GND |
| DATA_46 | DIO16 | 51 | 17 | DGND | GND |
| DATA_45 | DIO15 | 50 | 16 | DGND | GND |
| DATA_44 | DIO14 | 49 | 15 | DGND | GND |
| DATA_43 | DIO13 | 48 | 14 | DGND | GND |
| DATA_42 | DIO12 | 47 | 13 | DGND | GND |
| DATA_41 | DIO11 | 46 | 12 | DGND | GND |
| DATA_40 | DIO10 | 45 | 11 | DGND | GND |
| Load | DIO9 | 44 | 10 | DGND | GND |
| Tx_Data State | DIO8 | 43 | 9 | DGND | GND |
| TRswitch2 | DIO7 | 42 | 8 | DGND | GND |
| TRswitch1 | DIO6 | 41 | 7 | DGND | GND |
| Sngl_Dual | DIO5 | 40 | 6 | DGND | GND |
| Xover-switch1 | DIO4 | 39 | 5 | DGND | GND |
| Xover-switch2 | DIO3 | 38 | 4 | DGND | GND |
| Tx1 pwr on/off | DIO2 | 37 | 3 | DGND | GND |
| Tx2 pwr on/off | DIO1 | 36 | 2 | DGND | GND |
| Clock | DIO0 | 35 | 1 | DGND | GND |

**Table 7: Connector 2 Pin-out and Description**

**Connector 2 is responsible for twenty-six data lines and all ten of the control lines of . The clock line is placed on the end pin of the connector to help minimize interference from the other lines.**

Table 6 and Table 7 describe the strategy for transmitting the seventy-six digital lines through the standardized connections on the PXI-NI7851R. Connector 1 accounts for forty of the data lines; the rest of the data lines appear on Connector 2. All of the control lines appear on

Connector 2; next to accompanying grounds to minimize any interference between the lines. The +5V connections on either connector will not be used, as the interface board will not be powered using the NI7851R, but rather by an external source.

The output connections of the buffer board, those in route to the actual T/R modules, have yet to be defined by M/A-COM. Therefore these will be left open for the design to be finished when the specifications are defined.

### 3.3.2 –Resistors on the Output

To provide protection to the T/R modules and compensate for possible impedance mismatches on the output stages of the interface, it was asked to place shunt resistors near the output of our board for each digital output. However, because the specifications from the manufacturer of the T/R module are still not finalized, determining these resistor values is impossible. To compensate for this step later on in the design, the locations for these surface mount resistors were left in the interface design. For each digital output, there is a resistor in series with the line, and a pull up resistor to GND.

### 3.3.3 – Providing Power to the Interface Board

The interface board requires +5V, -5V and GND terminals to be operational. The power is to be supplied not by the PXI-7851R, but rather an external power supply. Therefore, the interface board will only require generic terminals for the external supply to connect. To compensate for any voltage rippling or any interference from the high frequency digital lines, an electrolytic 47µF capacitor and a 1µF capacitor lie in parallel from +5v to GND and -5V to GND. Also, as added protection, a 0.1µF capacitor is connected adjacent to each IC on the PCB, from the voltage supply at the pin to the appropriate “GND” at that point in the circuit.

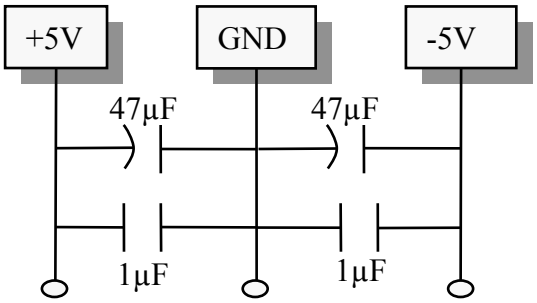


**Figure 22: Smoothing Power Supply Voltages at the Input of the Interface Board**
**Placing filter capacitors at the input of the interface board's power connections provides protection to the onboard components by insuring that the +5V, 0V, and -5V rails never spike, or pickup any ac voltages from the high frequency digital lines.**

## *3.4 – Multisim and Ultiboard*

National Instrument's Multisim circuit simulation software was used to draw the schematics electronically. Multisim gives the user opportunity to draw and simulate schematics using the Spice models that represent real life components. Unfortunately, most of the components that were essential to the design of the interface board did not have an existing Spice model. To work around the missing Spice models and come up with a schematic which would represent the written design, graphic components were developed which had the same footprints as the real life components. These user design components were merely space holders and did not function as their real life counterparts; thus computer simulations were not feasible.

To design the PCB, the schematics from Multisim were exported to another National Instrument software tool, Ultiboard. Imported from Multisim were the required parts and all the required connections. However, it was left up to the user how to topically arrange the design on the PCB. Placing the components required a click and drag of the appropriate footprint, and making the required connections required using an auto-routing feature . Using the auto-routing feature it became apparent that the routing of the all the traces would be impossible to accomplish without multiple layers. Due to cost, two PCB layers were determined to be the

maximum number of layers which would be utilized. This software tool proved extremely difficult to work with, however after trial and error a finished two-layer PCB was created.

The files which Ultiboard output, called Gerber files, were submitted to an online PCB manufacturing merchant. Advanced Circuits, the online merchant, reviewed the PCB design before completing any transactions. Advanced Circuits lets students order any number of PCB and offers a discount. Two PCBs of our design were ordered and delivered within a week.

Populating a PCB was completed quickly, as the module design consists of a handful of parts. The soldering of the surface mount parts was completed with the use of a solder iron, among other techniques. Once the board was populated, functionality testing began.

## *3.5 – Testing of Module Design Hardware*

Testing of the module hardware required the use of a dual power supply, function generator and oscilloscope; connected similarly to Figure 23: Setup of Testing Hardware. A dual channel power supply was used to create the +5V and -5V rail, using a standard technique. As can be seen in the figure below, the negative (-) input of the second channel is brought to the -5V rail of the PCB and the positive (+) input of the second channel is connected to ground. A function generator was connected to the input of the PCB, to simulate the FPGA's output, and grounded with the power supply ground. An oscilloscope was used to probe different points in the circuit and was also grounded with the power supply ground.

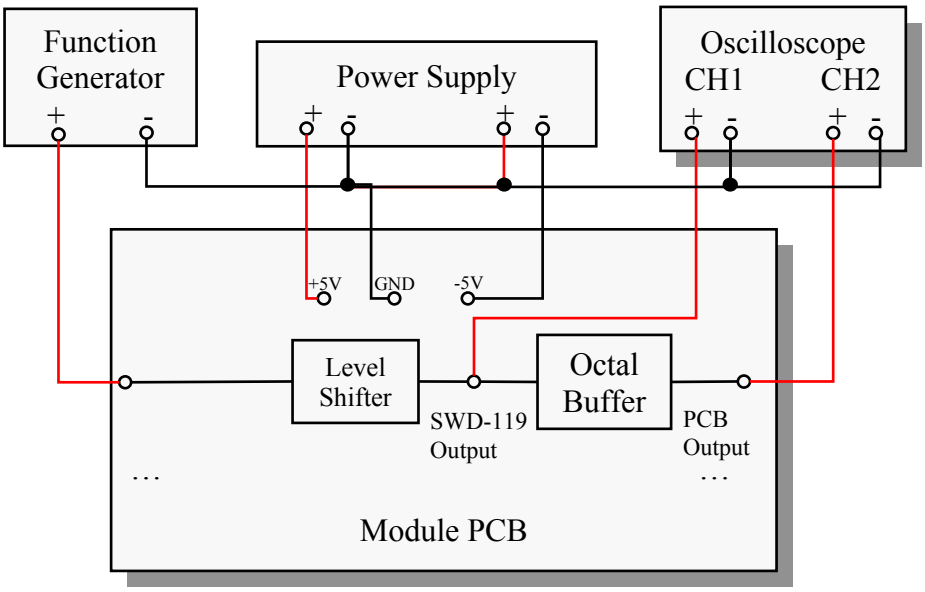


**Figure 23: Setup of Testing Hardware**
**A function generator, power supply, and oscilloscope was used to test the functionality of the module design PCB**

Testing was conducted between four variables: input waveform, output test location, output cable length, and output cable termination. The following sections explain the reasoning

behind testing these variables and how each test was set-up and conducted. Differential propagation delay was also tested.

### 3.5.1 – Input Waveform

To test the level shifting functionality of the SWD-119 IC, static tests needed to be performed. For the static tests, the input to the PCB was not connected to the function generator, instead it was connected to the power supply +5V and 0V rails, at separate times. The output of the PCB was then observed with the oscilloscope.

Two additional waveforms were used to test the PCBs response to frequency. A 1MHz and 20MHz, 0V to 5V square wave with a 50% duty cycle were produced by the function generator. The actual beam steering subsystem performs at 20MHz, but the 1MHz input was tested to see how the output of the design changes with an increase in frequency.

### 3.5.2 – Output Location

There are only two locations to observe an output waveform on the interface board design, from the output of the SWD-119 and from the output of the SN71ABT244A. These locations have been named the SWD-119 output and the PCB output, respectively. To test the different output locations, the oscilloscope probe was simply moved to each location.

### 3.5.3 – Output Cable Length

As mentioned before, the output of the interface board will be connected with a cable between one and three meters in length to the radar array. To test what effect the cable length has on the output of the interface board three conditions were tested: the use of no cable, the use of a one meter cable and the use of a three meter cable. The cable used was a twisted-pair flat cable and it was soldered to the PCB.

### 3.5.4 – Output Cable Termination

MA/COM, the manufacture of the T/R module, suggested the use of a 1KΩ pull-up resistor, to 0V, to terminate the cable connecting the interface board to the T/R module. This idea was tested against the use of a 220Ω /330Ω Thevenin termination, suggested by Lincoln Laboratory, shown in Figure 24. To test these scenarios, the actual resistor values were soldered to the end of the output cable. The oscilloscope was connected to the output of cables or the output of the PCB, between the termination resistors, if there was no cable.

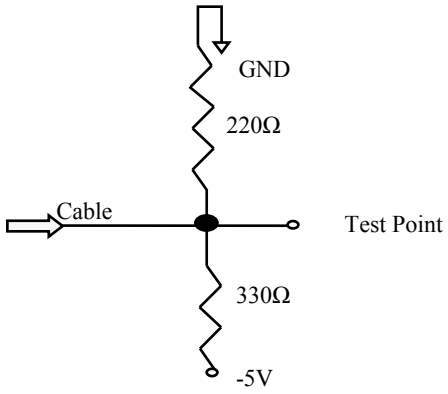


**Figure 24: Thevenin Termination at the Output of the PCB and Cable**
**In most cases during testing the output was terminated as shown in the figure. Because of the shifted voltage levels at this point in the design, the pull-up resistor is connected to GND, and vice-versa.**

### 3.5.5 – Differential Propagation Delay

Testing differential propagation delay proved to be extremely easy. The same input signal was connected to two of the paths on the PCB at the same time. The oscilloscope was used to view both of the outputs concurrently. The oscilloscope showed two separate signals separated by a delay. The difference in time between the leading edges of each signal was measured using an oscilloscope function, providing the differential propagation delay.

# 4.0 – Results

The results are broken into two sections: schematics and test results. The schematics section contains both the module and panel designs, describing in detail the individual sub-sections in the design. The module design also includes the design of the PCB to show an Ultiboard PCB layout. In the test results section, the results of the module design PCB tests are included to begin drawing conclusions about the interface board design developed in this project.

## *4.1 – Schematics*

### 4.1.1 – Module Design

The module design contains thirteen separate lines. A clock line, a single data line and a group of control lines all utilizing a common "path" from the input to the output. Upon input into the PCB, a Thevenin termination is applied using network resistors. A 220Ω network resistor to +5V and a 150Ω network resistor to ground, with the signal lines being the point between the resistors, completes the termination. Next, the SWD-119 level shifts the voltages by -5V. The output labeled Vopt (Pin 7) of the SWD-119 is connected to ground to provide the correct 0V/-5V on the output pins of the IC. From the SWD-119, the digital signals are buffered with the SN74ABT244A octal buffer. The buffers are operated at a shifted voltage level so that they correctly operate with the level shifted digital signals. Each buffer's ground pin (Pin 10) is connected to -5V while the Vcc pin (Pin 20) is connected to ground. From the output of the buffers, the signals arrive at the output of the interface board.

The shunt resistors, which were supposed to have been located on the output of the buffers, have not been included in the module design. However, the voltage rails utilize the capacitors required to decouple the voltage supplies to the interface board and to each IC.

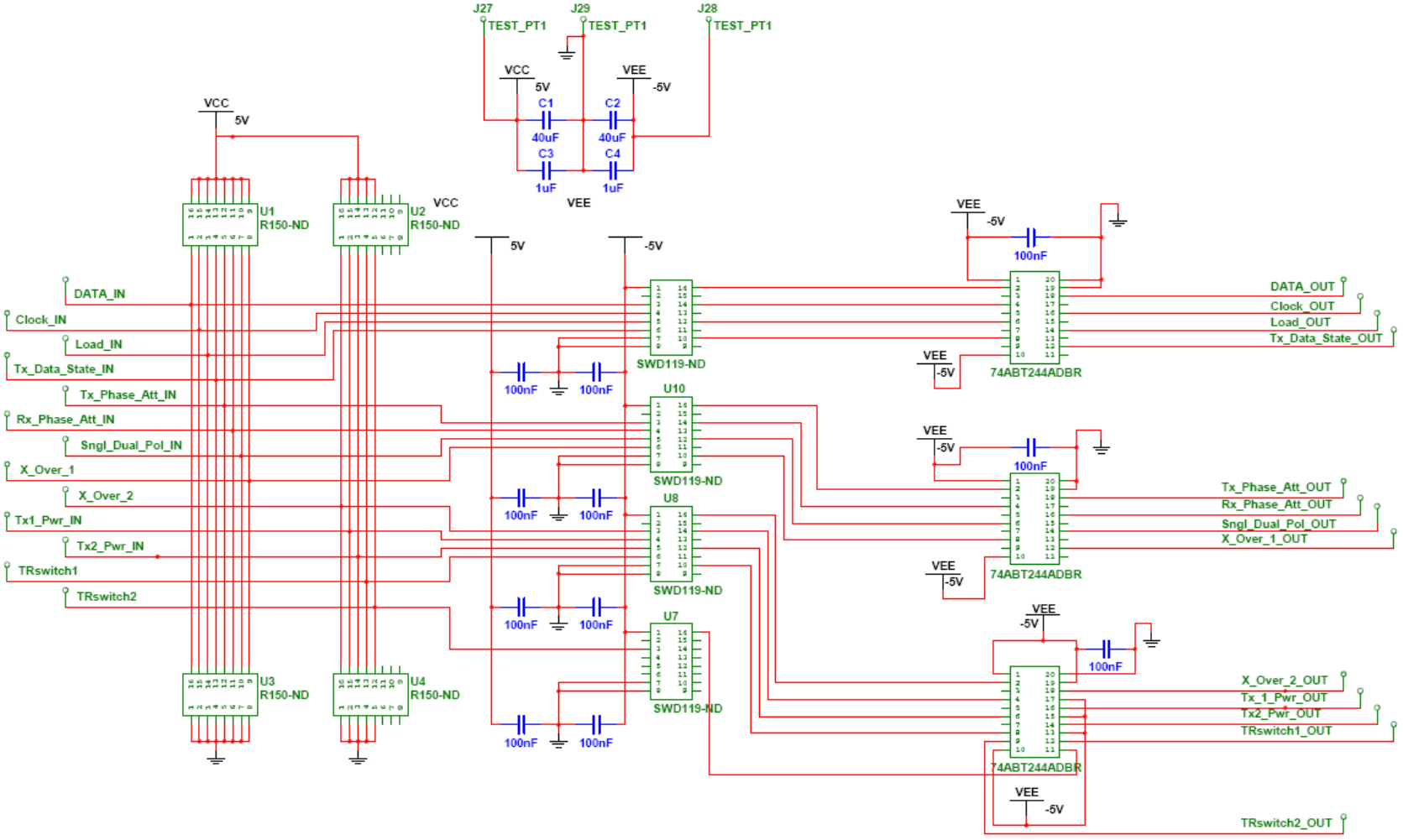


**Figure 25: The Module Design**

**This design is simplified, compared to the panel design, because of the limited number of I/Os. All ten control lines and only a single data line are included. This figure shows the Thevenin termination, the level shifting and the buffering stages of the design.**

### 4.1.2 – Module PCB design

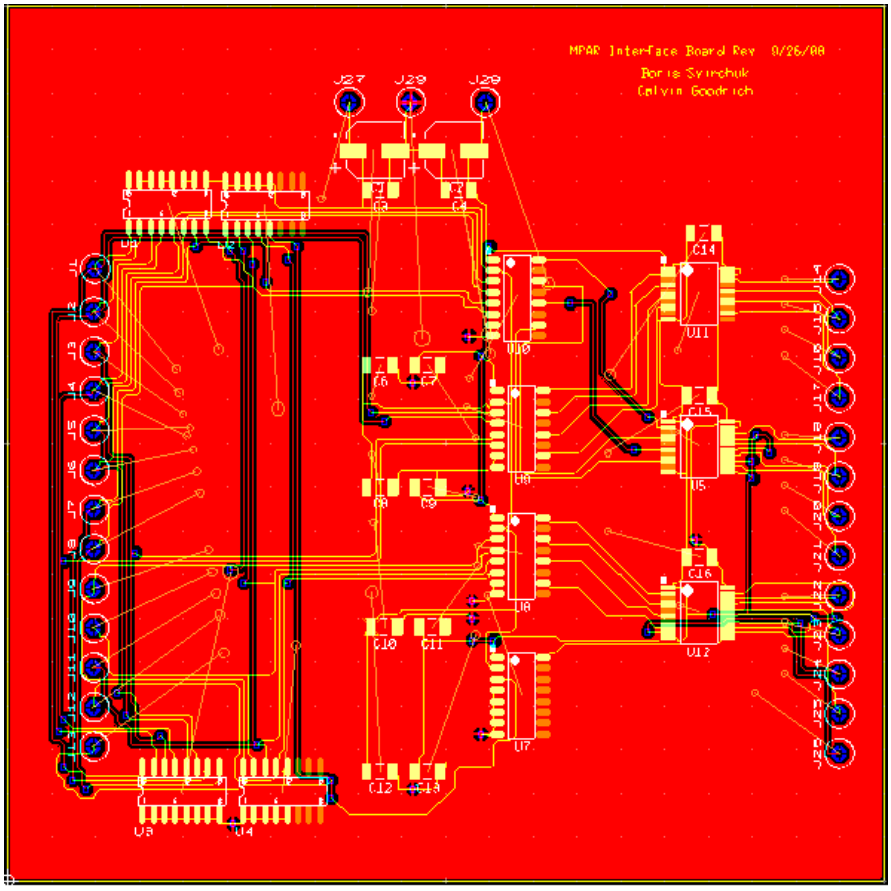


**Figure 26: The PCB layout of the Module Design**
**This figure shows the footprints where all the components will be mounted, in addition to all the traces connecting the components. As can be seen, only eleven ICs are included in this design, with fifteen capacitors.**

When the Multisim schematic shown in Figure 25 was imported to Ultiboard, it was left to the user to arrange the ICs on the PCB design. Figure 26 shows the final layout of the PCB design, with all of the appropriate connections. The footprints for each IC and decoupling capacitors (each is 150nF) are represented on the layout above. Figure 27 shows a 3-D model of the PCB designed with Multisim and Ultiboard.

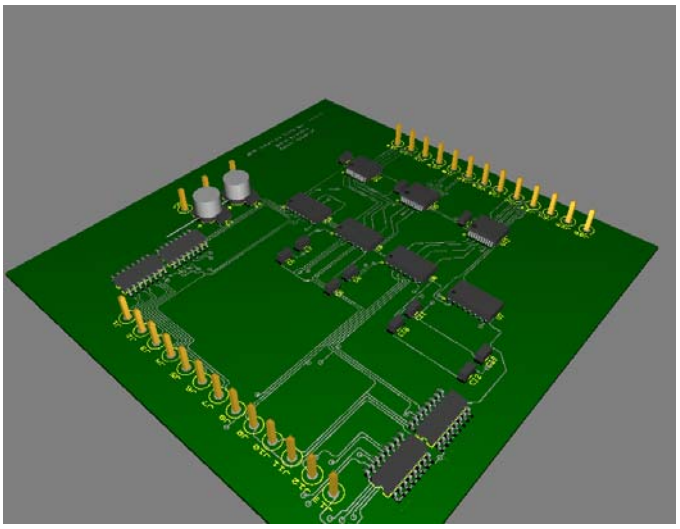

**Figure 27: A 3-D Model of the Module Design PCB**
**A three-dimensional representation of the module design PCB populated with all ICs and capacitors.**

### 4.1.3 – Panel Design

The panel design is the design which will be referenced by Lincoln Laboratory when developing their own interface board for their sixty-four module panel. Figure 28 shows the overall design schematic, the highest-level layout accounting for all data lines and all control lines. The figures following Figure 28 break the design up into sub-components and describe each part of the design. It is important to note that the panel design was developed after testing and verifying the module design, but appears here for the sake of organization.

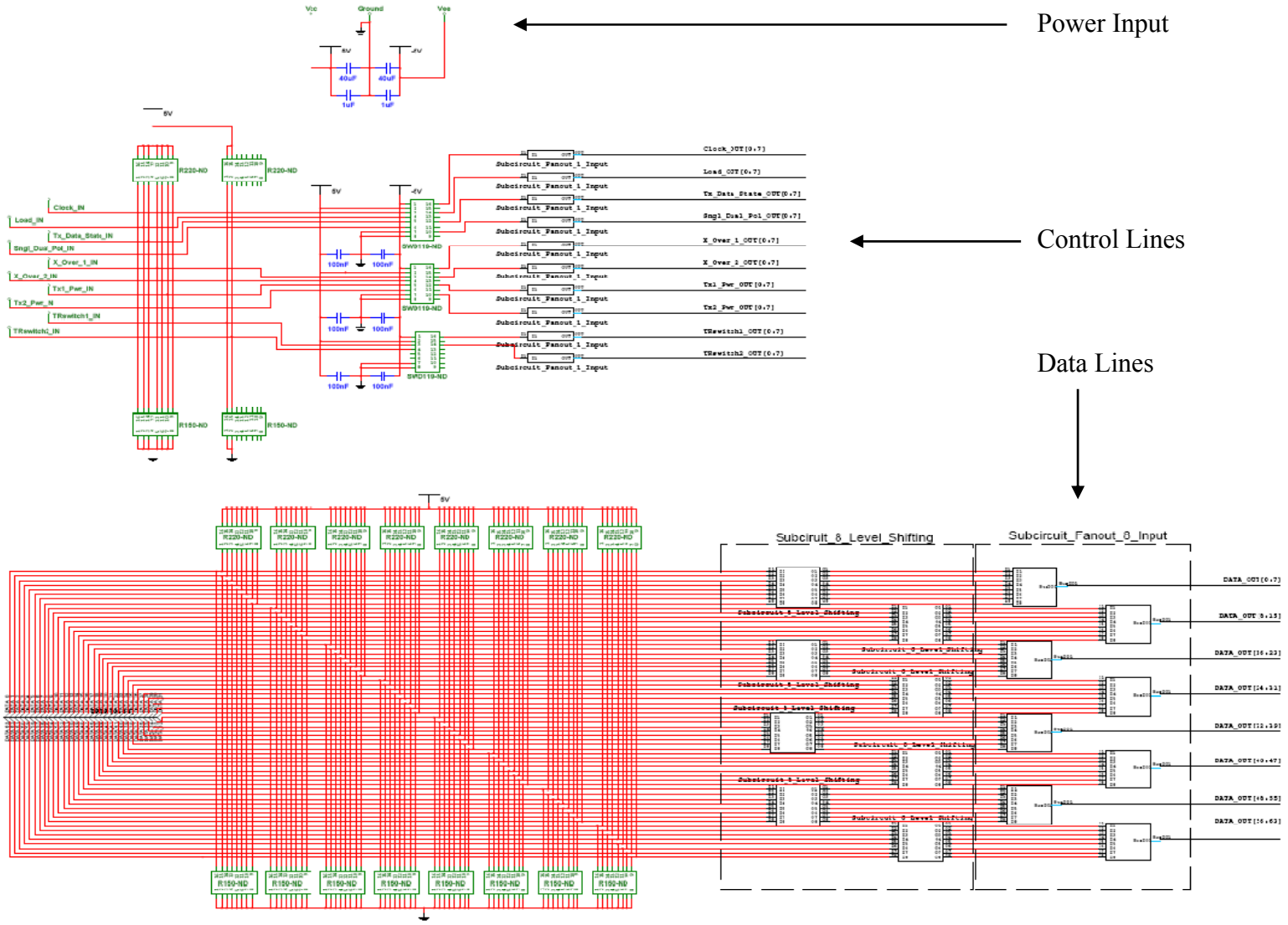


**Figure 28: The Panel Design**

**This schematic is quite large as it accounts for all inputs and outputs. There are three separate sections to the design; the power input, the control lines and the data lines. Use of Multisim's hierarchical blocks, or sub-circuits, are prevalent to simplify the schematic.**

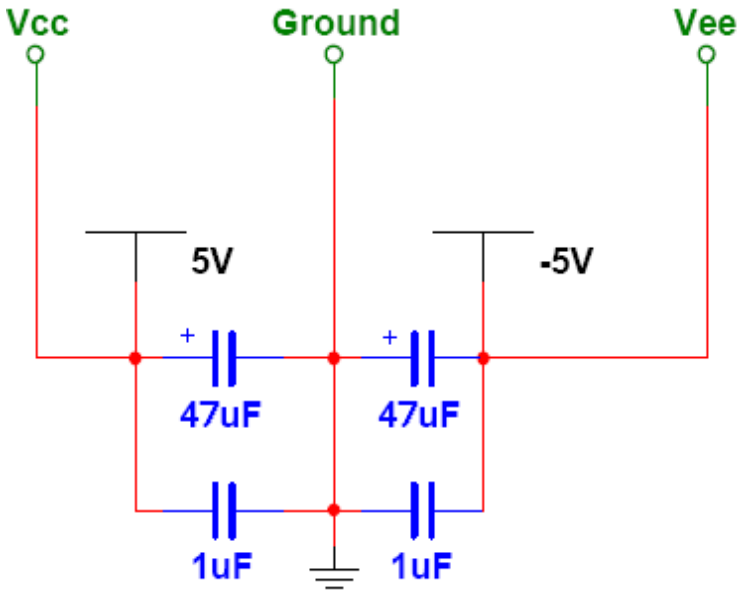


**Figure 29: Panel Design Power Connection to the Interface Board**
**The connection of the +5V, -5V, and Ground are all located at one place on the board. The capacitors are placed between the voltage rails to help "smooth" out any irregularities in the power supply voltage; helping to make sure that the voltage supplied does dip and cause intermittently malfunctions of the ICs on the interface board.**

Figure 29 shows the approach to adding the decoupling capacitors at the power supply inputs on the interface board. 47uF polarized caps and 1uF non-polarized capacitors are used to accomplish this design requirement. These values are standard for this type of application. Figure 30 shows a larger representation of the control lines from input to output. The termination, and level shifting, can be easily observed in this top level schematic. Figure 31 shows the sub-circuit used to fan-out and buffer a single control line to eight separate lines.

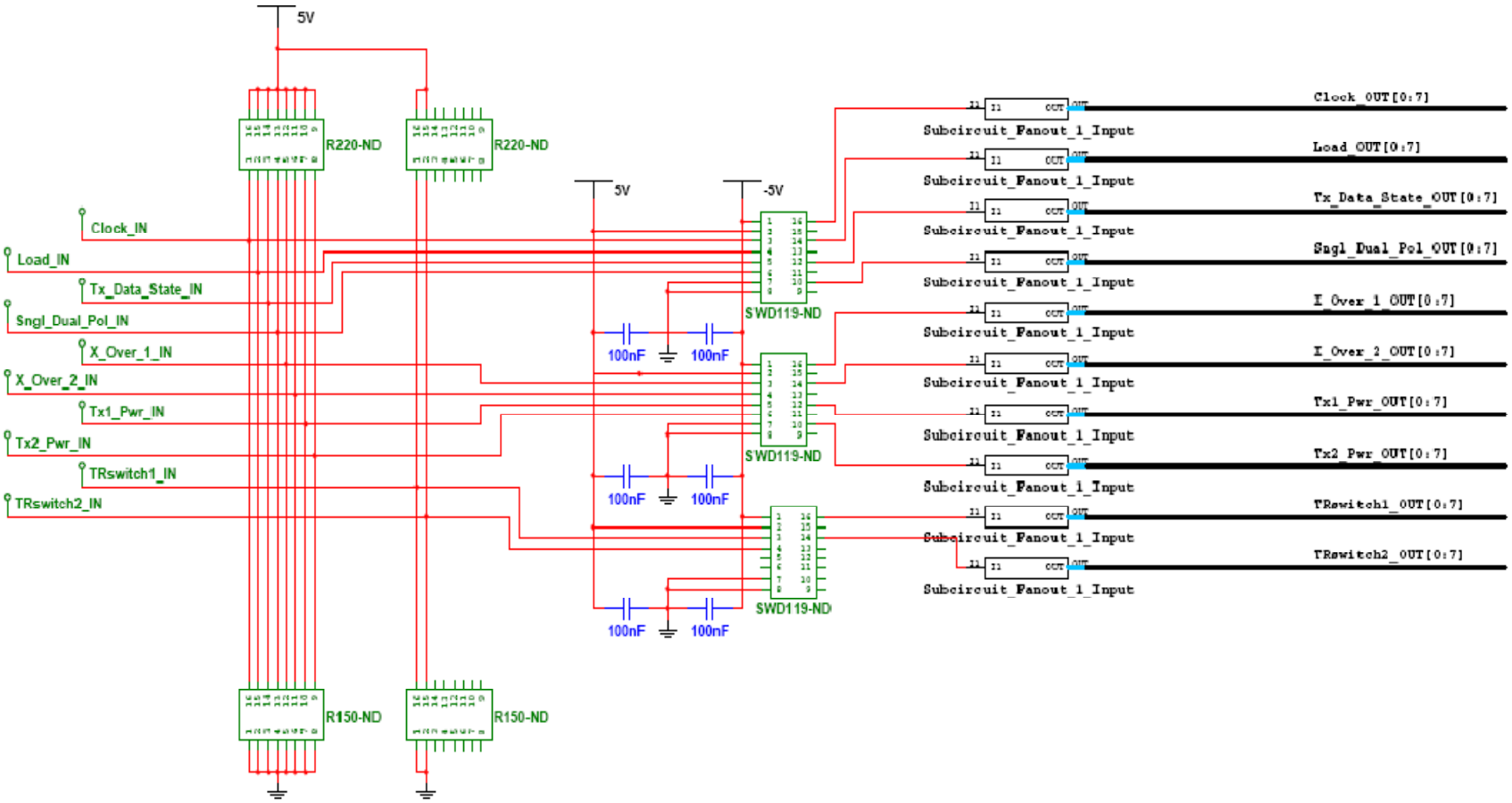


**Figure 30: Panel Design Control Lines**

**All ten control lines are passed through the interface board through similar paths. Upon input the control lines are terminated with network resistors; 220Ohms to Vcc and 150Ohms to Ground. Next, the control lines are level shifted, following the pin-out on the datasheet for the SWD-119. Only the non-inverting outputs (pins 10, 12, 14, 16 or the "A" outputs) are used. Vopt (Pin 7) is connected to Ground, to achieve the requested level shifted voltages. The 0.1uF capacitors are placed close to the Vcc and Vee input pins of each IC to further buffer the input voltages. Following the level-shifters is a fan-out sub-circuit, which outputs a bus of eight replicas of the control lines. The bus is used to ease the presentation of the schematic.**

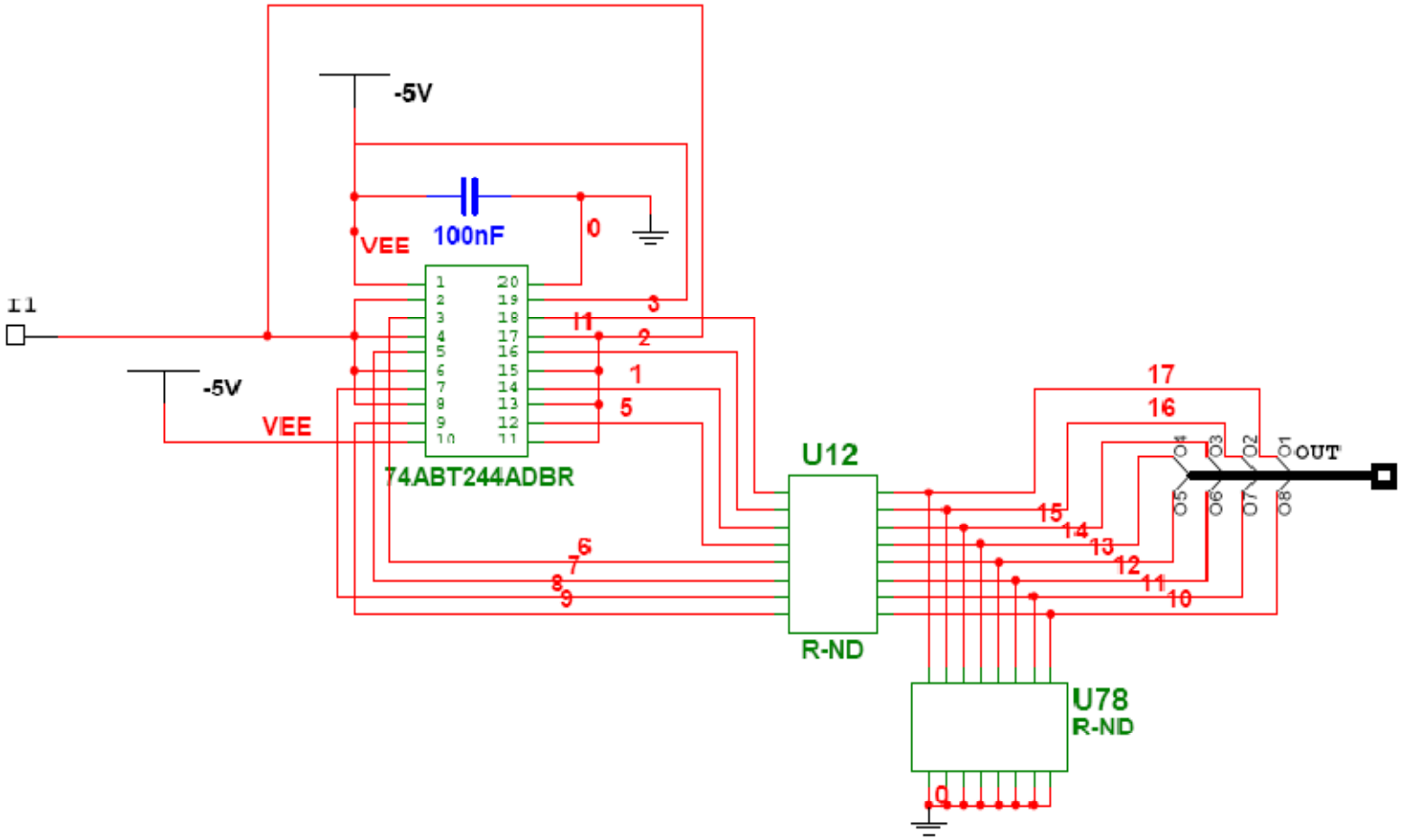


**Figure 31: Panel Design Control Line Fan-Out and Shunt Resistors Sub-Circuit**

**The single input is fanned-out to the input of each of the eight buffers, proving the current needed to drive the control signal to the T/R module. The Ground pin (pin 10) on the IC has been set to Vee and the Vcc pin (pin 20) on the IC has been set to Ground to be able to use the buffers at their level shifted values. Also, pin 1 and pin 19 are the inverted output enable pins for the two sets of buffers in the IC; these pins have been set to Vee (the new ground reference). Upon exiting the buffer a series network resistor of an unspecified value and a pull-up network resistor, to Ground, of unspecified value have been included. These resistor values will be determined later when the T/R modules specifications are resolved.**

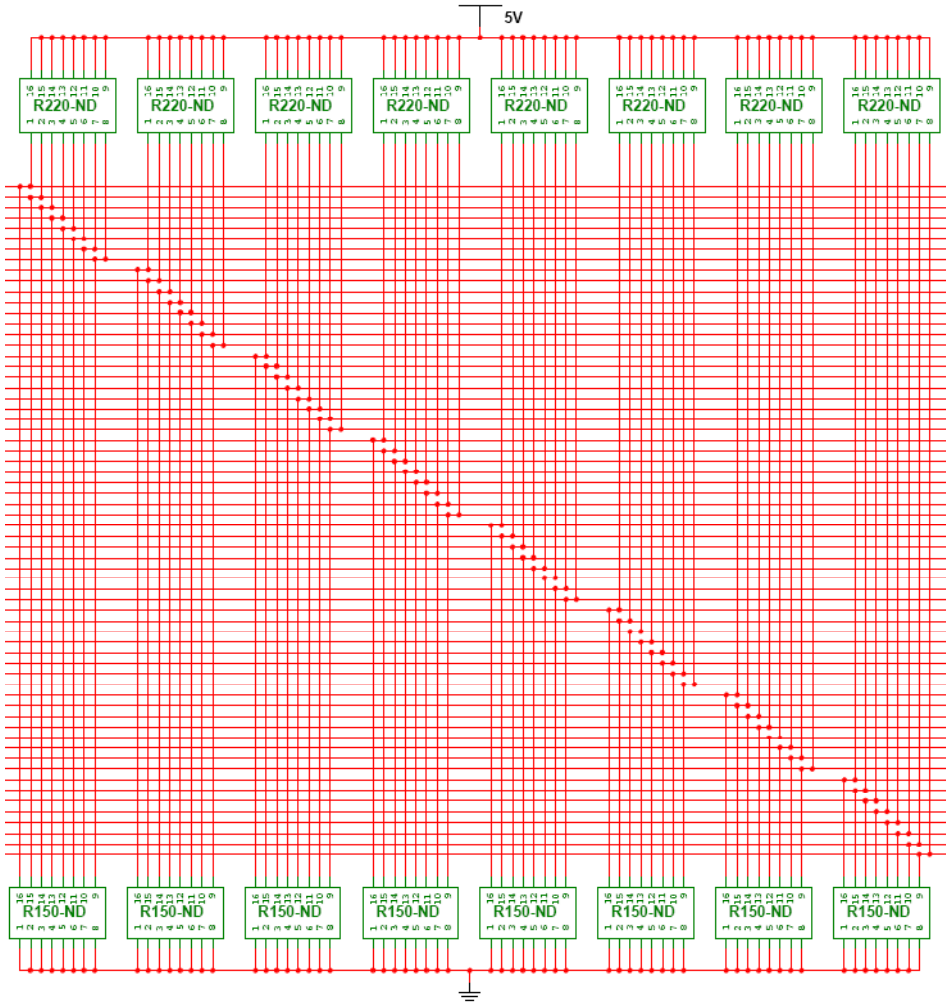


**Figure 32: Panel Design Termination of Data Lines**

**Sixty-four data lines are terminated with eight 220Ω network resistors to Vcc and eight 150Ω network resistors to Ground. The largest amount of leakage current will occur here; 13.5mA per path from Vcc through the network resistors to Ground.**

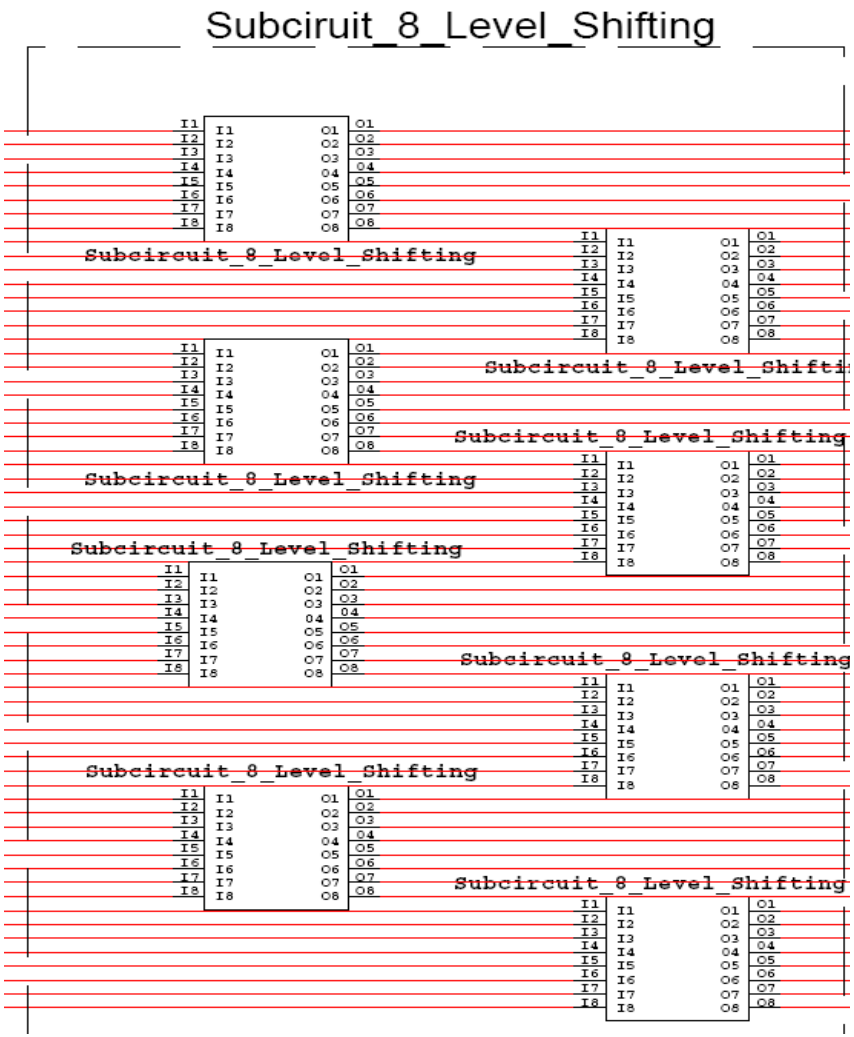


**Figure 33: Panel Design Paths To and From Level Shifting Sub-Circuits**

**This portion of the schematic shows the level shifting sub-circuits. As there are sixty-four data lines and each sub-circuit handles eight data lines, there are eight sub-circuits included.**

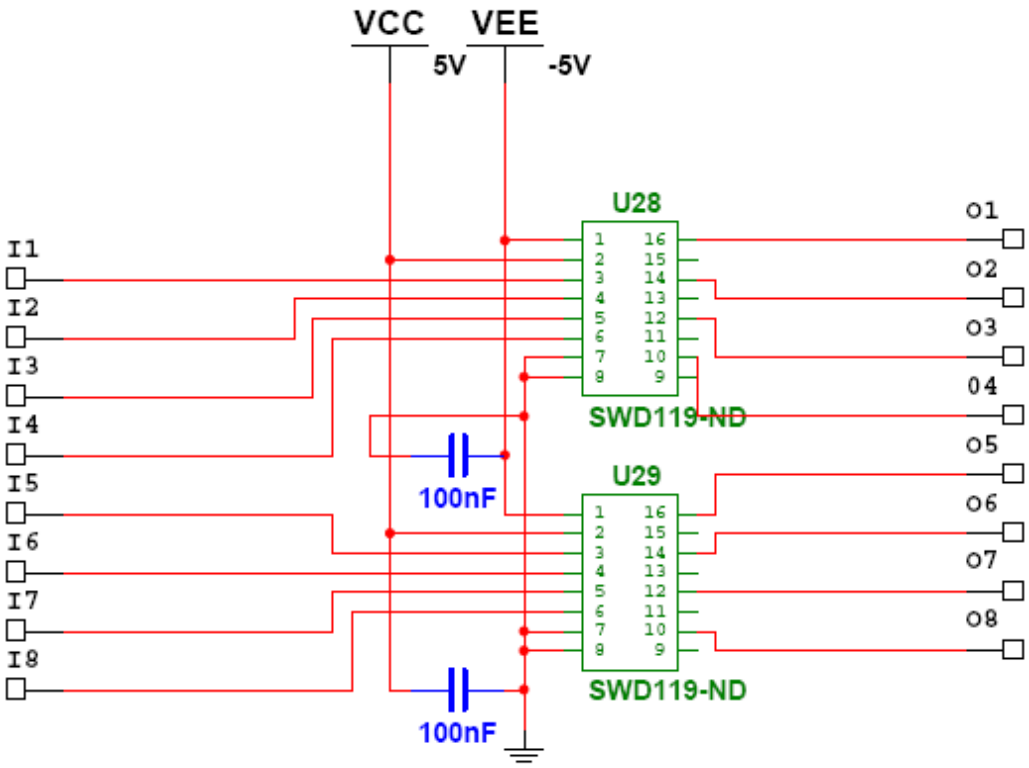


**Figure 34: Panel Design Level Shifting Sub-Circuit**

**As the SWD-119 is a quad channel chip, two chips are needed in this sub-circuit to handle the eight data lines being input. The inputs to this sub-circuit all use 0V to 5V logic voltage levels. At the output of this IC all signals are level shifted to -5V to 0V logic voltage levels. Only the non-inverting outputs (pins 10, 12, 14, 16 or the "A" outputs) are used. Vopt (Pin 7) is connected to Ground to achieve the requested level shifted voltages. The 0.1uF capacitors are placed close to the Vcc and Vee input pins of each IC to further buffer the input voltages.**

Figure 32 shows the termination of all sixty-four data lines. The largest amount of leakage current will occur here; 13.5mA per path from Vcc through the network resistors to Ground. Figure 34 shows the how the data lines are level shifted, in the same manner as the control lines.

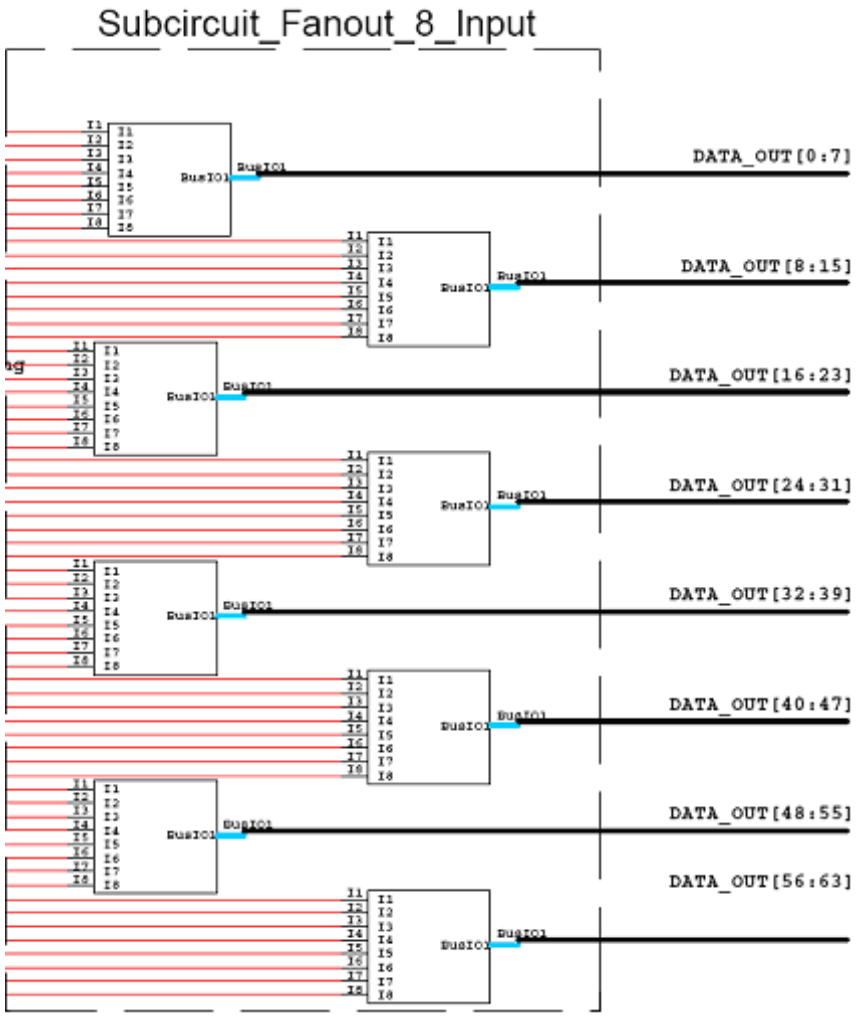


**Figure 35: Panel Design Paths To and From the Buffering Sub-Circuit**

**Each buffering sub-circuit handles eight data lines, and outputs the eight data lines in a bus. The busing symbols may or may not be used by Lincoln Laboratory.**

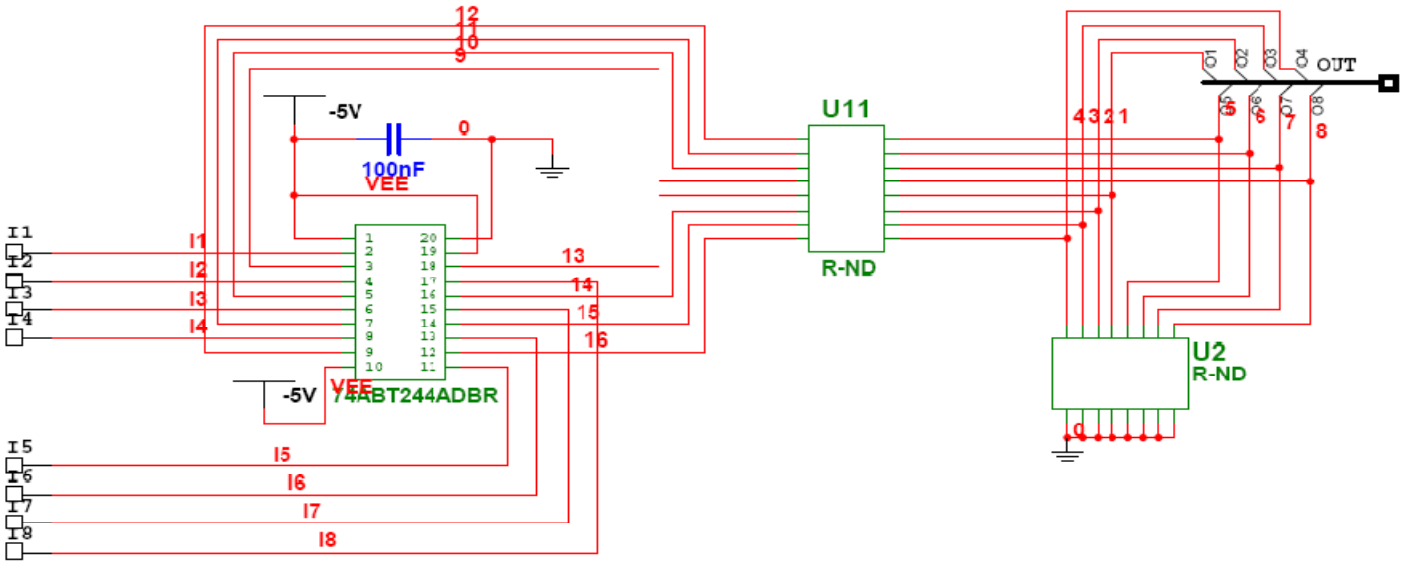


**Figure 36: Panel Design Data Line Buffering Sub-Circuit**

**Eight separate data lines are passed into this sub-circuit and are buffered by the SN74ABT24A octal buffer. The Ground pin (pin 10) on the IC has been set to Vee and the Vcc pin (pin 20) on the IC has been set to Ground to be able to use the buffers at their level shifted values. Also, pin 1 and pin 19 are the inverted output enable pins for the two sets of buffers in the IC; these pins have been set to Vee (the new ground reference). Upon exiting the buffer a series network resistor of an unspecified value and a pull-up network resistor, to Ground, of unspecified value have been included as requested by Lincoln Laboratory. The data lines are grouped into a bus on the output of the sub-circuit.**

Figure 36 shows how the data lines are not fanned out, but still require the use of the buffer to provide current to drive the cable which sends the signals at the output of this circuit to the radar array. Notice how Vcc (Pin20) is grounded and GND (Pin 10) is set to -5V, allowing the operation of the buffer at the shifted voltage levels.

## *4.2 – Test Results*

This section includes a collection of oscilloscope images from a series of different tests performed on the interface board. The major variables considered for testing were input signal, output cable length, output test location, and output cable termination. Also, there is a section which discusses differential propagation delay. Each caption lists the information needed to distinguish what the image is testing. The first piece of information is cable length (No cable, 1m, or 3m), the second is output location (PCB output or SWD-119 output), the third is whether or not the signal has been terminated on the output, and the last is the input (static voltage, 1 MHz, or 20MHz). Thevenin termination is accomplished with a 220Ω resistor to Ground and a 330Ω resistor to -5V. The input waveforms are either static voltages of 0V and 5V or are a square wave with 5V peak to peak and offset by 2.5V, therefore exhibiting voltages of 0V and 5V at the input.

For the following oscilloscope images, information regarding the axis scales is located across the bottom. The offset on the voltage scale is at different locations on a number of images, however 0V is determined by the marker on the left side of the image. The value of the offset can be found in the bottom left corner of the images. The timescale is found near the bottom right of the images.

## 4.2.1 – Static Voltages

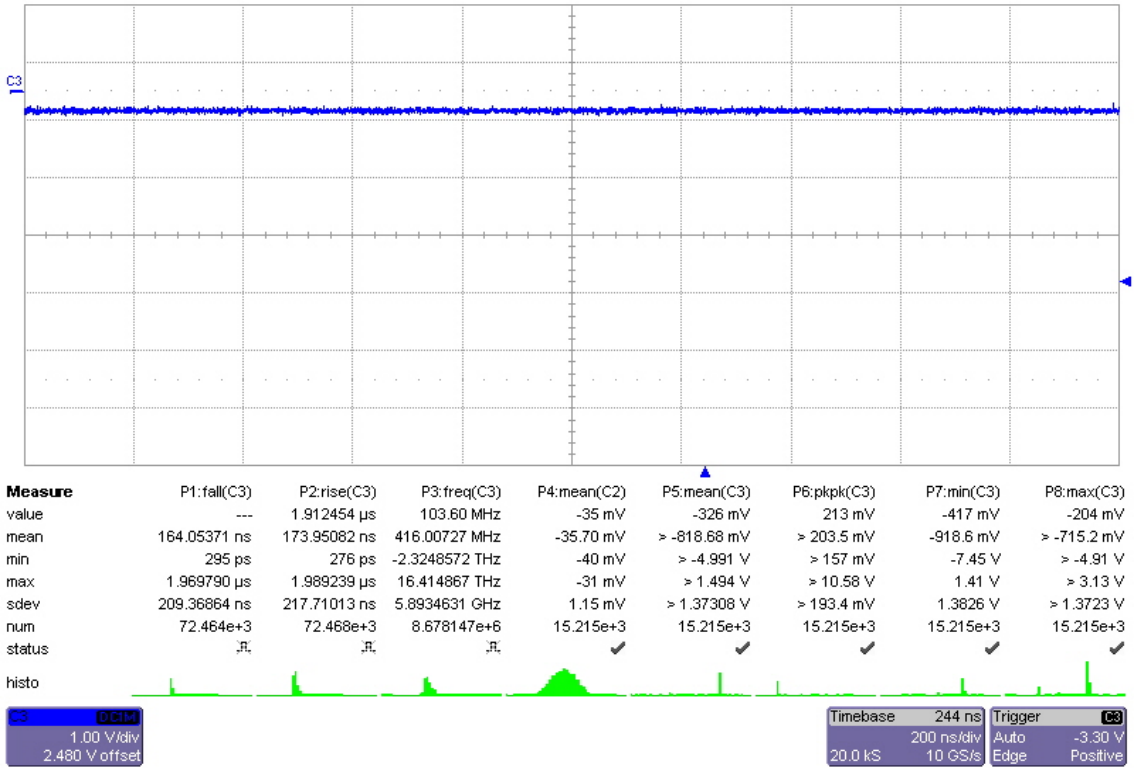


**Figure 37: No Cable, PCB Output, No Termination, Static 0V Input**

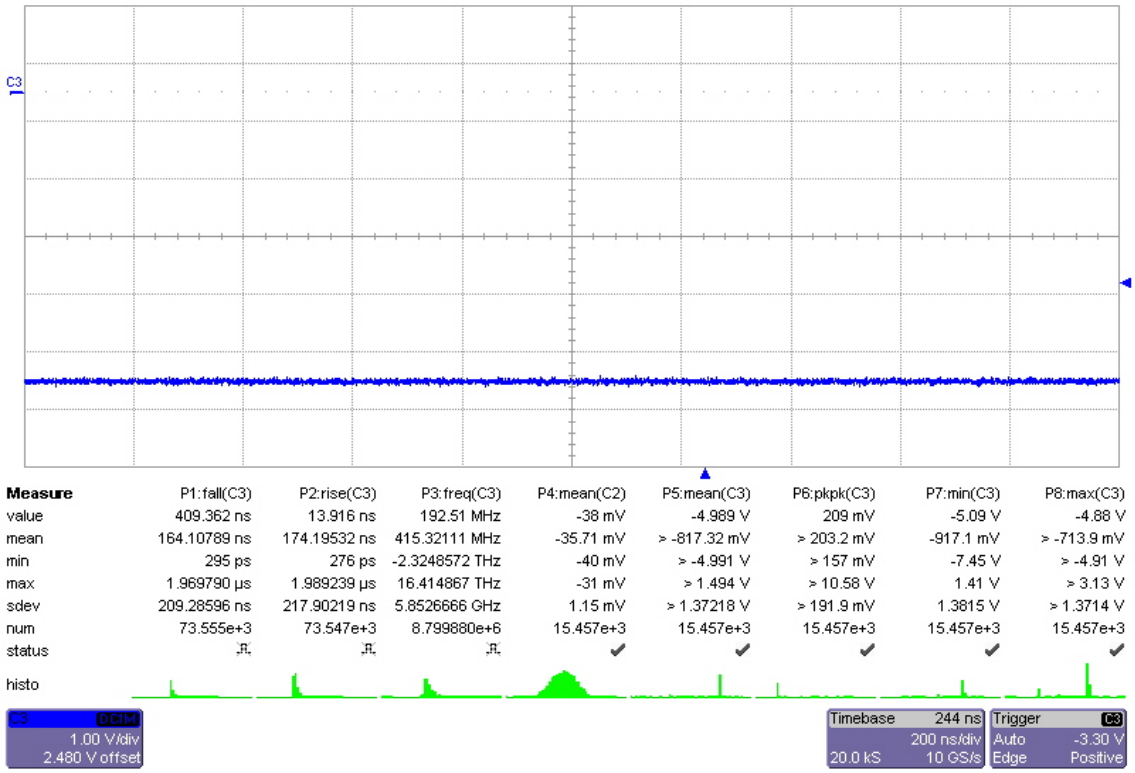


**Figure 38: No Cable, PCB Output, No Termination, Static 5V Input**

Figure 37 and Figure 38 show the results of a static 0V and 5V input at the output of the PCB with no termination. The most notable feature about these figures is that the output is inverted from what would be expected. If the input voltage is 0V, the output should be -5V. Instead, the output voltage is shown in Figure 37 to be -0.326V. Vice-versa in Figure 38, when the input voltage is 5V the output is expected to be 0V, while in fact it is -4.989V.

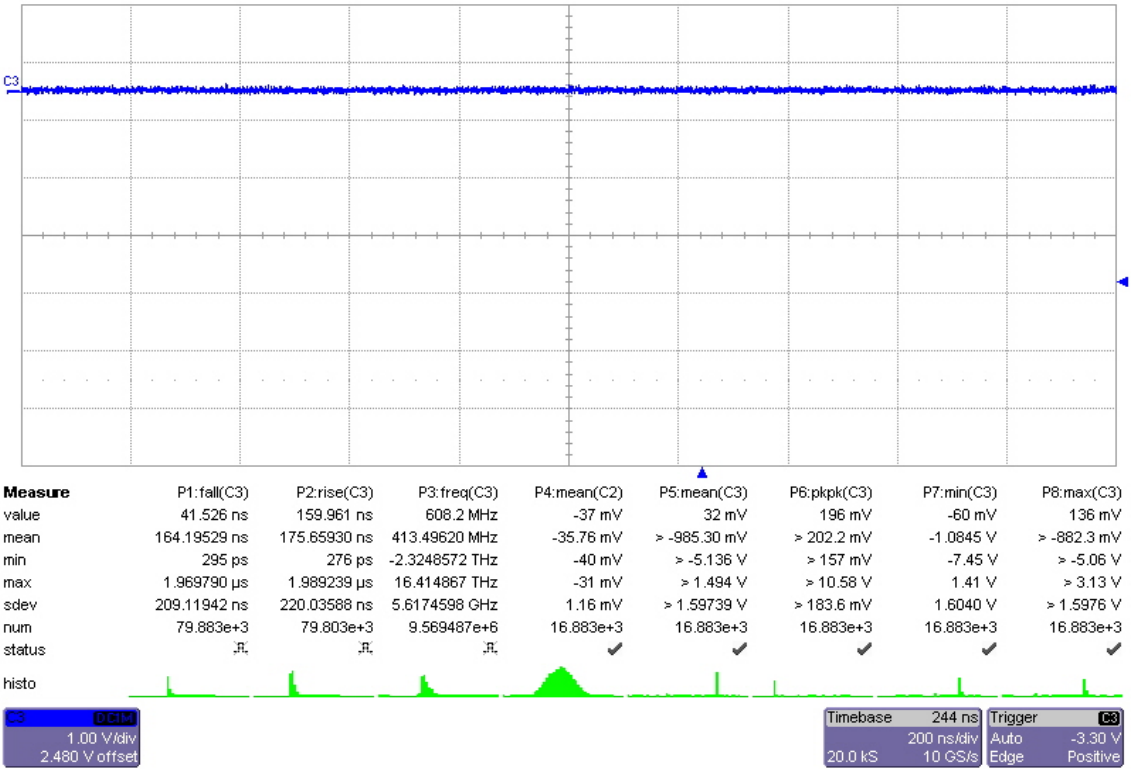


**Figure 39: No Cable, SWD-119 Output, No Termination, Static 0V Input**


**Figure 40: No Cable, SWD-119 Output, No Termination, Static 5V Input**

The only difference between output of the PCB and the output of the SWD-119 in this static test is that the output of the SWD-119 has a voltage truer to the voltage rails. The output of the PCB, Figure 37 and Figure 38, are -0.326V and -4.989V where as the output voltages of the SWD-119 are 0.032V and -5.008V. All of these voltage values have been taken without a cable or termination. Therefore, without a simulated load, the output voltage values are expected to be within specification of the IC, near the voltage rail supplies.

### 4.2.2 –Output Test Location

The following section contains comparisons between the PCB output and the SWD-119 output at 1MHz and 20MHz input signals. As in the previous cases, cables have been used in testing these cases and the point of measurement remains at the end of the cable. The location of the cable interface to the PCB is what differs in these cases.

## 4.2.2.1 – 1MHz 0V-5V Square Wave Input


**Figure 41: 3m Cable, PCB Output, Terminated, 1MHz Square Wave Input**

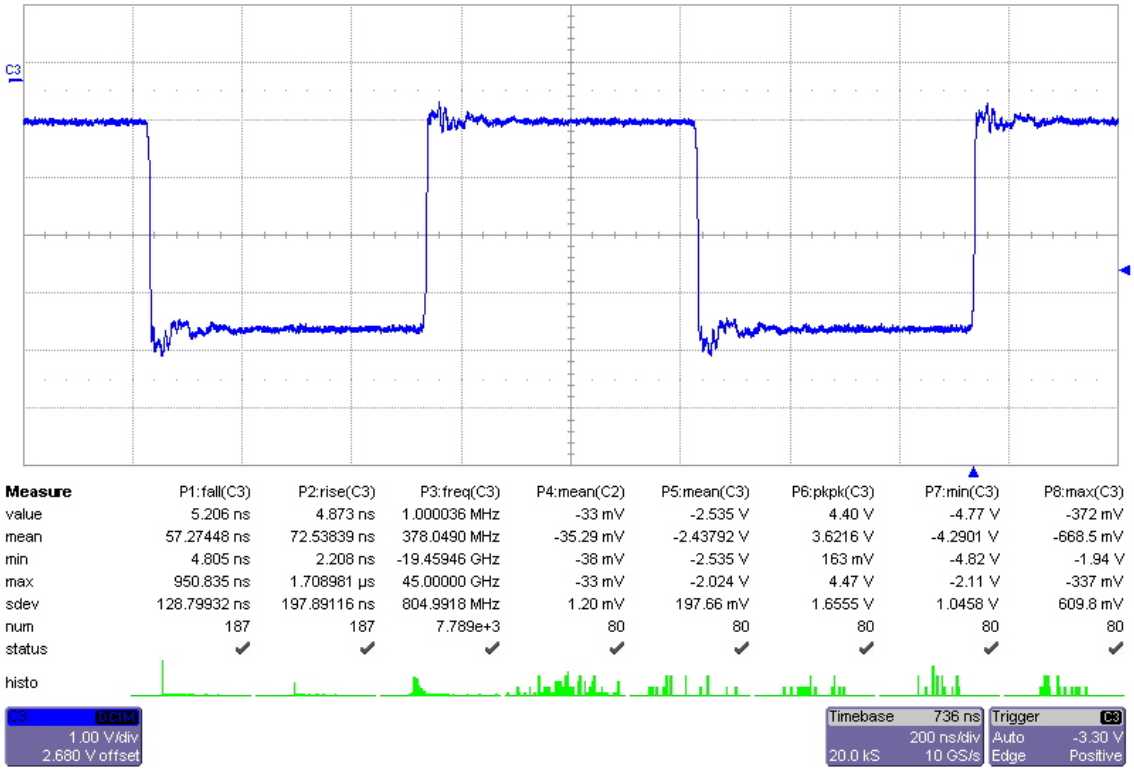


**Figure 42: 3m Cable, SWD-119 Output, Terminated, 1MHz Square Wave Input**

These results were taken using a three meter cable with an input signal of 1MHz in frequency. The main point of these images is to show how the PCB output exhibits much more ringing than the SWD-119 output. Also, the SWD-119 output has a mean voltage around -2.54V, unlike the mean -3.24V of the PCB output; remember that the mean of the input voltage is 2.5V. With the reduced ringing, and stable logic voltage levels, it would seem that the SWD-119, promises better output voltages than the buffer at 1MHz.

## 4.2.2.2 – 20MHz 0V-5V Square Wave Input

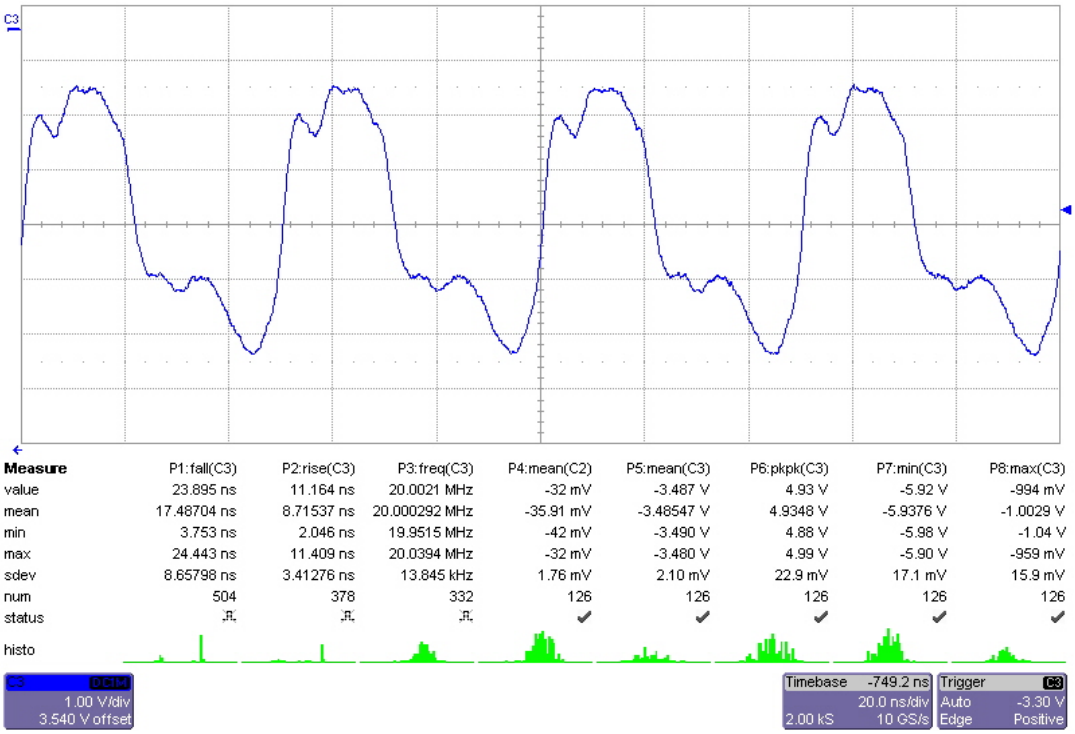


**Figure 43: 3m Cable, PCB Output, Terminated, 20MHz Square Wave Input**

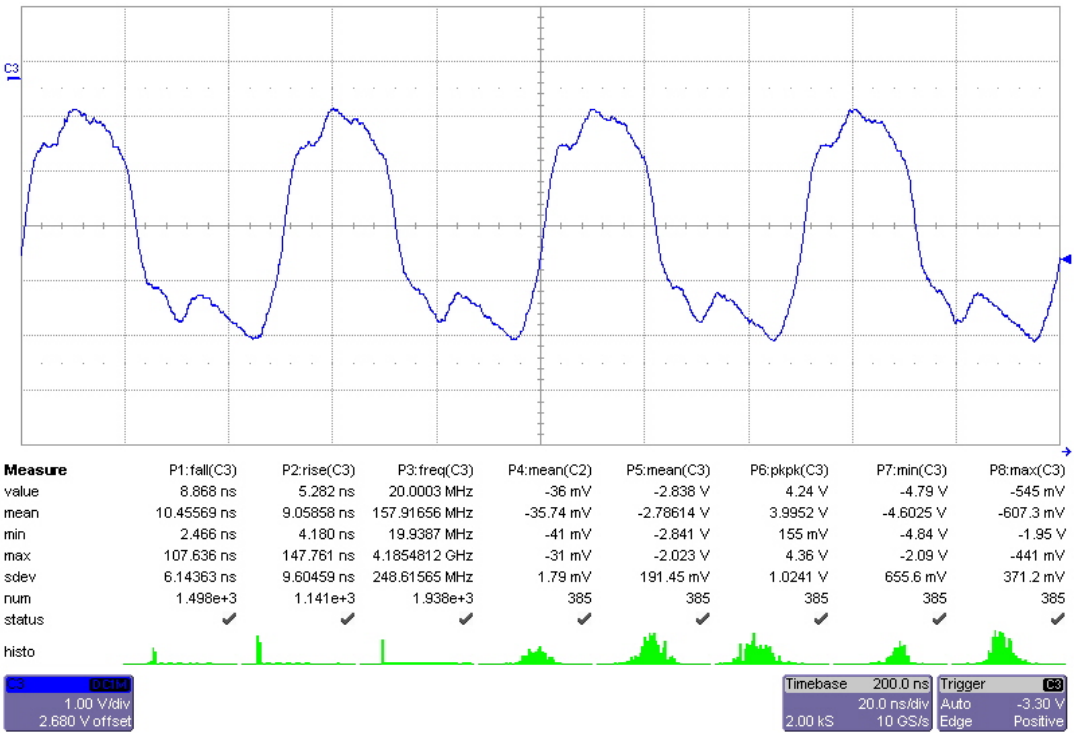


**Figure 44: 3m Cable, SWD-119 Output, Terminated, 20MHz Square Wave Input**

Figure 43 and Figure 44 show that at 20MHz the output of the PCB and the SWD-119 are similar in the fact that both no longer represent a square wave. In fact, the SWD-119 output is more smoothed out than the PCB output, leaving it to resemble more of a sine wave. One thing is for certain, these signals cannot be used in the T/R modules. There are no clear high or low logic voltage levels, and therefore determining a logic state would prove difficult. The rippling during the high and low logic voltages is so severe that there is no clear way to determine the voltages.

### 4.2.3 – Output Cable Length

Although the cable connecting the interface board to the radar array has been estimated to be around three meters in length, it was requested by the lead Lincoln Laboratory engineers to test using no cable, a twisted-pair flat one meter cable, and a twisted-pair flat three meter cable. The following sections show the effect of increasing cable length when passing the 1MHz and 20MHz square waves. The 1MHz input waveform represented a square wave quite well, while the 20MHz input waveform showed very slight overshoot on its edges.

#### 4.2.3.1 – 1MHz 0V-5V Square Wave Input

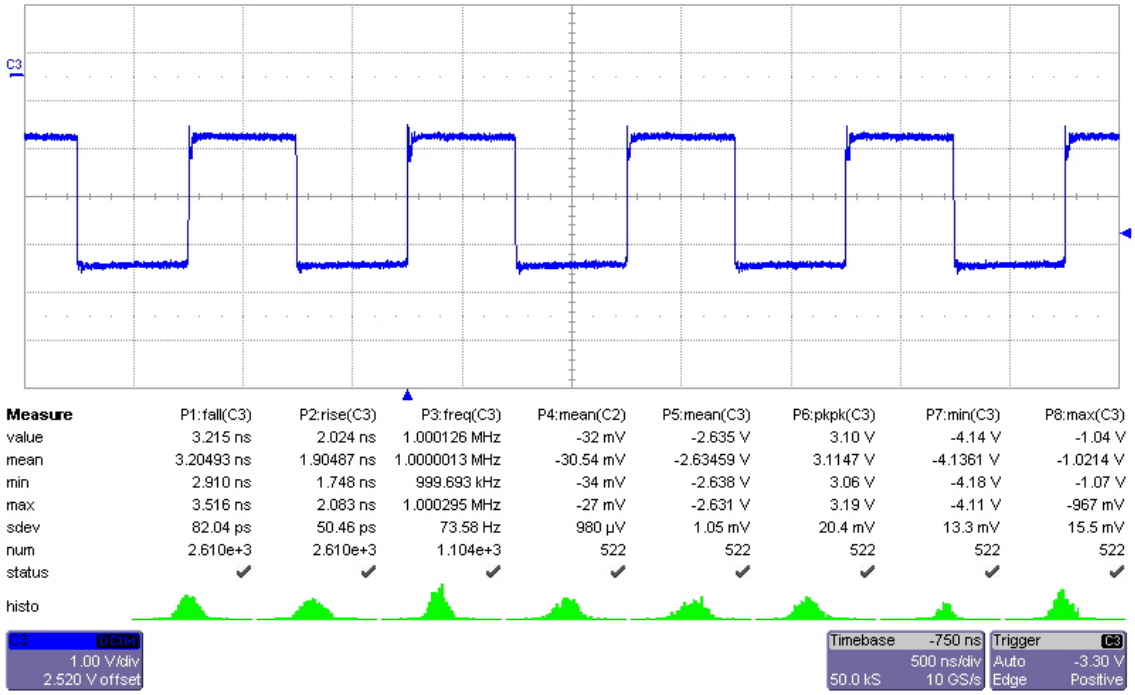


**Figure 45: No Cable, PCB Output, Terminated, 1MHz Square Wave Input**


**Figure 46: 1m Cable, PCB Output, Terminated, 1MHz Square Wave Input**


**Figure 47: 3m Cable, PCB Output, Terminated, 1MHz Square Wave Input**

**Note: This figure is the same as Figure 41, and is presented again here for ease of comparison to the data in Figure 46.**

Figure 45, Figure 46, and Figure 47 show how a difference in cable length affects a 1MHz square wave (0V-5V) input, from the output of the PCB. The main feature to notice in these three images is how an increase in cable length increases the amplitude and duration of ringing on the edges of the output. With the three meter cable, the duration of ringing is longer than a full period of 20MHz, which highlights a problem to be observed at the higher frequency. At 1 MHz the signal is clearly recognizable, and the peak to peak voltage is approximately the same for all waveforms, between 2.8 V and 3.1V. Figure 45 shows a minimum voltage of approximately 4.1V, which with ringing will cause the digital circuitry to misinterpret the signal; however in this case the signal is not driving a cable. In the cable driving cases the low voltage levels are near -4.5V, which is hopefully within tolerance for the T/R modules.

### 4.2.3.2 – 20MHz 0V-5V Square Wave Input

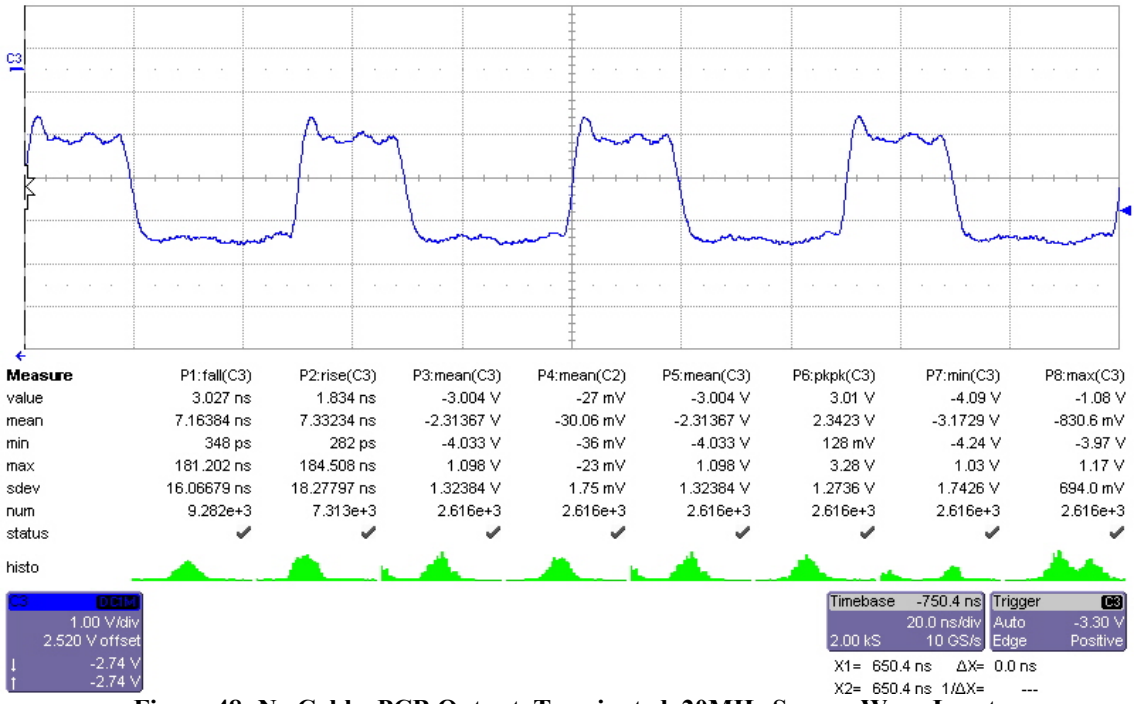


**Figure 48: No Cable, PCB Output, Terminated, 20MHz Square Wave Input**

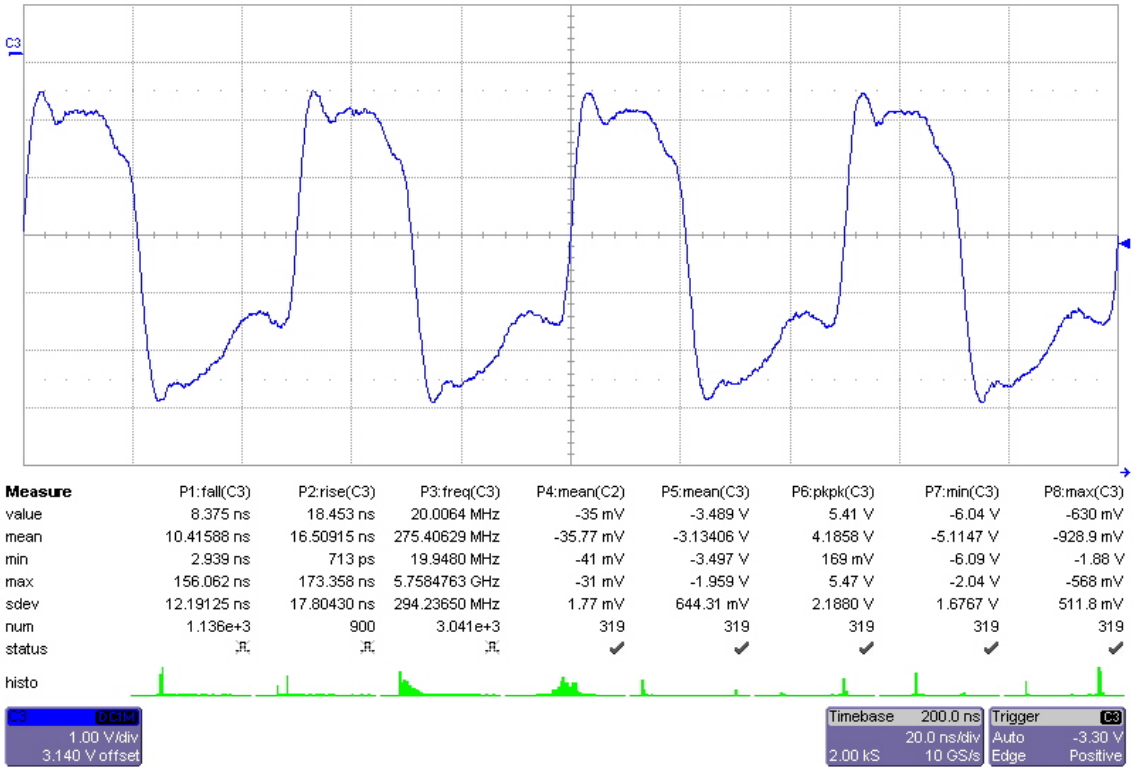


**Figure 49: 1m Cable, PCB Output, Terminated, 20MHz Square Wave Input**

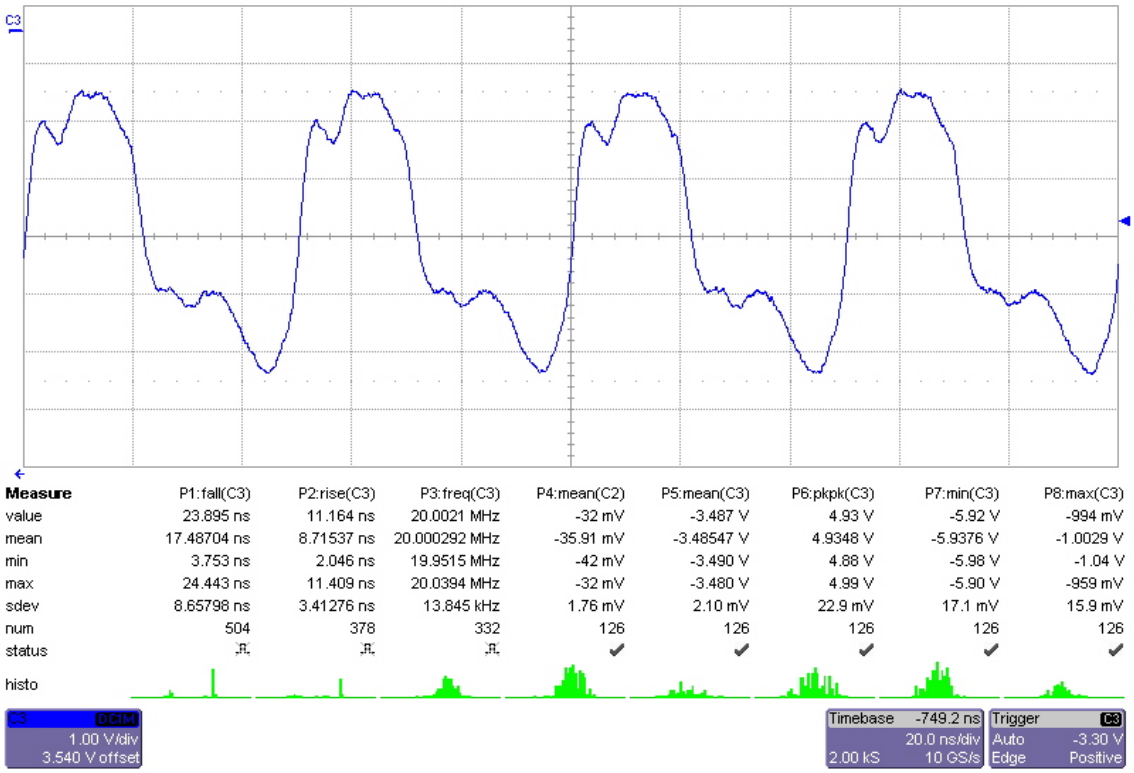


**Figure 50: 3m Cable, PCB Output, Terminated, 20MHz Square Wave Input**

**Note: This figure is the same as Figure 43, and is presented again here for ease of comparison to the data in Figure 49.**

Figure 48, Figure 49 and Figure 50 also show how cable length affects the output signal. Within these images, however, the signal is at a much higher frequency of 20MHz. Without a cable connected, the signal is very much still representative of a square wave; however the high logic voltage is rippled. As the cable length increases to a single meter, the output signal begins to become messy as a shoulder begins to develop, severely limiting the ability to distinguish which state the signal is in. As the cable extends to three meters, the signal is even more unreadable due to the rippling effects observable in the 1MHz output waveform, . As mentioned before, the 20MHz signal period falls within the duration of the ringing seen at 1MHz.The rippling of the voltages provides a peak to peak voltage range of approximately 5V; however the mean voltage is shifted from -2.5V to -3.5V. This means that the maximum voltage is near 1V while the minimum voltage is approximately -6V, with overshoot.

### 4.2.4 – Output Cable Termination

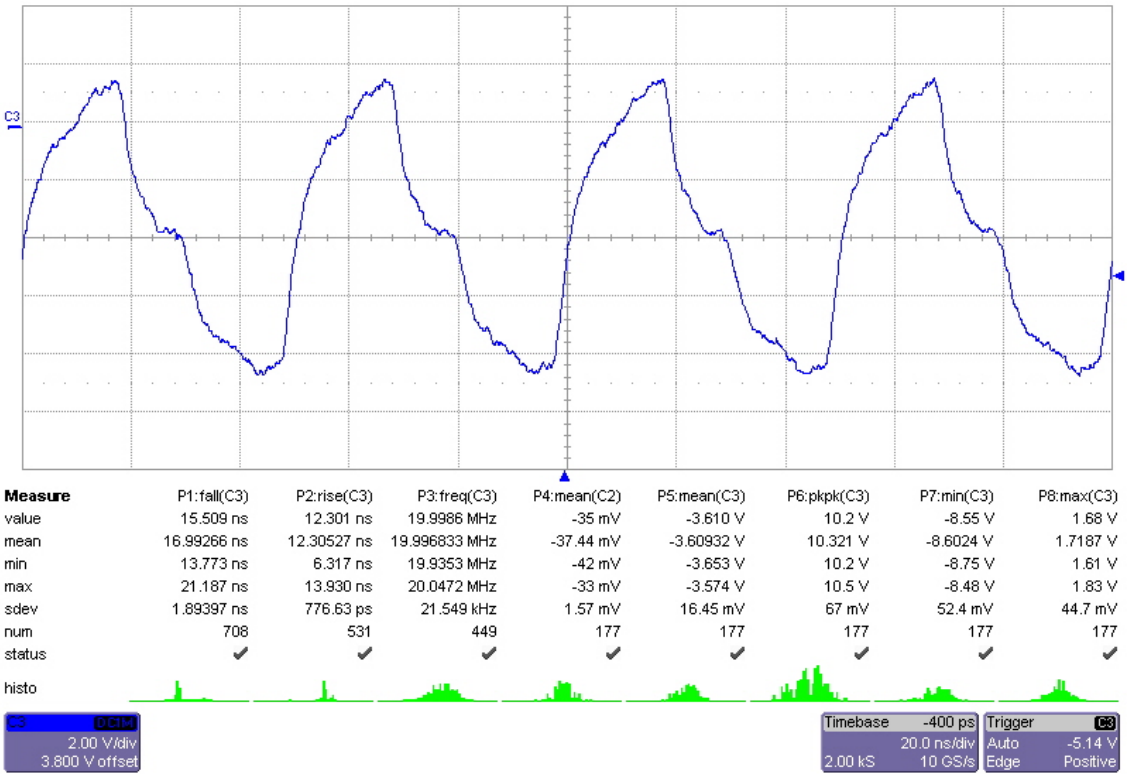


**Figure 51: 3m Cable, PCB Output, 1KΩ Pull-Up Termination, 20MHz Square Wave Input**

Observing Figure 51 shows that using a 1KΩ termination resistor on the end of the three meter output cable increases output waveform peak to peak voltage to 10.2V; Figure 51 expresses the voltage divisions as 2V/Div. The single pull up resistor also severely degrades signal integrity by forming the output into a triangle-looking waveform. Figure 50 shows the 220Ω/330Ω Thevenin termination technique, through the same three meter cable. The output, using this technique, does not exhibit the a large peak to peak voltage, showing an expected 4.93V peak to peak.

### 4.2.5 – Differential Propagation Delay

One of the most important design constraints was to make sure that the signals arrived at the output within 50ns of each other, ensuring proper loading of information from the signal lines into the T/R module. Testing the same signal through two separate paths on the interface board was fairly simplistic. The differential propagation delay was measured at 1MHz and 20MHz, with no cable and no termination and with a three meter cable with termination

Figure 52, Figure 53, Figure 54, and Figure 55 each show that the differential propagation delay does indeed fall below the 50ns margin. At worst case, a 12.3ns differential was measured leaving 37.3ns of time remaining in the margin. The differential propagation time is listed in the bottom right hand corner of the following images marked with a red circle. The value in the red circle is the differential time, in ns, between the two vertical measurement bars in each of the figures.

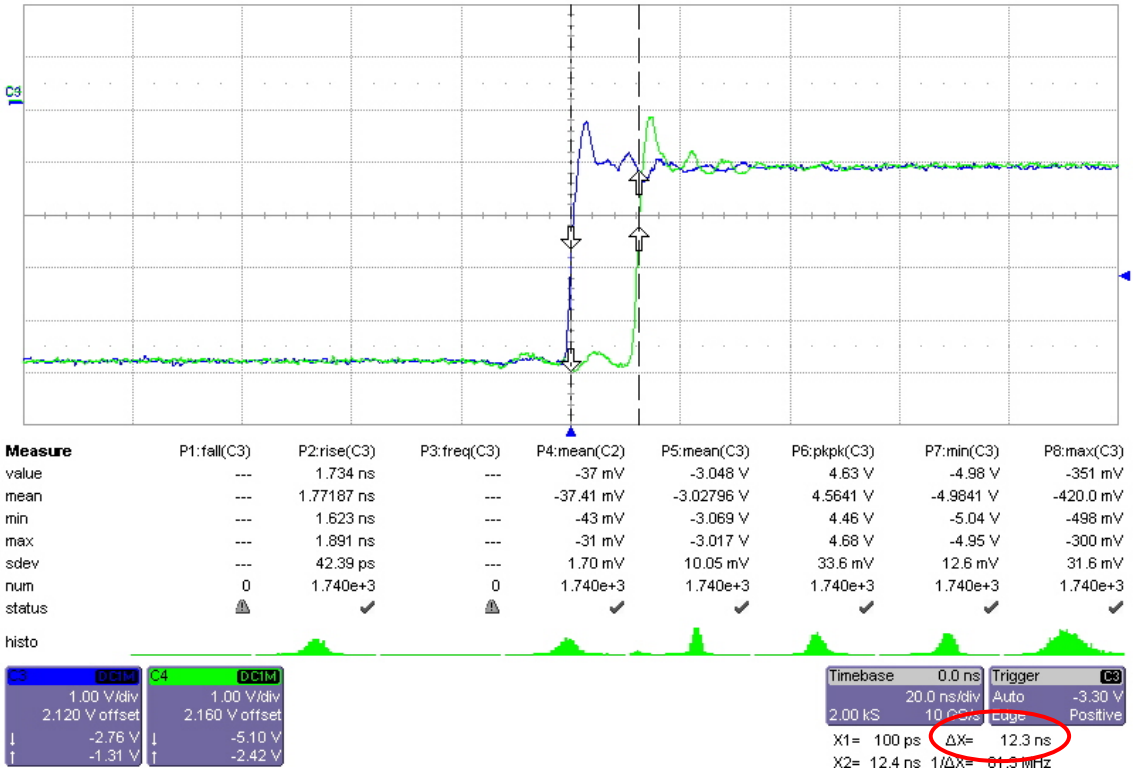


**Figure 52: Differential Propagation – No Cable, PCB Output, No Termination, 1MHz Square Wave Input**

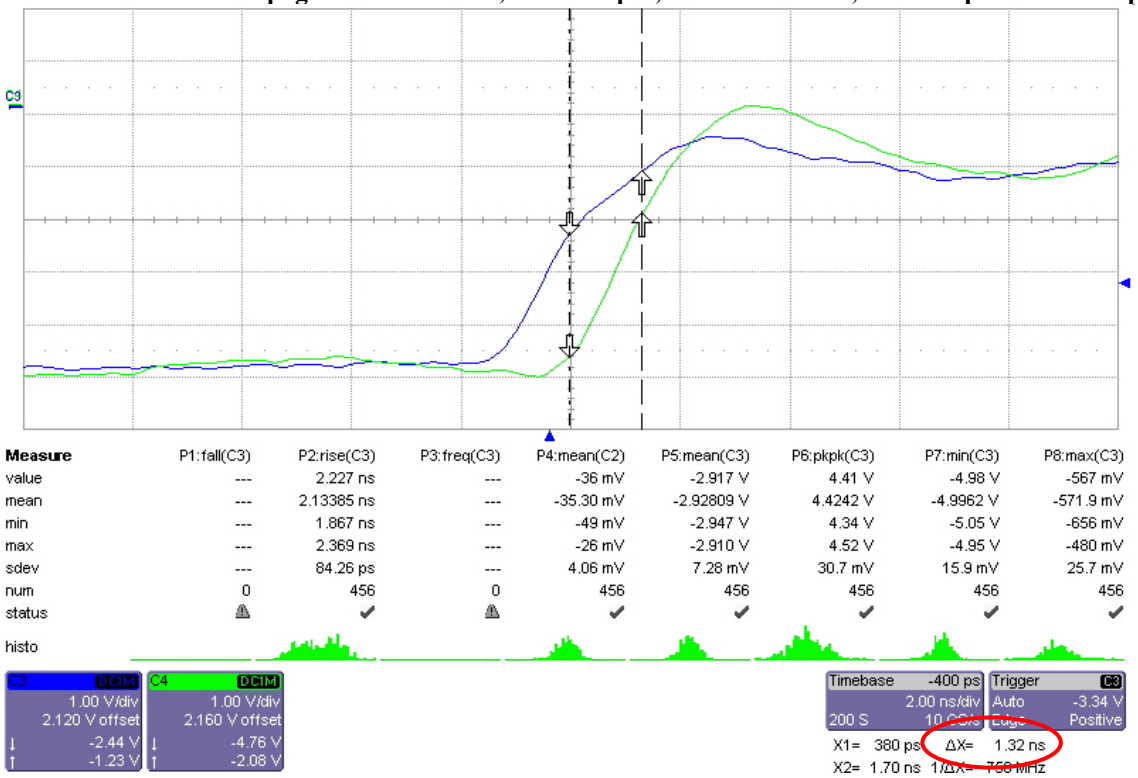


**Figure 53: Differential Propagation – No Cable, PCB Output, No Termination, 20MHz Square Wave Input**

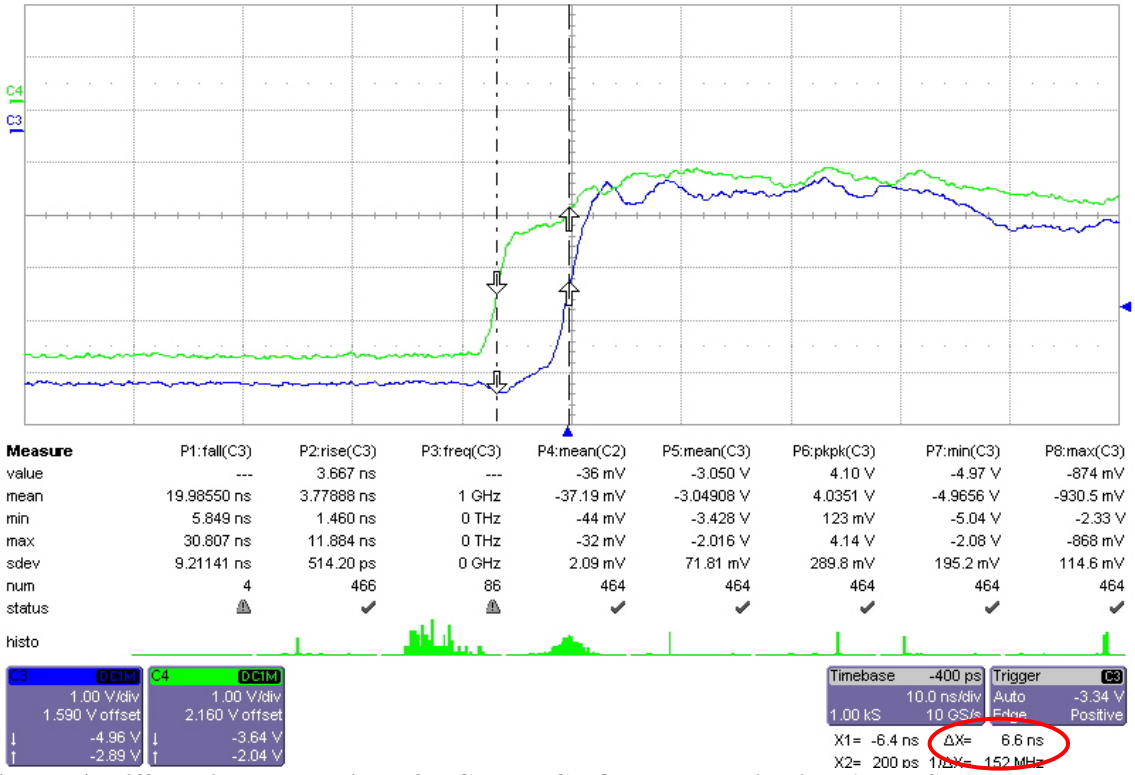


**Figure 54: Differential Propagation – 3m Cable, PCB Output, Termination, 1MHz Square Wave Input**

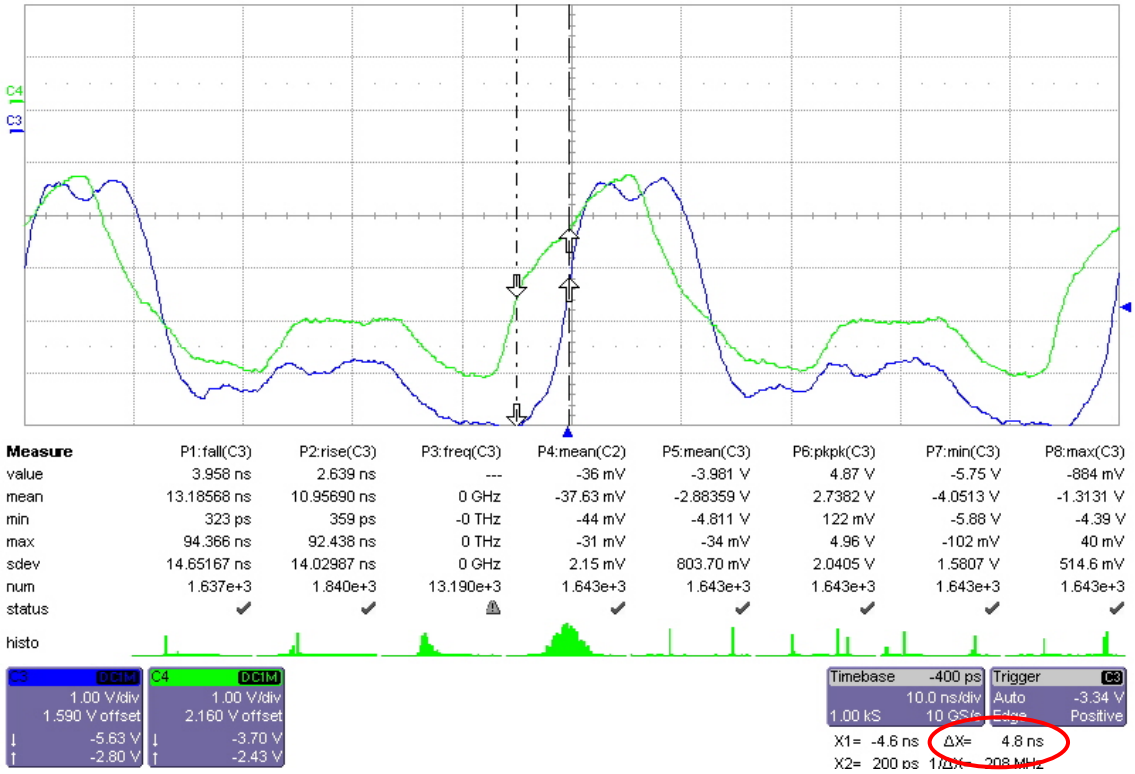


**Figure 55: Differential Propagation – 3m Cable, PCB Output, Termination, 20MHz Square Wave Input**

# 5.0 – Discussion

The differences in input waveform, output test location, output cable length, output cable termination, and differential propagation delay will be discussed to advance the development of the interface board. At the conclusion of the discussion, a restatement of project goals and requirements will be made and an analysis of the project's progression toward these goals will be reviewed. Figures have been repeated in this section for the ease of the reader to compare between the different scenarios being described.

## *5.1 – Static Voltages*

The fundamental operation of the interface board was confirmed with the static tests, however an inversion was observed on the output. When +5V is present at the input of the PCB the output is expected to be 0V, and when 0V is at the input of the PCB the output is expected to be at -5V. Instead, when +5V is at the input the output showed -5V and when 0V is at the input the output showed 0V. This inversion was traced back to the SWD-119 IC. The IC which is used in this project is a new, unreleased revision of the SWD-119; however no datasheet accompanies the new revision. Therefore, the datasheet for the older revision was referenced when determining the connections to the IC; see Appendix 9.2.2 for the datasheet. Apparently, the new revision of the SWD-119 inverses the outputs, inversing the truth table in the datasheet explaining the output connections. There are two outputs for each channel of the IC, labeled A and B, which are inverses of each other. The module design PCB utilized the A output, while it should have used the B output. For the purpose of subsequent testing with square waves, this inversion could be ignored.

The testing was done at two different points on the circuit board: at the output of the PCB, and at the output of the SWD-119 IC. The second testing point was introduced bypassing the SN74ABT244A buffer to be able to analyze the buffer's effect on the signal. The results from the static voltage tests show that the output of the SWD-119 exhibits practically ideal output voltage levels (0V and -5V) of 0.032V and -5.008V, while the output of the buffer shows -0.326V and -4.989V.

## *5.2 – Input Signal Frequency*

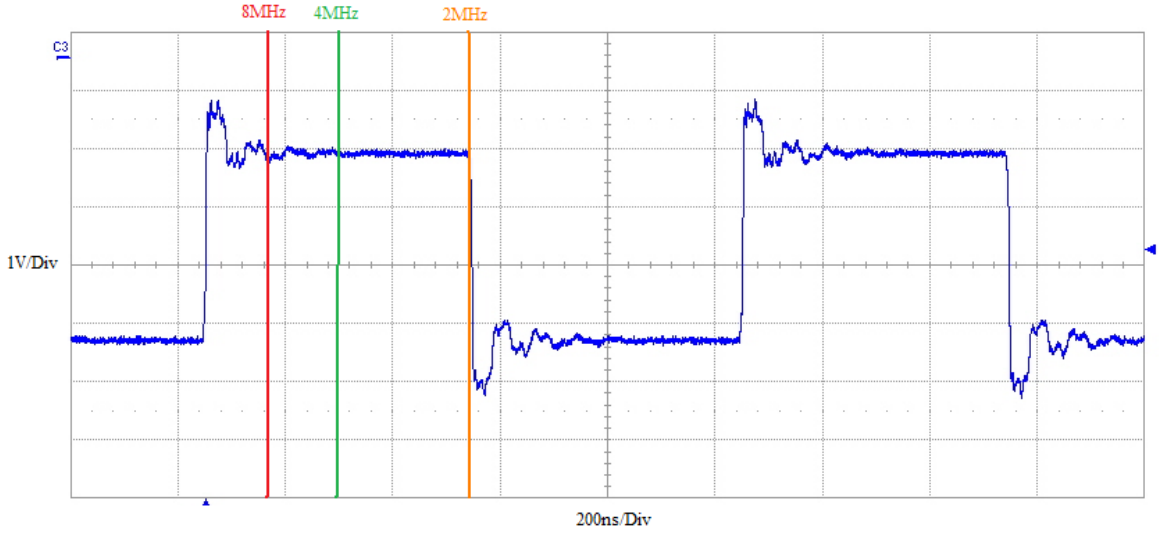


**Figure 56: 3m Cable, PCB Output, Terminated, 1MHz Square Wave Input**
**The red and green lines in the plot above show where the rising edge of an 8MHz and a 4MHz square wave signal would be expected. This shows that any signal greater than 8MHz in frequency would complete a full cycle while still in the ringing region of the signal.**

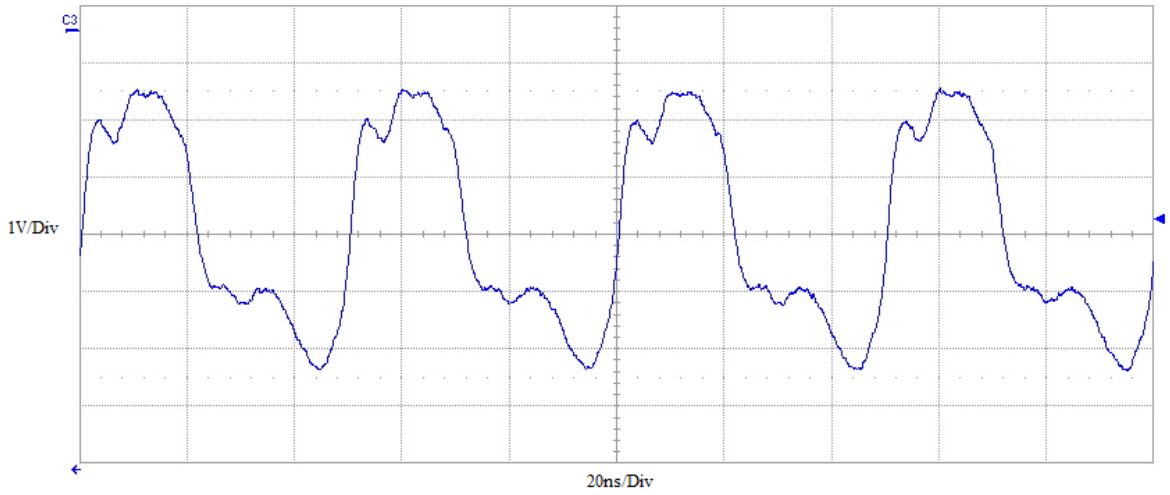


**Figure 57: 3m Cable, PCB Output, Terminated, 20MHz Square Wave Input**
**The output is severely distorted because, at 20MHZ, the signal does not have enough time to resolve its transient, and while in overshoot the signal is being driven to its opposite state.**

Observing the output waveform of a three meter terminated cable with a 1MHz square wave input shows an interesting fact. The transient observed at the rising and falling edges has duration near 200ns and approaches near 1V in excess from the steady-state voltage. The period of a 20MHz signal is 50ns, which means that the entire cycle of the 20MHz signal lies within the ringing region of the 1MHz signal. Observing Figure 56 shows that any input signal over 8MHz will fall entirely within the overshoot region, severely distorting the output signal. Figure 57 shows the 20MHz signal and its distortion caused by the ringing. Both of these signals leave the PCB at the PCB output, the output of the SN74ABT244A buffers. Therefore, the next section describes the difference between the PCB output and the SWD-119 output for non-static inputs.

## *5.3 – Output Test Location*

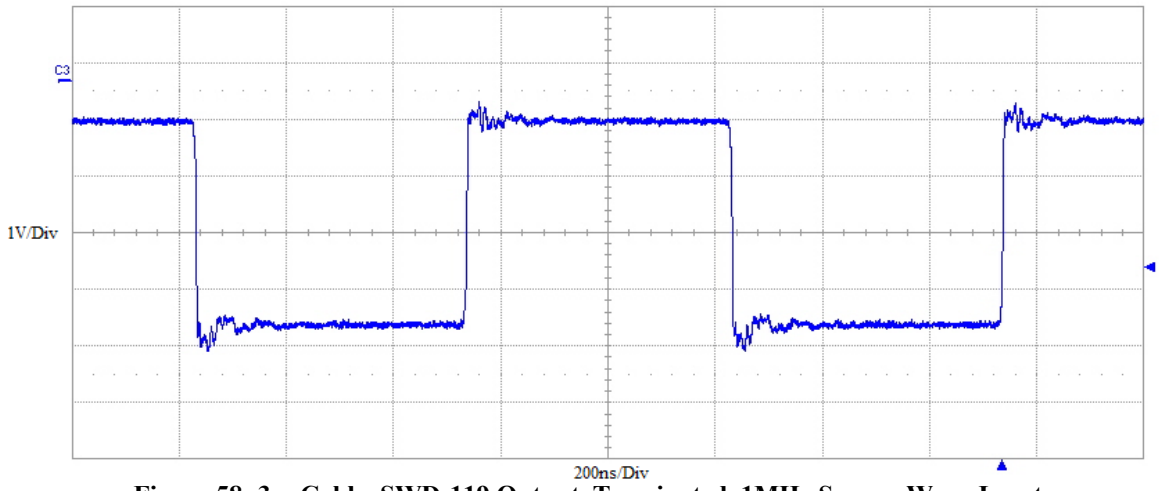


**Figure 58: 3m Cable, SWD-119 Output, Terminated, 1MHz Square Wave Input**

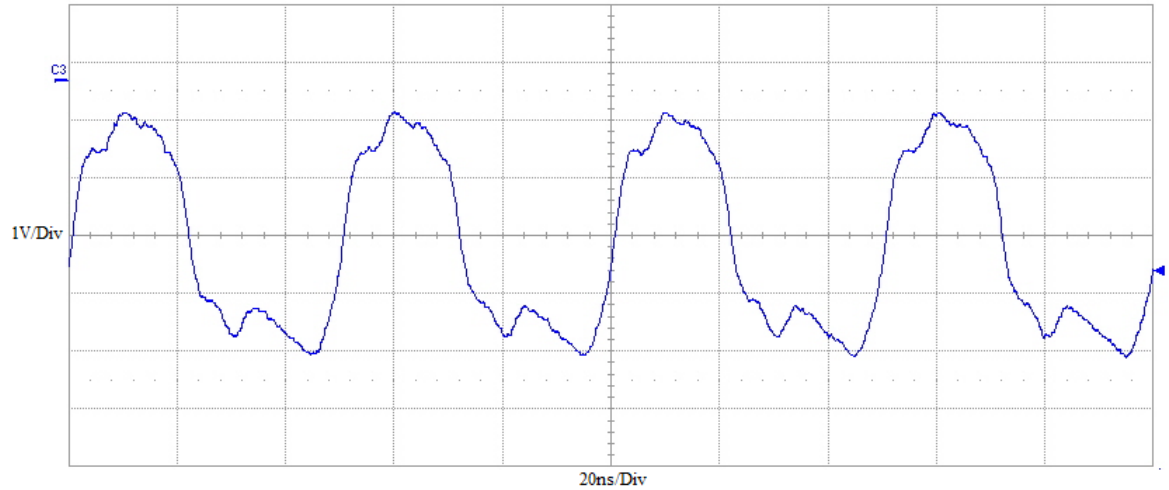


**Figure 59: 3m Cable, SWD-119 Output, Terminated, 20MHz Square Wave Input**

Figure 56 and Figure 58 compare the PCB output against the SWD-119 output for 1MHz square wave inputs driven through a three meter cable. It is immediately noticeable that the SWD-119 significantly reduces the ringing duration and amplitude of the output wave. While not nearly as bad as the PCB output, attention still needs to be paid to the ringing, as it still has a negative effect on the signal at 20MHz, shown in Figure 59.

Although the SWD-119 reduces ringing on the output it also has the tendency to raise the mean voltage, from -3.245V to -2.535V for the 1MHz input. The input waveform has a mean

voltage of +2.5V, and therefore an output mean of -2.5V would be expected. However, because the peak to peak voltage is reduced from 5V to 3.7V, the raising of the mean voltage is actually not beneficial. At the SWD-119 output, the output high voltage is -0.6V but the output low voltage is near -4.3V, which may be too high to be considered a logic low output; the voltage requirements for the T/R module are not yet specified. Conversely, for the PCB output, the output high voltage is near -1.5V and output low voltage is near -4.8V. The SWD-119 actually increases the peak to peak voltage, from 3.3V from the PCB output. However, the adjustment to the mean voltage renders the signal unusable. This effect causes the 20MHz signal output from the SWD-119 IC to ripple around -4.2V, as shown in Figure 60.

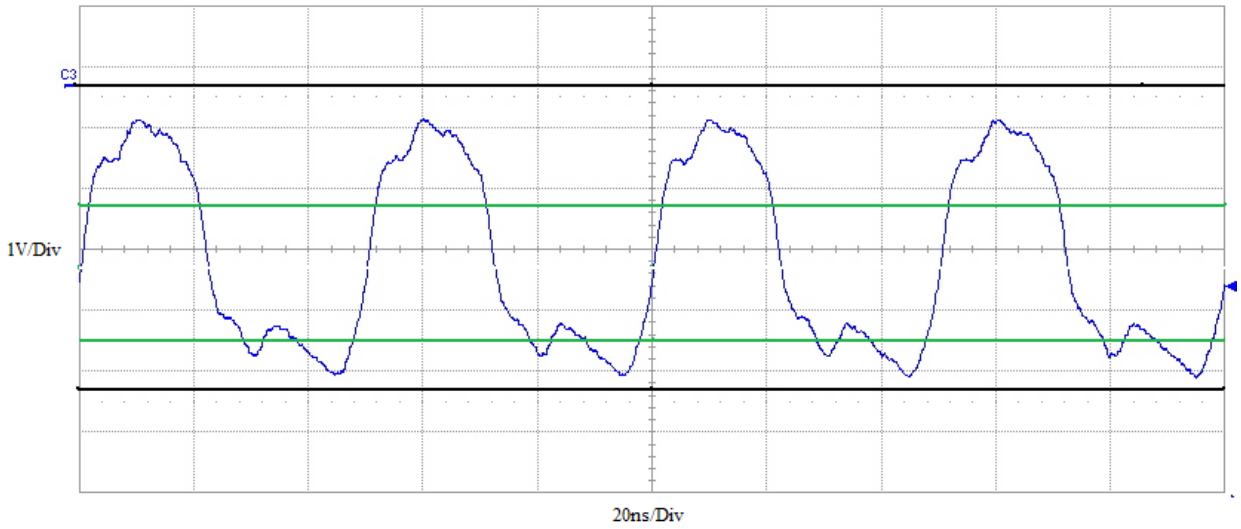


**Figure 60: Acceptable Logic Level Voltages Based on TTL Logic Voltage Levels**
**In TTL logic, voltages from 0V to 0.8V are considered Logic 0 and voltages from3V to 5V are considered Logic 1. Level shifted, these values correspond to -5V to -4.2V and -2V to 0V. Here, the lower logic voltage ripples above and below the threshold which may cause the determination of the logic state to become false.**

The digital voltage level requirements for T/R modules have yet to be specified. Therefore, for the sake of interpreting the oscilloscope plots, a TTL based logic description will be used, of course it is level shifted. Any voltage between the lower green line (-4.2V) and the lower black line (-5V) in Figure 60 would be considered logic 0 while any voltage between the higher green line (-2V) and the higher black line (0V) would represent logic 1.

The rippling above and below the logic voltage threshold will cause a false reading of the logic state. This means, in all aspects, that this voltage waveform would not be satisfactory to use for this application; again basing the digital logic voltages levels to be as TTL logic. When the manufacturer of the T/R module has a clearer idea of the required voltage levels, the design can be modified.

In addition, the SWD-119 IC can only provide 1mA of current at its output, but the control signals need to be fanned-out eight ways, the main reason why the buffer stage is included. However, in case there is a signal that has specifications that require higher logic levels, the output of the SWD-119 is one option. Depending on the requirements of the T/R module, the output of the SWD-119 might be a suitable alternative.

## *5.4 – Output Cable Length*

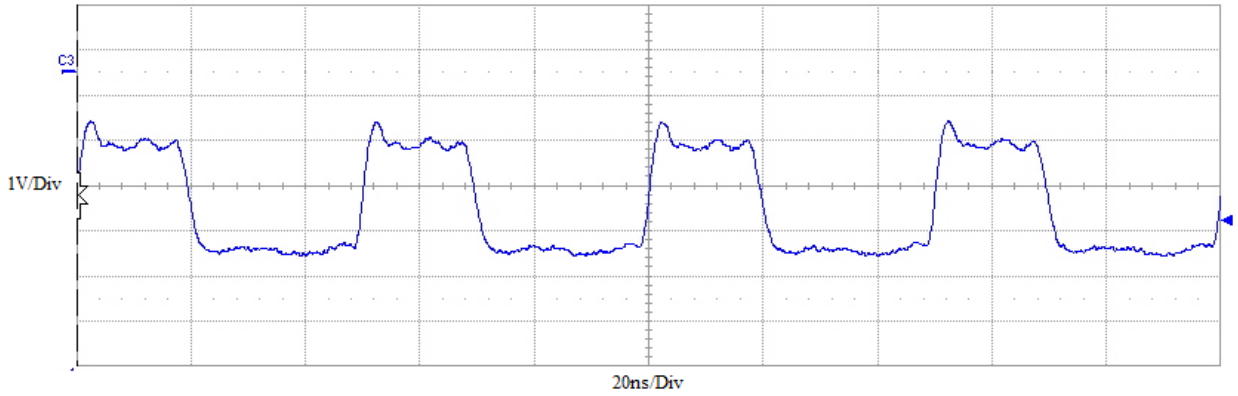


**Figure 61: No Cable, PCB Output, Terminated, 20MHz Square Wave Input**

The cable length projected to connect the interface board to the radar array is three meters. Observing Figure 57 and Figure 61, it is apparent that cable length is a large factor in signal coherence. With no cable, the output represents, very well, the square wave input; however not using an output cable is an extremely unlikely scenario in the MPAR design. Without using a cable, the peak to peak voltage of the output waveform has been reduced from

5V, on the input, to approximately 2.5V. This makes the use of this scenario even more unlikely as it is unable to attain a low logic voltage near -5V.

The 20MHz output waveform, Figure 57, is an extremely messy signal which does not resemble a square wave at all. The distortion of the signal can be attributed to the aforementioned ringing issues, in addition to an increased impedance mismatch caused by adding the cable to the path. The impedance mismatch causes reflections and increases the presence of harmonics of the square wave ultimately distorting the signal.

## *5.5 – Output Cable Termination*

MA/COM suggested the use of a 1KΩ pull-up resistor to terminate the cable connecting the interface board to the T/R modules. Their idea was tested against a 220Ω/330Ω Thevenin termination. Figure 62 shows that using the 1KΩ pull-up resistor outputs a 10.2V peak to peak waveform, with voltages from +1.68V to -8.55V. Therefore, using the 1KΩ pull-up resistor is not a viable option. Using the 220Ω/330Ω Thevenin termination, see Figure 57, provides an output waveform with a peak to peak voltage near 4.8V. Even though the output waveform with the Thevenin termination is still distorted, the signal will most likely not damage any downstream digital ICs, making it a better termination technique than the MA/COM suggestion.

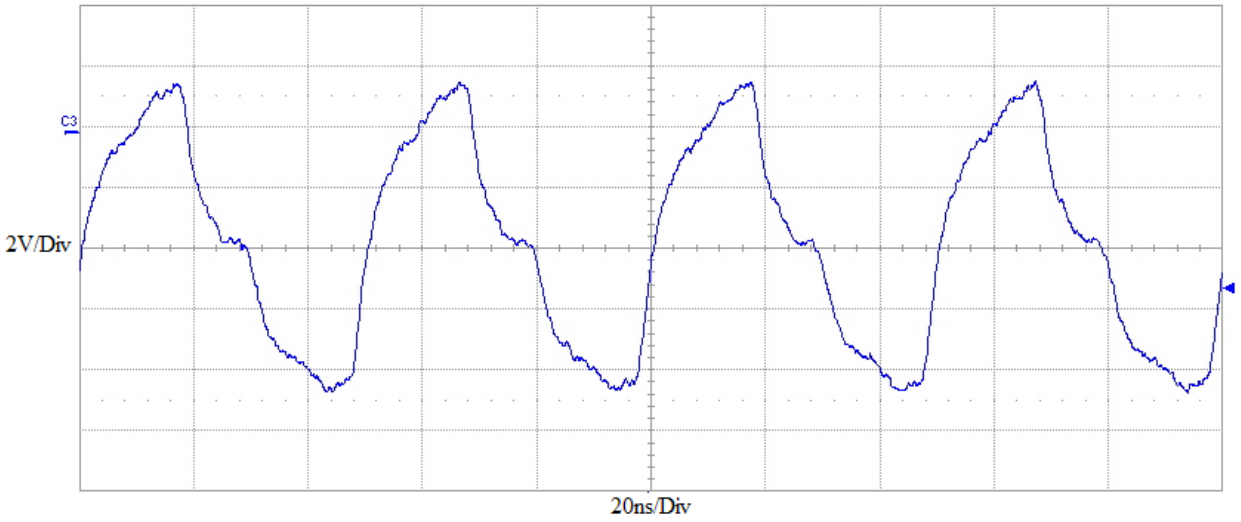


**Figure 62: 3m Cable, PCB Output, 1KΩ Pull-Up Termination, 20MHz Square Wave Input**

## *5.6 – Differential Propagation*

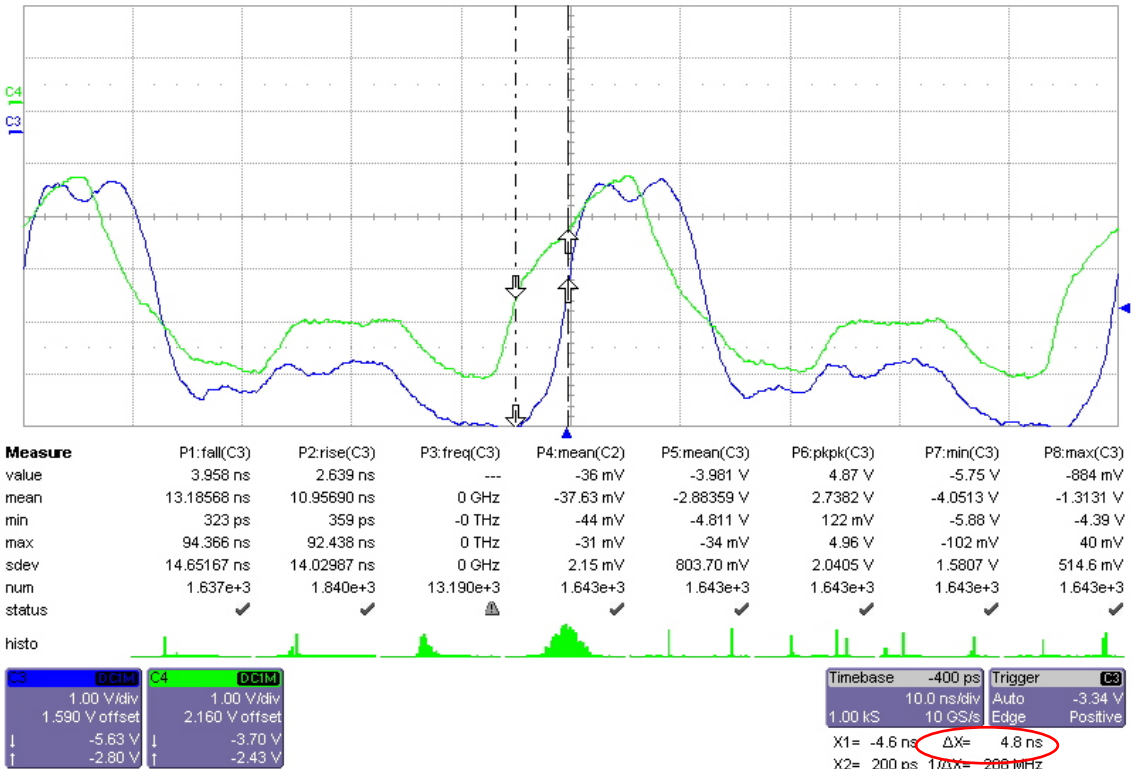


**Figure 63: Differential Propagation – 3m Cable, PCB Output, Termination, 20MHz Square Wave Input**
**At 20MHz the differential propagation delay measured was only 4.8ns.**

The worst case differential propagation delay was measured during a 1MHz input and was only measured at 12.3ns. Figure 63 exhibits a signal with only a 4.8ns differential propagation delay, even though it is being driven through a three meter cable . The output waveform shown in Figure 63 looks to be distorted more than previously recorded, which can be attributed to the shorter timescale being observed, 10ns instead of 20ns. However, using this figure to show the differential propagation delay proves that the interface design falls within spec of the suggested 50ns limitation.

## *5.7 – Suggestions*

Four ideas have been developed which could help to increase integrity of the 20MHz output waveform. The first of these methods includes using a low-pass filter at the output of the PCB to remove any high frequency noise on the signal, which results in a general distortion of the output waveform. Using this technique, however, will also round the square wave corners.

The second method includes redesigning the PCB into a more efficient design. Because of the cost and debugging capabilities, the PCB traces were not placed in the most efficient way. Some of the traces' lengths greatly exceeded the shortest required distance, making unnecessary bends in order to be able to route on a 2-layer PCB. At such high frequencies, these bends act as inductors and add to the reflections in the trace, greatly distorting the signal. The PCB may have been the leading cause for distortions, which could be avoided by cutting down the length of the traces or even using wider traces.

The third method would require rethinking the termination technique used in testing the PCB. The termination used in the testing represents the termination at the input of the T/R modules. Although using the 220Ω pull-up resistor and a 330Ω pull-down resistor is a standard way to terminate a long wire, other termination methods might be considered. Using a purely resistive termination technique does not account for the complex impedances found in the lines and traces.

The last idea was to research into a buffer which would reduce output ringing and provide better output voltage range specifications. If the buffer could reduce the ringing duration and amplitude, the output waveform would resemble a level shifted square wave much more than it does now. All of these methods are pure speculation, and future research into these ideas may prove better functionality of the interface design.

# 6.0 – Virtex-5 FPGA Development in MPAR

## *6.1 – Introduction*

In the current phase of the MPAR project, most of the front end hardware has yet to be optimized for space. Each sixty-four T/R module panel requires its own FPGA, and considering that the full-scale MPAR array consists of twenty-thousand T/R modules, there will need to be approximately three-hundred-thirteen FPGA units. Using the NI PXI-7851R evaluation board to accomplish this task would be extremely inefficient due to the amount of overhead hardware required to operate it. The evaluation board requires the use of a NI PXI chassis and an embedded computer to actively input signals to the FPGA itself, see Figure 64.

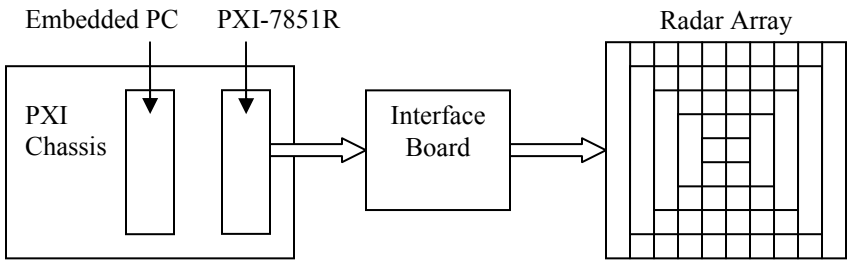


**Figure 64: Current Hardware Setup**
**The PXI-7851R contains the Virtex-5 FPGA and needs to be housed in a PXI chassis, requiring the use of an embedded computer. The amount of overhead hardware will be too much to realize a full MPAR.**

Looking ahead into the future of the MPAR project, the beam steering subsystem, which is currently substituted by the PXI-7851R controlled by LabVIEW software, will still utilize a Xilinx Virtex-5 FPGA. However, the FPGA will be integrated onto the interface board developed in this report instead of being located on an evaluation board. This change implies modifications to the interface board design which will result in a condensed piece of hardware, less reliant on auxiliary hardware.

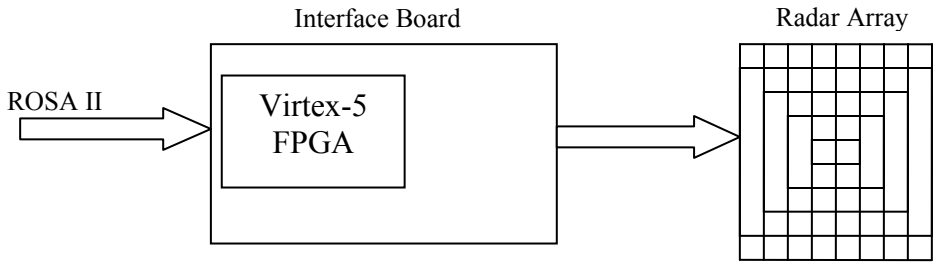


**Figure 65: Projected Hardware Setup**
**Isolating the FPGA and required components from the PXI-7851R and integrating them onto the interface board design removes reliance on auxiliary hardware and optimizes the physical space required for implementation.**

The FPGA is not a standalone piece of hardware. To integrate the Virtex-5 onto the interface board additional components need to be included to assist FPGA operation. The goal of this section is to develop a system level description of the essential components needed to implement the FPGA onto the interface board for the MPAR project.

## *6.2 – Collection of Information*

Various sources were utilized to gather information about the Virtex-5 FPGA. The FPGA's user guide, numerous PDF documents from the Xilinx website, Lincoln Laboratory Presentations, and even Lincoln Laboratory personnel were used to determine the best approach to this task. Most of the information about the FPGA on the Xilinx website was too technical to be utilized in a system level design. The bulk of the information determined to be useful for this discussion came from internal Lincoln Laboratory resources.

Another group at Lincoln Laboratory had already researched into the topic and developed hardware prototypes in an initiative named RAPID or Rapid Advanced Processor In Development. One of the goals of this initiative was to develop a semi-customizable FPGA platform which can be easily integrated into various applications. Their method of approach was very intuitive and is the subject of the next section.

## *6.3 – Method of Determining Needed Components*

When researching into how to isolate the Virtex-5 FPGA from an evaluation board, it was perceptive to realize that most of the work had already been done by Xilinx, the FPGA's manufacturer. The evaluation board contains all of the needed components to run the FPGA in addition to a handful of other non-essential peripherals. The "extras" on the evaluation board are the components that are unwanted in the MPAR project and therefore are the components which want to be removed, minimizing the space requirements for the FPGA. Xilinx was contacted and asked to share the PCB layout and schematics for the evaluation board. Xilinx granted the request, providing the group access to the files.

With the files in hand, it was easy to determine the essential components needed to provide the FPGAs functionality, as they were grouped together on the evaluation board. The files also provided the required connections from the FPGA to the components, significantly reducing development time for the RAPID prototype. The working "tile" was schematically extracted and integrated onto the custom RAPID PCB.

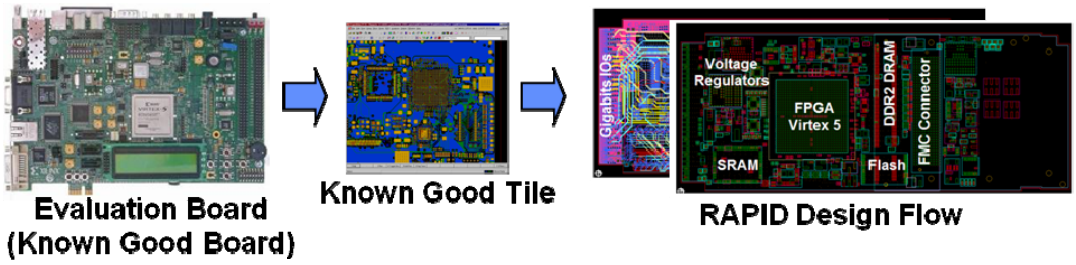


**Figure 66: A Graphical Representation of RAPID's Method to Isolating the Virtex-5 FPGA**
**From layout and schematic files of an evaluation board, the FPGA and required components were extracted and incorporated into RAPID. [Nguyen, 2008]**

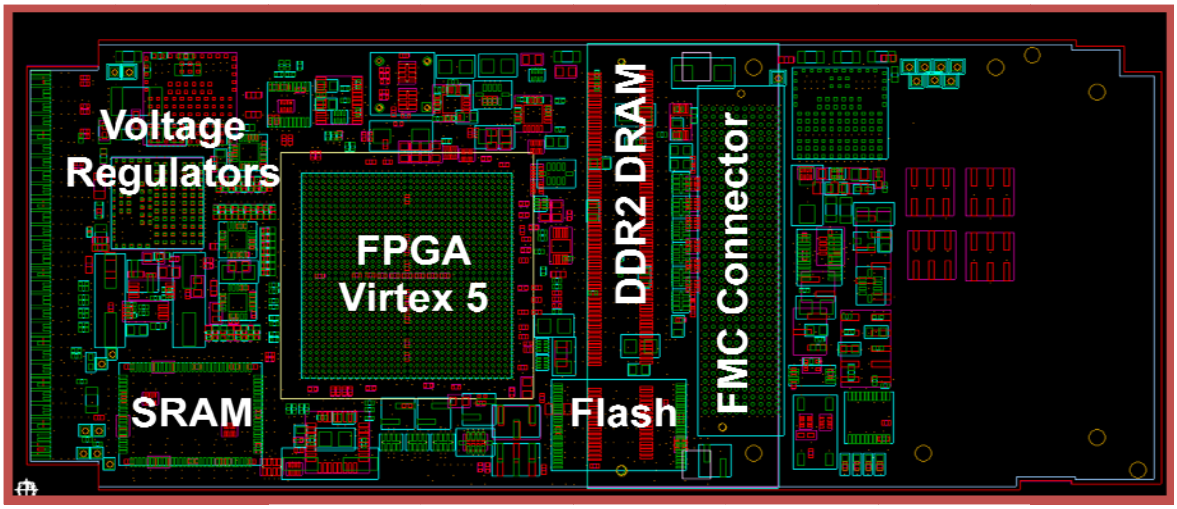


**Figure 67: RAPID PCB Design**
**Memory and voltage regulators are the major components needed to use the FPGA. [Nguyen, 2008]**

The Lincoln Laboratory group working on the RAPID initiative provided a PCB layout of the RAPID FPGA platform for reference. Included on the PCB layout are labels marking the components required for FPGA integration. Figure 67 and Figure 68 clearly label the required components needed when translating the FPGA from an evaluation board to the interface design.

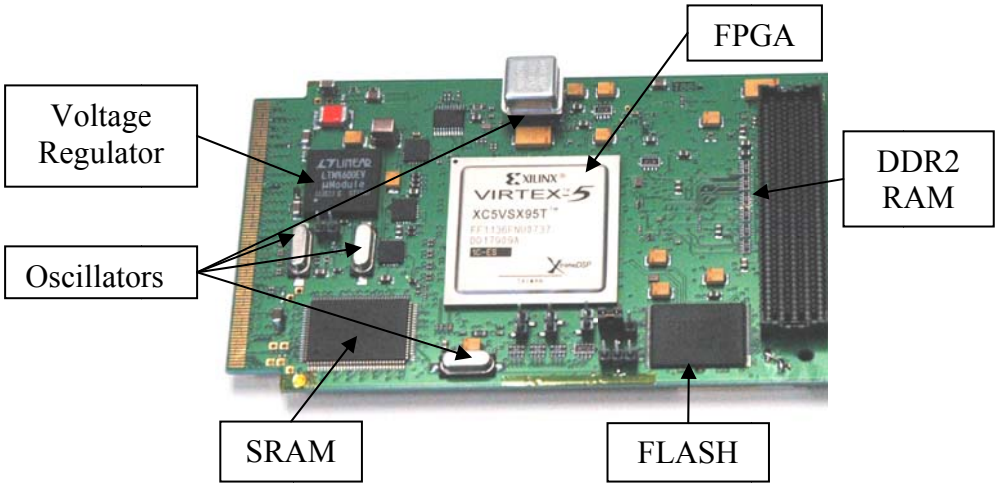


**Figure 68: Hardware Solution to FPGA Design by Group 102**
**This is a section of the prototype hardware designed for RAPID. This section of the board contains all necessary components to run the FPGA for RAPID. [Nguyen, 2008]**

## *6.4 – The Required Components*

As stated before, the FPGA is not a standalone piece of hardware. It requires additional hardware to function properly under the requirements of the MPAR project. The components needed to provide the requested functionality are SRAM, FLASH memory, DDR2 RAM, a voltage regulator, oscillators and a gigabit Ethernet controller.

It is extremely important to provide a constant DC voltage to the FPGA. Doing so prevents damage to the FPGA and prevents intermittent problems in FPGA functioning. To provide a constant voltage to the FPGA a voltage regulator is implemented near the FPGA. The regulator provides a constant output voltage with reference to another voltage potential, usually ground.

A gigabit Ethernet controller was requested by Lincoln Laboratory to allow an interface with ROSA II. ROSA II is expected to utilize gigabit Ethernet as a standard. Therefore complying with this standard will minimize the effort to interface the FPGA and ROSA II later on in development.

There are multiple types of memory utilized to provide versatile functionality of the FPGA. The FLASH memory provides a non-volatile storage which will be utilized to store routines to initialize the FPGA during power-up. The SRAM and DDR2 RAM provide volatile storage for the FPGA. The DDR2 RAM could be utilized to store ROSA II Universal Control Messages while they wait for processing. The SRAM is located closer to the FPGA to be utilized as a separate memory dedicated for FPGA operations.

## *6.5 – FPGA Conclusions*

Figure 69 shows a system level block diagram of FPGA integration onto the interface board design. ROSA II information would be sent to the FPGA over gigabit Ethernet, where it would be sent to the DDR2 RAM to wait for the FPGA to process it. The FPGA uses the FLASH memory to initialize itself upon startup. The SRAM is located close to the FPGA, as it is dedicated for FPGA operations.

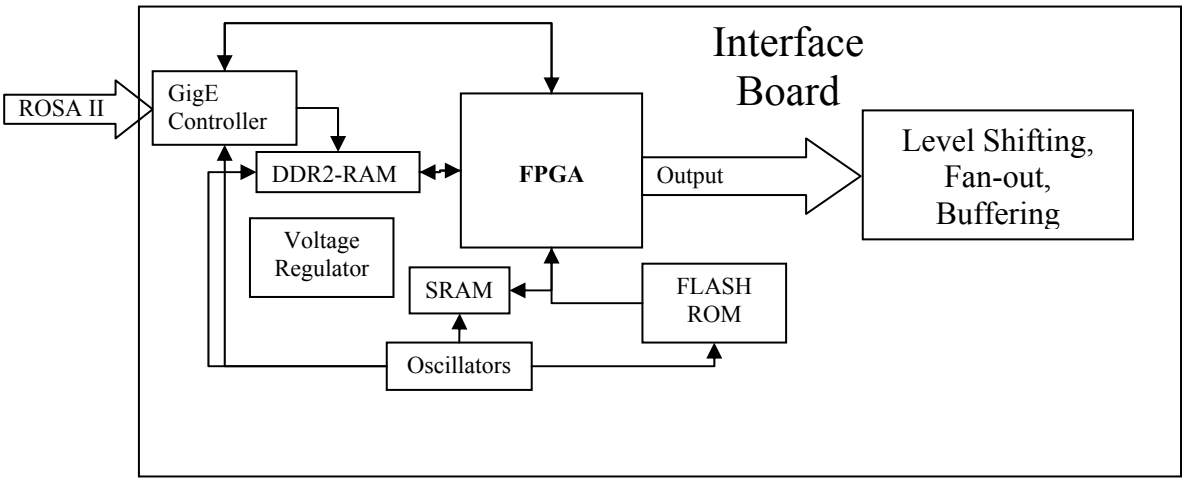


**Figure 69: System Level Block Diagram of FPGA Integration onto the Interface Board**
**The block diagram above shows all necessary components for FPGA operation specified by the MPAR project. The interactions of the components are designated by arrows.**

The engineers for the MPAR project have a choice; they can utilize RAPID or they can design a more customized PCB with the FPGA blocks mentioned above. The first option would significantly reduce development time for the MPAR project. Although RAPID requires the use of some auxiliary hardware, the reduced physical size of the hardware and the technical experience of RAPID's development team are definite benefits. The later choice might prove to be better fitted with the previously developed form factor requirements of the interface board expected to be fitted on the back of the radar panel; however this method would require substantial resources.

# 7.0 – Conclusions

The goals for this project, as listed in the Introduction, included a module schematic design, a hardware realization of the module design accompanied with test results proving the functionality of the design, a panel schematic design, and a system level block diagram concerning the integration of the beam steering FPGA on the interface board. Each of these goals have been met satisfactorily, with the exception of testing the module PCB design. Due to time constraints in ordering the PCB, only a single day was allotted to test the PCB. This proved to be barely enough time to fully understand the functioning of the interface design. With more time, some of the suggested ideas for resolving the output waveform ringing could have been tested to further advance the design.

Testing, however, did prove the functionality of the level shifter, although inverted, while also verifying the differential propagation delay requirement. The tests also helped determine that a 1KΩ pull-up terminating resistor on the T/R module side of a transmitted cable is not an effective method of terminating, and requires the use of both pull-up and pull-down resistors.

Testing also gave light to negative results. The worst case output possible in the testing environment, achievable by driving a 20MHz square wave through a three meter cable from the output of the PCB, terminated with generic Thevenin resistor values, renders the design in its current state to be, most likely, unusable by Lincoln Laboratory. The two major concerns for the output of the PCB are the ringing and the output voltage levels.

Lincoln Laboratory does however, have an appropriate preliminary interface board design, which could later be redesigned when more specifications for the MPAR project are established. The second revision of the PCB could be much smaller, reducing the issues found in this first revision and making it an ample design to be used for MPAR.

# 8.0 – References


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# 9.0 – Appendices

## *9.1 – Appendix A: Oscilloscope Images*

For the following oscilloscope images, information regarding the axis scales is located across the bottom. The offset on the voltage scale is at different locations on a number of images; however 0V is determined by the marker on the left side of the image. The value of the offset, along with the voltage scale, can be found in the bottom left corner of the images. The timescale is found near the bottom right of the images.

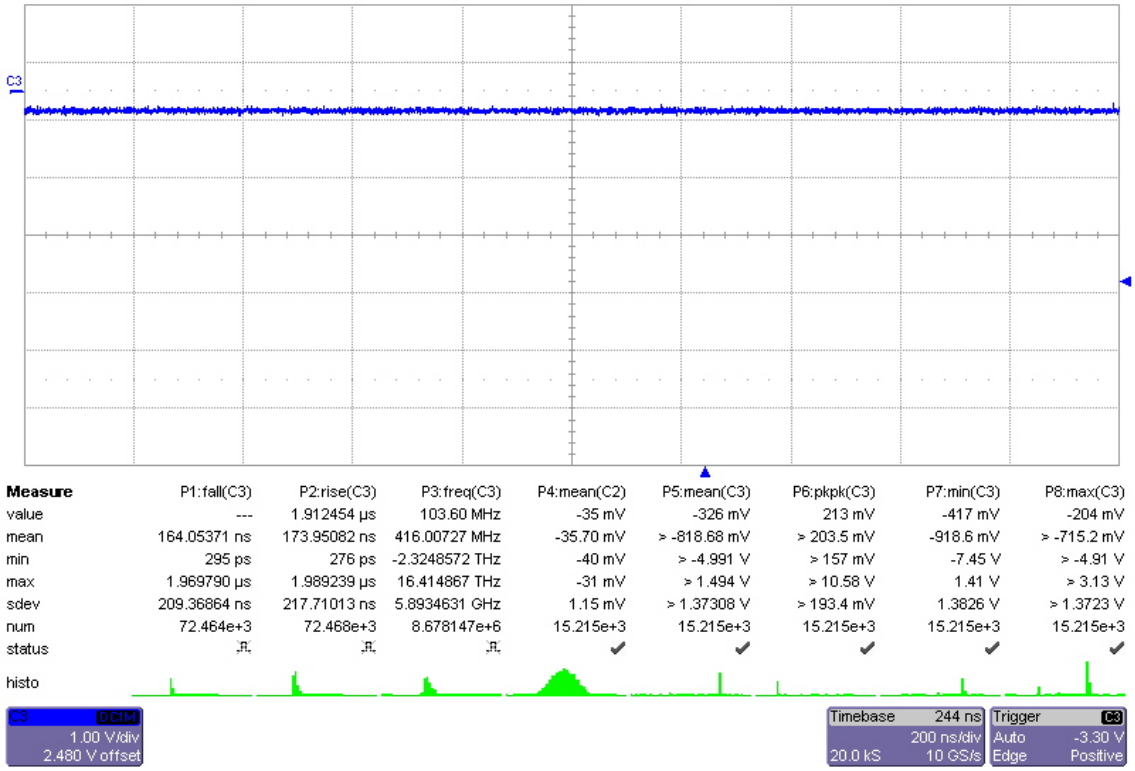


**Figure 70: No Cable, PCB Output, No Termination, Static 0V Input**


**Figure 71: No Cable, PCB Output, No Termination, Static 5V Input**

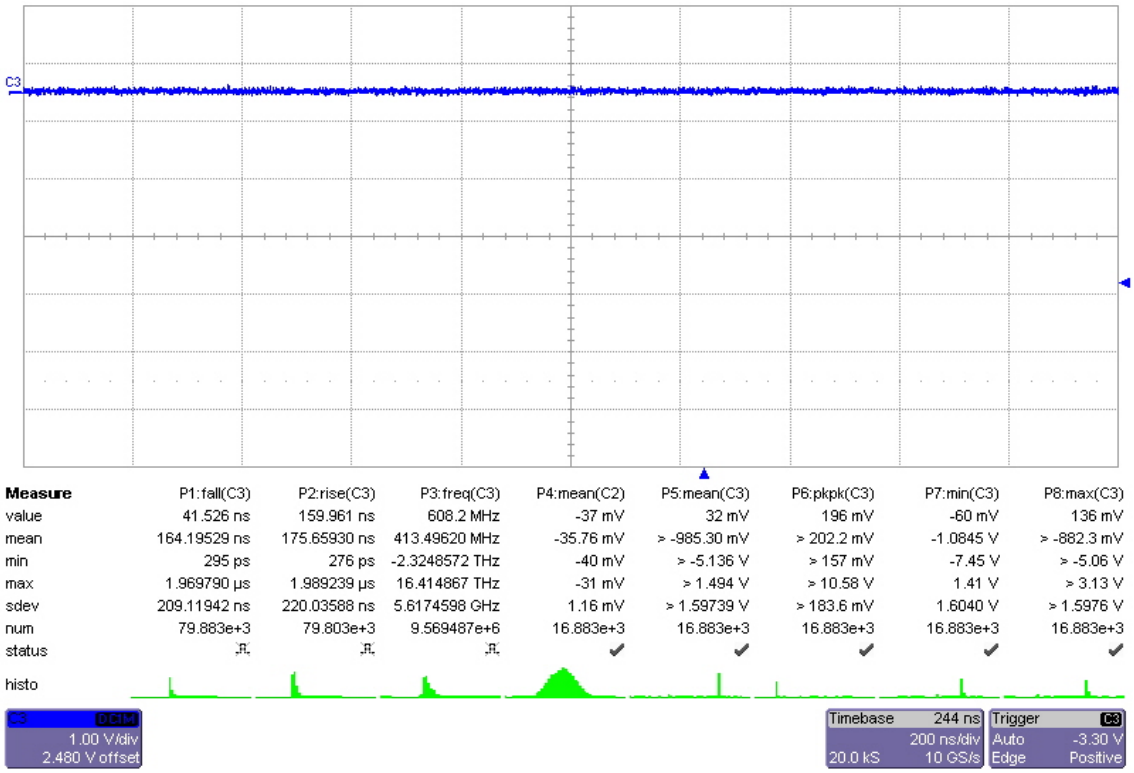


**Figure 72: No Cable, SWD-119 Output, No Termination, Static 0V Input**


**Figure 73: No Cable, SWD-119 Output, No Termination, Static 5V Input**

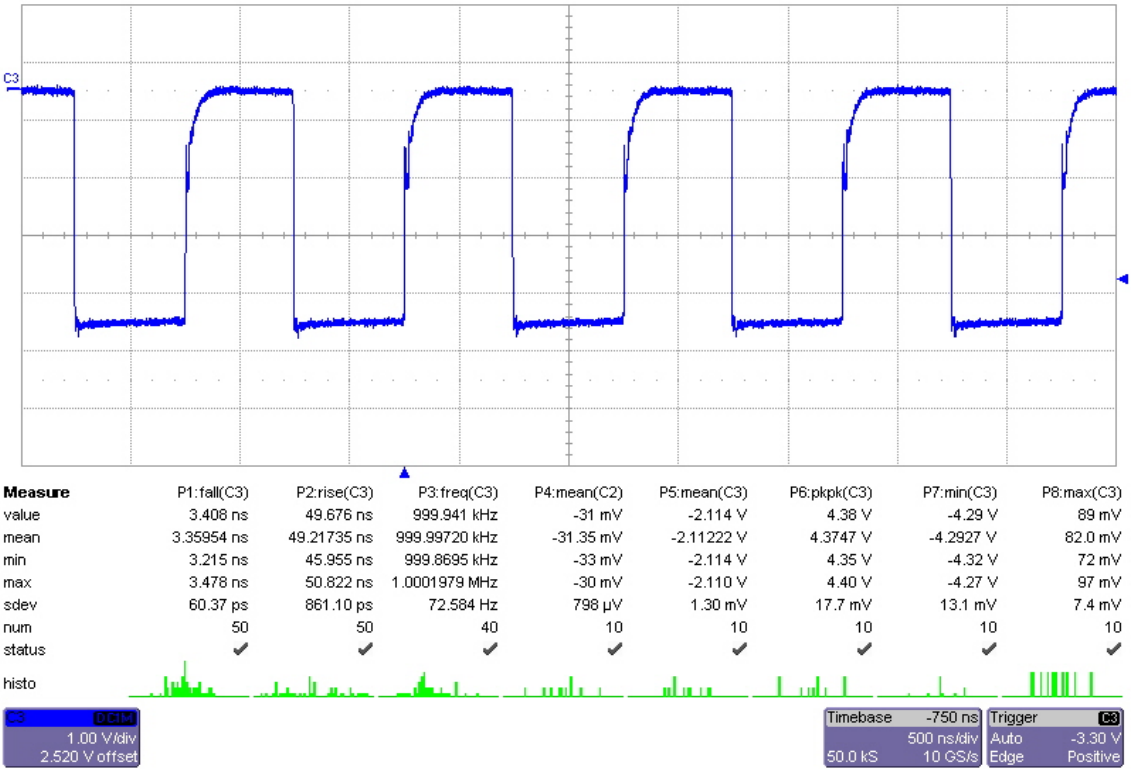


**Figure 74: No Cable, PCB Output, No Termination, 1MHz Square Wave Input**

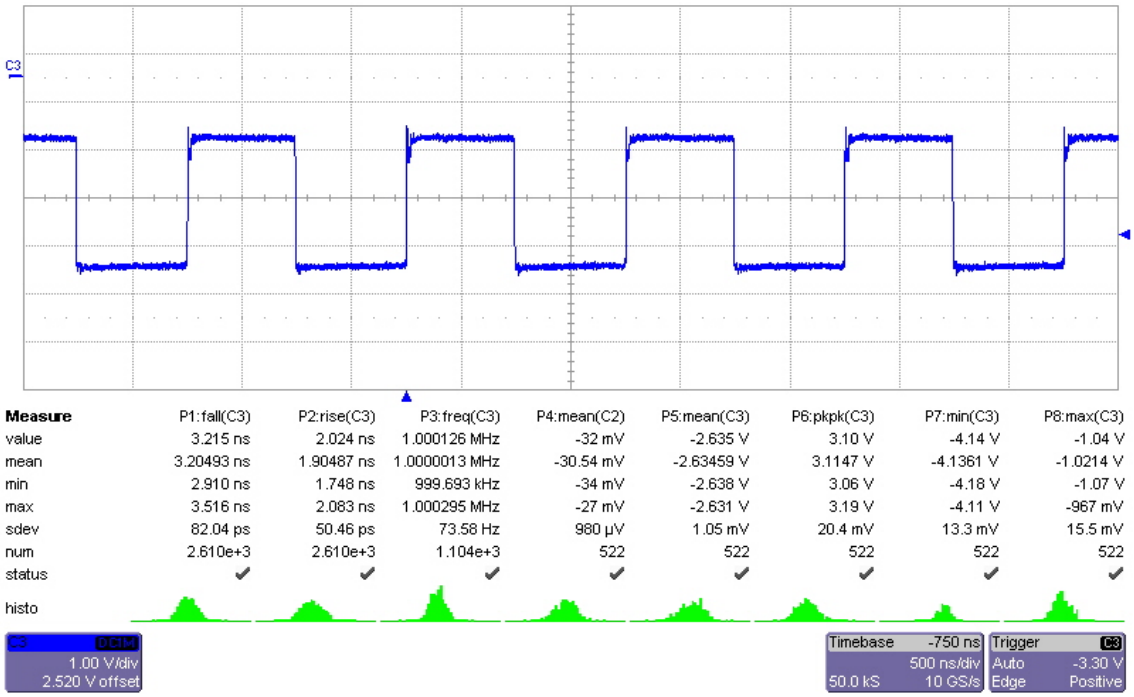


**Figure 75: No Cable, PCB Output, Terminated, 1MHz Square Wave Input**

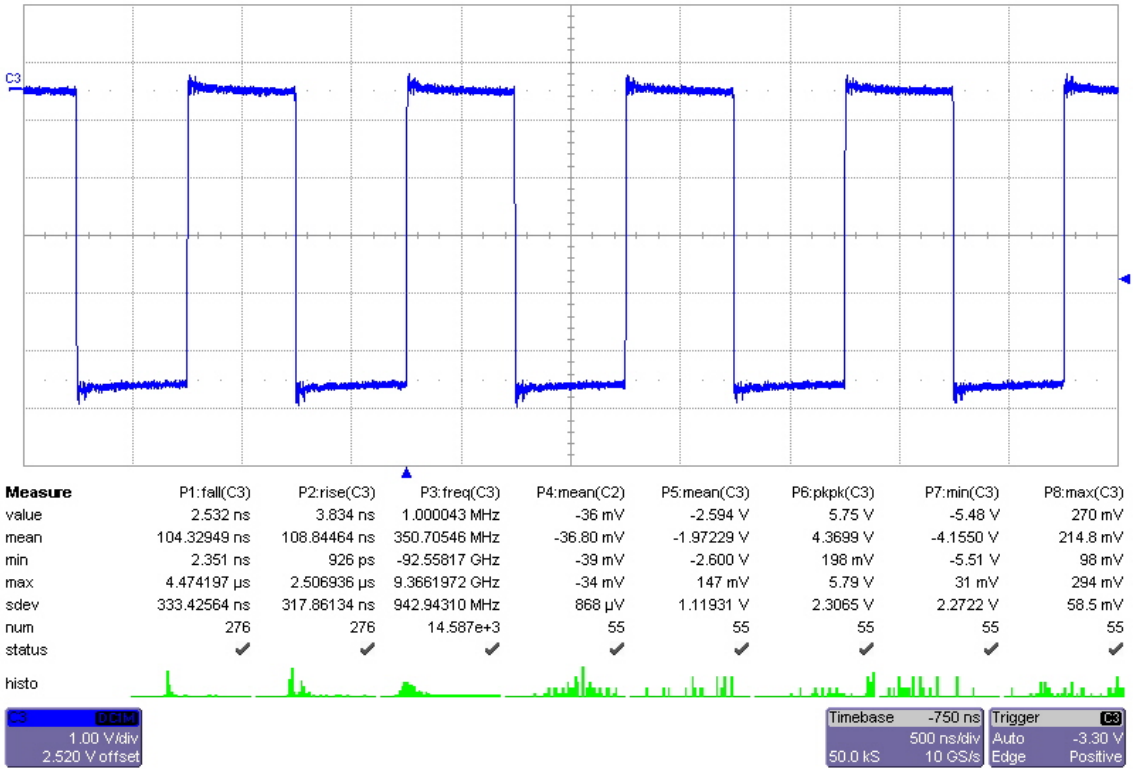


**Figure 76: No Cable, SWD-119 Output, No Termination, 1MHz Square Wave Input**


**Figure 77: No Cable, PCB Output, No Termination, 20MHz Square Wave Input**

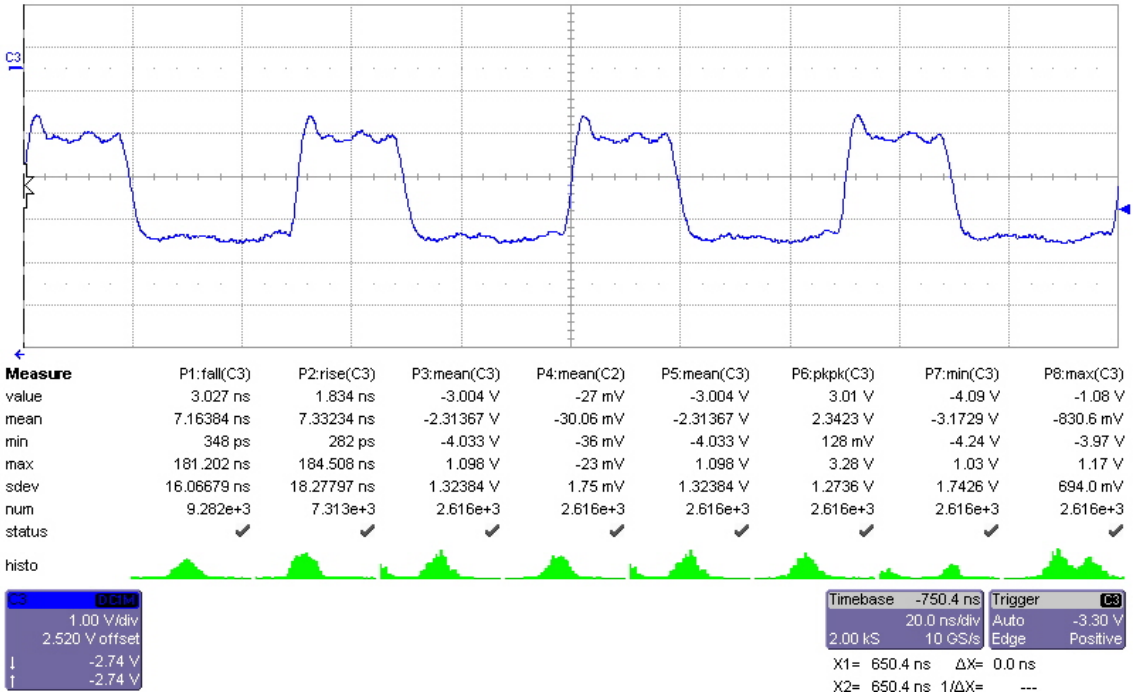


**Figure 78: No Cable, PCB Output, Terminated, 20MHz Square Wave Input**

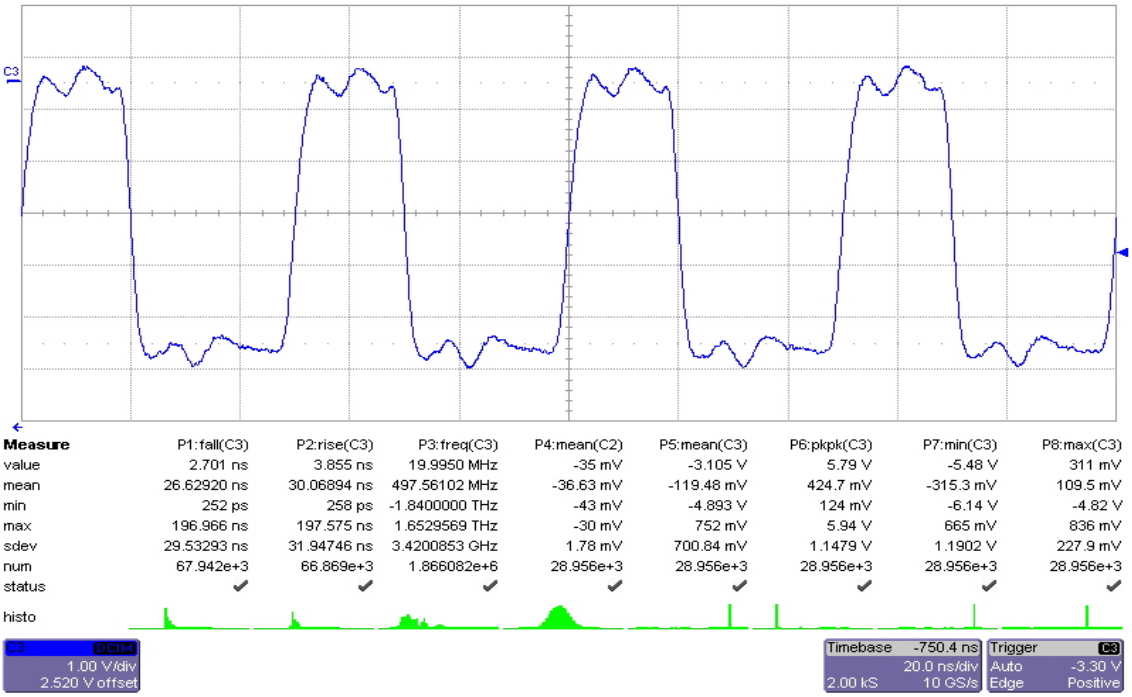


**Figure 79; No Cable, SWD-119 Output, No Termination, 20MHz Square Wave Input**

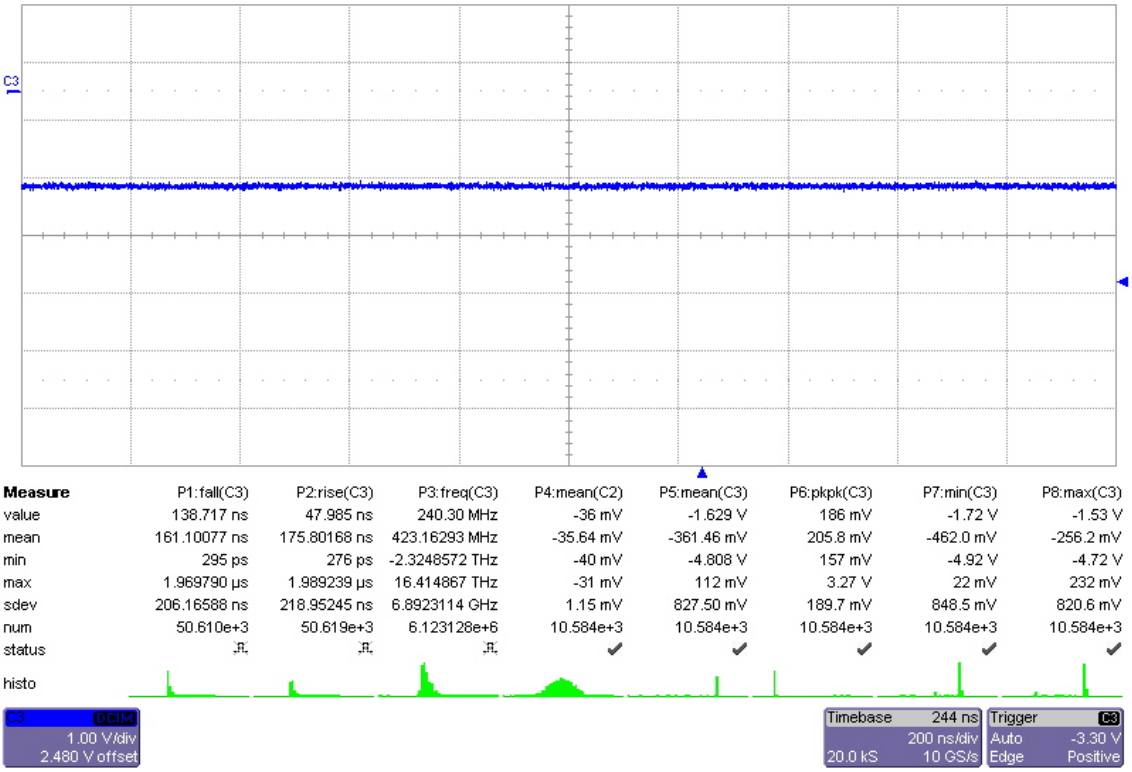


**Figure 80: 1m Cable, PCB Output, Terminated, Static 0V Input**

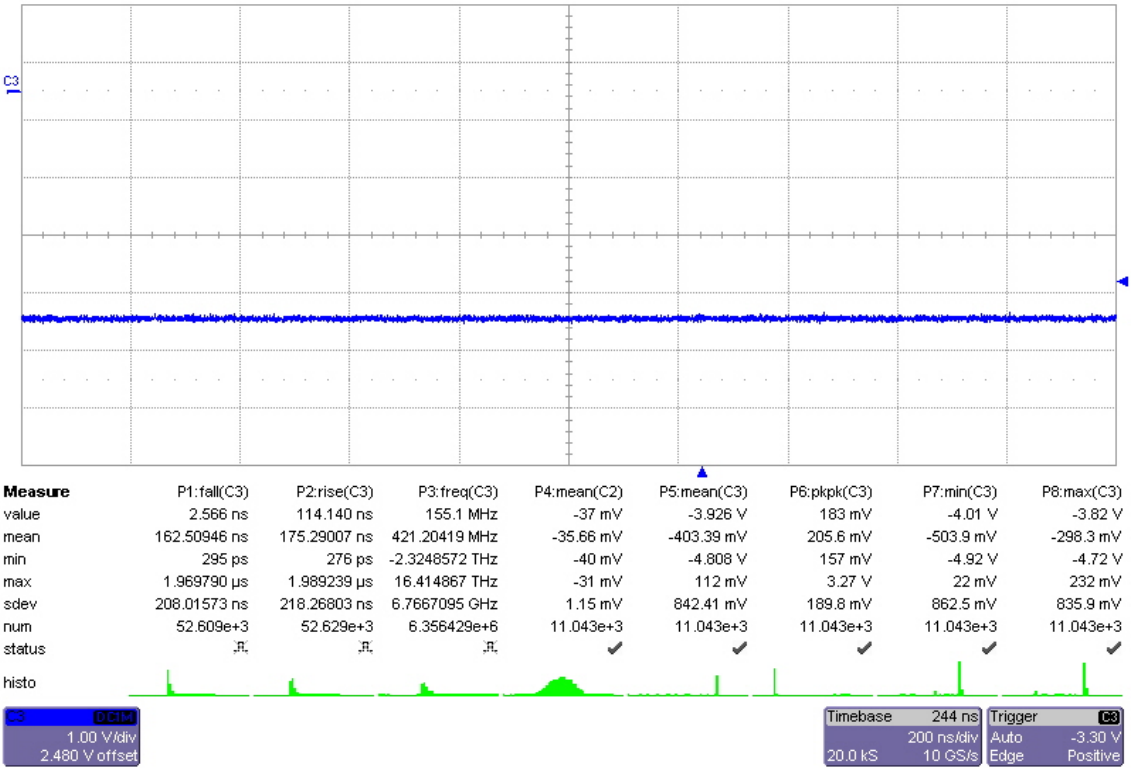


**Figure 81: 1m Cable, PCB Output, Terminated, Static 5V Input**

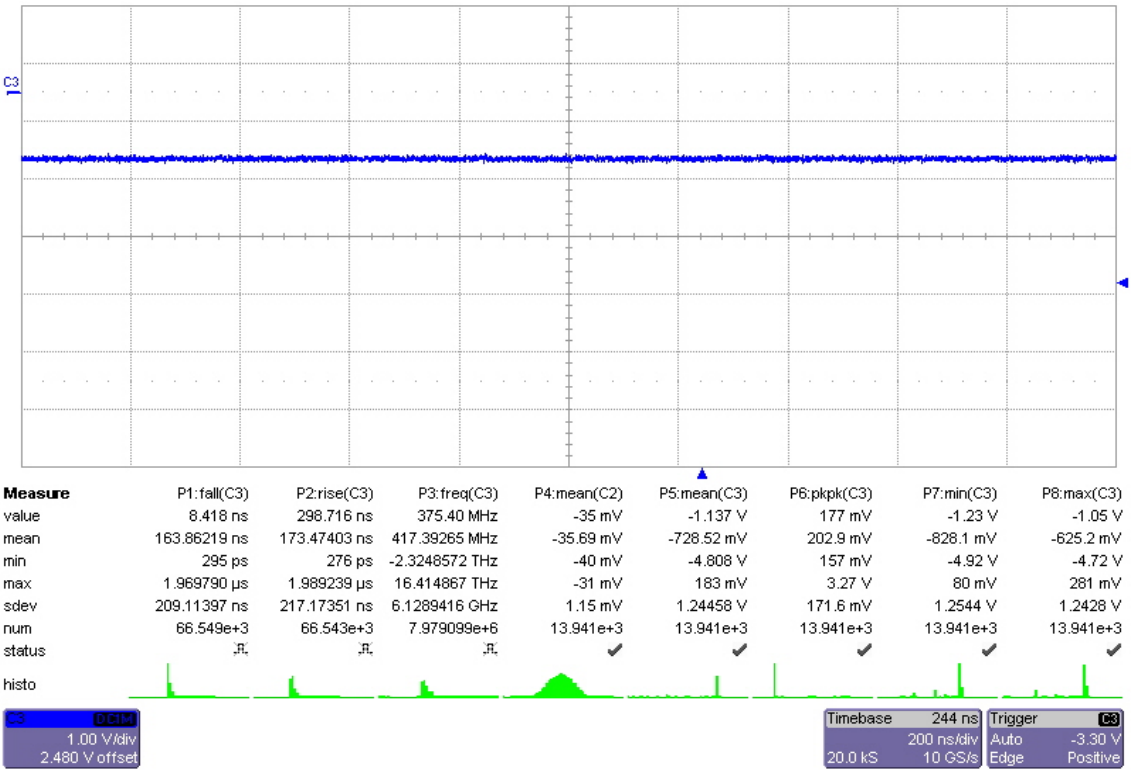


**Figure 82: 1m Cable, SWD-119 Output, Terminated, Static 0V Input**

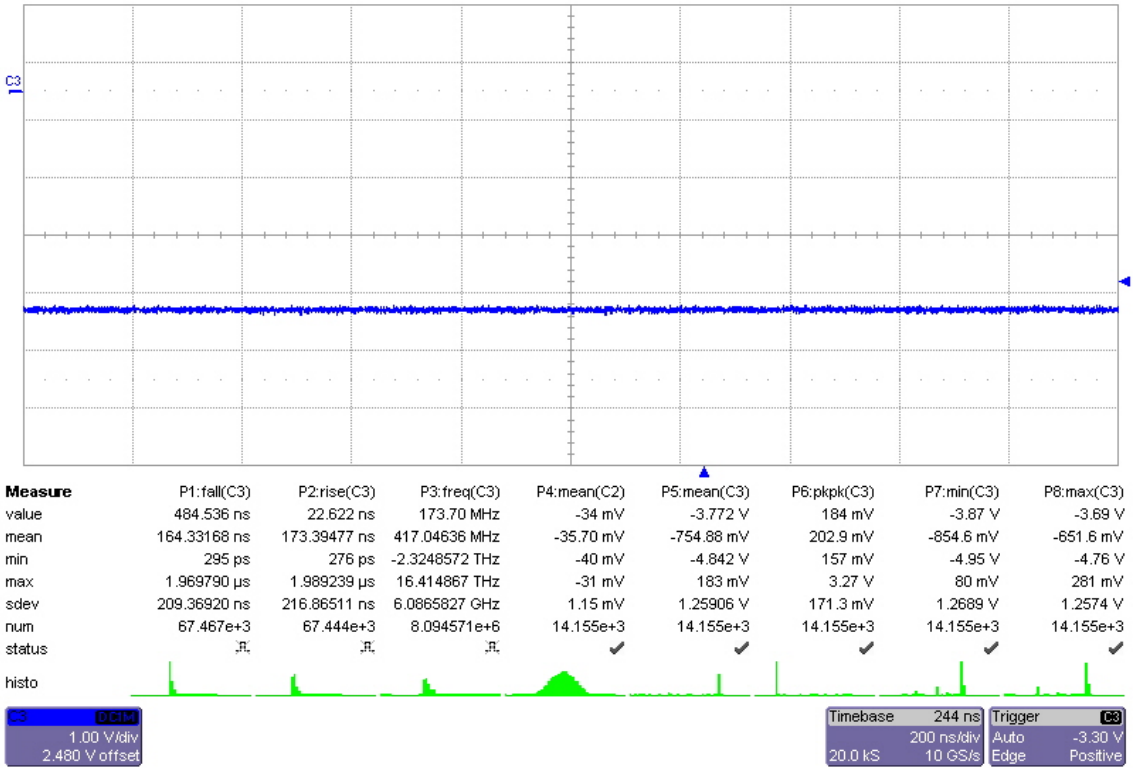


**Figure 83: 1m Cable, SWD-119 Output, Terminated, Static 5V Input**


**Figure 84: 1m Cable, PCB Output, Terminated, 1MHz Square Wave Input**


**Figure 85: 1m Cable, SWD-119 Output, Terminated, 1MHz Square Wave Input**

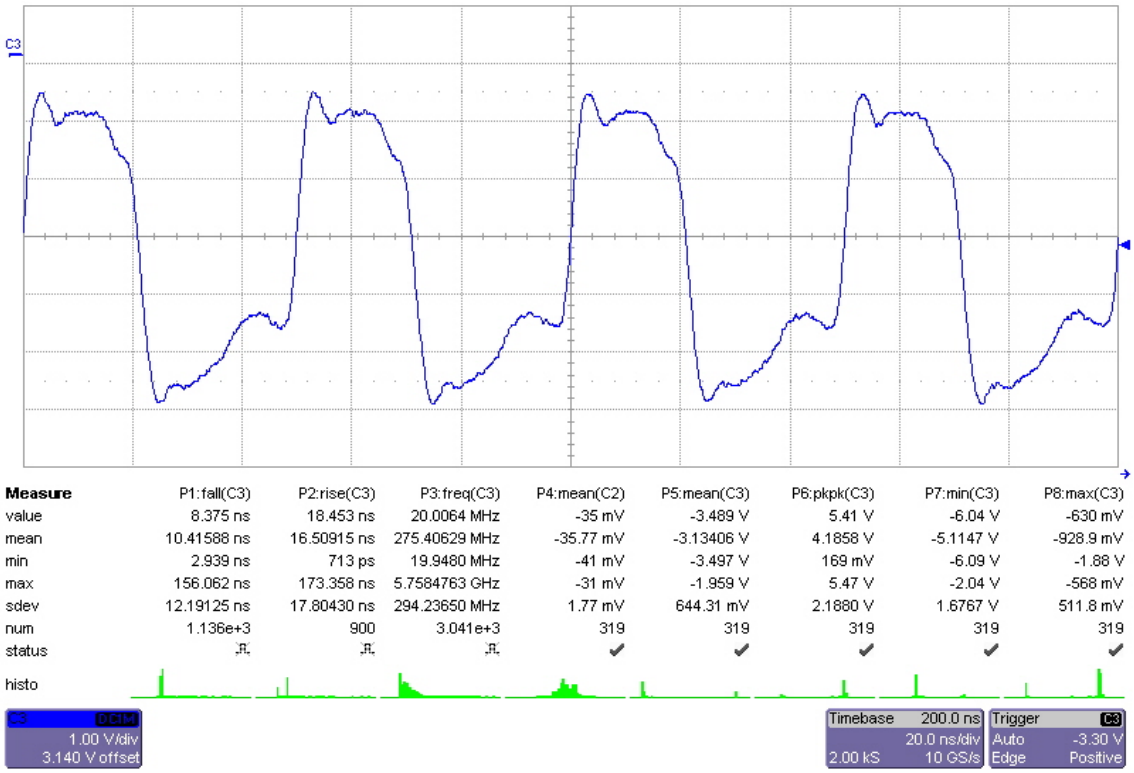


**Figure 86: 1m Cable, PCB Output, Terminated, 20MHz Square Wave Input**

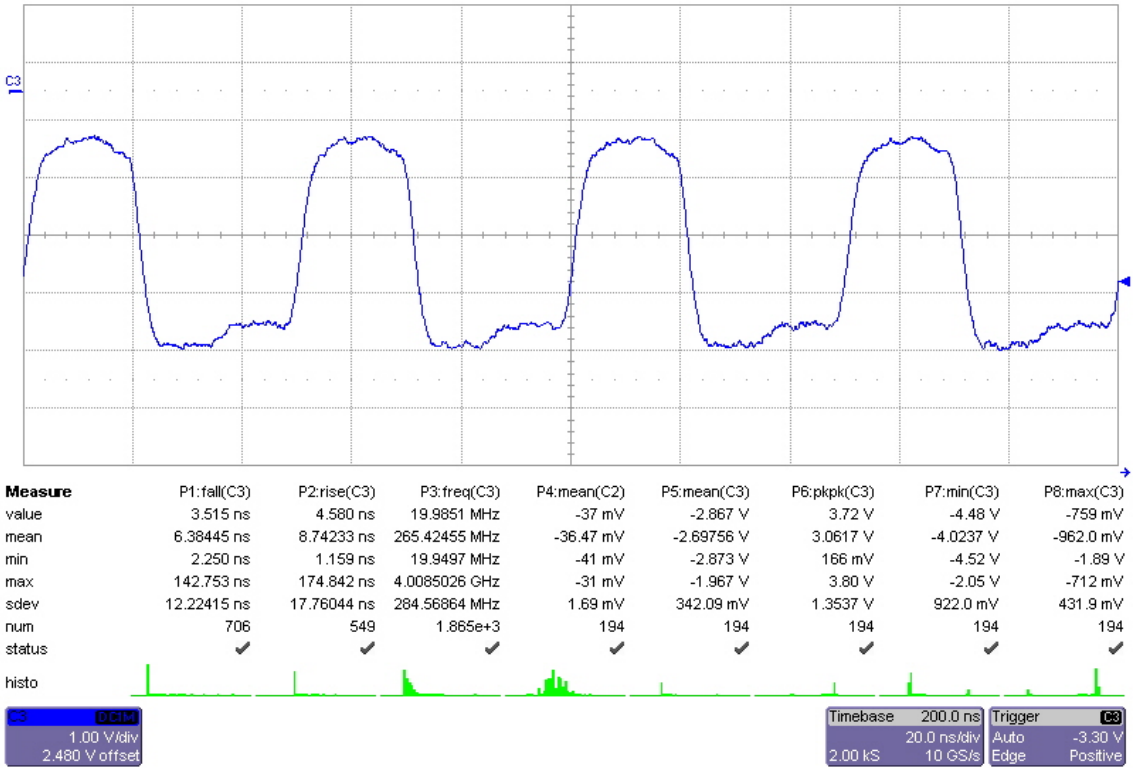


**Figure 87: 1m Cable, SWD-119 Output, Terminated, 20MHz Square Wave Input**


**Figure 88: 3m Cable, PCB Output, Terminated, 1MHz Square Wave Input**


**Figure 89: 3m Cable, SWD-119 Output, Terminated, 1MHz Square Wave Input**

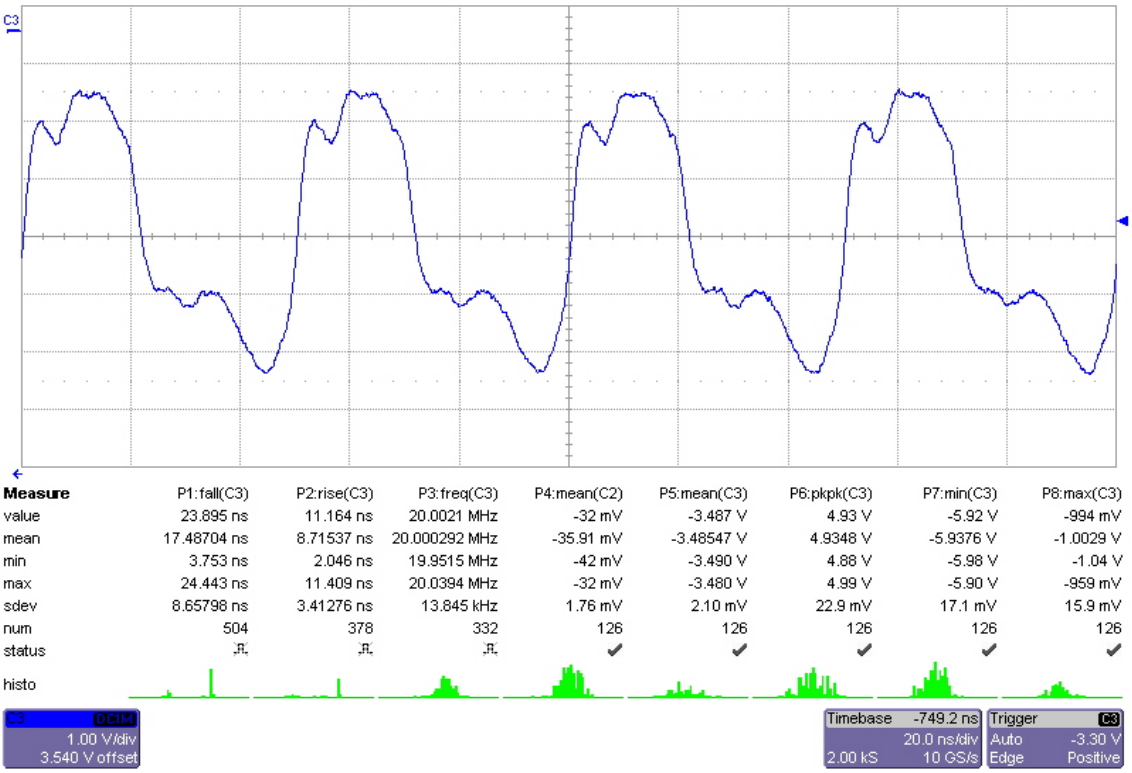


**Figure 90: 3m Cable, PCB Output, Terminated, 20MHz Square Wave Input**

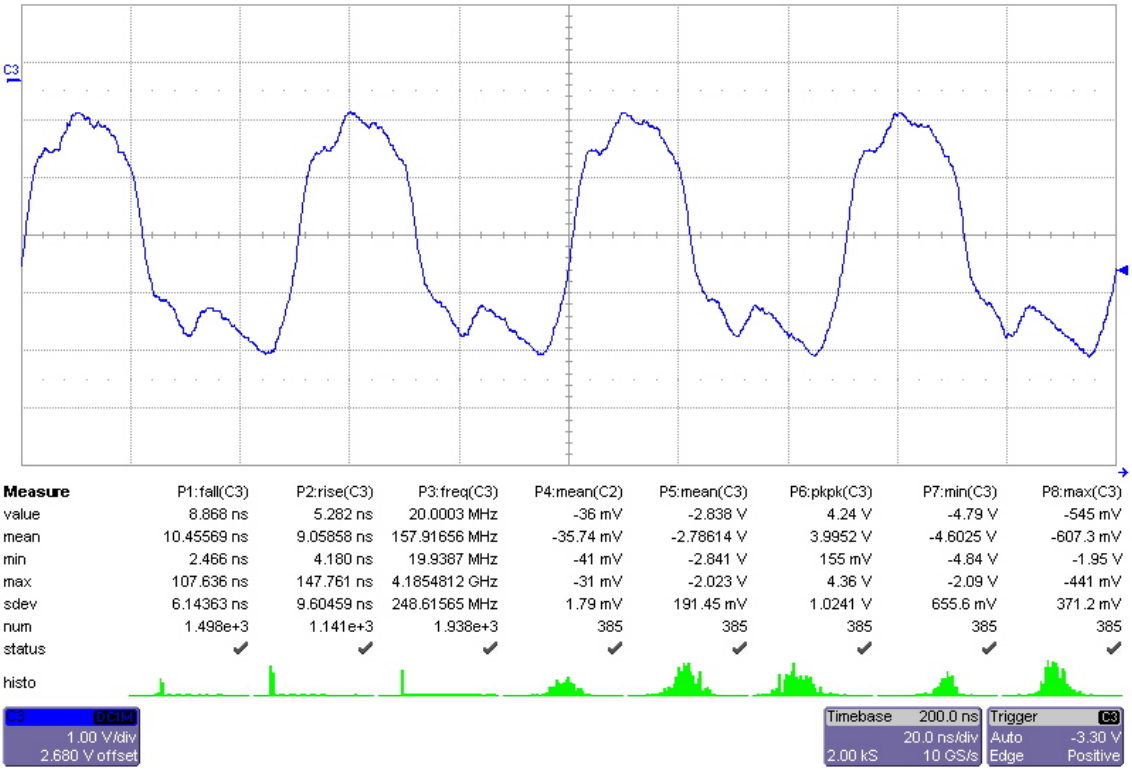


**Figure 91: 3m Cable, SWD-119 Output, Terminated, 20MHz Square Wave Input**

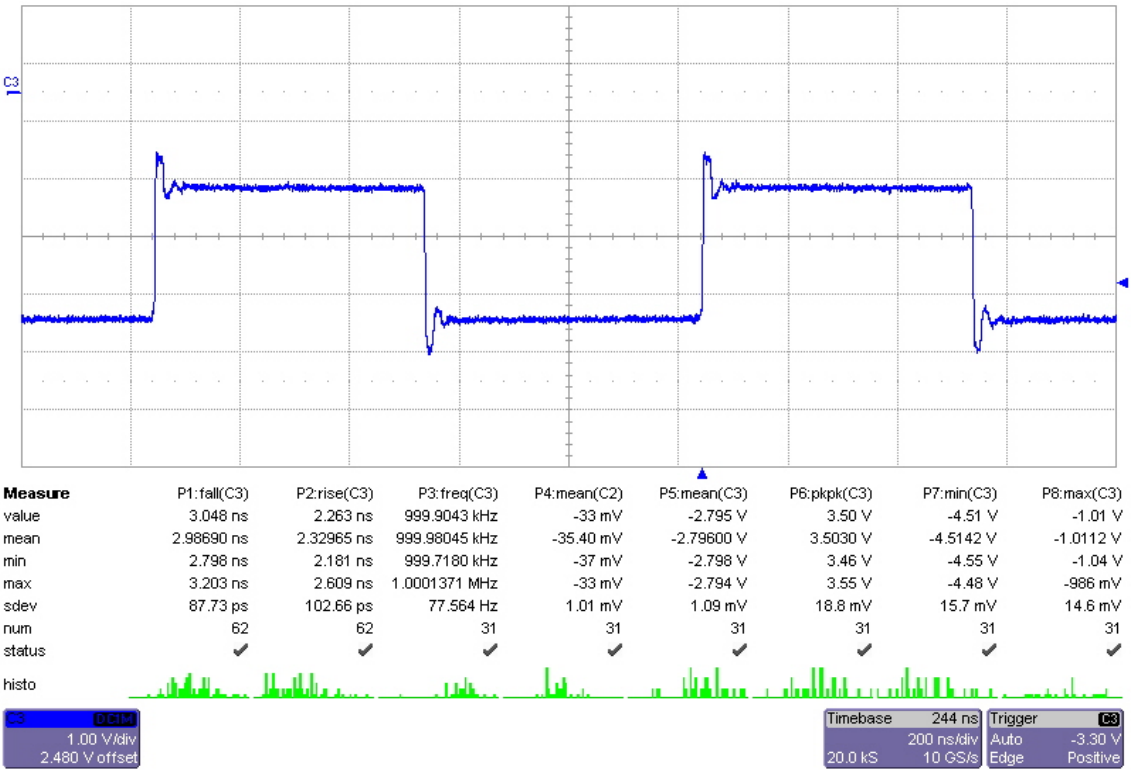


**Figure 92: 1m Cable, PCB Output, Dual Termination, 1MHz Square Wave Input**


**Figure 93: 1m Cable, SWD_119 Output, Dual Termination, 1MHz Square Wave Input**

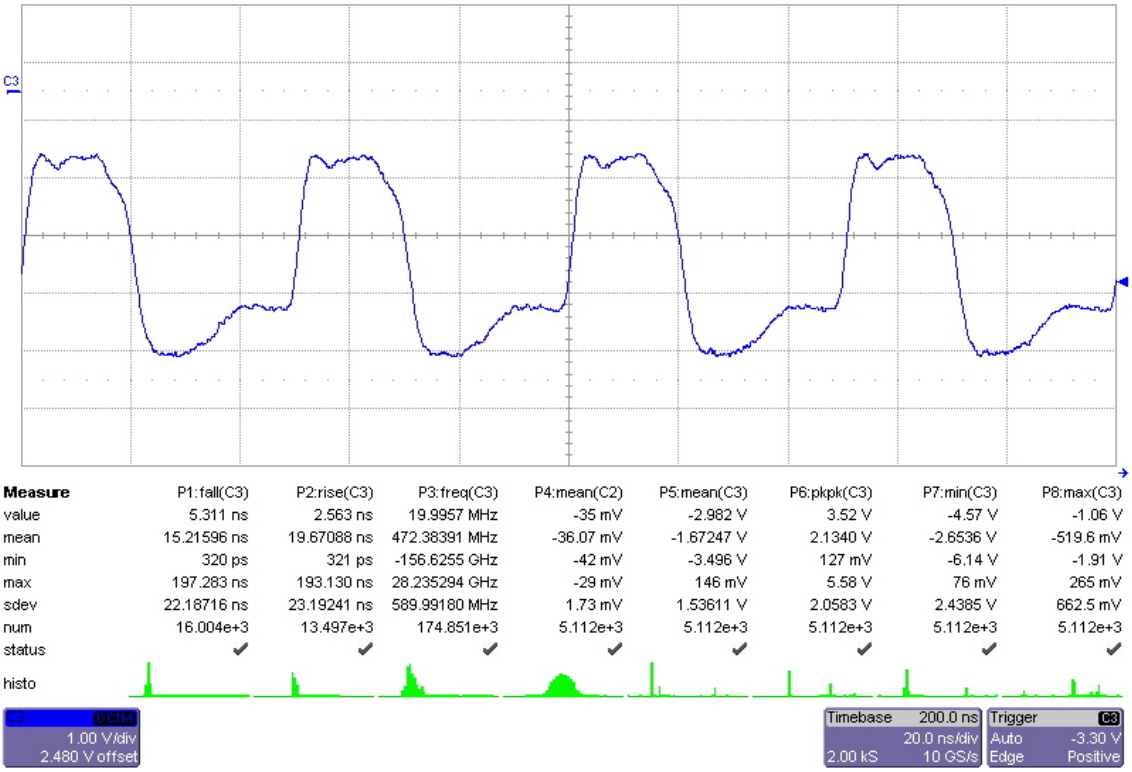


**Figure 94: 1m Cable, PCB Output, Dual Termination, 20MHz Square Wave Input**

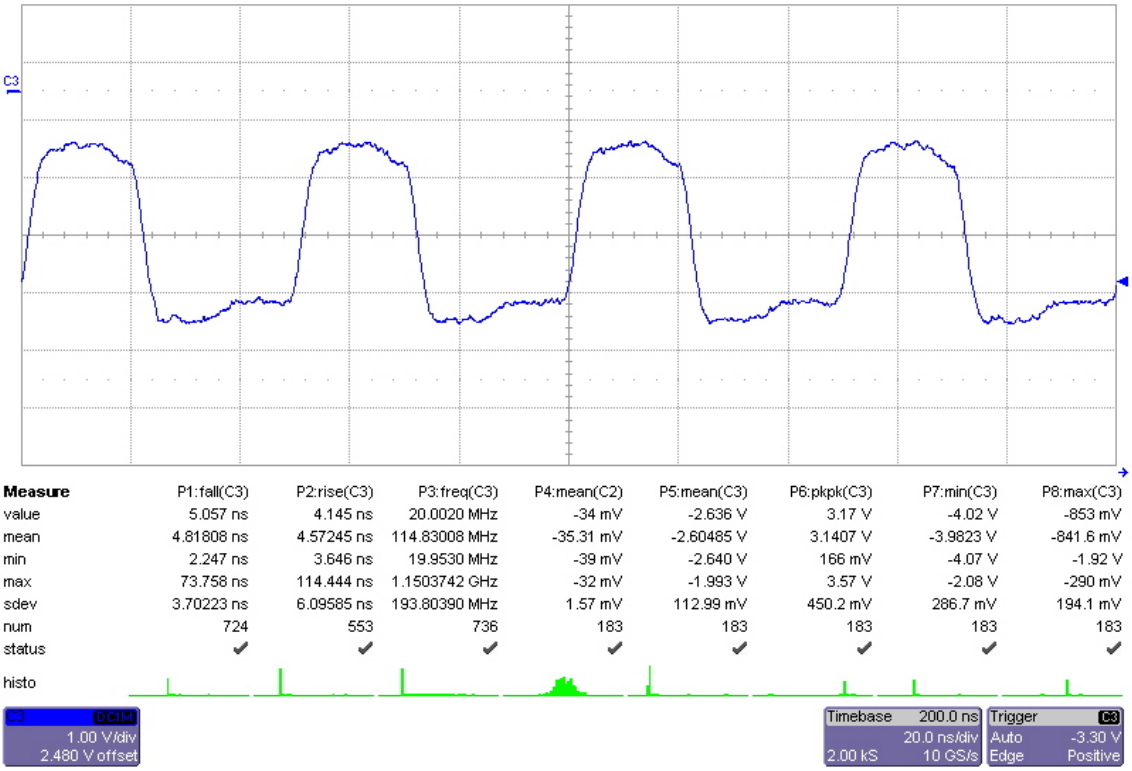


**Figure 95: 1m Cable, swd-119 Output, Dual Termination, 20MHz Square Wave Input**


**Figure 96: 3m Cable, PCB Output, Dual Termination, 1MHz Square Wave Input**

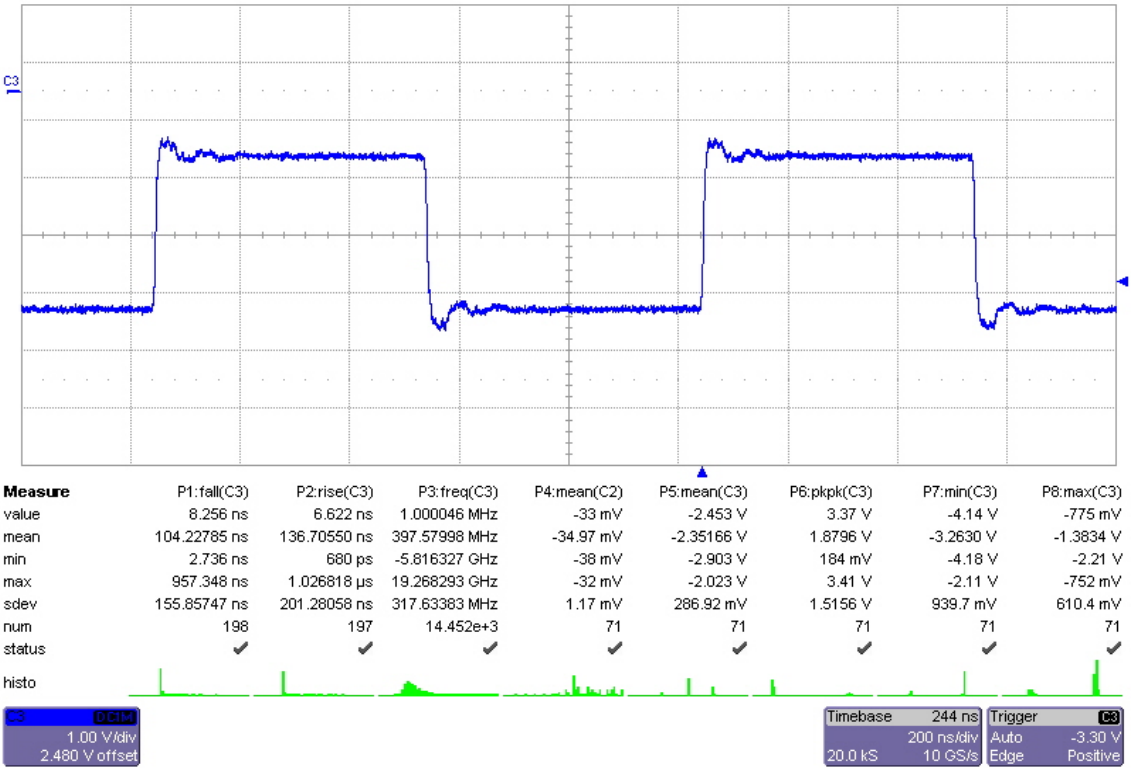


**Figure 97: 3m Cable, SWD-119 Output, Dual Termination, 1MHz Square Wave Input**

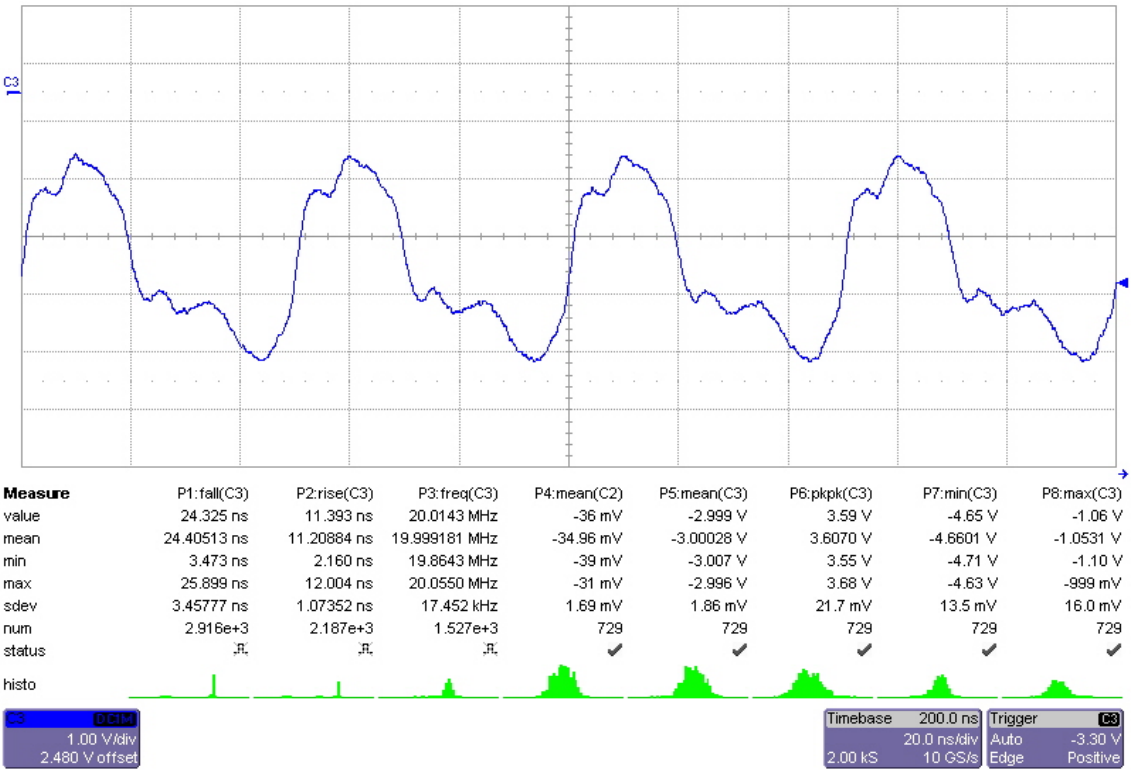


**Figure 98: 3m Cable, PCB Output, Dual Termination, 20MHz Square Wave Input**

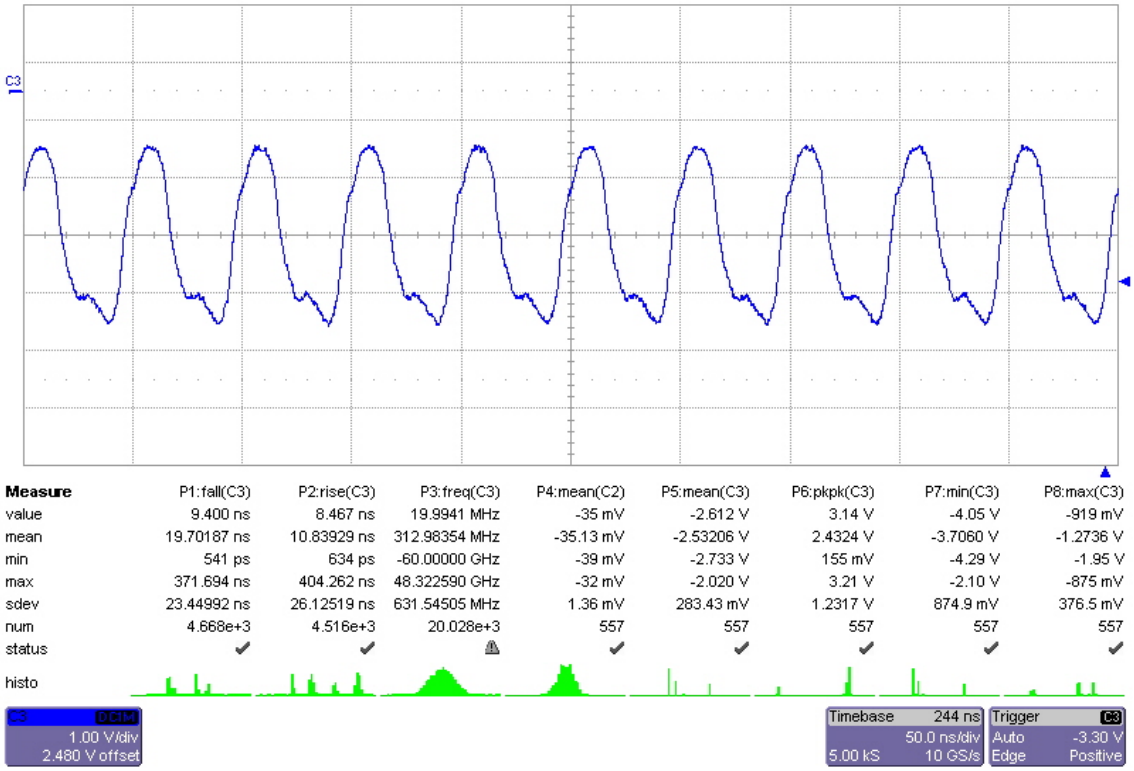


**Figure 99: 3m Cable, SWD-119 Output, Dual Termination, 1MHz Square Wave Input**

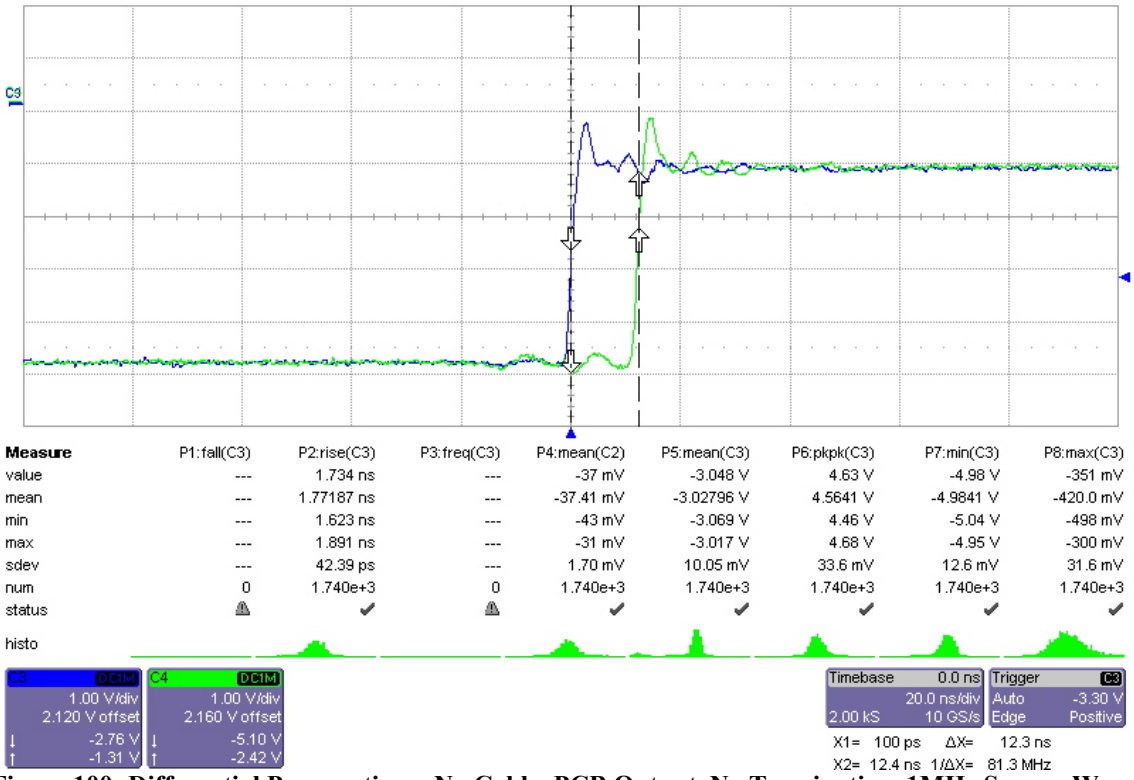


**Figure 100: Differential Propagation – No Cable, PCB Output, No Termination, 1MHz Square Wave**

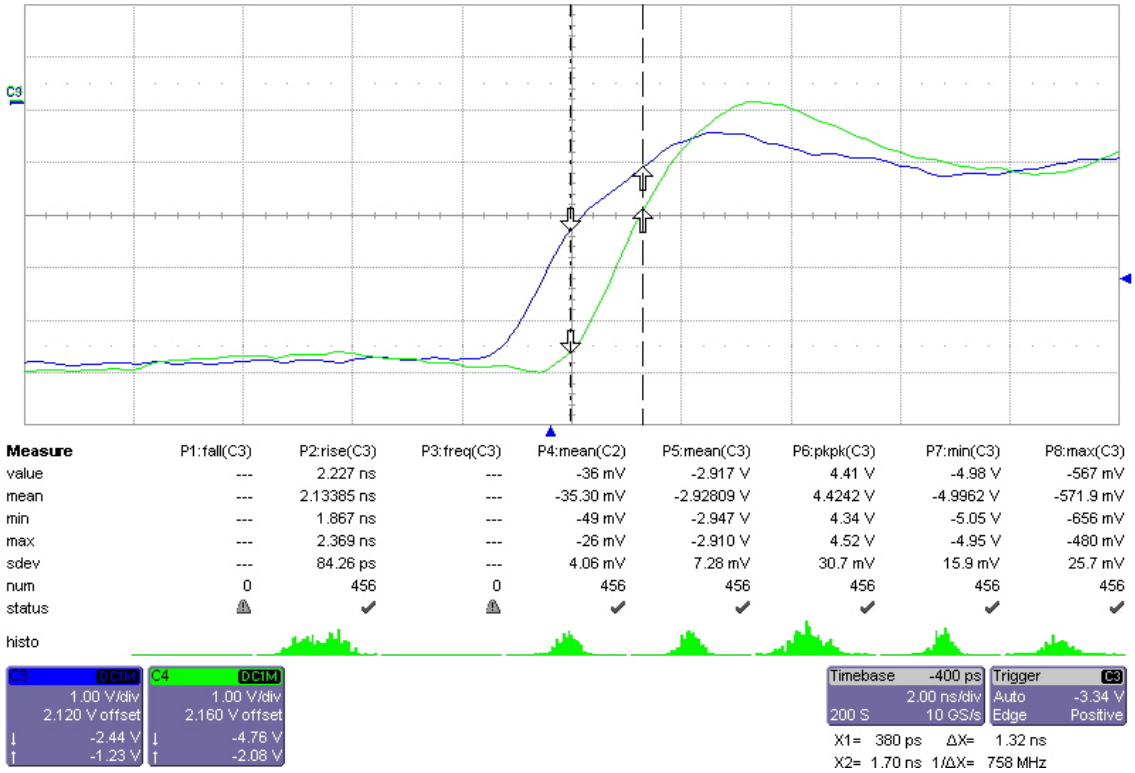


**Figure 101: Differential Propagation – No Cable, PCB Output, No Termination, 20MHz Square Wave**

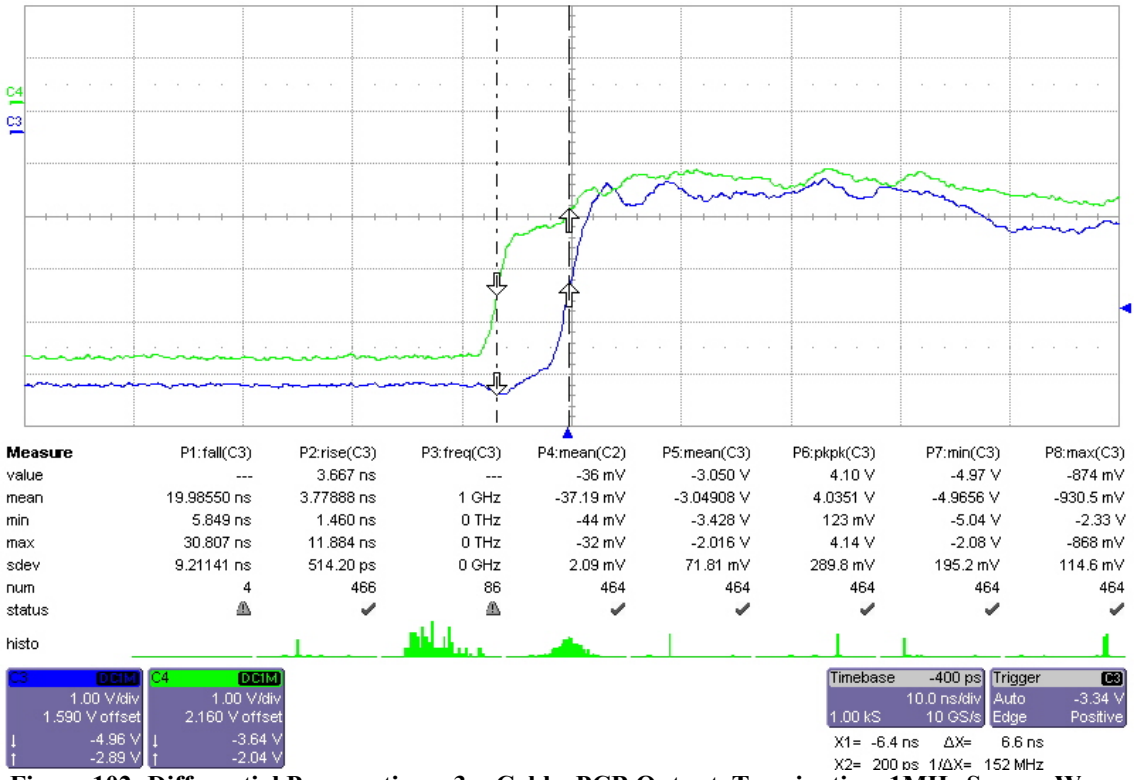


**Figure 102: Differential Propagation – 3m Cable, PCB Output, Termination, 1MHz Square Wave**

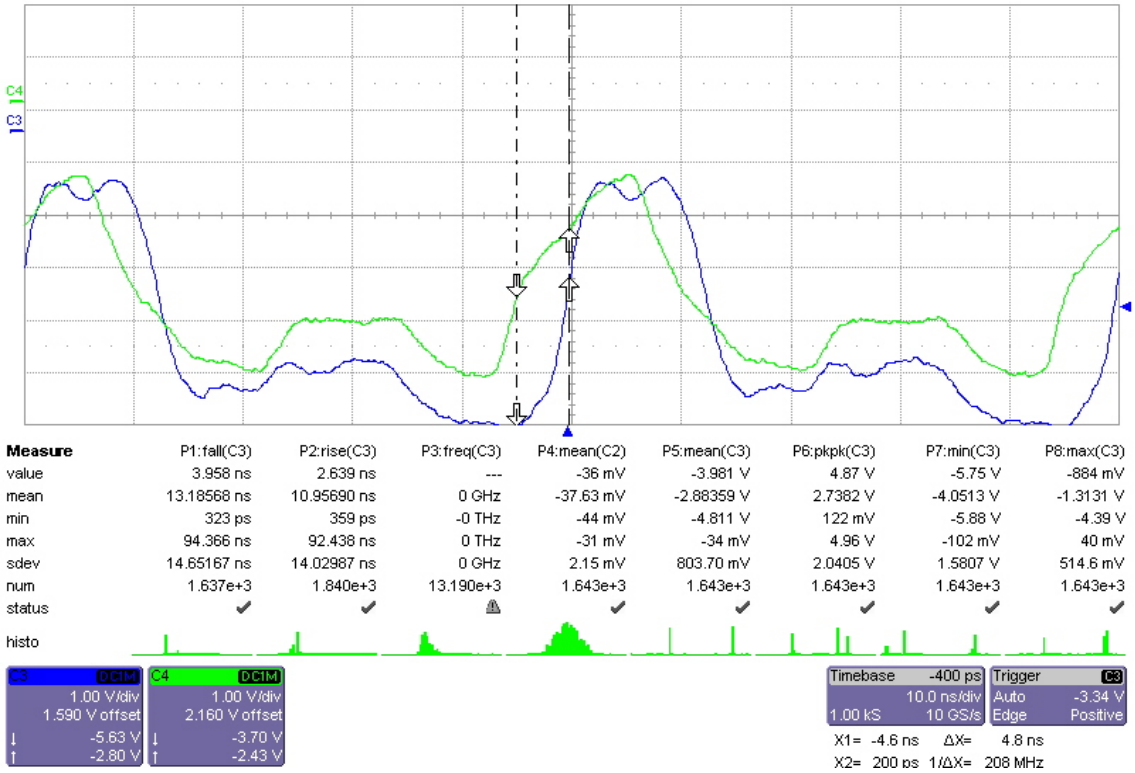


**Figure 103: Differential Propagation – 3m Cable, PCB Output, Termination, 20MHz Square Wave**

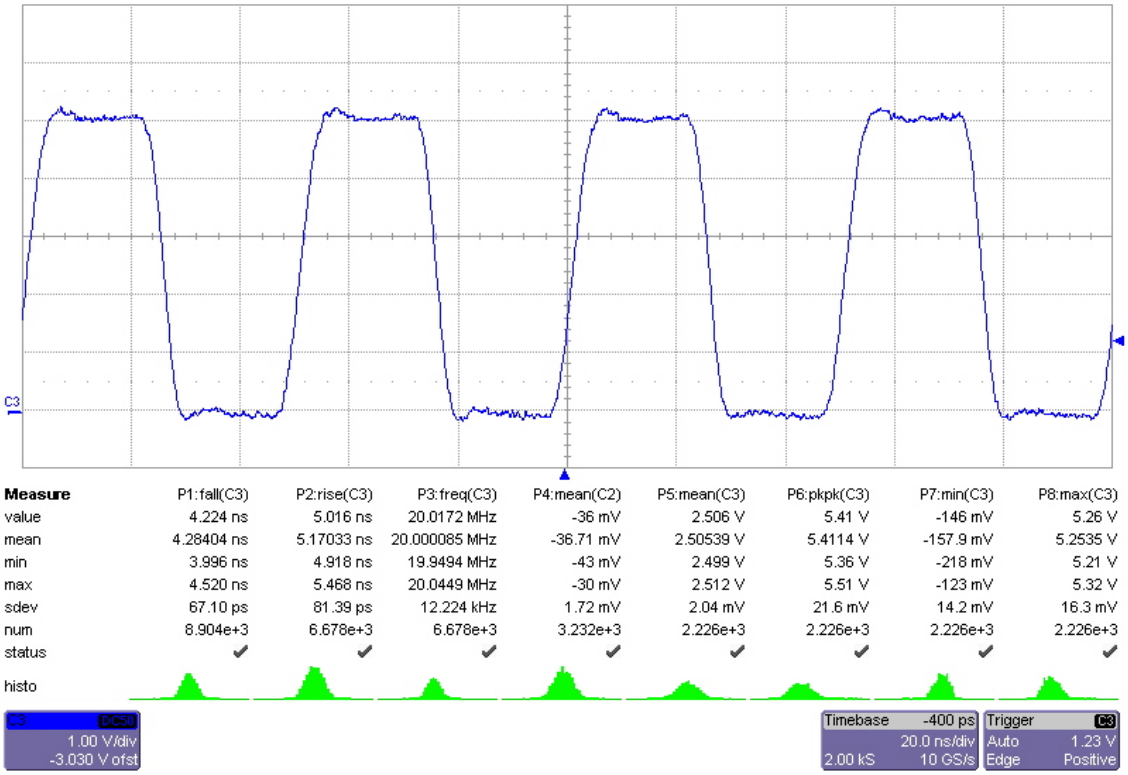


**Figure 104: Input Waveform 20MHz**

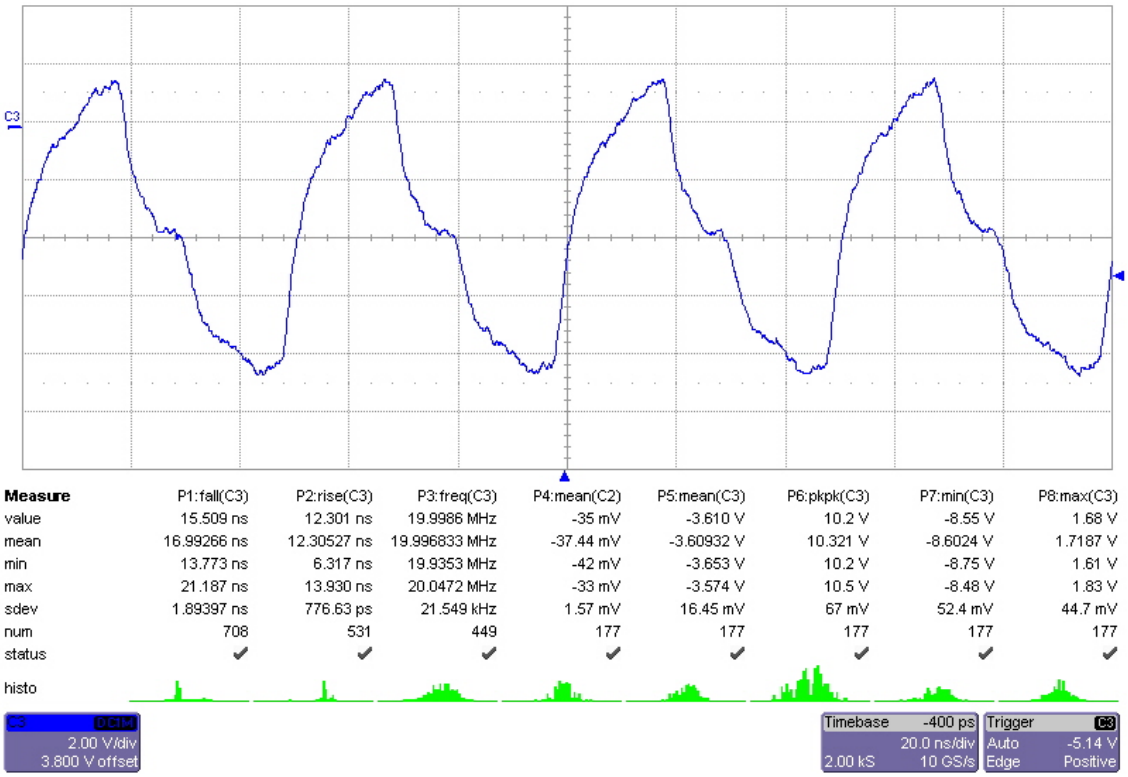


**Figure 105: 3m, PCB Output, 1K Pull-up, 20MHz Square Wave**

## *9.2 – Appendix B: Datasheets of Used Components*

### 9.2.1 – NI PXI-7851R

# R Series Intelligent DAQ with Onboard Processing

## NI R Series

- Onboard FPGA chip, programmable with the LabVIEW FPGA Module
- User-defined triggering, timing, and decision making in hardware with 25 ns resolution
- Up to 8 analog inputs, independent sampling rates up to 750 kHz, 16-bit resolution
- Up to 8 analog outputs, independent update rates up to 1 MHz, 16-bit resolution
- Up to 160 digital lines configurable as inputs, outputs, counters, or custom logic at rates up to 40 MHz
- Direct memory access (DMA) channels for high-speed data streaming
- Implement custom control logic, inline signal processing, and digital communication protocols

**Operating Systems**
- Windows XP/2000
- LabVIEW Real-Time

**Recommended Software**
- LabVIEW
- LabVIEW FPGA Module
  - LabVIEW code compiler for FPGAs
  - Emulated debugging mode
- LabVIEW Real-Time Module

**Driver Software (included)**
- NI-RIO

**Calibration Certificate Available**

| Product | Bus/Form Factor | FPGA | 16-Bit Analog Inputs | Max Sampling Rate per Channel (kS/s) | 16-Bit Analog Outputs | Max Update Rate per Channel (MS/s) | Digital I/O |
|---|---|---|---|---|---|---|---|
| **Multifunction R Series** | | | | | | | |
| NI 7851R | PXI | Virtex-5 LX30 | 8 | 750 | 8 | 1 | 96 |
| NI 7852R | PXI | Virtex-5 LX50 | 8 | 750 | 8 | 1 | 96 |
| NI 7841R | PXI | Virtex-5 LX30 | 8 | 200 | 8 | 1 | 96 |
| NI 7842R | PXI | Virtex-5 LX50 | 8 | 200 | 8 | 1 | 96 |
| NI 7830R | PCI, PXI | Virtex-II 1M gates | 4 | 200 | 4 | 1 | 56 |
| NI 7831R | PCI, PXI | Virtex-II 1M gates | 8 | 200 | 8 | 1 | 96 |
| NI 7833R | PCI, PXI | Virtex-II 3M gates | 8 | 200 | 8 | 1 | 96 |
| **Digital R Series** | | | | | | | |
| NI 7811R | PCI, PXI | Virtex-II 1M gates | – | – | – | – | 160 |
| NI 7813R | PCI, PXI | Virtex-II 3M gates | – | – | – | – | 160 |

*Table 1. R Series Selection Guide*

## Overview

Intelligent DAQ is multifunction data acquisition that features user-defined onboard processing as well as complete flexibility of I/O timing and triggering. You can configure all device functionality by creating NI LabVIEW block diagrams with the LabVIEW FPGA Module. Your block diagram executes in hardware, giving you direct, immediate control of all I/O signals on the PXI or PCI device. With R Series and LabVIEW FPGA, you can configure user-defined hardware for a wide variety of applications requiring precise timing and control such as:

- Data acquisition with flexible triggering and onboard processing
- High-speed analog and discrete control loops
- Pulse-width modulation (PWM) and encoder interfacing
- User-defined digital communication protocols
- Custom counters with up to 64-bit resolution
- Hardware-timed decision making at 40 MHz

## Key Features

Through programming in LabVIEW FPGA, you can control each of the I/O signal lines independently or synchronize a line with other channels. You can configure the digital I/O lines as custom counter/timers, PWM channels, or communication buses for user-defined protocols. All multifunction R Series devices have dedicated analog-to-digital converters/digital-to-analog converters on every analog I/O channel. This offers specialized functionality such as multirate sampling and individual channel triggering, which are beyond the capabilities of typical data acquisition hardware. You can sample every analog input channel on an R Series device simultaneously at rates up to 750 kHz, and you can program every analog output on an R Series device to update simultaneously at rates up to 1 MHz. You can also store your compiled LabVIEW FPGA application in the onboard flash memory of any R Series device and configure it for automatic loading and/or execution at power up.

NATIONAL INSTRUMENTS

## New Virtex-5 FPGAs

The new NI PXI-784x and PXI-785x R Series modules use new Virtex-5 field-programmable gate arrays (FPGAs) with improved optimization capabilities that provide faster code execution and increased code capacity. These Virtex-5 FPGAs feature a new six-input look-up table (LUT) architecture for substantially improved resource utilization as well as DSP48 slices that make it possible for you to implement more complex digital signal processing at faster rates. Previous-generation Virtex-II FPGAs use four-input LUTs for up to 16 combinations of digital logic values. The new Virtex-5 FPGAs use six-input LUTs for up to 64 combinations, increasing the amount of logic that you can implement per slice. In addition, the slices themselves are placed in closer proximity to each other to reduce the propagation delay of electrons and increase overall execution rates. The single-cycle timed loop structure in LabVIEW FPGA takes full advantage of six-input LUTs for substantially improved resource utilization. This means you can optimize more LabVIEW FPGA code to fit within Virtex-5 FPGAs and perform more operations per clock cycle.

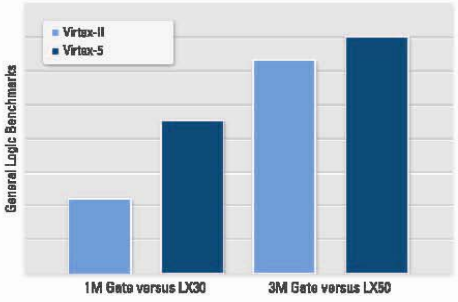


*Figure 1. General logic benchmarks show that Virtex-5 FPGAs offer larger sizes when compared to Virtex-II FPGAs.*

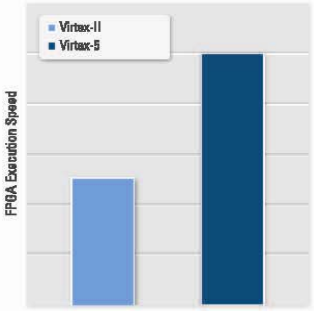


*Figure 2. Execution speed benchmarks show that Virtex-5 FPGAs feature faster processing capabilities when compared to Virtex-II FPGAs.*

For more information on LabVIEW FPGA benchmarks for Virtex-5 FPGAs, visit **ni.com/info** and enter lvfpgabenchmarks.

## Recommended Accessories

### High Performance

**SHC68-68-RMIO** – High-performance shielded 68-conductor cable terminated with a VHDCI 68-pin male connector at one end and a 68-pin female 0.050 D-type connector at the other end that has been specifically designed for the multifunction I/O connector on R Series intelligent DAQ devices.

1 m .....189588-01
2 m .....189588-02

**SHC68-68-RDIO** – High-performance shielded 68-conductor cable terminated with a VHDCI 68-pin male connector at one end and a 68-pin female 0.050 D-type connector at the other end that has been specifically designed for the digital I/O connector on R Series intelligent DAQ devices.

1 m .....191667-01

**SCB-68** – Shielded I/O connector block for rugged, very low-noise signal termination for connecting to 68-pin devices. The SCB-68 also includes two general-purpose breadboard areas.
Dimensions – 19.5 by 15.2 by 4.5 cm (7.7 by 6.0 by 1.8 in.)

SCB-68 .....776844-01

### Low Cost

**SH68-C68-S** – General-purpose shielded cable that connects any type of R Series connector to 68-pin connector blocks.

0.5 m.....186381-0R5
1 m .....186381-01
2 m .....186381-02

### Custom Cabling

**SHC68-NT-S** – Shielded 68-conductor cable terminated with a 68-pin male VHDCI connector at one end and unterminated bare wires at the other. Use this cable, ideal for OEM applications, to create custom cabling solutions for R Series devices.

2 m .....189041-02

**NSC68-262650** – Shielded cable terminated with a VHDCI 68-pin male connector at one end and two 26-pin ribbon connectors and one 50-pin ribbon connector on the other; designed to connect the R Series RMIO connector to standard ribbon cable accessories.

1 m .....189151-01

**NSC68-5050** – Shielded cable terminated with a VHDCI 68-pin male connector at one end and two 50-pin ribbon connectors on the other; designed to connect R Series RDIO connectors to standard ribbon cable accessories.

1 m .....189152-01

### Required Software for R Series Intelligent DAQ

- NI 781xR and 783xR devices require the LabVIEW FPGA Module 7.1 or later, and NI-RIO driver software 1.3 or later.
- NI 784xR and 785xR devices require the LabVIEW FPGA Module 8.5.1 or later, and NI-RIO driver software 2.4 or later.

### Ordering Information

**PCI**

NI PCI-7811R.....779363-01
NI PCI-7813R.....779370-01
NI PCI-7830R.....779361-01
NI PCI-7831R.....778797-01
NI PCI-7833R.....779359-01

**PXI**

NI PXI-7811R.....778800-01
NI PXI-7813R.....779362-01
NI PXI-7830R.....779364-01
NI PXI-7831R.....778668-01
NI PXI-7833R.....779360-01
NI PXI-7841R.....780337-01
NI PXI-7842R.....780338-01
NI PXI-7851R.....780339-01
NI PXI-7852R.....780340-01

*Includes NI-RIO driver software.*

***BUY NOW!***

For complete product specifications, pricing, and accessory information, call 800 813 3693 (U.S.) or go to **ni.com/rseries**.

## Specifications

### Analog Input (NI 783xR/784xR/785xR Only)

#### Input Characteristics

Number of channels
- NI 7830R ..... 4
- NI 7831R/7833R/7841R/ 7842R/7851R/7852R ..... 8

Input modes ..... DIFF, RSE, NRSE (software-selectable; selection applies to all channels)
Type of ADC ..... Successive approximation
Resolution ..... 16 bits, 1 in 65,536
Conversion time
- NI 783xR/NI 784xR ..... 4 µs
- NI 785xR ..... 1 µs

Maximum sampling rate
- NI 783xR/NI 784xR ..... 200 kS/s (per channel)
- NI 785xR ..... 750 kS/s (per channel)

Input impedance
- Powered on ..... 10 GΩ in parallel with 100 pF
- Powered off/overload ..... 4.0 kΩ min

Input signal range ..... ±10 V
Input bias current
- NI 783xR ..... ±2 nA
- NI 784xR/785xR ..... ±5 nA

Input offset current
- NI 783xR ..... ±1 nA
- NI 784xR/785xR ..... ±5 nA

Input coupling ..... DC
- Maximum working voltage (signal + common mode) ..... Inputs should remain within ±12 V of ground
- Overvoltage protection
  - Powered on ..... ±42 V
  - Powered off ..... ±35 V

Data transfers ..... DMA, interrupts, programmed I/O

### Accuracy Information – NI 783xR

| Nominal Range (V) | | Absolute Accuracy | | | | | | | Relative Accuracy | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | % of Reading | | | Noise + Quantization | | | | Resolution (µV) | |
| Positive Full Scale | Negative Full Scale | 24 Hours | 1 Year | Offset (µV) | Single Point | Averaged | Temp Drift (%/°C) | Absolute Accuracy at Full Scale (±mV) | Single Point | Averaged |
| 10.0 | -10.0 | 0.0496 | 0.0507 | 2,542 | 1779 | 165 | 0.0005 | 7.78 | 2,170 | 217 |

**Note:** Accuracies are valid for measurements following an internal calibration. Averaged numbers assume dithering and averaging of 100 single-channel readings. Measurement accuracies are listed for operational temperatures within ±1 °C of internal calibration temperature and ±10 °C of external or factory-calibration temperature.

### Accuracy Information – NI 784xR/785xR

| Nominal Range (V) | | Absolute Accuracy | | | | | | | Relative Accuracy | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | % of Reading | | | Noise + Quantization | | | | Resolution (µV) | |
| Positive Full Scale | Negative Full Scale | 24 Hours | 1 Year | Offset (µV) | Single Point | Averaged | Temp Drift (%/°C) | Absolute Accuracy at Full Scale (±mV) | Single Point | Averaged |
| 10.0 | -10.0 | 0.0186 | 0.0228 | 1,591 | 1,029 | 91.6 | 0.0005 | 3.97 | 1,205 | 121 |

**Note:** Accuracies are valid for measurements following an internal calibration. Averaged numbers assume dithering and averaging of 100 single-channel readings. Measurement accuracies are listed for operational temperatures within ±1 °C of internal calibration temperature and ±10 °C of external or factory-calibration temperature.

#### DC Transfer Characteristics

INL
- NI 783xR ..... ±3 LSB typ, ±6 LSB max
- NI 784xR/785xR ..... ±1 LSB typ, ±3 LSB max

DNL
- NI 783xR ..... -1.0 to +2.0 LSB max
- NI 784xR/785xR ..... ±0.4 LSB typ, ±0.9 LSB max

No missing codes
- NI 783xR ..... 16 bits typ, 15 bits min
- NI 784xR/785xR ..... 16 bits guaranteed

CMRR, DC to 60 Hz ..... -86 dB

#### Settling Time

| Device | Step Size | Accuracy | | |
|---|---|---|---|---|
| | | 16 LSB | 4 LSB | 2 LSB |
| NI 783xR | ±20.0 V | 7.5 µs | 10.3 µs | 40 µs |
| | ±2.0 V | 2.7 µs | 4.1 µs | 5.1 µs |
| | ±0.2 V | 1.7 µs | 2.9 µs | 3.6 µs |
| NI 784xR/ 785xR | ±20.0 V | 2.1 µs | 4.2 µs | 8 µs |
| | ±2.0 V | 1.3 µs | 1.6 µs | 1.8 µs |
| | ±0.2 V | 0.8 µs | 1.1 µs | 1.2 µs |

Crosstalk ..... -80 dB, DC to 100 kHz

#### Dynamic Characteristics

Bandwidth
- NI 783xR
  - Small signal (-3 dB) ..... 650 kHz
  - Large signal (1% THD) ..... 55 kHz
- NI 784xR/785xR
  - Small signal (-3 dB) ..... 1 MHz
  - Large signal (1% THD) ..... 500 kHz

### Analog Output (NI 783xR/784xR/785xR Only)

#### Output Characteristics

Output type ..... Single-ended, voltage output
Number of channels
- NI 7830R ..... 4
- NI 7831R/7833R/7841R/ 7842R/7851R/7852R ..... 8

Resolution ..... 16 bits, 1 in 65,536
Update time ..... 1.0 µs
Maximum update rate ..... 1 MS/s
Type of DAC ..... Enhanced R-2R
Data transfers ..... DMA, interrupts, programmed I/O

## Voltage Output

| | |
|---|---|
| Range | ±10 V |
| Output coupling | DC |
| Output impedance | |
| NI 783xR | 1.25 Ω |
| NI 784xR/785xR | 0.5 Ω |
| Current drive | ±2.5 mA |
| Protection | Short-circuit to ground |
| Power-on state | User configurable |

## Accuracy Information

| Absolute Accuracy | | | | | | |
|---|---|---|---|---|---|---|
| Nominal Range (V) | | % of Reading | | | | Absolute |
| Positive Full Scale | Negative Full Scale | 24 Hours | 1 Year | Offset (µv) | Temp Drift (%/°C) | Accuracy at Full Scale (mV) |
| 10.0 | -10.0 | 0.0335 | 0.0351 | 2,366 | 0.0005 | 5.88 |

*Note:* Accuracies are valid for analog output following an internal calibration. Analog output accuracies are listed for operation temperatures within ±1 °C of internal calibration temperature and ±10 °C of external or factory calibration temperature. Temperature drift applies only if ambient is greater than ±10 °C of previous external calibration.

## DC Transfer Characteristics

| | |
|---|---|
| INL | ±0.5 LSB typ, ±4.0 LSB max |
| DNL | ±0.5 LSB typ, ±1 LSB max |
| Monotonicity | 16 bits, guaranteed |

## Settling Time

| Step Size | Accuracy | | |
|---|---|---|---|
| | 16 LSB | 4 LSB | 2 LSB |
| ±20.0 V | 6.0 µs | 6.2 µs | 7.2 µs |
| ±2.0 V | 2.2 µs | 2.9 µs | 3.8 µs |
| ±0.2 V | 1.5 µs | 2.6 µs | 3.6 µs |

## Dynamic Characteristics

| | |
|---|---|
| Slew rate | 10 V/µs |
| Noise | 150 $\mu V_{rms}$, DC to 1 MHz |
| Glitch energy at midscale transition | ±200 mV for 3 µs |

## Digital I/O

| | |
|---|---|
| Number of channels | |
| NI 7811R/7813R | 160 |
| NI 7830R | 56 |
| NI 7831R/7833R/7841R/ 7842R/7851R/7852R | 96 |
| Digital logic levels | 3.3 V TTL, 5 V TTL Compatible |

| Level | Min (V) | Max (V) |
|---|---|---|
| Input low voltage ($V_{IL}$) | 0.0 V | 0.8 V |
| Input high voltage ($V_{IH}$) | 2.0 V | 5.5 V |
| Output low voltage ($V_{OL}$), where $I_{OUT}$ = -4 mA | – | 0.4 V |
| Output high voltage ($V_{OH}$), where $I_{OUT}$ = 4 mA | 2.4 V | 3.3 V |

| | |
|---|---|
| Output current | |
| Source | 4.0 mA |
| Sink | 4.0 mA |
| Input leakage current | ±10 µA |
| Power-on state | Programmable, by line |
| Data transfers | DMA, interrupts, programmed I/O |
| Protection | |
| Input | |
| NI 781xR/783xR | -0.5 to 7.0 V, single line |
| NI 784xR/785xR | -20.0 to 20.0 V, single line |
| Output | Short-circuit (up to eight lines may be shorted at a time) |
| Minimum pulse width | |
| Input | 25 ns |
| Output | 12.5 ns |
| Minimum sampling period | |
| NI 781xR/783xR | 5 ns |
| NI 784xR/785xR | 8.33 ns |

## Reconfigurable FPGA

### NI 7811R/7830R/7831R

| | |
|---|---|
| FPGA type | Virtex-II 1000 |
| Number of flip-flops | 10,240 |
| Number of 4-input LUTs | 10,240 |
| Number of 18x18 multipliers | 40 |
| Embedded block RAM | 720 kb |

### NI 7813R/7833R

| | |
|---|---|
| FPGA type | Virtex-II 3000 |
| Number of flip-flops | 28,672 |
| Number of 4-input LUTs | 28,672 |
| Number of 18x18 multipliers | 96 |
| Embedded block RAM | 1,728 kb |

### NI 7841R/7851R

| | |
|---|---|
| FPGA type | Virtex-5 LX30 |
| Number of flip-flops | 19,200 |
| Number of 6-input LUTs | 19,200 |
| Number of DSP48 slices (25x18 multipliers) | 32 |
| Embedded block RAM | 1,152 kb |

### NI 7842R/7852R

| | |
|---|---|
| FPGA type | Virtex-5 LX50 |
| Number of flip-flops | 28,800 |
| Number of 6-input LUTs | 28,800 |
| Number of DSP48 slices (25x18 multipliers) | 48 |
| Embedded block RAM | 1,728 kb |

## Timebases

| | |
|---|---|
| NI 781xR/783xR | 40, 80, 120, 160, or 200 MHz |
| NI 784xR/785xR | 40, 80, or 120 MHz |
| Timebase reference sources | |
| NI PCI-781xR/783xR | Onboard clock only |
| NI PXI-78xxR | Onboard clock, phase-locked to PXI 10 MHz clock |
| Timebase accuracy, onboard clock | ±100 ppm, 250 ps peak-to-peak jitter |
| Phase-locked to PXI 10 MHz clock (NI PXI-78xxR only) | Adds 350 ps peak-to-peak jitter |

Additional frequency-dependent peak-to-peak jitter

| | |
|---|---|
| NI 781xR/783xR | |
| 40 MHz | None |
| 80 MHz | 400 ps |
| 120 MHz | 720 ps |
| 160 MHz | 710 ps |
| 200 MHz | 700 ps |
| NI 784xR/785xR | |
| 40 MHz | None |
| 80 MHz | 460 ps |
| 120 MHz | 172 ps |

## Calibration (NI 783xR/784xR/785xR Only)

| | |
|---|---|
| Recommended warm-up time | 15 minutes |
| Calibration interval | 1 year |
| Onboard calibration reference | |
| DC level | 5.000 V (±3.5 mV) (actual value stored in flash memory) |
| Temperature coefficient | ±5 ppm/°C max |
| Long-term stability | ±20 ppm/$\sqrt{1{,}000\ h}$ |

**Note:** Refer to Calibration Certificates at **ni.com/calibration** to generate a calibration certificate for the NI 783xR.

## Bus Interface

| | |
|---|---|
| PXI (NI PXI-78xxR only) | Master, slave |
| PCI (NI PCI-781xR/783xR only) | Master, slave |

## Physical

| | |
|---|---|
| Dimensions (not including connectors) | |
| NI PCI-781xR/783xR | 17 by 11 cm (6.7 by 4.3 in.) |
| NI PXI-78xxR | 16 by 10 cm (6.3 by 3.9 in.) |
| Weight | |
| NI PCI-781xR/783xR | 112 g |
| NI PXI-78xxR | 152 g |
| I/O connectors | |
| NI 781xR | Four 68-pin female high-density VHDCI type |
| NI 783xR/784xR/785xR | Three 68-pin female high-density VHDCI type |

## Maximum Working Voltage

Maximum working voltage refers to the signal voltage plus the common-mode voltage.

| | |
|---|---|
| Channel-to-earth | ±12 V, Measurement Category I |
| Channel-to-channel | ±24 V, Measurement Category I |

**Caution:** Do not use the NI 783xR/784xR/785xR for connection to signals in Measurement Category II, III, or IV.

## Power Requirement

| | |
|---|---|
| +5 VDC (±5%)[1] | |
| NI 781xR | 9 mA (typ), 50 mA (max) |
| NI 7830R/7831R | 330 mA (typ), 355 mA (max) |
| NI 7833R | 364 mA (typ), 586 mA (max) |
| NI 7841R/7851R | 125 mA (typ), 252 mA (max) |
| NI 7842R/7852R | 136 mA (typ), 291 mA (max) |
| +3.3 VDC (±5%)[2] | |
| NI 7811R | 650 mA (typ), 1,000 mA (max) |
| NI 7813R | 850 mA (typ), 1,350 mA (max) |
| NI 7830R/7831R | 462 mA (typ), 660 mA (max) |
| NI 7833R | 727 mA (typ), 1,148 mA (max) |
| NI 7841R/7851R | 525 mA (typ), 1,244 mA (max) |
| NI 7842R/7852R | 604 mA (typ), 1,484 mA (max) |
| +12 V | |
| NI 784xR/785xR | 0.5 A |
| -12 V | |
| NI 784xR/785xR | 0.25 A |
| +5 V terminal | |
| Connector 0 | 0.5 A max |
| Connector 1 | 0.5 A max |
| Connector 2 | 0.5 A max |
| All connectors | 1.5 A max[3] |

To calculate the total current sourced by the digital outputs use the following equation:

$$\sum_{i=1}^{j} \text{current sourced on channel } i$$

| | |
|---|---|
| Power available at I/O connectors | 4.50 to 5.25 VDC at 1 A total, 250 mA per I/O connector pin |

*[1] Does not include current drawn from the +5 V line on the I/O connectors.*

*[2] Does not include current sourced by the digital outputs.*

*[3] The NI 784xR/785xR devices have a user-replaceable socketed fuse that opens when current exceeds the current specification. Refer to the* R Series Intelligent DAQ User Manual, *available at ni.com/manuals, for information about fuse replacement.*

## Environmental

NI 78xxR devices are intended for indoor use only.

### Operating Environment

| | |
|---|---|
| NI 781xR | 0 to 55 °C (tested in accordance with IEC-60068-2-1 and IEC-60068-2-2) |
| NI 7830R, NI 7831R | |
| 40 or 80 MHz timebase | 0 to 55 °C (tested in accordance with IEC-60068-2-1 and IEC-60068-2-2) |
| NI 7833R/7841R/7842R/7851R/7852R | |
| 40 MHz timebase | 0 to 55 °C (tested in accordance with IEC-60068-2-1 and IEC-60068-2-2) |
| 80 MHz timebase | 0 to 55 °C except the following: 0 to 45 °C when installed in an NI PXI-1000/B or NI PXI-101x (tested in accordance with IEC-60068-2-1 and IEC-60068-2-2) |
| Relative humidity range | 10 to 90%, noncondensing (tested in accordance with IEC-60068-2-56) |
| Altitude | 2,000 m at 25 °C ambient temperature |

### Storage Environment

| | |
|---|---|
| Ambient temperature range | -20 to 70 °C (tested in accordance with IEC-60068-2-1 and IEC-60068-2-2) |
| Relative humidity range | 5 to 95%, noncondensing (tested in accordance with IEC-60068-2-56) |

**Note:** Clean the device with a soft, nonmetallic brush. Make sure that the device is completely dry and free from contaminants before returning it to service.

### Shock and Vibration (for NI PXI-78xxR Only)

| | |
|---|---|
| Operational Shock | 30 g peak, half-sine, 11 ms pulse (tested in accordance with IEC-60068-2-27; test profile developed in accordance with MIL-PRF-28800F) |
| Random Vibration | |
| Operating | 5 to 500 Hz, 0.3 $g_{rms}$ |
| Nonoperating | 5 to 500 Hz, 2.4 $g_{rms}$ (tested in accordance with IEC-60068-2-64; nonoperating test profile exceeds the requirements of MIL-PRF-28800F, Class 3) |

## Safety and Compliance

### Safety

NI 78xxR devices are designed to meet the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1

**Note:** For UL and other safety certifications, refer to the product label or visit **ni.com/certification**, search by model number or product line, and click the appropriate link in the Certification column.

### Electromagnetic Compatibility

This product is designed to meet the requirements of the following standards of EMC for electrical equipment for measurement, control, and laboratory use:

- EN 61326 EMC requirements; Minimum Immunity
- EN 55011 Emissions; Group 1, Class A
- CE, C-Tick, ICES, and FCC Part 15 Emissions; Class A

**Note:** For EMC compliance, operate this device according to product documentation.

### CE Compliance

This product meets the essential requirements of applicable European Directives, as amended for CE marking, as follows:

- 2006/95/EC; Low-Voltage Directive (safety)
- 2004/108/EC; Electromagnetic Compatibility Directive (EMC)

**Note:** Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, visit **ni.com/certification**, search by model number or product line, and click the appropriate link in the Certification column.

### Environmental Management

National Instruments is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial not only to the environment but also to NI customers.

For additional environmental information, refer to the NI and the Environment Web page at **ni.com/environment**. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

### Waste Electrical and Electronic Equipment (WEEE)

**EU Customers:** At the end of their life cycle, all products must be sent to a WEEE recycling center. For more information about WEEE recycling centers and National Instruments WEEE initiatives, visit **ni.com/environment/weee.htm**.

电子信息产品污染控制管理办法（中国 RoHS）

中国客户 National Instruments 符合中国电子信息产品中限制使用其益有害物质指令（RoHS）。关于 National Instruments 中国 RoHS 合规性信息，请登录 ni.com/environment/rohs_china。(For information about China RoHS compliance, go to ni.com/environment/rohs_china.)

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We also offer service programs that provide automatic upgrades to your application development environment and higher levels of technical support. Visit **ni.com/ssp**.

## Hardware Services

### NI Factory Installation Services

NI Factory Installation Services (FIS) is the fastest and easiest way to use your PXI or PXI/SCXI combination systems right out of the box. Trained NI technicians install the software and hardware and configure the system to your specifications. NI extends the standard warranty by one year on hardware components (controllers, chassis, modules) purchased with FIS. To use FIS, simply configure your system online with **ni.com/pxiadvisor**.

### Calibration Services

NI recognizes the need to maintain properly calibrated devices for high-accuracy measurements. We provide manual calibration procedures, services to recalibrate your products, and automated calibration software specifically designed for use by metrology laboratories. Visit **ni.com/calibration**.

### Repair and Extended Warranty

NI provides complete repair services for our products. Express repair and advance replacement services are also available. We offer extended warranties to help you meet project life-cycle requirements. Visit **ni.com/services**.

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351588A-01 2008-9412-301-101-D

## 9.2.2 – SWD-119 Datasheet

tyco Electronics

M/A-COM

**Quad Driver for GaAs FET Switches and Attenuators** — **SWD-119 V6**

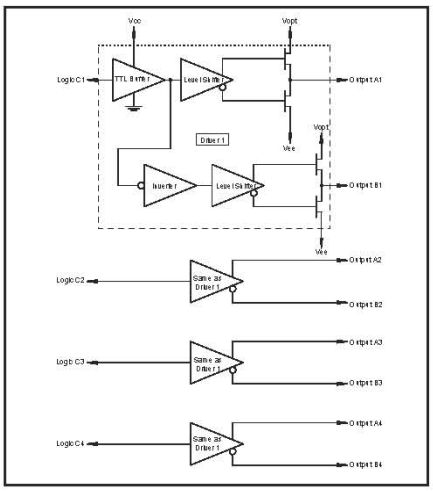
### Features

- High Speed CMOS Technology
- Quad Channel
- Positive Voltage Control
- Low Power Dissipation
- Low Cost Plastic SOIC-16 Package

### Description

The SWD-119 is a quad channel driver used to translate TTL control inputs into gate control voltages for GaAs FET microwave switches and attenuators. High speed analog CMOS technology is utilized to achieve low power dissipation at moderate to high speeds, encompassing most microwave switching applications. The output HIGH level is optionally 0 to +2.0V (relative to GND) to optimize the intermodulation products of the control devices at low frequencies.

### Functional Schematic




### Ordering Information

| Part Number | Package |
|---|---|
| SWD-119 PIN | Bulk Packaging |
| SWD-119TR | 1000 piece reel |

Note: Reference Application Note M513 for reel size information.

### Truth Table

| Input | Outputs | |
|---|---|---|
| CX | A | B |
| Logic "0" | $V_{EE}$ | $V_{OPT}$ |
| Logic "1" | $V_{OPT}$ | $V_{EE}$ |

### Pin Configuration

| Pin No. | Function | Pin No. | Function |
|---|---|---|---|
| 1 | Vee | 9 | Output A1 |
| 2 | Vcc | 10 | Output B1 |
| 3 | C4 | 11 | Output A2 |
| 4 | C3 | 12 | Output B2 |
| 5 | C2 | 13 | Output A3 |
| 6 | C1 | 14 | Output B3 |
| 7 | Vopt | 15 | Output A4 |
| 8 | Ground | 16 | Output B4 |



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## Guaranteed Operating Ranges

| Symbol | Parameter [1] | Unit | Min. | Typ. | Max. |
|---|---|---|---|---|---|
| $V_{CC}$ | Positive DC Supply Voltage | V | 4.5 | 5.0 | 5.5 |
| $V_{EE}$ | Negative DC Supply Voltage | V | -8.5 | -5.0 | -4.5 |
| $V_{OPT}$ [2] | Optional DC Output Supply Voltage | V | 0 | 1.0 | 2.0 |
| $V_{OPT}$-$V_{EE}$ | Negative Supply Voltage Range | V | 4.5 | 6.5 | 8.5 |
| $V_{CC}$-$V_{EE}$ | Positive to negative Supply Range | V | 9.0 | 10.0 | 14.0 |
| $T_A$ | Operating Ambient temperature | °C | -40 | +25 | +85 |
| $I_{OH}$ | DC Output Current - High | mA | — | — | -1.0 |
| $I_{OL}$ | DC Output Current - Low | mA | — | — | 1.0 |
| $T_{rise}$, $T_{fall}$ | Maximum Input Rise or Fall Time | nS | — | — | 500 |

1. All voltages are relative to GND.
2. $V_{OPT}$ is grounded for most applications. To improve the intermodulation performance and the 1 dB compression point of GaAs control devices at low frequencies, $V_{OPT}$ can be increased to between 1.0 and 2.0V. The nonlinear characteristics of the GaAs control devices will approximate performance at 500 MHz. It should be noted that the control current that is on the GaAs MMICs will increase when positive controls are applied.

## DC Characteristics over Guaranteed Operating Range

| Symbol | Parameter | Test Conditions | | Units | Min. | Typ. | Max. |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | Guaranteed High Input Voltage | | V | 2.0 | — | — |
| $V_{IL}$ | Input Low Voltage | Guaranteed Low Input Voltage | | V | — | — | 0.8 |
| $V_{IH}$ | Output High Voltage | $I_{OH}$ = -1 mA | $V_{EE}$ = Max | V | $V_{OPT}$ -0.1 | — | — |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 1 mA | $V_{EE}$ = Max | V | — | — | $V_{EE}$ +0.1 |
| $I_{IN}$ | Input Leakage Current | $V_{IN}$ = $V_{CC}$ or GND | $V_{EE}$ = Min | µA | -1.0 | 0 | 1.0 |
| $I_{CC}$ | Quiescent Supply Current | $V_{CC}$ = Max<br>$V_{OPT}$ = Min or Max | $V_{EE}$ = Min<br>$V_{IN}$ = $V_{CC}$ or GND | µA | — | 250 | 400 |
| $\Delta I_{CC}$ | Additional Supply Current, per TTL Input pin | $V_{CC}$= Max | $V_{IN}$ = $V_{CC}$ -2.1V | mA | — | — | 1.0 |





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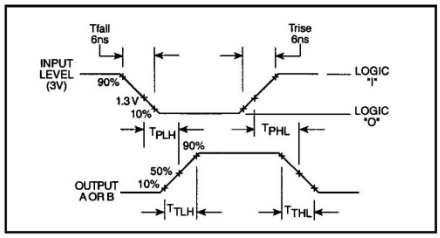
## AC Characteristics Over Guaranteed Operating Range [3]

| Symbol | Parameter | -55 to +25°C | ≤+85°C | ≤+125°C | Unit |
|---|---|---|---|---|---|
| $T_{PLH}$ | Propagation Delay | 22 | 25 | 30 | nS |
| $T_{PHL}$ | Propagation Delay | 22 | 25 | 30 | nS |
| $T_{TLH}$ | Output Rising Transition Time | 9.0 | 9.0 | 9.0 | nS |
| $T_{THL}$ | Output Falling Transition Time | 8.0 | 8.0 | 8.0 | nS |
| $T_{skew}$ | Delay Skew, Output A to Output B | 4.0 | 4.0 | 4.0 | nS |
| $C_{IN}$ | Input Capacitance | 10 | 10 | 10 | pF |
| $C_{PDC}$ | Power Dissipation Capacitance [4] | 10 | 10 | 10 | pF |
| $C_{PDE}$ | Power Dissipation Capacitance [4] | 140 | 140 | 140 | pF |

3. $V_{CC}$ = 4.5V, $V_{OPT}$ - $V_{EE}$ = min or max, $V_{OPT}$ = 0V, $C_L$ = 25 pF, Trise, Tfall = 6nS. These conditions represent the worst case for slow delays.
4. Total Power Dissipation is calculated by the following formula: PD = $V_{CC}$ $^2$f$C_{PDC}$ + ($V_{OPT}$-$V_{EE}$) $^2$f$C_{PDE}$

## Switching Waveforms




## Absolute Maximum Ratings[5]

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Positive DC Supply Voltage | -0.5 | 7.0 | V |
| $V_{EE}$ | Negative DC Supply Voltage | -9.0 | 0.5 | V |
| $V_{OPT}$ | Optional DC Output Supply Voltage | -0.5 | Vcc +0.5 | V |
| $V_{OPT}$-$V_{EE}$ | Output to Negative Supply Voltage Range | -0.5 | 9.0 | V |
| $V_{CC}$-$V_{EE}$ | Positive to Negative Supply Voltage Range | -0.5 | 14.5 | V |
| $V_I$ | DC Input Voltage | -0.5 | $V_{CC}$ +0.5 | V |
| $I_I$ | DC Input Current | -25 | 25 | mA |
| $V_O$ | DC Output Voltage | $V_{EE}$ –0.5 | $V_{OPT}$ +0.5 | V |
| $P_D$[6] | Power Dissipation in Still Air | — | 500 | mW |
| $T_{STG}$ | Storage Temperature | -65 | 150 | °C |

5. All voltages are referenced to GND. All inputs and outputs incorporate latch-up protection structures.
6. Derate -7 mW/°C from 65°C to 85°C.





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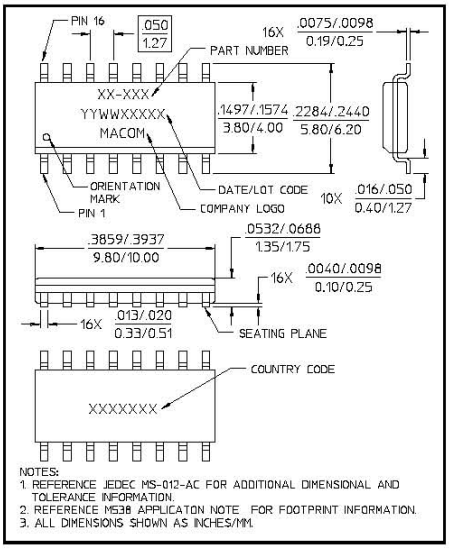
## SO-16





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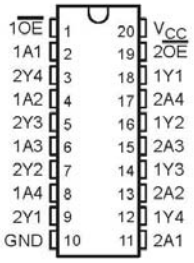
## 9.2.3 – SN74ABT244A Datasheet

**SN54ABT244, SN74ABT244A**
**OCTAL BUFFERS/DRIVERS**
**WITH 3-STATE OUTPUTS**

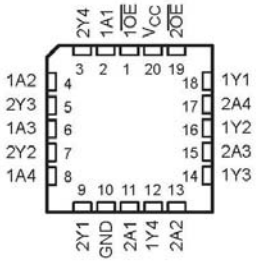
SCBS099J – JANUARY 1991 – REVISED APRIL 2005

- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Typical $V_{OLP}$ (Output Ground Bounce) < 1 V at $V_{CC}$ = 5 V, $T_A$ = 25°C**
- **High-Drive Outputs (−32-mA $I_{OH}$, 64-mA $I_{OL}$)**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Plastic (N) and Ceramic (J) DIPs, and Ceramic Flat (W) Package**

**SN54ABT244 . . . J OR W PACKAGE**
**SN74ABT244A . . . DB, DW, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54ABT244 . . . FK PACKAGE**
**(TOP VIEW)**




### description

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Together with the SN54ABT240, SN74ABT240A, SN54ABT241, and SN74ABT241A, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical active-low output-enable ($\overline{OE}$) inputs, and complementary OE and $\overline{OE}$ inputs.

The SN54ABT244 and SN74ABT244A are organized as two 4-bit buffers/line drivers with separate $\overline{OE}$ inputs. When $\overline{OE}$ is low, the devices pass noninverted data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

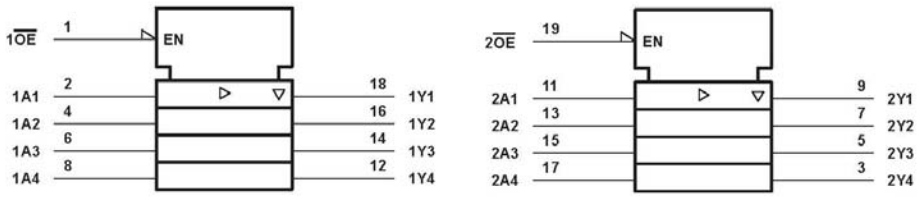
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT244 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ABT244A is characterized for operation from −40°C to 85°C.

**FUNCTION TABLE**
**(each buffer)**

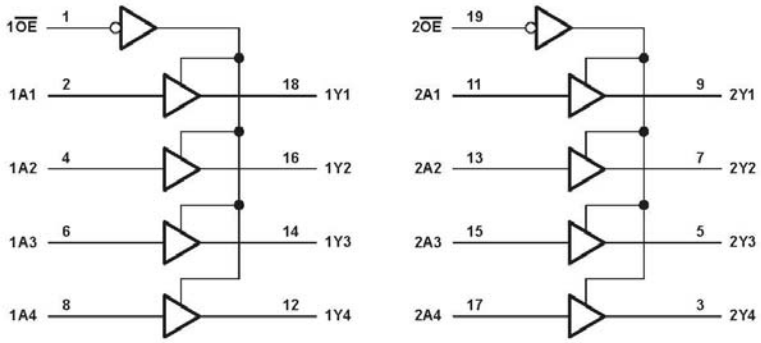
| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{OE}$ | A | Y |
| L | H | H |
| L | L | L |
| H | X | Z |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . −0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, $V_O$ . . . . . −0.5 V to 5.5 V
Current into any output in the low state, $I_O$: SN54ABT244 . . . . . 96 mA
SN74ABT244A . . . . . 128 mA
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . −18 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0) . . . . . −50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package . . . . . 115°C/W
DW package . . . . . 97°C/W
N package . . . . . 67°C/W
PW package . . . . . 128°C/W
Storage temperature range, $T_{stg}$ . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

### recommended operating conditions (see Note 3)

| | | | SN54ABT244 | | SN74ABT244A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | | −24 | | −32 | mA |
| $I_{OL}$ | Low-level output current | | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Outputs enabled | | 5 | | 5 | ns/V |
| $T_A$ | Operating free-air temperature | | −55 | 125 | −40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER | | TEST CONDITIONS | | $T_A$ = 25°C | | | SN54ABT244 | | SN74ABT244A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | | −1.2 | | −1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −3 mA | 2.5 | | | 2.5 | | 2.5 | | V |
| | | $V_{CC}$ = 5 V, | $I_{OH}$ = −3 mA | 3 | | | 3 | | 3 | | |
| | | $V_{CC}$ = 4.5 V | $I_{OH}$ = −24 mA | 2 | | | 2 | | | | |
| | | | $I_{OH}$ = −32 mA | 2* | | | | | 2 | | |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V | $I_{OL}$ = 48 mA | | | 0.55 | | 0.55 | | | V |
| | | | $I_{OL}$ = 64 mA | | | 0.55* | | | | 0.55 | |
| $V_{hys}$ | | | | | 100 | | | | | | mV |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ or GND | | | ±1 | | ±1 | | ±1 | µA |
| $I_{OZH}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 10 | | 10 | | 10 | µA |
| $I_{OZL}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | | −10 | | −10 | | −10 | µA |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_I$ or $V_O$ ≤ 5.5 V | | | ±100 | | | | ±100 | µA |
| $I_{CEX}$ | | $V_{CC}$ = 5.5 V | Outputs high | | | 50 | | 50 | | 50 | µA |
| $I_O$‡ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.5 V | −50 | −100 | −180 | −50 | −180 | −50 | −180 | mA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | Outputs high | | 1 | 250 | | 250 | | 250 | µA |
| | | | Outputs low | | 24 | 30 | | 30 | | 30 | mA |
| | | | Outputs disabled | | 0.5 | 250 | | 250 | | 250 | µA |
| $\Delta I_{CC}$§ | Data inputs | $V_{CC}$ = 5.5 V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND | Outputs enabled | | | 1.5 | | 1.5 | | 1.5 | mA |
| | | | Outputs disabled | | | 0.05 | | 0.05 | | 0.05 | |
| | Control inputs | $V_{CC}$ = 5.5 V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND | | | | 1.5 | | 1.5 | | 1.5 | |
| $C_i$ | | $V_I$ = 2.5 V or 0.5 V | | | 3.5 | | | | | | pF |
| $C_o$ | | $V_O$ = 2.5 V or 0.5 V | | | 7.5 | | | | | | pF |

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at $V_{CC}$ = 5 V.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than $V_{CC}$ or GND.

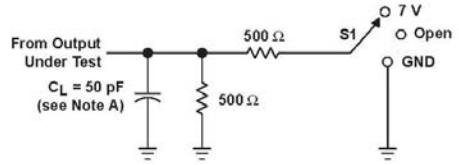
**switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54ABT244 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | MIN | MAX | |
| | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A | Y | 1 | 2.6 | 4.1 | 1 | 5.3 | ns |
| $t_{PHL}$ | | | 1 | 2.9 | 4.2 | 1 | 5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | 1.1 | 3.1 | 4.6 | 0.8 | 5.7 | ns |
| $t_{PZL}$ | | | 2.1 | 4.1 | 5.6 | 1.2 | 7.9 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | 2.1 | 4.1 | 5.6 | 1.2 | 7.6 | ns |
| $t_{PLZ}$ | | | 1.5 | 3.7 | 5.6 | 1 | 7.9 | |

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)**

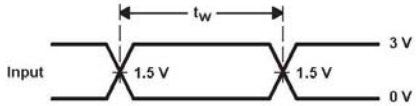
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN74ABT244A | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | MIN | MAX | |
| | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A | Y | 1 | 2.6 | 4.1 | 1 | 4.6 | ns |
| $t_{PHL}$ | | | 1 | 2.9 | 4.3 | 1 | 4.6 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | 1.1 | 3.1 | 4.6 | 1.1 | 5.1 | ns |
| $t_{PZL}$ | | | 2.1 | 4.1 | 5.6 | 2.1 | 6.1 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | 1.8 | 4.1 | 5.6 | 1.8 | 6.6 | ns |
| $t_{PLZ}$ | | | 1.4 | 3.7 | 5.2 | 1.4 | 5.7 | |

## PARAMETER MEASUREMENT INFORMATION

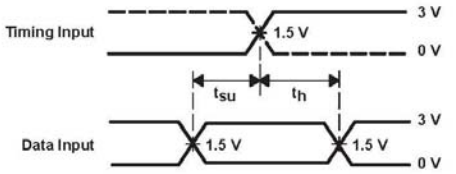



LOAD CIRCUIT

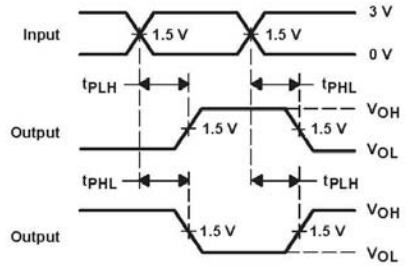
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V |
| $t_{PHZ}/t_{PZH}$ | Open |



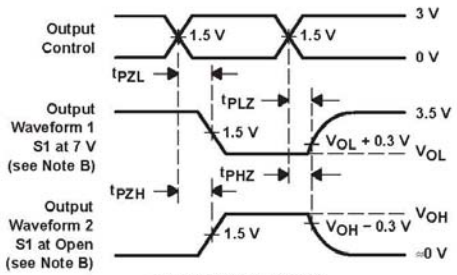

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| 5962-9214701M2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| 5962-9214701MRA | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| 5962-9214701MSA | ACTIVE | CFP | W | 20 | 1 | TBD | Call TI | N / A for Pkg Type |
| SN74ABT244ADB | ACTIVE | SSOP | DB | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT244ADBE4 | ACTIVE | SSOP | DB | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT244ADBG4 | ACTIVE | SSOP | DB | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT244ADBLE | OBSOLETE | SSOP | DB | 20 | | TBD | Call TI | Call TI |
| SN74ABT244ADBR | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT244ADBRG4 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT244ADW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT244ADWE4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT244ADWG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT244ADWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT244ADWRE4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT244ADWRG4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT244AN | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74ABT244ANE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74ABT244ANSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT244ANSRE4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT244ANSRG4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT244APW | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT244APWE4 | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT244APWG4 | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT244APWLE | OBSOLETE | TSSOP | PW | 20 | | TBD | Call TI | Call TI |
| SN74ABT244APWR | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT244APWRE4 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT244APWRG4 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| SNJ54ABT244FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| SNJ54ABT244J | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| SNJ54ABT244W | ACTIVE | CFP | W | 20 | 1 | TBD | Call TI | N / A for Pkg Type |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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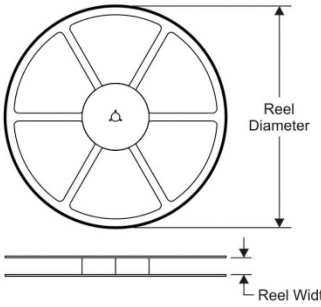
**OTHER QUALIFIED VERSIONS OF SN54ABT244, SN74ABT244A :**
- Catalog: SN74ABT244
- Enhanced Product: SN74ABT244A-EP

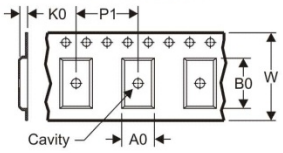
NOTE: Qualified Version Definitions:
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

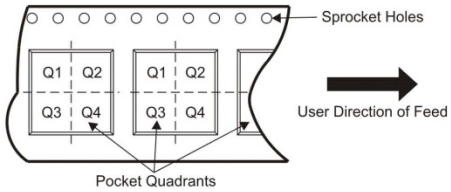



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

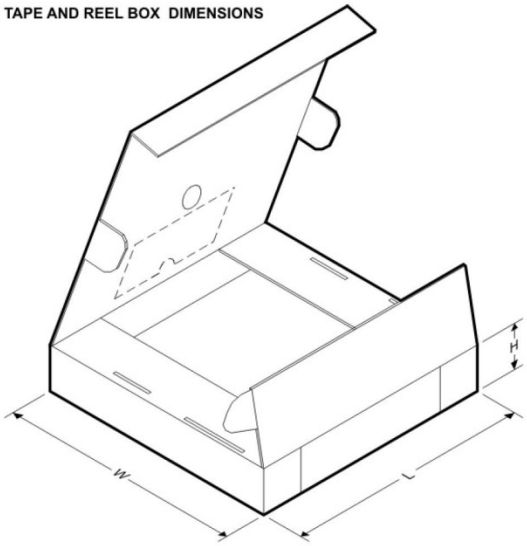
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74ABT244ADBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74ABT244ADWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.0 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74ABT244ANSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.2 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74ABT244APWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



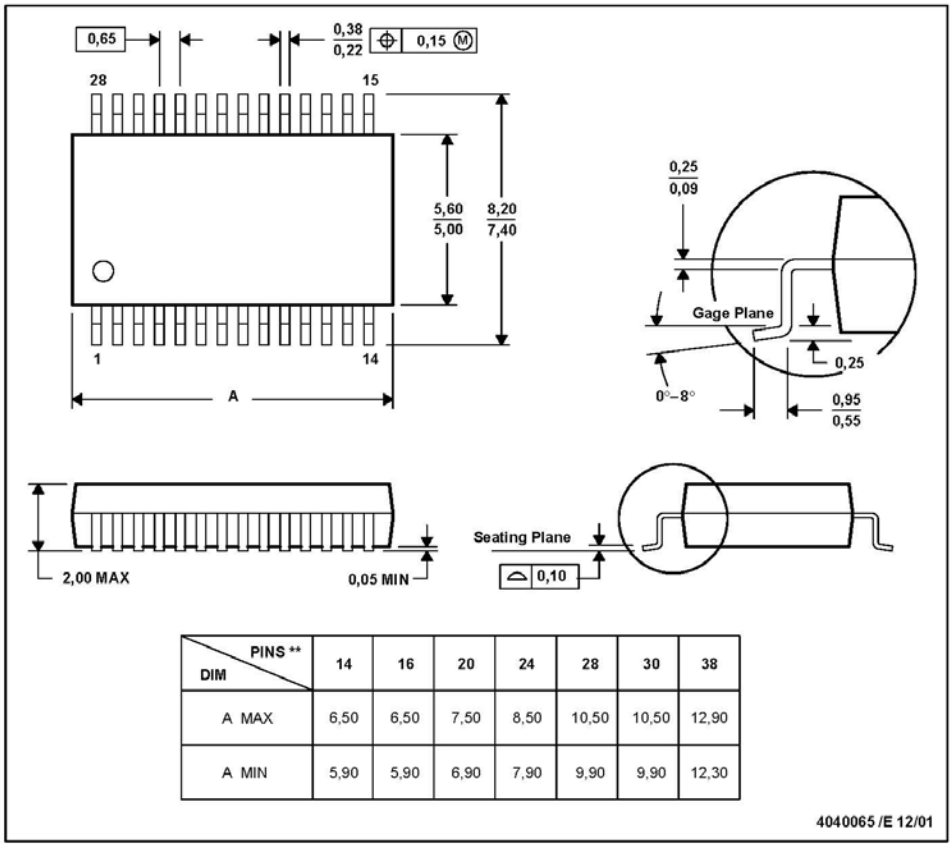

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74ABT244ADBR | SSOP | DB | 20 | 2000 | 346.0 | 346.0 | 33.0 |
| SN74ABT244ADWR | SOIC | DW | 20 | 2000 | 346.0 | 346.0 | 41.0 |
| SN74ABT244ANSR | SO | NS | 20 | 2000 | 346.0 | 346.0 | 41.0 |
| SN74ABT244APWR | TSSOP | PW | 20 | 2000 | 346.0 | 346.0 | 33.0 |

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

**DB (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 20 | 24 | 28 | 30 | 38 |
|---|---|---|---|---|---|---|---|
| A MAX | 6,50 | 6,50 | 7,50 | 8,50 | 10,50 | 10,50 | 12,90 |
| A MIN | 5,90 | 5,90 | 6,90 | 7,90 | 9,90 | 9,90 | 12,30 |

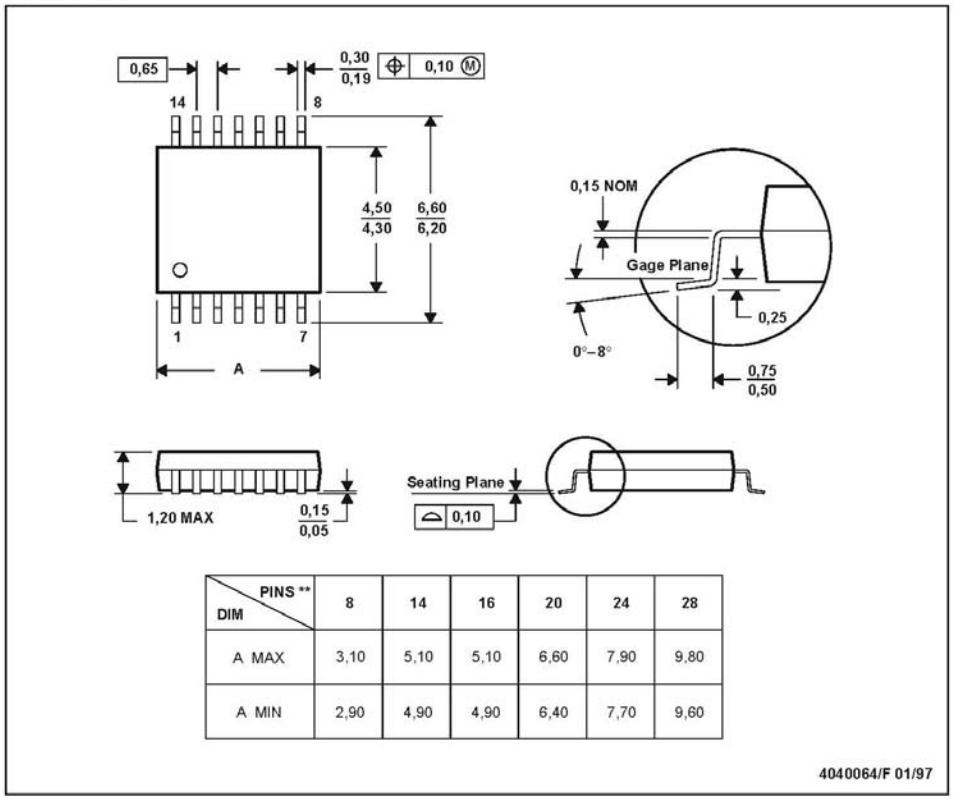
4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

MTSS001C – JANUARY 1995 – REVISED FEBRUARY 1999

**PW (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN




| DIM \ PINS ** | 8 | 14 | 16 | 20 | 24 | 28 |
|---|---|---|---|---|---|---|
| A MAX | 3,10 | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| A MIN | 2,90 | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

## 9.2.4 – 767 Series Network Resistor Datasheet

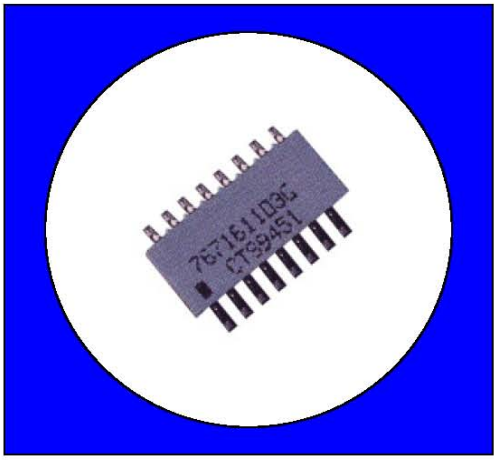
CTS

Leaded Surface Mount Series 767

# Technical Data

### Features

- Medium Body Design
- Solid Ceramic Construction
- No Internal Dendrite Growth
- Meets EIA PDP SOGN-0001 Outline
- Packaged in Tape & Reel or Slide Packs
- Application Specific Circuits Are Available
- Compatible With Reflow Solder Process
- RoHS Compliant



**Resistance Tolerance:**
Standard: ±2% or 0.5Ω (whichever is greater)
Special: ±0.25% or 0.3Ω (whichever is greater)

**Resistance Range:**
Standard: 10Ω to 1 MegΩ

**Operating Temperature Range:**
-55°C to +125°C

**Dielectric Strength:**
100 VAC

**Temperature Coefficient:**
Standard: 100Ω to 1 MegΩ
100PPM/°C typical
10Ω to 99Ω
±200PPM/°C typical

**Maximum Operating Voltage:**
50V not to exceed rated power

**Power Rating (Total Network Power):**

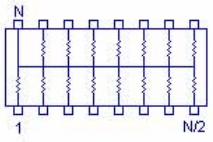
| | 14 Pin | 16 Pin |
|---|---|---|
| @25°C | 2.0w | 2.3w |
| @70°C | 1.3w | 1.5w |

**Maximum Resistor Power:**
(Not to Exceed Total Network Power)

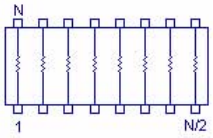
| Schematic | 1 | 3 | 5 | 7 |
|---|---|---|---|---|
| @25°C | 0.15w | 0.30w | 0.15w | 0.15w |
| @70°C | 0.10w | 0.20w | 0.10w | 0.10w |

## Types of Circuits

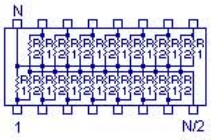
**Bussed (Schematic 1)**



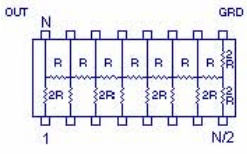

**Isolated (Schematic 3)**

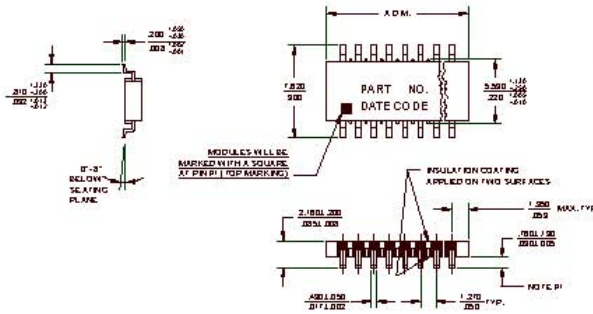



**Dual Terminator (Schematic 5)**



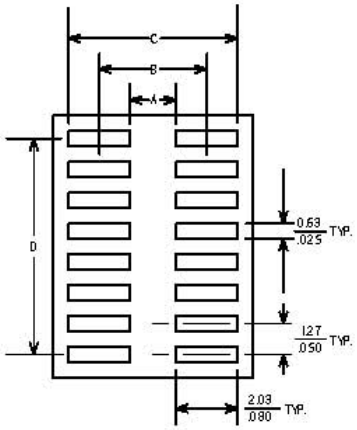

**R/2R Ladder (Schematic 7)**




| No. of Pins | "A" Dimension | |
|---|---|---|
| | mm | in. |
| 14 | 9.91 ±0.25 | 0.390 ±0.010 |
| 16 | 11.18 ±0.25 | 0.440 ±0.010 |
| Notes | | |
| 1. Lead COPLANARITY | | mm 0.10 MAX |
| | | in. 0.004 |
| General Tolerances | | mm ±0.25 |
| | | in. ±0.010 |
| mm & in. DIMENSIONS ARE NOT EQUIVALENT | | |

## Land Patterns




| LEAD COUNT | | A | B | C | D |
|---|---|---|---|---|---|
| 14P | mm | 5.34 | 7.37 | 9.40 | 7.60 |
| | In. | 0.21 | 0.29 | 0.37 | 0.30 |
| 16P | mm | 5.34 | 7.37 | 9.40 | 8.90 |
| | In. | 0.21 | 0.29 | 0.37 | 0.35 |

## Standard Resistor Values & EIA Code

| Ohms | Code | Ohms | Code | Ohms | Code | Ohms | Code | Ohms | Code | Ohms | Code |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 000X | 68 | 680 | 470 | 471 | 3.3K | 332 | 27K | 273 | 220K | 224 |
| 10 | 100 | 75 | 750 | 510 | 511 | 3.9K | 392 | 33K | 333 | 270K | 274 |
| 12 | 120 | 82 | 820 | 560 | 561 | 4.7K | 472 | 39K | 393 | 330K | 334 |
| 15 | 150 | 100 | 101 | 680 | 681 | 5.1K | 512 | 47K | 473 | 390K | 394 |
| 18 | 180 | 110 | 111 | 820 | 821 | 5.6K | 562 | 51K | 513 | 470K | 474 |
| 22 | 220 | 120 | 121 | 1K | 102 | 6.8K | 682 | 56K | 563 | 510K | 514 |
| 27 | 270 | 150 | 151 | 1.2K | 122 | 8.2K | 822 | 68K | 683 | 560K | 564 |
| 33 | 330 | 180 | 181 | 1.5K | 152 | 10K | 103 | 82K | 823 | 680K | 684 |
| 39 | 390 | 220 | 221 | 1.8K | 182 | 12K | 123 | 100K | 104 | 820K | 824 |
| 47 | 470 | 270 | 271 | 2.0K | 202 | 15K | 153 | 120K | 124 | 1M | 105 |
| 51 | 510 | 330 | 331 | 2.2K | 222 | 18K | 183 | 150K | 154 | | |
| 56 | 560 | 390 | 391 | 2.7K | 272 | 22K | 223 | 180K | 184 | | |

## Dual Terminator Resistor Values

The Series 767 part number includes the EIA Code value of the Thevenin equivalent resistances of R1 and R2. The Thevenin equivalent resistance is calculated in the following way: The suffix letter relates only to the sequence of variations that equal the same equivalent resistance. Reference Thevenin Equivalent Resistance Chart

$$R_{eq}=R_1R_2/(R_1 + R_2)$$

| Example: | | | |
|---|---|---|---|
| 767145191A | R1=330 Ohms | R2=470 Ohms | Req=194 Ohms |

Pin N/2 is common to R2 and Pin N is common to R1 on CTS Series 767.

### Thevenin Equivalent Resistance Chart

| R1 Ohms | R2 Ohms | Thevenin Equivalent | CTS Code | R1 Ohms | R2 Ohms | Thevenin Equivalent | CTS Code |
|---|---|---|---|---|---|---|---|
| 25 | 50 | 17 ohm | 150A | 110 | 220 | 73 ohm | 730A |
| 30 | 50 | 19 ohm | 190A | 118 | 178 | 71 ohm | 710A |
| 30 | 620 | 29 ohm | 290A | 120 | 200 | 75 ohm | 750B |
| 33 | 4.7K | 33 ohm | 330A | 120 | 180 | 72 ohm | 720A |
| 36 | 620 | 34 ohm | 340A | 120 | 120 | 60 ohm | 600B |
| 43 | 620 | 40 ohm | 400A | 150 | 150 | 75 ohm | 750A |
| 68 | 189 | 50 ohm | 500B | 160 | 260 | 99 ohm | 990A |
| 75 | 620 | 67 ohm | 670A | 160 | 240 | 96 ohm | 960A |
| 80 | 220 | 59 ohm | 590A | 160 | 270 | 100 ohm | 101D |
| 81 | 130 | 50 ohm | 500A | 162 | 260 | 100 ohm | 101B |
| 81 | 2.2K | 78 ohm | 780A | 180 | 300 | 113 ohm | 111B |
| 100 | 200 | 67 ohm | 670B | 180 | 470 | 130 ohm | 131C |
| 100 | 430 | 81 ohm | 810A | 180 | 390 | 123 ohm | 121A |
| 100 | 150 | 60 ohm | 600A | 180 | 270 | 108 ohm | 111A |
| 106 | 169 | 65 ohm | 650A | 180 | 220 | 99 ohm | 101A |

(Cont.)

## (Cont.) Thevenin Equivalent Resistance Chart

| R1 Ohms | R2 Ohms | Thevenin Equivalent | CTS Code | R1 Ohms | R2 Ohms | Thevenin Equivalent | CTS Code |
|---|---|---|---|---|---|---|---|
| 200 | 1.5K | 176 ohm | 171D | 560 | 1K | 359 ohm | 361A |
| 220 | 330 | 132 ohm | 131A | 680 | 1K | 405 ohm | 401A |
| 220 | 270 | 121 ohm | 121B | 750 | 750 | 375 ohm | 381A |
| 220 | 220 | 110 ohm | 111D | 750 | 2.3K | 566 ohm | 571A |
| 240 | 170 | 100 ohm | 101C | 1K | 3.3K | 767 ohm | 771A |
| 240 | 620 | 173 ohm | 171C | 1K | 2K | 667 ohm | 671A |
| 250 | 250 | 125 ohm | 131B | 1.1K | 2.2K | 733 ohm | 731A |
| 270 | 470 | 171 ohm | 171A | 1.2K | 1.2K | 600 ohm | 601A |
| 270 | 180 | 108 ohm | 111C | 1.5K | 1.5K | 750 ohm | 751A |
| 271 | 131 | 88 ohm | 880A | 1.5K | 3.3K | 1031 ohm | 102A |
| 330 | 470 | 194 ohm | 191A | 2K | 2K | 1000 ohm | 102B |
| 330 | 680 | 222 ohm | 221A | 2.2K | 5.6K | 1579 ohm | 162A |
| 330 | 390 | 179 ohm | 181A | 2.2K | 4.4K | 1467 ohm | 152A |
| 330 | 220 | 132 ohm | 131D | 2.2K | 3.3K | 1320 ohm | 132A |
| 330 | 330 | 165 ohm | 171B | 3K | 6.2K | 2022 ohm | 202A |
| 360 | 720 | 240 ohm | 241B | 3K | 2K | 1200 ohm | 122A |
| 360 | 600 | 225 ohm | 231A | 3.3K | 4.7K | 1939 ohm | 192A |
| 390 | 620 | 239 ohm | 241A | 3.9K | 3.3K | 1788 ohm | 182A |
| 470 | 1K | 320 ohm | 321A | 4.7K | 22K | 3873 ohm | 392A |
| 470 | 680 | 278 ohm | 281A | 5K | 5K | 2500 ohm | 252A |
| 470 | 940 | 313 ohm | 311A | 6.8K | 22K | 5194 ohm | 522A |
| 500 | 500 | 250 ohm | 251A | 10K | 51K | 8361 ohm | 842A |
| 560 | 910 | 347 ohm | 351A | 50K | 100K | 33,333 ohm | 333A |

1. All tolerances +/-2%. 2. Other values available on request. 3. Suffix letter has no significance - assigned in sequential order.

## How to Order

| 767 | 14 | 1 | 103 | G | P | TR13 |
|---|---|---|---|---|---|---|

**Part Number Series**

**Number of Pins**

**Schematic**

1 Bussed
3 Isolated
5 Dual Terminator
7 Ladder

**Resistor Code**

Refer to the EIA Code Schematics
**1 & 3**: Page 3
**5**: Pages 3 & 4

**Packaging**
SP = Slide Pack
TR = Tape & Reel
**Reel Size** – 13 = 13"

**RoHS Compliant**
Solder dipped 96.5Sn/03Ag/.5Cu over Ni on Cu lead wire.

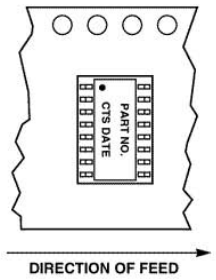
**Tolerance**

| Schematic **1 & 3** | Schematic **5** | Schematic **7** |
|---|---|---|
| J = ±5%<br>G = ±2% (Std.)<br>F = ±1%<br>D = ±1/2% | Tolerance is 2% standard. Refer to dual terminator codes on pages 3&4. Not necessary to add "G" after dual terminator code. | F= ±1LSB<br>D= ±1/2LSB (LSB=Least Significant Bit) |

NOTE: No dashes or spaces to appear in part number.
Example: 767141103GPTR13

## Packaging

| Tape & Reel | 14P | 16P |
|---|---|---|
| Tape width | 24mm | 24mm |
| Tape pitch | 12mm | 12mm |
| Reel diameter | 13" | 13" |
| #parts/reel | 2,000 | 2,000 |
| **Slide Packs** | | |
| Tube length | 20" | 20" |
| #parts/slide pac | 48 | 43 |




## Environmental Performance Specifications

| Test | Max. % Delta R | Mil. Std. 202 Method | Test Cond. | Test Description |
|---|---|---|---|---|
| Thermal Cycling | 0.25% | 107 | B | 5 cycles, -65°C to +125°C |
| Short Time Overload | 0.25% | | | 2 1/2 x rated voltage, 5 sec (100V Max.) |
| Moisture Resistance | 0.5% | 106 | | 240 hours, 0.1 rated load, -10°C to +65°C, 90% RH |
| Load Humidity | 1.0% | | | 1000 hours, 0.1 rated load, 70°C, 85-92% RH |
| High Temp Exposure | 1.0% | | | 240 hours, no load, @ 125°C |
| Load Life | 1.0% | 108 | F | 2000 hours @ 70°C rated load |
| Resistance to Solder Heat | 0.25% | | | 30 seconds @ 218°C, dwell |
| Mechanical Shock | 0.25% | 213 | I | 100g, 1 msec., 3 shocks each plane |
| Vibration | 0.25% | 204 | D | 20g, 10-2000Hz, 4 hours/plane |
| Terminal Strength | 0.25% | | | 0.9 Kg. Pull, 30 sec., two 45° bends |
| Low Temp Storage | 0.25% | | | 24 hours @ -65°C, no load |
| Low Temp Operation | 0.25% | | | 45 min @ -65°C, full load |
| Flammability | N/A | | | 94V-0 |
| Non-Fungus | Pass | | | per MIL-STD 810C |
| Resistance to Solvents | Pass | | | Isopropyl alcohol |
| Solderability | Pass | | | RMA Flux, 230°C, 5 seconds dip, 95% coverage |