# DC/DC Converter for Fuel Cell Bus Charging

A Major Qualifying Project submitted to the faculty of
WORCESTER POLYTECHNIC INSTITUTE
in partial fulfillment of the requirements for the Degree of Bachelor of Science


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**Date:** April 25, 2024


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# Abstract

Our team designed a 3.25kW DC/DC converter (from 50V–100V input to 280–400V output) to charge a LiPo battery from a polymer electrolyte fuel cell for unmanned autonomous vehicle applications. After research and simulation of several boost converter topologies and integrated circuits, we proposed a non-isolated and isolated push-pull design. The push-pull design was favored due to its high efficiency, ease of digital control, and compliance with our design criteria. Our schematic facilitates the design and testing of a PCB layout of the converter in the future.

# Acknowledgements

The members of the team would like to thank our project advisor, Dr. Noetscher, for his support and guidance throughout the academic year. The team would also like to thank Honeywell for mentoring and sponsoring us in this project. In particular, we extend our gratitude to Honeywell engineers Ryan Bussett and Phil Del Signore, who helped our team navigate the challenges of designing a 3.25kW DC/DC boost converter.

# Executive Summary

The project's goal was to design a DC/DC converter for an unmanned autonomous vehicle to charge a lithium-ion battery using power from a fuel cell. Weight and size were among constraints, along with software-selectable limits for input power, output current, and voltage.

The advantages and disadvantages of several boost converter designs, including the quadratic, double cascade, flying capacitor, and interleaved N-phase boost converters, were evaluated. Ultimately, the project's emphasis shifted to investigating integrated circuits for more efficient converter development.

A design process for the DC/DC converter was used to iterate through designs from specifications to PCB layout. We developed design criteria in collaboration with Honeywell and provided a rationale for each criterion to ensure coherence with project objectives.

1. Digital Control Constraints
2. Fuel Cell Constraints
3. Battery Constraints
4. Converter Constraints

Two converters were designed: a non-isolated boost converter, and an isolated push-pull converter. The non-isolated boost converter integrated various converter types that were previously researched, and included a buck-boost, DC/AC, and AC/DC stages. MOSFET drivers and an oscillator stage were also added to ensure proper switching and signal generation. Despite drawbacks such as load dependency and low efficiency, the techniques employed in the design may be applicable to future projects. On the other hand, the isolated push-pull boost converter employed a primary stage with NMOS transistors for switching and a secondary stage with rectifier diodes for waveform rectification. A push-pull PWM controller with the LTC3721 and a DAC for voltage control were also utilized. The transformer selection was prioritized in the design process to minimize weight, alongside the implementation of current mode control with the LTC3721.

In order to accurately simulate the converters, three different methods were developed. One method used variable components for both the PEMFC and the LiPo battery, whereas another represented the PEMFC as a static voltage source in series with a resistor. Although we lacked fuel cell and battery models, the simulations still provided insightful information that helped us improve our designs. A comparative analysis of the two converters favored the isolated design due to its higher efficiency and simpler control mechanisms.

To move forward with our isolated push-pull converter, we tackled component selection, Altium schematic design, and PCB layout. We completed the schematic design; however, the PCB layout never fully came to realization since the focus of our project turned to designing a robust converter schematic, rather than fast-tracking the design process to ensure a PCB layout. Several recommendations were given regarding modifications to our current converter, as well as how to carry out the development of the PCB board.

Ultimately, the isolated push-pull converter was selected as the favored design. Despite not developing a PCB, valuable schematics and insights were provided to Honeywell. Recommendations include further investigating non-isolated topologies; consulting a magnetics company for a custom transformer; exploring synchronization techniques for converter phases; investigating EMI emissions; exploring wide bandgap semiconductor materials; and exploring weight reduction methods while considering thermal management. These recommendations aim to optimize converter performance and practicality for future iterations.

# Authorship Table

| Section Title | Primary Author(s) | Editor(s) |
|---|---|---|
| **Abstract** | Edison | All |
| **Acknowledgments** | Efthymios | All |
| **Executive Summary** | Ryan, Katie | All |
| **1. Introduction** | Katie | Edison |
| **2. Background Research** | | |
| 2.1 General Overview of DC/DC Converters | Katie, Efthymios | Katie, Edison |
| 2.2 The Unmanned Autonomous Vehicle DC/DC Converter | Ryan | Katie, Edison |
| 2.3 The Source and Load | | |
| 2.3.1 The Polymer Electrolyte Membrane Fuel Cell | Edison | Katie, Ryan |
| 2.3.2 The Lithium-Ion Battery | Edison | Katie, Ryan |
| **3. Design Process & Criteria** | | |
| 3.1 The Design Process | Edison | Katie, Ryan |
| 3.2 Design Criteria | | |
| 3.2.1 Honeywell Constraints | Edison | Katie |
| 3.2.2 Fuel Cell Constraints | Edison | Katie |
| 3.2.3 Battery Constraints | Edison | Katie |
| 3.2.4 Converter Constraints | Edison | Katie |
| **4. Open-Loop Boost Converter Topologies** | | |
| 4.1 A Note About the Final Design | Katie | Katie, Ryan |
| 4.2 Quadratic Boost Converter | Katie | Katie, Ryan |

| | | |
|---|---|---|
| 4.3 Double Cascaded Boost Converter | Ryan | Katie |
| 4.4 Flying Capacitor Boost Converter | Efthymios | Katie, Edison |
| 4.5 Interleaved N-Phase Boost Converter | Edison | Edison, Katie |
| 4.6 Converter Research Conclusion & Subsequent Actions | Katie | Edison, Katie |
| **5. Simulation Methodology** | | |
| 5.1 The Modeling Problem | Edison | Katie |
| 5.2 Modeling Approaches | Edison | Katie, Ryan |
| 5.3 Simulation Limitations | Edison | Katie |
| **6. Initial Design: Non-Isolated Boost Converter** | | |
| 6.1 Block Diagram Description | Edison | Katie |
| 6.1.1 Buck-Boost Stage Description | Edison | Katie |
| 6.1.2 DC/AC Stage Description | Edison | Katie |
| 6.1.3 MOSFET Driver Stage Description | Edison | Katie |
| 6.1.4 AC/DC Stage Description | Edison | Katie |
| 6.1.5 Oscillator Stage Description | Edison | Katie |
| 6.2 Design Process | | |
| 6.2.1 Buck-Boost Stage Design | Edison | Katie |
| 6.2.2 DC/AC Stage Design | Edison | Katie |
| 6.2.3 MOSFET Driver Stage Design | Edison | All |
| 6.2.4 AC/DC Stage Design | Edison | Katie |
| 6.2.5 Oscillator Stage Design | Edison | All |
| 6.3 Limitations & Potential Issues | | |
| 6.3.1 Load Dependency | Meng | Edison, Katie |
| 6.3.2 Low Efficiency | Meng | Edison, Katie |

| | | |
|---|---|---|
| **7. Final Design: Isolated Push-Pull Boost Converter** | | |
| 7.1 Block Diagram Description | | |
| 7.1.1 Primary Stage Description | Edison, Ryan, Meng | Katie, Ryan |
| 7.1.2 Secondary Stage Description | Edison, Ryan, Meng | Katie, Ryan |
| 7.1.3 Push-Pull PWM Controller Stage Description | Edison, Ryan, Meng | Katie, Ryan |
| 7.2 Design Process | | |
| 7.2.1 Primary Stage Design | Edison, Ryan, Meng | Katie |
| 7.2.2 Secondary Stage Design | Edison, Ryan, Meng | Katie |
| 7.2.3 Push-Pull PWM Controller Stage Design | Edison, Ryan, Meng | All |
| 7.3 Converter Control | | |
| 7.3.1 Current Mode Control Operation | Edison | Katie |
| 7.3.2 Limiting the Output Voltage, Input Power, & Output Current | Edison, Ryan, Meng | Katie |
| 7.4 Drawbacks & Concerns | | |
| 7.4.1 LTC3721 Limitations | Edison, Efthymios | Katie |
| 7.4.2 Component Ratings | Edison, Efthymios | Katie |
| 7.5 Simulation Test Results | All | All |
| **8. Assessing the Designs** | | |
| 8.1 Comparing the Designs | Edison, Katie | Katie, Ryan |
| 8.2 Design Selection Rationale | Edison, Katie | Katie, Ryan |
| 8.3 Compliance of Selected Design with Design Criteria | Edison, Katie | All |

| | | |
|---|---|---|
| **9. Altium Schematic & PCB Layout** | | |
| 9.1 PCB Development of Our Unmanned Autonomous Vehicle Converter | | |
| 9.1.1 Component Selection and Placement | Meng, Ryan | Katie |
| 9.1.2 Schematic Design and Review | Meng, Ryan | Katie |
| 9.2 Research & Layout Considerations | | |
| 9.2.1 Issue One: High Current Handling | Meng, Ryan | Katie |
| 9.2.2 Issue Two: Effect of Parasitic Inductance & Capacitance | Meng, Ryan | Katie |
| 9.3 Altium Schematic Recommendations & PCB Layout Plan | | |
| 9.3.1 Recommendations for Our Altium Schematic | Meng, Ryan, Edison | Katie |
| 9.3.2 PCB Layout Plan for a Single Phase | Meng, Ryan, Edison | Katie |
| **10. Conclusion & Recommendations** | | |
| 10.1 Conclusion | Katie | Katie, Ryan |
| 10.2 Recommendations | | |
| 10.2.1 Further Investigate Non-Isolated Topologies | Ryan | Katie |
| 10.2.2 Consult a Magnetics Company for a More Practical Transformer | Edison | Katie |
| 10.2.3 Synchronize Each Phase of the Push Pull Converter | Efthymios, Edison | Katie |
| 10.2.4 Investigate Conducted & Radiated Emissions of the Push-Pull Converter | Edison | Katie |
| 10.2.5 Further Investigate MOSFET Selection for the Push-Pull Converter | Katie | Katie, Ryan |
| 10.2.6 Explore the Feasibility of Reducing the Number of Components for the Push-Pull Converter | Edison | Katie |

| **Other Contributions** | | |
|---|---|---|
| **Report Formatting** | Katie, Ryan, Edison | Katie, Ryan, Edison |
| **Bibliography** | Ryan | Ryan |
| **Appendix A: Modeling Method for Chapter 4 Topologies** | Edison | Katie |
| **Appendix B: Simulation Results for Chapter 4 Topologies** | | |
| B.1 Quadratic Boost Converter Simulations | Katie | Katie, Ryan, Edison |
| B.2 Double Cascade Boost Converter Simulations | Ryan | Katie, Ryan, Edison |
| B.3 Interleaved N-Phase Boost Converter Simulations | Edison | Katie, Ryan, Edison |
| **Appendix C: Maximum Input RMS Current of a Buck Converter** | Edison | Ryan |
| **Appendix D: Isolated Design Output Voltage, Output Capacitance, and Inductor Equations** | Edison | Ryan |
| **Appendix E: Input Voltage & Transformer Saturation** | Edison | Ryan |
| **Appendix F: Simulation Test Graphs & Setup** | | |
| F.1 Simulation Test One | Ryan, Edison | Ryan |
| F.2 Simulation Test Two | Ryan, Edison | Ryan |
| F.3 Simulation Test Three | Edison | Ryan |
| F.4 Simulation Test Four | Edison | Ryan |
| F.5 Simulation Test Five | Efthymios, Edison | Ryan |
| F.6 Simulation Test Six | Efthymios, Edison | Ryan |
| F.7 Simulation Test Seven | Meng, Edison | Ryan |
| F.8 Simulation Test Eight | Meng, Edison | Ryan |

# Table of Contents

# List of Figures

# List of Tables

# List of Equations

# 1. Introduction

The goal of this project was to design a 50V–100V input to a 280–400V output DC/DC converter suitable for charging the batteries in an unmanned autonomous vehicle. More specifically, the converter needed to be capable of conditioning 3.25kW of power for a lithium-ion polymer battery from a polymer electrolyte fuel cell, while satisfying the constraints imposed by the fuel cell, battery, and unmanned autonomous vehicle. The intended unmanned autonomous vehicle for the converter was an unmanned aerial vehicle (UAV), but the converter may also be suitable for other types of unmanned vehicles. In addition to the aforementioned constraints, the converter needed to possess the following software-selectable limits:

- Limit the input power to protect the fuel cell from poor operating conditions.
- Limit the total output current (per phase) to reduce heat generation.
- Limit the output voltage and battery charge current to safely charge the battery.

The engineers at Honeywell provided a block diagram of the intended use case.

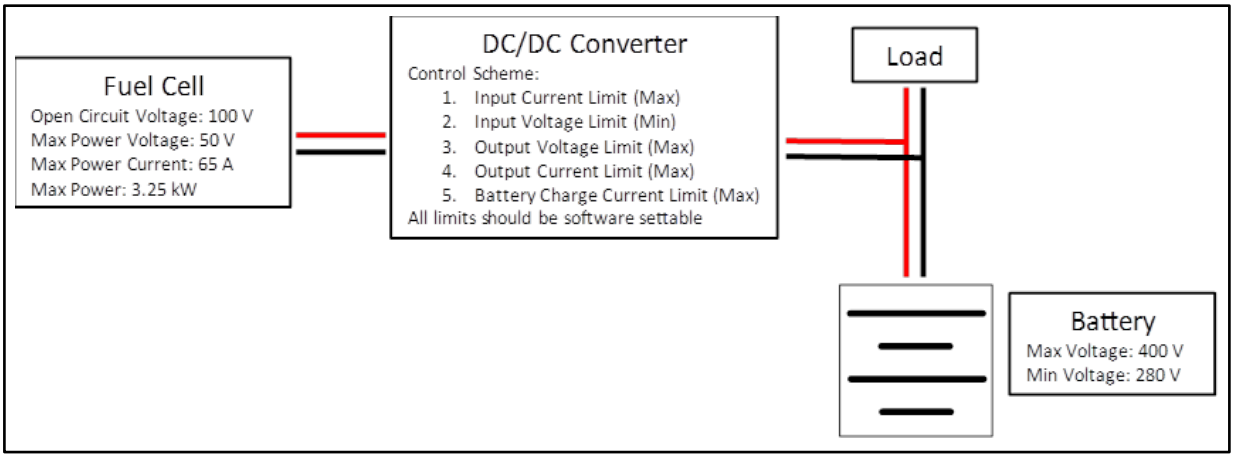


Figure 1.1. Intended use case for the DC/DC converter [1].

The project began by researching and evaluating the feasibility of existing DC/DC converter boost topologies and integrated circuits (ICs). As the project progressed, the focus shifted from designing a converter that could achieve the desired specifications, regardless of size, to designing for smaller weight and size. Our design phase yielded two converters: a non-isolated and an isolated push-pull converter with three phases. Honeywell favored the push-pull converter. As such, the remainder of the project was spent polishing the isolated push-pull converter into a robust schematic to facilitate the development of the printed circuit board (PCB). With more time, the PCB of the push-pull converter would have been designed, tested, and, if needed, redesigned for more suitable characteristics. This paper details the entire design process and provides recommendations for future iterations of the project.

# 2. Background Research

This chapter begins by providing a broad overview on DC/DC converters. Thereafter, we explore the unmanned autonomous vehicle application and provide a description of the source and the load connected to the converter.

## 2.1 General Overview of DC/DC Converters

DC/DC converters are electric circuits that transform voltage and current levels, ideally with the highest possible efficiency. We primarily focused on boost converters, where the output voltage is greater than the input voltage, because our unmanned autonomous vehicle application required a net increase in voltage from the output to the input. DC/DC converters are also classified by how they allow power to flow. Unidirectional converters only allow power to propagate from the input to the output, whereas bidirectional converters allow power to move in either direction. As elaborated upon in Chapter 3, the focus of this project was on unidirectional converters.

The conventional boost converter acted as the basis for our research, so it was important to fully understand the converter in order to make apt comparisons to it. Figure 2.1 illustrates the conventional boost converter.

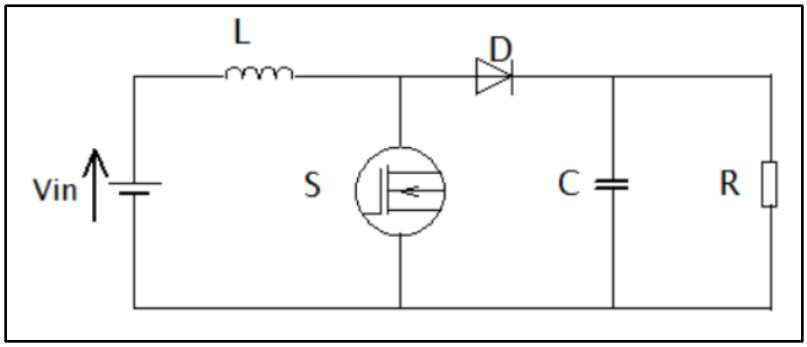


Figure 2.1. Circuit diagram for a conventional boost converter [2].

The conventional boost converter consists of one active switch (MOSFET), one passive switch (diode), as well as an inductor, capacitor, input source, and load. With minimal components, the boost converter can achieve high efficiency if the duty cycle is sufficiently low. Despite its advantages, the single switch and phase can lead to high voltage and current stress, and the ripple current at the input may require a large inductor. We decided to inquire into alternative topologies to achieve a larger conversion ratio while maintaining stable operating conditions for the rest of the system. First, however, we needed to investigate DC/DC converters specifically in unmanned autonomous vehicle applications.

## 2.2 The Unmanned Autonomous Vehicle DC/DC Converter

When designing a DC/DC converter for unmanned autonomous vehicles, general principles should be followed. These criteria aid in the design process to ensure that the converter is functional and appropriate for the application. The desired requirements for our application include, but are not limited to:

1. A conversion ratio (voltage gain) of 8.

2. Unidirectional or bidirectional power flow, depending on the fuel cell system.
3. High power density (influenced by the mass of the converter and cooling equipment).
4. High efficiency.
5. Negligible electromagnetic interference (EMI).
6. Reliability.

The method employed to satisfy these criteria is critical to the design process. For example, to satisfy criterion 3, one approach involves increasing the switching frequency. A high switching frequency can reduce conduction losses, but at the cost of increasing switching losses, likely lowering the efficiency of the converter. As such, the efficiency of the converter could be improved if soft-switching is implemented, lowering the size of cooling equipment. In turn, this can improve the power density of the converter. The power density constraint emphasizes the need for delivering sufficient power while maintaining a sufficiently low overall mass for the system. This is an important consideration in our intended UAV application since weight has a direct influence on flight performance and duration.

Contrary to the other criteria, the EMI criterion does not possess an adequately defined expectation. This is because, as of April 2024, EMI regulations have not been developed for UAV applications. However, once the regulations are developed, it is necessary to determine if the converter complies with the standards. This guarantees that the converter does not interfere with other electronic systems in its vicinity, while also potentially protecting the battery from unexpected voltage transients if an input filter is implemented. Furthermore, meeting these requirements assures the converter's efficacy, contributing to the overall success and safety of UAV flights [3], [4], [5].

## 2.3 The Source and Load

To appropriately design the DC/DC converter, it was necessary to attain an understanding of the fuel cell and battery.

### 2.3.1 The Polymer Electrolyte Membrane Fuel Cell

The input, or power source, to our DC/DC converter is a fuel cell, an electrochemical device. A fuel cell undergoes chemical reactions to produce DC electricity, and, as byproducts, heat and water, when supplied with an appropriate fuel source. The fuel cell that constrained our converter design in this project was a non-regenerative (unidirectional current) 3.25kW 102-cell stack polymer electrolyte fuel cell (PEMFC). These cells were stacked in series to obtain an open-circuit voltage of approximately 100 Volts DC (VDC).

The electrolyte of a PEMFC is a polymer membrane typically coated with a metal catalyst with the purpose of facilitating the flow of ions from the anode to the cathode and vice versa per cell [6]. Within the PEMFC, the electrolyte is located between the anode and cathode of each cell, as illustrated in Figure 2.2.

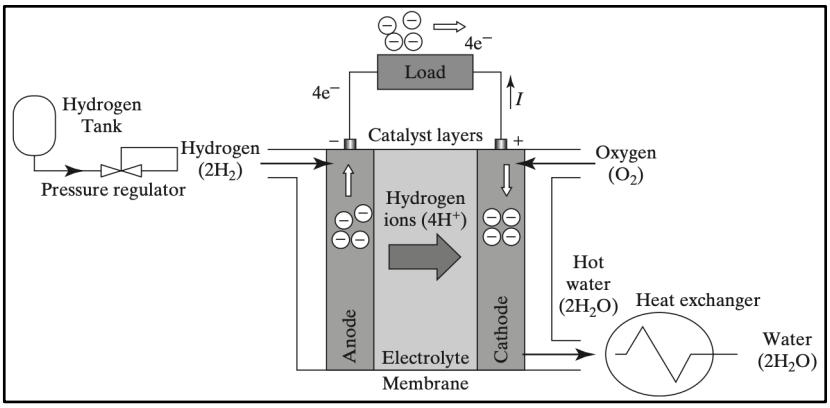


Figure 2.2. Diagram for a single cell of a PEMFC [7].

The chemical process that the PEMFC undergoes to produce electricity and heat can be simplified as follows: hydrogen gas—the fuel source of the PEMFC—is inserted into a channel of the anode. Next, the metal catalyst coating the electrolyte oxidizes hydrogen molecules into hydrogen ions and electrons. The free electrons flow through the electrical load and enter the cathode, whereas the hydrogen ions flow through the electrolyte membrane and reach the surface of the cathode. The free electrons and hydrogen ions combine with oxygen from the surrounding environment to synthesize hot water and heat [7]. The rate free electrons flow from the anode to the cathode of the PEMFC influences the voltage across the terminals of the PEMFC, as evidenced by the IV-characteristic in Figure 2.3.

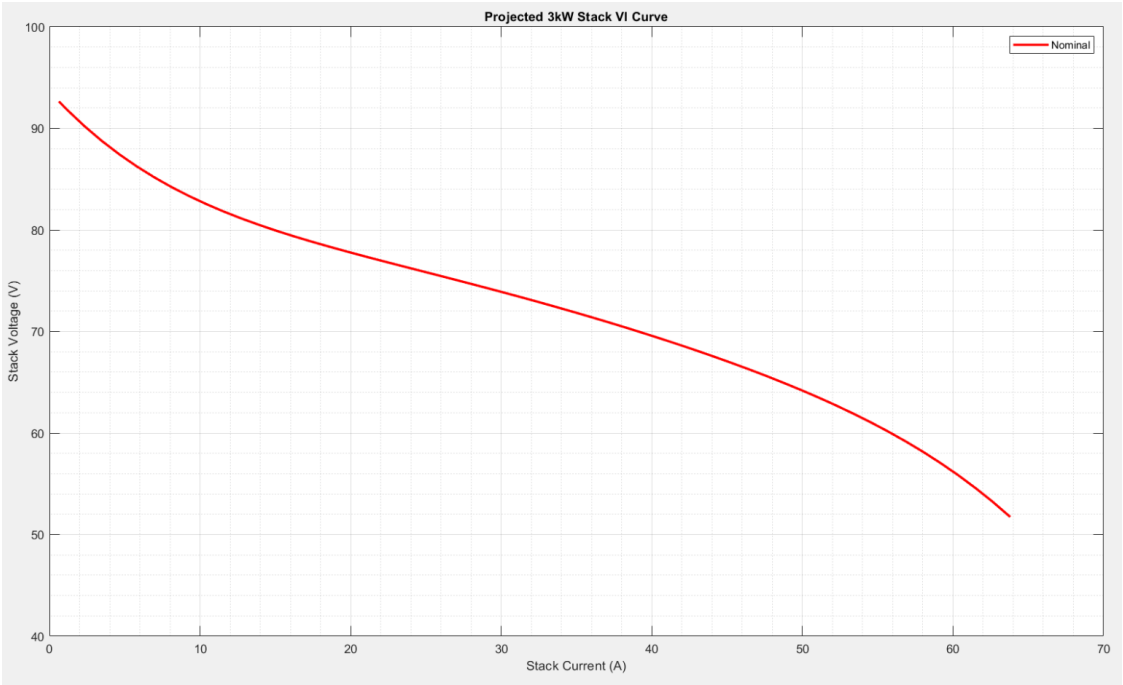


Figure 2.3. Projection of the IV-characteristic of the 3.25 kW 102-cell stack PEMFC [1].

If the rate that the electrons flow from the anode to the cathode is rapid (voltage across the terminals is near zero), the voltage is primarily determined by activation power losses. On the contrary, when electrons flow at a much slower rate from the anode to the cathode (voltage across

terminals is near the open-circuit voltage), the voltage is primarily dictated by mobility inhibition and concentration polarization losses, both can cause power shutdown. When the rate that the electrons flow is between rapid and slow, the voltage across the fuel cell terminals is primarily determined by the ohmic losses of the fuel cell [6]. If the rate that the electrons flow changes quickly, for instance, from the mobility inhibition region to the active region, the voltage across the terminals will undershoot before reaching a steady-state value, reducing the lifetime of the fuel cell [8], [9]. This further implies that, if the rate that the electron flow changes (ripple current) is sufficiently large, the fuel cell lifetime will be further reduced [10], [11]. Hence, the change in the input voltage/power of the converter must be limited and the input ripple current should be sufficiently small to avoid damage to the PEMFC.

### 2.3.2 The Lithium-Ion Polymer Battery

The output, or load, to our DC/DC converter is a multicell lithium-ion battery. In particular, the battery is of the lithium-ion polymer (LiPo) variety, sharing identical operation and construction to the lithium-ion battery technology [12]. LiPo batteries are similar to fuel cells by being electrochemical devices able to undergo chemical reactions to produce DC electricity. However, unlike the PEMFC used in our application, the LiPo battery can convert electrical energy into chemical energy for charging purposes. As a result, the LiPo battery is classified as a secondary battery—a battery that can be electrically recharged and discharged several times. In the context of the unmanned autonomous vehicle application, the LiPo battery is intended to be used as an energy storage device which can be charged when required [13].

Structurally, a cell of a LiPo battery mirrors a PEMFC: an anode and cathode with a porous separation layer which facilitates the flow of ions from the anode to cathode or vice versa. The basic construction of a LiPo cell is depicted in Figure 2.4.

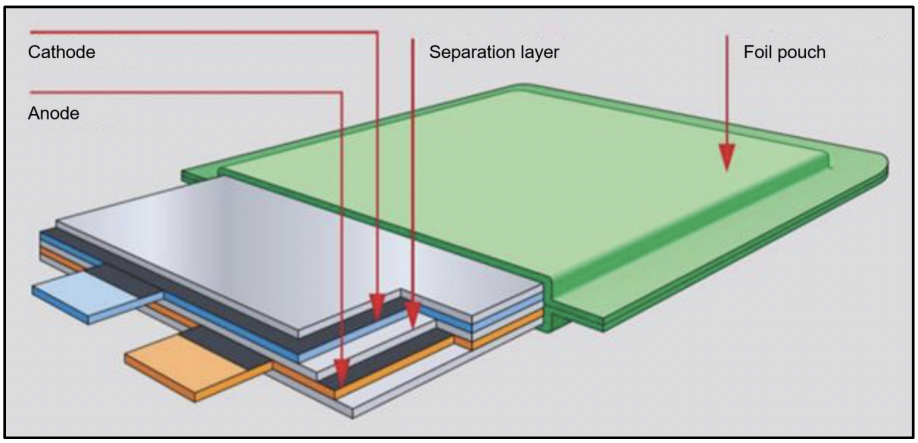


Figure 2.4. Diagram of the basic construction of a LiPo cell [12].

LiPo batteries differ from PEMFCs in regards to the type of compounds which reside in their structure [13]. For voltage applications as high as 400V, the cell in Figure 2.4 consists of a graphite compound at its anode and a lithium metal oxide compound at its cathode [12]. The composition of compounds influences the electrical behavior of the battery, such as its IV-characteristic. The IV-characteristic of Lithium-ion type batteries follow a similar trend to the IV-characteristic of PEMFCs, as observed in Figure 2.5.

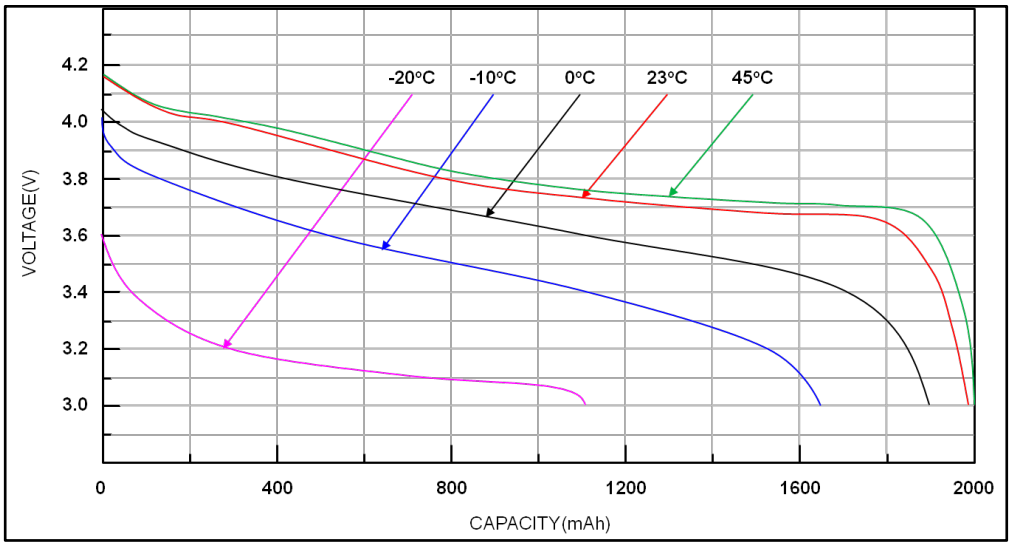

Figure 2.5. IV-characteristic for a Lithium-ion type battery at various temperatures [14].

Figure 2.5 suggests that the rate that free electrons move from the anode to the cathode or vice versa of a LiPo battery influences the voltage across the terminals of the battery, as was the case for the PEMFC. This further implies that if the output voltage ripple of the DC/DC converter is sufficiently large—and therefore the output current ripple can become sufficiently large—at the maximum output current, the battery may overheat [15]. The power dissipated in the internal resistance of the LiPo battery causes this overheating phenomenon. As the battery overheats, the current the LiPo battery draws from the converter increases too. If the converter is not designed properly, the LiPo battery can draw a significantly large charge current, which will inevitably damage the battery, and potentially the components in the converter [14].

# 3. Design Process & Criteria

Chapter 3 details the design process, as well as the design criteria of our DC/DC converter. With the assistance of Honeywell, and through the literature on high power density converter design, fuel cells, and lithium-ion batteries, we developed specific design criteria that the converter had to meet.

## 3.1 The Design Process

Despite the dynamic nature of any design process, we can outline a general procedure for DC/DC converter design in any application. Figure 3.1 outlines a general design procedure for any type of converter.

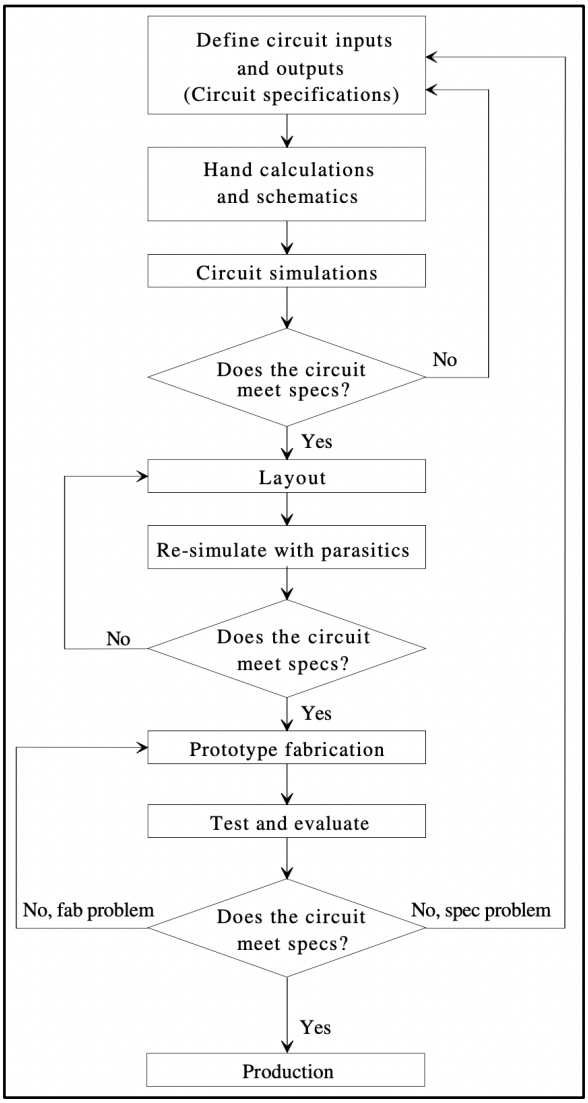


Figure 3.1. Flowchart for a general DC/DC converter design process [16].

Each section of the report corresponds to different parts of the design process. Chapters 3 and 4 define the circuit specifications and investigate potential topologies (schematics),

respectively. Chapters 5, 6, and 7 describe the schematic and circuit simulation stage. Chapter 8 details the "does the circuit meet specifications?" phase of the process. Lastly, Chapter 9 surveys high-power PCB layout. Due to various challenges described in later sections, our design did not reach the production phase.

## 3.2 Design Criteria

Our research informed the following design criteria, which we developed in conjunction with Honeywell. The criteria provided the basic outline for our design phase, and are divided into four sections:

1. Honeywell Constraints
2. Fuel Cell Constraints
3. Battery Constraints
4. Converter Constraints

The following sections outline and justify the design criteria.

### 3.2.1 Digital Control Constraints

The digital control constraints are criteria that inform the overall design. These criteria are the general requirements for the converter that Honeywell requested:

1. The topology needs to be capable of supporting a digital control system which can limit the maximum power point (MPP) to 3.25kW; maximum input voltage to 100VDC; maximum output voltage to 400VDC; maximum output current to approximately 10.4A (calculated assuming 90% efficiency at MPP); and maximum input current to 65A. The converter must also be able to withstand such maximum values.

   Rationale for Creating this Criterion:
   We must limit the parameters as specified in criterion one to protect the fuel cell from operating in undesirable conditions, and to prevent the converter from feeding too much DC current to the battery. If this criterion is not satisfied, our topology may become incompatible with the fuel cell and battery.

2. The topology needs to be able to support a digital control system that can limit the minimum output voltage to 280VDC; minimum input voltage to 50VDC; minimum input current of 0A; and minimum output current of 0A. The converter must also be able to withstand such minimum values.

   Rationale for Creating this Criterion:
   We must limit the parameters as specified in criterion two to ensure the fuel cell is operating appropriately at its minimum values. Evidently, if this criterion is not satisfied, the converter won't be suitable for our application.

### 3.2.2 Fuel Cell Constraints

The fuel cell constraints detail the requirements for our converter's operation that are reliant on the operation of the fuel cell:

3. Since the fuel cell is a non-regenerative (meaning it cannot convert electricity to an appropriate ion in the electrolyte) proton exchange membrane fuel cell (PEMFC), the converter must be of the unidirectional variety.

   Rationale for Creating this Criterion:

   Although a fuel cell can charge a battery by delivering electrical power to the battery, a non-regenerative fuel cell cannot be charged by the same method. Instead, to charge a non-regenerative fuel cell, it must be supplied with appropriate ions [6].

4. The fuel cell input current slope, or input power, during the transition from 100VDC (open circuit voltage of the fuel cell) to a voltage at or above 50VDC must be limited to a maximum absolute value between 500W per second and 2.5kW per second. During this transition, the output voltage of the converter must not significantly deviate from its steady-state value [17], [18].

   Rationale for Creating this Criterion:
   If the fuel cell input current or power slope is not limited to a maximum absolute value, the hydrogen/fuel cell starvation phenomenon can occur. When this phenomenon occurs, the voltage being supplied by the fuel cell will initially undershoot before it attains it's steady-state value, reducing the lifetime of the fuel cell [8], [9].

5. The low-frequency ripple of the fuel cell input current must be no more than 4% of the DC component of the input current [10]. High-frequency current ripple (> 10 kHz) should also be limited, but it is not necessary to limit it as much as the low-frequency ripple [11]. To ensure the fuel cell is not damaged, we can attempt to limit the high-frequency ripple to no more than 4% to 5% of the DC component.

   Rationale for Creating this Criterion:
   It is desirable to minimize the ripple of the low-frequency and high-frequency current being drawn from a fuel cell. Otherwise, the fuel cell lifetime will be reduced.

### 3.2.3 Battery Constraints

The battery constraints are dependent on the battery used in the whole system, and specify voltage and current ratings:

6. Assuming the DC output current is close to the rated current of the battery, the ripple of the output current waveform (high and low frequency components) must be small enough such that the peak of the output current does not exceed the rating of the Li-battery. Whether or not the DC output current is close to the rated current, the ripple of the output current waveform should be minimized to minimize the output voltage ripple across the

Li-battery [15].

Rationale for Creating this Criterion:
The Li-battery in our application must receive a DC voltage. If the output voltage of the converter is not approximately DC, we may risk reducing the lifetime of the battery.

### 3.2.4 Converter Constraints

The converter constraints specify the requirements for the converter itself, and how that will impact the rest of the system:

7. Aim for a topology which can support a sufficiently large switching frequency so that we may minimize conduction losses. The switching losses can then be reduced via soft switching, if applicable. However, if the converter follows the same relationship as the traditional boost converter, the switching frequency cannot be so low as to make the conversion ratio of the converter load dependent.

   Rationale for Creating this Criterion:
   To reduce the size of the cooling equipment in our application, it can be advantageous to reduce the conduction losses by increasing the switching frequency. Thereafter, the switching losses can be decreased by implementing soft switching to improve the overall efficiency if the conduction losses are much smaller than the switching losses. However, the conversion ratio must remain load independent in this application, meaning the frequency cannot be too low.

8. The converter needs to be capable of providing a voltage gain of at least 8 (400VDC divided by 50VDC) while maintaining an efficiency greater than 80%.

   Rationale for Creating this Criterion:
   In some converters, such as the classical boost converter, obtaining a voltage gain of 8 would imply the duty cycle must be 0.875. The conduction losses increase significantly at such a duty cycle for the classical boost converter. As a result, assuming the switching period of the converter remains constant, the overall efficiency of the converter will decrease. It is important that our converter does not suffer the same drawback.

9. The ratio of the output power to a sufficiently small overall mass of our system (the sum of the mass of the converter and cooling equipment) must be sufficiently large. Ideally, the ratio will be at least 62 kW/kg for the intended UAV application, which implies the overall mass of the system will ideally be 50g or less (in practice, this may likely be extremely difficult to achieve for a 3.25kW design).

   Rationale for Creating this Criterion:
   If the weight of the converter exceeds a specified weight, the UAV may no longer be able to function as intended. Therefore, it is important we maximize the ratio of the output power to the overall mass of our system.

10. Must comply with conducted and radiated EMI regulations, or at least not interfere with the operation of electronic equipment in its vicinity. In other words, our converter should be capable of sufficiently attenuating very large harmonics via an input filter or other mechanism.

    Rationale for Creating this Criterion:
    All power electronics must comply with EMI regulations, or not interfere with other electronic equipment. Furthermore, in designing a mechanism which reduces conducted EMI, such as an input filter, we also protect the converter and the battery from unexpected transients in the fuel cell input voltage [3].

# 4. Open-Loop Boost Converter Topologies

The following sections present descriptions of various boost converter topologies. Each of the topologies presented below are discussed with comparison to the conventional boost converter, which was described in Chapter 3. Simulation results of a few of the topologies can be found in Appendix B, and Appendix A describes the simulation methodology.

## 4.1 A Note About the Final Design

The following chapter details the initial converter topologies we researched and simulated. None of the topologies in this section were chosen for the final design. Instead, the purpose of this chapter is to summarize the basic converter designs which were investigated at the beginning of our design process. We used this information to further narrow our scope of research when we began investigating ICs, designing, and simulating the converter. Chapters 6 and 7 explore our more in-depth converter designs.

## 4.2 Quadratic Boost Converter

A quadratic boost converter can be created by the cascading of two conventional boost converters that utilize one switch.

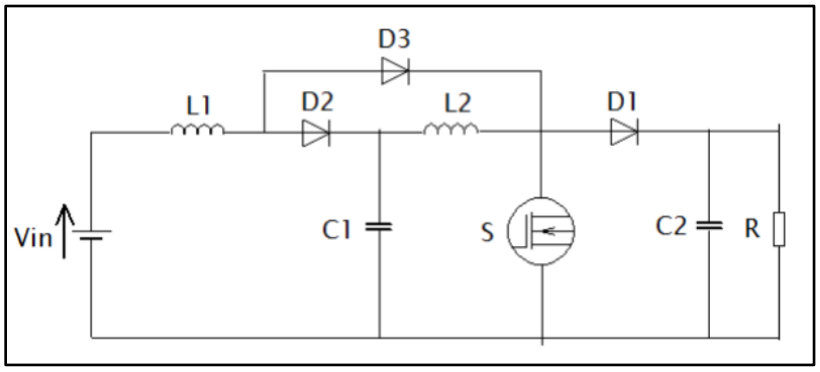


Figure 4.1. Circuit diagram for the quadratic boost converter [2].

The converter shown in Figure 4.1 operates in the following two states:

1. The on-state, where diodes D1 and D2 are OFF, while diode D3 and switch S are ON.
2. The off-state, where diode D3 and switch S are OFF, while diodes D2 and D1 are ON.

The quadratic boost converter operates at the following duty cycle, which can be used to find both inductor current values:

$$D = 1 - \sqrt{\frac{V_{in}}{V_{out}}} \qquad \text{(eq. 4.1)}$$

$$I_{L1} = \frac{I_{out}}{(1-D)^2} \qquad \text{(eq. 4.2)}$$

$$I_{L2} = \frac{I_{out}}{(1-D)} \quad \text{(eq. 4.3)}$$

The inductor and capacitor values for the quadratic boost converter can then be found using the ripple current of each inductor and ripple voltage of the capacitors:

$$L_1 = \frac{DV_{in}}{f\Delta i_{L1}} \quad \text{(eq. 4.4)}$$

$$L_2 = \frac{DV_{in}}{f\Delta i_{L2}} \quad \text{(eq. 4.5)}$$

$$C_1 = C_2 = \frac{DV_{in}}{(1-D)Rf\Delta V_C} \quad \text{(eq. 4.6)}$$

Compared to the conventional boost converter, the quadratic boost converter achieves a wider voltage conversion range, and a significant reduction in ripple current [2]. The single switch makes the converter useful in operations at higher frequencies. One of the tradeoffs of this design, however, is the efficiency. In an LTspice comparison of quadratic and conventional boost converters, the quadratic boost had an efficiency of about 89%, while the conventional boost had an efficiency of about 95% [19]. Despite the lower efficiency, the quadratic boost converter is still a viable option due to the high voltage output and low ripple current.

Table 4.1. Pros and cons of the quadratic boost converter.

| Pros | Cons |
|---|---|
| • Achieves a high voltage conversion ratio<br>• Provides better output voltage regulation<br>• Provides more precise control over input and output stages for improved adaptability<br>• Achieves lower ripple current values | • More complex, making it more challenging to design and troubleshoot<br>• More components contribute to larger size and weight<br>• Lower efficiency than boost converter |

## 4.3 Double Cascade Boost Converter

The double cascade boost converter, also known as two-stage boost converter, combines two conventional boost converters by connecting them in series. The circuit includes an input voltage, two switches, two diodes, two capacitors, and two inductors. Figure 4.2 shows the circuit configuration for this topology.

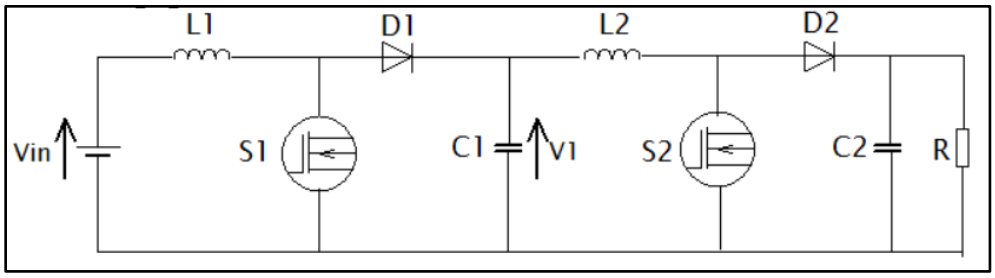

Figure 4.2. Circuit diagram for the double cascade boost converter [2].

The double cascade boost converter operates in two states:

1. S1 is ON: the inductor charges from the input voltage source, while S2 remains OFF.
2. S1 is OFF: S2 is switched ON and the energy is transferred to the second stage through the second inductor.

The double cascade boost converter provides several advantages when compared to the conventional boost converter. Notably, it achieves a significantly higher voltage conversion ratio. The converter also provides a stable output voltage even when input voltage fluctuations occur. This helps with delivering consistent power. The converter has proven to have high efficiency in high-voltage applications as well. For an input voltage of 18V and output voltage of 400V, the converter resulted in a 94.52% efficiency, while the conventional boost converter had an efficiency of 85.32% [2]. A higher efficiency ensures an enhanced overall performance and prolonged flight times. The distribution of the voltage across two stages is another benefit. This reduces stress on components and the likelihood of component failures while enhancing reliability.

However, several disadvantages arise when using a double cascade boost converter. In particular, the two-stage aspect introduces complexities into the design and troubleshooting process. In addition, the two-stage design may present additional energy losses between the two stages once parasitics and real-world challenges are applied. Lastly, we are unable to estimate the weight and density of the converter due to the lack of available research on this topic. Table 5.2 shows a summary of the pros and cons for the double cascade boost converter in relation to the conventional boost converter. For the design equation, refer to Appendix B.

Table 4.2. Pros and cons of the double cascade boost converter.

| Pros | Cons |
|---|---|
| • Achieves a high voltage conversion ratio<br>• Provides better output voltage regulation<br>• Offers potential for higher efficiency, especially across variable input voltages<br>• Provides more precise control over input and output stages for improved adaptability<br>• Distributes voltage conversion, | • More complex, making it more challenging to design and troubleshoot<br>• May experience additional energy losses due to two-stage conversion<br>• Might be larger and heavier |

| | |
|---|---|
| reducing stress on components and improving reliability | |

## 4.4 Flying Capacitor Boost Converter

The Flying Capacitor Multilevel Inverter (FCMI) is a topology that utilizes capacitors which float in various electric potentials. The FCMI is often used as a multilevel inverter in applications such as solar panels, electric vehicles, and battery management systems. The flying capacitor stores and transfers energy between different levels of the inverter and has the advantages of frequency multiplication, low switching losses, and negligible voltage and current ripple [20].

Similar to the FCMI, the Flying Capacitor Boost Converter (FCBC), utilizes capacitors floating at various electric potentials depending on the switching state of the semiconductor.

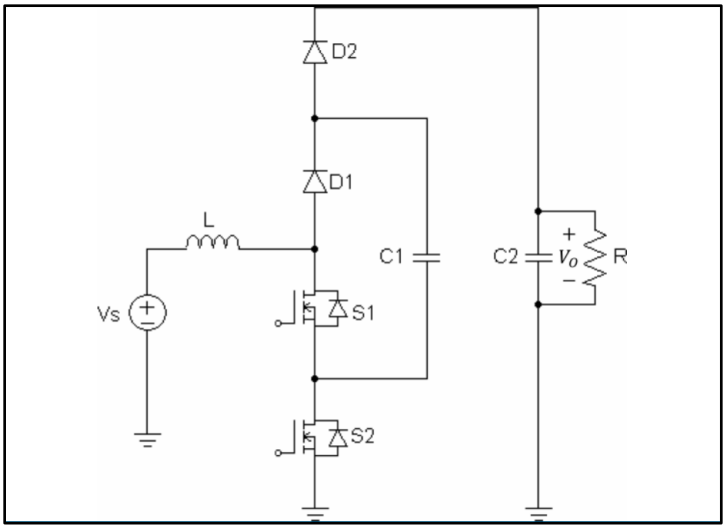


Figure 4.3. Circuit diagram for the two-stage flying capacitor boost converter [20].

Every switching period, $T_s$, the topology cycles through the following states:

1. The topology charges inductor L by keeping switches S1 and S2 closed [21].
2. At time $t = DT_s/2$–where $D$ is the duty cycle–switch S1 is opened while S2 remains closed, transferring the energy stored by the inductor into capacitor C1 [21].
3. At $t = T_s/2$, switches S1 and S2 are closed, charging inductor L again [21].
4. At $t = (T_s/2) + (DT_s/2)$, switch S2 is opened and the energy stored in capacitor C1 and inductor L is delivered to capacitor C2 [21].

To calculate the circuit parameters, we use the following equations:

$$I_s = I_o\left(\frac{2}{1-D}\right) \quad \text{(eq. 4.7)}$$

where $I_s$ the source current and $I_o$ the desired output current.

The voltage conversion ratio can be calculated using:

$$\frac{V_o}{V_s} = \frac{2}{1-D}\left(\frac{1}{1+\frac{(r_{ds1}+r_{ds2})(\frac{1+D}{2})+(r_{ds1}+r_{ds2})(\frac{1-D}{2})+r_L}{(\frac{1-D}{2})^2 R}}\right) \quad \text{(eq. 4.8)}$$

where $V_o$ is the output voltage, $V_s$ is the source voltage. Furthermore, $r_{ds1}$, $r_{ds2}$, and $r_L$ represent the resistance of switch S1, S2, and inductor, respectively. The inductance for inductor L is given from:

$$L = \frac{(V_s)D}{4\,(\Delta I_s) f_s} \quad \text{(eq. 4.9)}$$

and

$$\Delta I_L = \frac{V_S(V_o - 2V_s)}{2Lf_s V_o} \quad \text{(eq. 4.10)}$$

where $f_s$ is the switching frequency and $\Delta I_L$ is the inductor current ripple.

The values for capacitors C1 and C2 can be calculated using the following equations:

$$C_1 = \frac{V_o}{2R\Delta V_{C1} f_s} \quad \text{(eq. 4.11)}$$

$$C_2 = \frac{V_o(1+D)}{4R\Delta V_o f_s} \quad \text{(eq. 4.12)}$$

The frequency of the ripple of the current flowing through inductor L is given from:

$$f_{ILripple} = 2f_s \quad \text{(eq. 4.13)}$$

Table 4.3. Pros and cons of the flying capacitor boost converter.

| Pros | Cons |
|---|---|
| • Low current ripple<br>• Low inductor core and copper losses<br>• High voltage gain<br>• Low voltage stresses on power switches; enables use of low RDS MOSFET<br>• Low voltage stress on diodes<br>• High frequency inductor ripple enables use of a smaller inductor | • Complicated control for tracking voltage level on capacitors<br>• Precharging capacitors to same voltage and their start up is a difficult procedure |

## 4.5 Interleaved N-Phase Boost Converter

As mentioned in the conventional boost converter section, some of the disadvantages of the conventional boost are a high fuel cell ripple current unless the inductor at the input is sufficiently large. However, a larger inductor would likely increase the weight of the converter. The interleaved N-phase boost converter has the potential to mitigate the fuel cell ripple current issue, as well as several other problems.

The topology of the interleaved N-phase boost converter is similar to the conventional boost converter topology, except the interleaved topology consists of several inductor-diode-switch branches in parallel with each other, as shown in Figure 4.4.

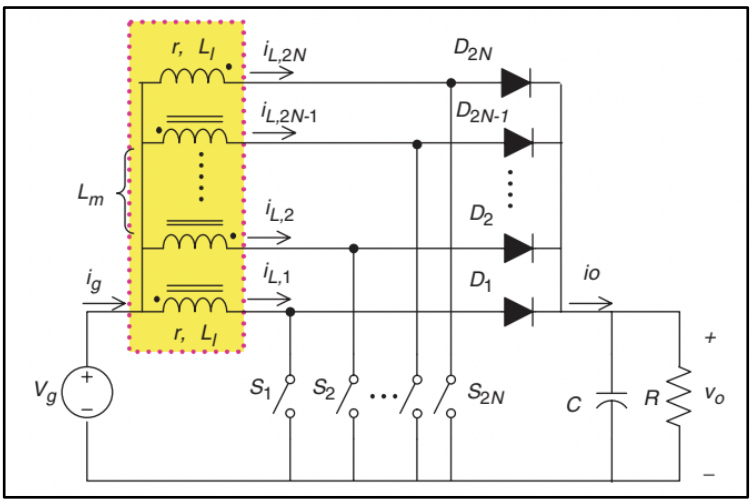


Figure 4.4. Circuit diagram for the interleaved N-phase boost converter [22].

In addition to having similar structures, the interleaved and conventional boost converters are similar in terms of steady-state operation:

1. When $S_i$–where $i \in \{1, 2, \ldots, 2N\}$–is closed and all other switches are open, the magnetic field energy in the inductor increases quadratically due to a linearly increasing current.
2. If $S_i$ is open and all other switches are closed, the inductor polarity reverses and releases magnetic field energy through the diode and into the load.

Ideally, the magnitude of the current through each phase of the N-phase interleaved converter will be the same. This implies that, if the approximate DC current drawn from the fuel cell is $I_g$, then the DC current through each phase will be $I_g/N$, where $N$ is the number of phases. Since the DC current, $I_g$, is split into several phases, the ripple of the current through each phase is larger than the fuel cell current ripple, assuming that the pulse-width modulation scheme dictates that each waveform is phase-shifted by $2\pi/N$ relative to a preceding phase. Figure 4.5 and 4.6 illustrate this concept.

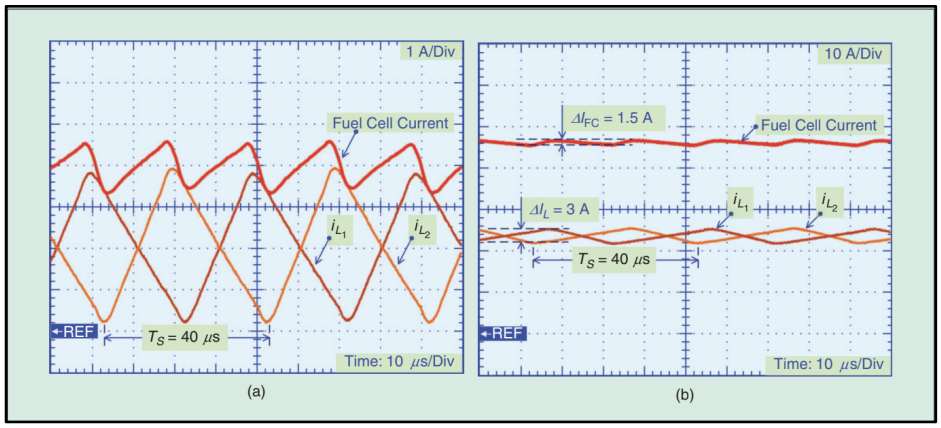


Figure 4.5. Waveforms for a two-phase interleaved boost converter in steady-state, for an input of (a) $I_g = 4\text{A}$ and (b) $I_g = 46\text{A}$ [23].

Furthermore, as the number of phases increases, the ripple of the current through each phase decreases further, resulting in a smaller fuel cell ripple current, as presented in Figure 4.6. As the number of phases increases, however, the DC component of the current through each phase decreases. This trade off suggests that the DC component of the current through each phase will approach the AC component, and the risk of discontinuous conduction mode (DCM) operation increases.

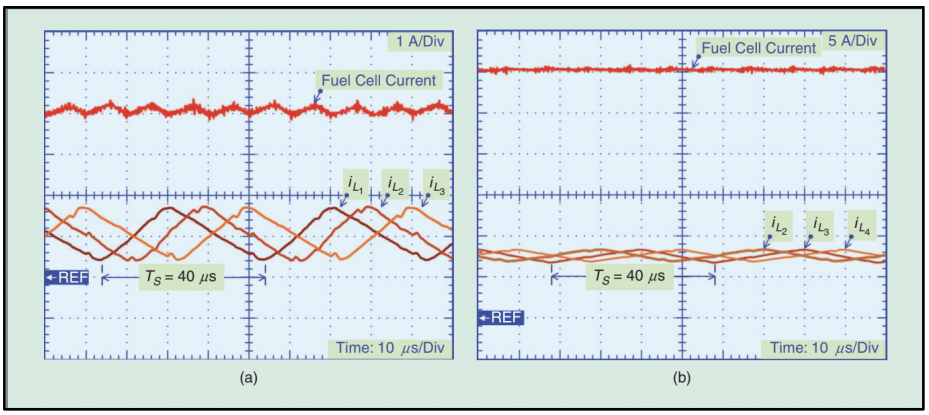


Figure 4.6. Waveforms for a four-phase interleaved boost converter in steady-state, for an input of (a) $I_g = 4\text{A}$ and (b) $I_g = 46\text{A}$ [23].

As a consequence of the behavior discussed above, the frequency of the fuel cell ripple current becomes $Nf_s$, where $f_s$ is the switching frequency of the waveforms applied to the switches. This allows for the reduction in size of any inductors or capacitors present at the input of the converter. Moreover, since the ripple of the fuel cell current is reduced, the ripple of the output current will theoretically be reduced. This implies the output voltage ripple will be reduced, so the size of the output capacitor is scaled down if the output voltage of the converter is sufficiently small. Although the interleaved N-phase boost converter yields multiple benefits, it also has its drawbacks. The disadvantages of the converter, as well as advantages, are summarized in Table 4.4. For the design equations, refer to Appendix B.

Table 4.4. Pros and cons of the interleaved N-phase boost converter.

| Pros | Cons |
| --- | --- |
| ● Size and volume of input inductors and output capacitors are reduced<br>● Input and output ripple current is reduced<br>○ Controllable ripple<br>○ Ripple frequency increases (size reduction)<br>● Heat dissipation is distributed<br>● Current ratings of components is reduced per phase, reducing size of components | ● Added complexity due to multiple phases<br>● Control system required for each phase<br>● Cannot achieve a voltage gain of eight when $D \leq 1/K$, where $K$ is the number of phases<br>○ Voltage multiplier<br>○ Multiple stages<br>○ Parallel converters |

## 4.6 Converter Research Conclusion & Subsequent Actions

Although investigating the above topologies was an important aspect to this project, we determined the most appropriate next step would be to investigate suitable ICs. The above research provided a useful starting point, but developing the converter using solely discrete components would not be efficient given the timeframe of this project. By utilizing and designing around ICs in LTspice, developing our converter design became faster, simpler, and more cost-effective. The following chapter details our design and simulation process for developing unmanned autonomous vehicle converters with ICs.

# 5. Simulation Methodology

In Chapters 6 and 7, simulation results for our unmanned autonomous vehicle converters are presented. Before reviewing the simulation results from LTspice, the simulation methodology must be discussed to properly interpret the results.

## 5.1 The Modeling Problem

Recall from the IV-characteristic in Section 2.3.1 that when the voltage across the terminals of the PEMFC is 50VDC, it is only possible to draw about 65A from the fuel cell in steady-state. It is not physically possible to draw more or less current unless the chemistry of the fuel cell is altered. The chemistry of the fuel cell is what dictates its IV-characteristic.

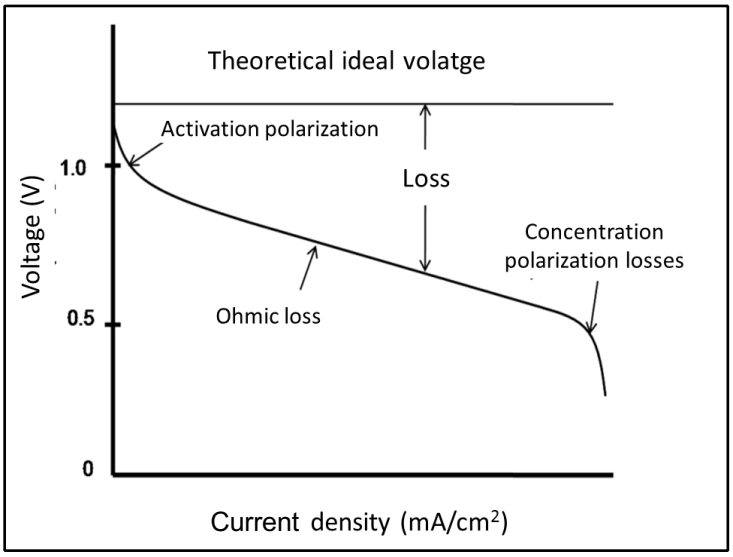


Figure 5.1. IV-characteristics for a single cell of the 3.25kW 102-cell stack PEMFC and theoretical ideal voltage source [1].

Figure 5.1 shows the IV-characteristics of a single-cell, associated with the 3.25kW 102-cell stack PEMFC, and the theoretical ideal voltage source. The shape of the IV-characteristic for a single cell of the PEMFC differs drastically from that of the ideal voltage source. Consequently, if an ideal 50VDC source is connected to the input of a power converter topology in LTspice, it's probable that the DC current drawn from the ideal voltage source will not be 65A in steady-state. Instead, it could be significantly more or less because of how different the IV characteristic of an ideal voltage source is from a PEMFC. Similarly, the Li-battery cannot be accurately modeled as a current source, voltage source, or resistor, since the IV-characteristic of the LiPo battery differs from such circuit elements. Thus, the topologies cannot be accurately simulated with a static combination of circuit elements at the input or output.

## 5.2 Modeling Approaches

Three approaches to simulating converters in LTspice were developed. Of the three approaches, one was used exclusively for simulating the topologies in Chapter 4. As a result, this

modeling method has been delegated to Appendix A. The other two modeling methods were employed in the simulation of the push-pull converter in Chapter 7.

One approach to simulating the push-pull converter in LTspice is to treat the PEMFC as a static 100V independent voltage source in series with a static 0.7Ω resistor, while treating the LiPo battery as a variable resistor. This method is equivalent to measuring the slope of the IV-characteristic from endpoints of the characteristic, as shown below. As a consequence of the push-pull converter drawing a significant amount of current at the MPP, this method is best suited for measuring the converter's response to disturbances in the input voltage.

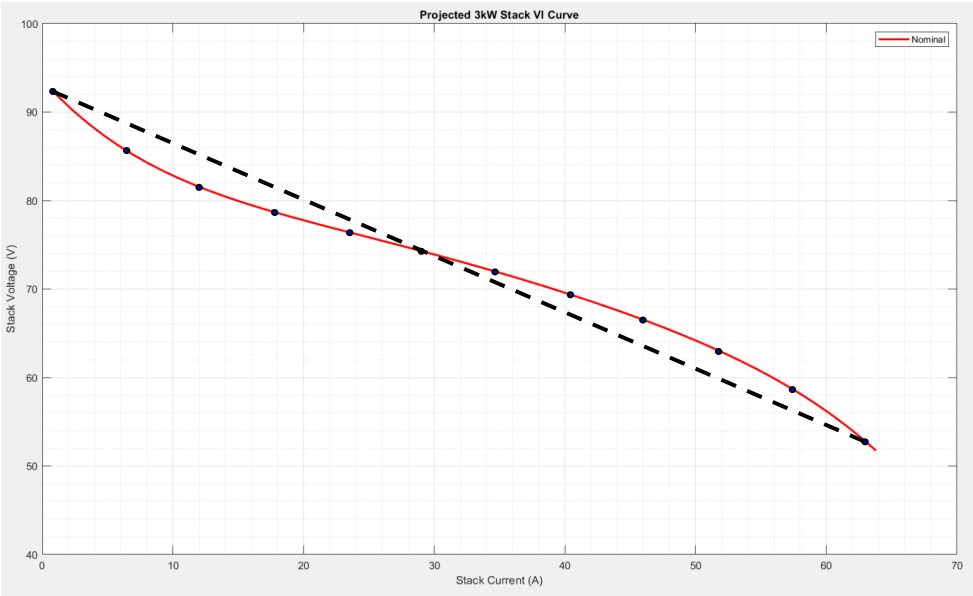


Figure 5.2. IV-characteristic for the PEMFC modeled as a line for DCM or CCM modeling purposes. Adapted from [1].

An alternative method to simulating the push-pull converter in LTspice involves implementing a variable independent voltage source as the PEMFC and a variable resistor as the LiPo battery. This approach allows for the measurement of the converter's response to variations in the output voltage via the digital-to-analog converter (DAC) while suppressing excursions in the input voltage.[1] Since the PEMFC is modeled as a variable voltage source, the method is clarified with the following procedure:

1. Select a coordinate on the PEMFC IV-characteristic to simulate at, and calculate the corresponding power, $P_I$.
2. Choose an output voltage, $V_O$, between 280VDC and 400VDC to simulate at.
3. Calculate the corresponding load resistance value with the following equation: $R = (V_0)^2/P_I$.

[1] The DAC is described in Section 7.3.2.

If it is desired to simulate a single-phase of the push-pull converter for faster simulations, the procedure above is still applicable with one modification: the load resistance must be calculated through:

$$R = ((V_0)^2/P_I)k \quad \text{(eq. 5.1)}$$

where $k$ is the total number of phases.

## 5.3 Simulation Limitations

The simulation procedure has several limitations. To obtain a sense of how accurate the simulation results are, it is important to review these limitations. Limitations include, but are not limited to:

- The model for the PEMFC does not match the IV-characteristic of the PEMFC.
- The model for the Li-Battery does not match the IV-characteristic of the Li-Battery.
- All transformer models utilized did not model the magnetizing inductance, meaning the current waveforms of the converters with transformers in LTspice are distorted.
- It was assumed the inductance of the inductors does not change with the DC current which travels through them.
- It was assumed the capacitance of the capacitors does not change with the DC voltage which is applied across them.
- The resistance and reactance of the traces were neglected.
- Transient simulation results are likely not accurate with the methodology utilized for these simulations.
- Other discrepancies between SPICE models and behavior in reality.

Despite these limitations, we simulated our converter designs as adequately as possible to develop a robust final schematic.

# 6. Initial Design: Non-Isolated Boost Converter

Our initial design was a non-isolated design we approached with more innovative methods. The non-isolated converter combines various properties of the quadratic, double cascade, flying capacitor, and interleaved N-phase boost converter. More specifically, the non-isolated design consists of buck-boost, DC/AC, AC/DC, MOSFET driver, and oscillator stages.

## 6.1 Block Diagram Description

A schematic of the non-isolated design and a description of each block delineated within the schematic can be reviewed in Figure 6.1.

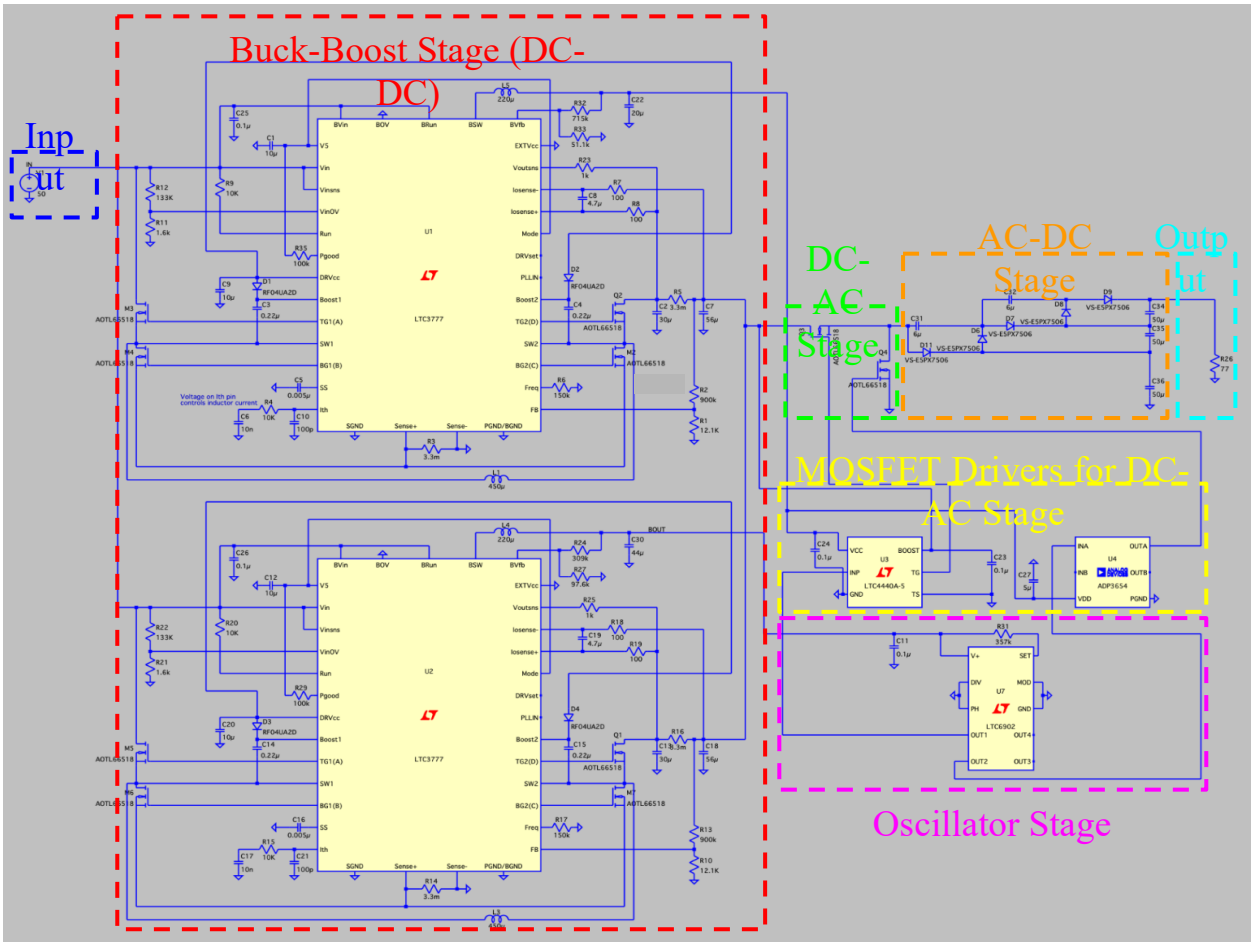


Figure 6.1. Schematic for the non-isolated design with delineated blocks.

The buck-boost stage of the non-isolated design borrows properties from the interleaved two-phase converter. It consists of two LTC3777 ICs connected in parallel which boost a 50-100VDC input to approximately 110VDC. When operating in boost mode, the two LTC3777 ICs in parallel are nearly equivalent to the operation of a two-phase interleaved boost converter, the primary distinction being the PWM scheme described in Section 7.1.1. The AC/DC stage–known

as a charge pump topology–is similar to the flying capacitor converter, as applied input waveforms may be sensed only at periodic instants of time. In short, both topologies are switched-capacitor circuits. Lastly, the interconnection between the buck-boost stage and DC/AC to AC/DC stage is comparable to the quadratic or double cascade boost converters' ability to achieve a sufficiently high voltage gain.

### 6.1.1 Buck-Boost Stage Description

The buck-boost stage is comprised of two LTC3777 ICs in parallel to manage power dissipation. From a high-level perspective, the LTC3777 IC is a synchronous four-switch buck-boost controller with a switching bias supply. The LTC3777 ICs are currently configured to bias other ICs in the converter. The LTC3777 ICs were set to be unidirectional (pulse-skipping mode), have a switching frequency of 560kHz, a soft-start of 1.2ms, and provide an output voltage 90VDC. Together, the LTC3777 ICs operate similarly to the two-phase interleaved boost converter when $V_{in,buck-boost} << V_{out,buck-boost}$. The boost operation prevents the component sizes of the AC-DC stage from becoming impractically large.

In the case where there is an unexpected transient which causes $V_{in,buck-boost} >> V_{out,buck-boost}$, the LTC3777 is capable of bucking the input voltage to regulate the output voltage. When in boost mode, the buck-boost stage's H-bridge operates as follows:

- M3 and M5 are always ON
- M4 and M6 are always OFF

Additionally, Q2, M2, Q1, and M7 alternate in the following manner:

- Q1 and Q2 are ON; M2 and M7 are OFF
- Q1 and Q2 are OFF; M2 and M7 are ON

While in buck mode, the operation of the switches is opposite of the behavior in boost mode. The amplitude of the signals from the TG2(D) and BG2(C) pins (which drive Q2, M2, Q1, and M7) are set by the DRVset pin, which plays a large role in optimizing the efficiency of this stage. Lastly, the top LTC3777 IC biases both MOSFET drivers at 12VDC, whereas the bottom LTC3777 IC biases the multiphase oscillator at 3.3VDC.

### 6.1.2 DC/AC Stage Description

The DC/AC stage in Figure 6.1 utilizes the PHM21NQ15T NMOS devices. The two NMOS devices are connected such that the source terminal of Q3 is connected to the drain terminal of Q4, and the source terminal of Q4 is connected to ground. Q3 and Q4 transform the output of the buck-boost stage (a DC signal) into a square-wave which is fed to the AC/DC stage. More specifically, Q3 and Q4 theoretically operate so they are never simultaneously on or off. The oscillator stage, in tandem with the MOSFET driver stage, determines whether the DC/AC stage follows this ideal switching behavior.

### 6.1.3 MOSFET Driver Stage Description

The MOSFET driver stage for the DC/AC stage is made of the LTC4440A-5 and ADP3654 ICs. The LTC4440A-5 is a high speed, high voltage, high side gate driver. On the contrary, the ADP3654 is a high speed, dual, low side 4A gate driver. In other words, the primary difference between these two ICs is as follows; the LTC4440A-5 is only capable of driving MOSFETs which do not have their source terminals connected to ground, whereas the ADP3654 can only drive MOSFETs with source terminals which are connected to ground. The LTC4440A-5 was designed such that the boost pin is connected to the output of the buck-boost stage and TS is referenced to ground. Thus, the output signal from the TG pin follows the output of the buck-boost stage, swinging between TS and BOOST. In turn, the gate-source voltage of Q3 is minimized since, with respect to ground, the gate voltage rises at the same rate as the voltage of the source terminal, reducing the risk of exceeding the maximum gate-source voltage.

To generate an output waveform of appropriate frequency, the LTC4440A-5 utilized the signal from the oscillator as a reference. The design of the ADP3654 is much simpler than the LTC4440A-5. The ADP3654 simply uses the reference signal from the oscillator to drive Q4 so the gate-source voltage of Q4 is never exceeded.

### 6.1.4 AC/DC Stage Description

The AC/DC stage is a charge pump that rectifies and boosts the output of the DC/AC stage by a factor of three. It is composed of five VS-E5PX7506 diodes, two 5μF capacitors, and three 50μF capacitors. The two 5μF capacitors boost the output waveform by 100VDC each, suggesting the output waveform of the AC/DC stage is 200VDC higher than the amplitude of the input waveform; the three 50μF capacitors make the output voltage at the end of each 5 μF capacitor less susceptible to variations in the input waveform to the AC/DC stage, decreasing voltage ripple by limiting $\frac{\partial v_{cap}}{\partial t}$. Additionally, the three 50μF capacitors allow the output voltage at the end of each 5μF capacitor to stack. The diodes switch on and off so the voltage across each 5μF capacitor approaches a steady value.

### 6.1.5 Oscillator Stage Description

The oscillator stage consists of the LTC6902. The LTC6902 is a multiphase oscillator with spread spectrum frequency modulation. In the current design, the LTC6902 frequency modulation ability is disabled. Instead, the LTC6902 is configured for two-phase operation, and the oscillation frequency is approximately 560kHz. The purpose of the LTC6902 is to provide low voltage square-wave signals to the two MOSFET drivers from OUT1 and OUT2. OUT1 and OUT2 are created via a delay matched inverting circuit, yielding delays around 100ps [24]. This implies that OUT1 is the inverse of OUT2. Ideally, this will ensure that the two MOSFETs in the DC/AC stage will not be on simultaneously.

## 6.2 Design Process

To understand why specific components were selected, it is paramount to understand the purpose of each component described in Section 6.1.1. All equations presented in Section 6.2.1 can be located within the datasheet of the IC, diode, or MOSFET associated with the discussion.

### 6.2.1 Buck-Boost Stage Design

The components in the power-path of the buck-boost stage (the inductor, sense resistors, power MOSFETs, and input and output capacitors) were selected based on the following criteria:

1. Since this converter is intended for a UAV application, the switching frequency, $f_{SW}$, should be sufficiently large to avoid sizable inductors, but not so high that the efficiency of the buck-boost stage is compromised.
2. The output voltage, $V_{OUT}$, of the buck-boost stage must be large enough for the output voltage of the non-isolated converter to reach 400VDC without exceeding the voltage ratings of stages it is connected to.
3. The stage must be designed to withstand input voltages from 50VDC ($V_{IN(MIN)}$) to 100VDC ($V_{IN(MAX)}$).
4. As a consequence of the parallel configuration of the two LTC3777 ICs, each phase must be designed to tolerate a maximum output current, $I_{OUT(MAX)}$, of about 18A when the input power is 3.25kW (assuming an efficiency of nearly 100% for this stage).
5. The maximum ambient temperature cannot exceed 50ºC.

The switching frequency was selected as 560kHz to keep the inductance value of the inductor in each phase below or equal to 500µH. According to Figure 6.2, the switching frequency of the LTC3777, $f_{SW}$, can be set to 560kHz by connecting a resistor of approximately 150kΩ to the FREQ pin.

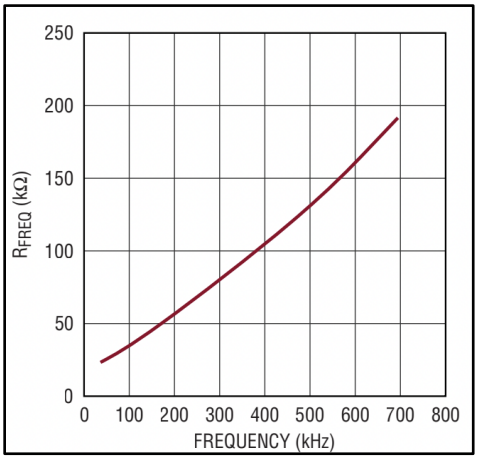


Figure 6.2. FREQ pin resistor value plotted against frequency [25].

Moreover, since the absolute maximum voltage rating of the BOOST pin of the LTC440A-5 is 95VDC, the output voltage of the buck-boost stage cannot exceed 90VDC. In other words, the resistive divider connected to the FB pin must be configured to regulate the output voltage at 90VDC. The LTC3777 regulates the output voltage when the voltage of the FB pin is 1.2V with respect to ground, as evidenced by Figure 6.3. Therefore, if $R2$ in Figure 6.3 is assumed to be 12.kΩ, $R1$ can be calculated as follows:

$$R1 = \frac{(V_{OUT})(R2)}{1.2V} - R2 \qquad \text{(eq. 6.1)}$$

Accordingly, $R1$ was selected to be 900kΩ.

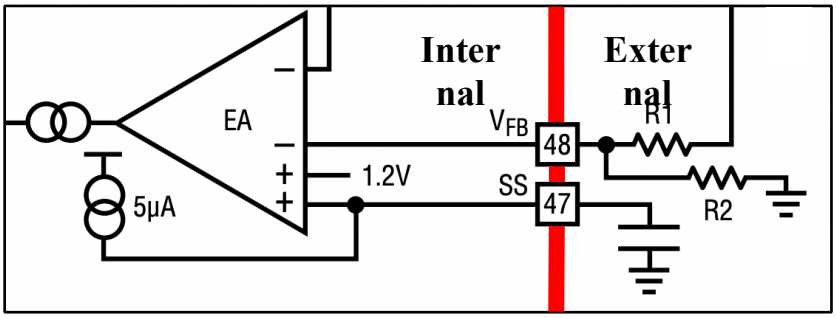


Figure 6.3. Block diagram of the LTC3777 in the vicinity of the FB pin [25].

Given the following parameters:

- Output voltage of the buck-boost stage is 90VDC
- Switching frequency is 560kHz
- Maximum output current is nearly 18A at 3.25kW input power
- Assumed inductor current ripple is 30% of average inductor current

The minimum inductance value can be calculated with Equation (6.2) when the LTC3777 operates in the boost region:

$$L_{BOOST(MIN)} > \frac{(V_{IN(MIN)})^2(V_{OUT}-V_{IN(MIN)})(100)}{(f_{SW})(I_{OUT(MAX)})(\%Ripple)(V_{OUT})^2} \qquad \text{(eq. 6.2)}$$

Substituting the correct values into the equation above yields an inductance value of approximately 410µH. Similarly, in the case where the input voltage is greater than 90VDC, the minimum inductance value is given by the following equation:

$$L_{BUCK(MIN)} > \frac{(V_{OUT})(V_{IN(MAX)}-V_{OUT})(100)}{(f_{SW})(I_{OUT(MAX)})(\%Ripple)(V_{IN(MAX)})} \qquad \text{(eq. 6.3)}$$

This suggests the minimum inductance value is approximately 300µH. Considering that $L_{BOOST(MIN)} > L_{BUCK(MIN)}$ and the minimum inductance value will likely be larger in practice due

to the ideal efficiency assumed in the calculations, the inductance value, $L$, was selected to be 450μH in both phases. Note, in the boost region ($V_{IN} < 90VDC$), which is the primary mode of operation for the buck-boost stage, the ripple current is:

$$\Delta I_L = \frac{V_{in}}{(f_{SW})(L)}\left(1 - \frac{V_{in}}{V_{out}}\right) \quad \text{(eq. 6.4)}$$

Consequently, if the PEMFC is delivering 3.25kW of power to the converter, the ripple of the inductor current is projected to be approximately 88mA.

The information above allows for the calculation of the sense resistor value, $R_{SENSE}$:

$$R_{SENSE} = \frac{2(140mV)(V_{IN(MIN)})}{2(I_{OUT(MAX)})(V_{OUT}) + (\Delta i_{L,BOOST})(V_{IN(MIN)})} \quad \text{(eq. 6.5)}$$

Accommodating for a 30% margin in the $R_{SENSE}$ value gives a value of $4.3m\Omega/1.3 \approx 3.3m\Omega$.

The primary determinants in selecting the MOSFETs of the buck-boost stage were the drain and gate to source voltage ratings, as well as the $R_{DS(ON)}$ value. The MOSFETs on the left side of the buck-boost stage needed to be selected such that the drain-source voltage rating was at least 150VDC (since the output voltage is 95VDC). Additionally, the positive gate-source voltage rating could be no less than +10VDC, whereas the negative gate-source voltage could be no greater than -10VDC. The $R_{DS(ON)}$ value was limited by the maximum power dissipated in the MOSFETs. If it is assumed that the junction-to-ambient thermal resistance of a MOSFET, $\theta_{JA}$, is 30ºC/W and the maximum junction temperature, $T_J$, is 175ºC, the maximum power dissipated in the aforementioned MOSFETs is:

$$P_{LEFT(MAX)} = \frac{T_J - T_A}{\theta_{JA}} \quad \text{(eq. 6.6)}$$

$T_A$, the ambient temperature, is assumed to be a maximum of 50ºC. Accordingly, $P_{LEFT(MAX)} \approx 4.17W$.

When operating in boost region, the maximum $R_{DS(ON)}$ of M3 and M5 (seen in Figure 6.1) can be determined by realizing that, in the boost region, the maximum power dissipated in M3 and M5 occurs at the maximum input current:

$$R_{DS(ON),M3-M5} < (P_{LEFT(MAX)})\left(\frac{V_{IN(MIN)}}{(V_{OUT})(I_{OUT(MAX)})}\right)^2 \quad \text{(eq. 6.7)}$$

This suggests that the maximum $R_{DS(ON)}$ for transistors M3 and M5 is approximately 4mΩ. For M4 and M6, the maximum power dissipation occurs at the maximum input voltage when operating in the buck region. As such, the MOSFET which satisfies the $R_{DS(ON)}$ constraint of M3 and M5 will also satisfy M4 and M6.

The $R_{DS(ON)}$ requirement of MOSFETs M2, M7, Q2, and Q1, is not as constraining as was for MOSFETs M3 and M5 because the buck-boost stage primarily operates in boost mode; this means the conduction losses of M3 and M5 will be much larger. Hence, if the MOSFET selected for M3 and M5 possesses sufficient switching characteristics, the same MOSFETs can be used for M2, M7, Q2, and Q1. Thus, it was determined that the AOTL66518 MOSFETs are suitable for the buck-boost stage[2], as further evidenced by Figure 6.4 and Table 6.1. For instance, Figure 6.4 suggests that when the gate-source voltage is 8V or 10V, the on-resistance remains less than 4mΩ for sufficiently small junction temperatures. However, a safe operating area curve analysis was not performed for the MOSFETs in the buck-boost stage due to issues described in Section 6.3 which prevented the design from progressing.

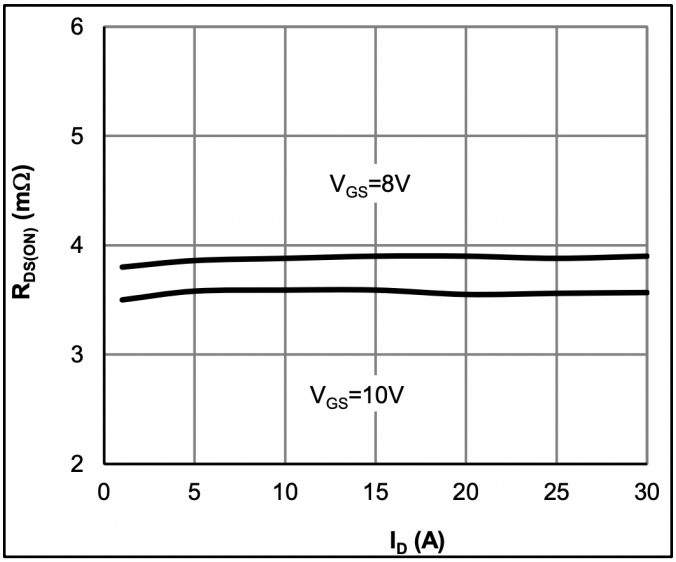


Figure 6.4. AOTL66518 MOSFET on-resistance vs. drain-current and gate-source voltage [26].

Table 6.1. A few of the switching characteristics of the AOTL66518 MOSFET. For all parameters in the table, $(t \cdot f_{SW})100 \approx 2.8\%$ at maximum [26].

| | | | | | | |
|---|---|---|---|---|---|---|
| $t_{D(on)}$ | Turn-On DelayTime | $V_{GS}$=10V, $V_{DS}$=75V, $R_L$=3.75Ω, $R_{GEN}$=3Ω | | 27 | | ns |
| $t_r$ | Turn-On Rise Time | | | 20 | | ns |
| $t_{D(off)}$ | Turn-Off DelayTime | | | 49 | | ns |
| $t_f$ | Turn-Off Fall Time | | | 28 | | ns |

After completing the MOSFET computations, calculations were performed to establish the desired properties of the input and output capacitors for each phase. The input capacitance, $C_{IN}$, is governed by the necessity to filter the square wave input current when the buck-boost stage is in buck mode. Thus, the selected input capacitor should have sufficiently low equivalent series

[2] Refer to the AOTL66518 MOSFET datasheet if desired.

resistance (ESR) which can tolerate an RMS current of half the maximum output current: 9A.[3] Contrary to the input capacitor, the output capacitor must impede voltage ripple at the output of the buck-boost stage in boost mode. The voltage ripple in boost and buck modes are given by the following equations:

$$\Delta V_{RIPPLE(BOOST,CAP)} = \frac{I_{OUT(MAX)}(V_{OUT}-V_{IN(MIN)})}{(C_{OUT(BOOST)})(V_{OUT})(f_{SW})} \quad \text{(eq. 6.8)}$$

$$\Delta V_{RIPPLE(BUCK,CAP)} = \Delta I_L(ESR + \frac{1}{8(f_{SW})C_{OUT(BUCK)}}) \quad \text{(eq. 6.9)}$$

For a desired output ripple of 1% of $V_{OUT}$, $C_{OUT(BOOST)} = 15\mu F$ and $C_{OUT(BUCK)} \approx 21.8nF$, assuming that multiple capacitors were configured in parallel at the output so the equivalent ESR was negligible. From this analysis, the output of each phase was selected to have a net capacitance of approximately 90µF to account for tolerances and circuit behavior that Equations (6.8) and (6.9) neglected. Because our non-isolated design had limitations that prevented the design from progressing, as discussed in Section 6.3, a specific capacitor component from a vendor was not selected. However, a low ESR and sufficiently high ripple current rating conductive polymer aluminum solid capacitor would have been implemented at the input and output for this application.

All components not included in the power-path of the buck-boost stage were selected based on constraints specified by the LTC3777 datasheet. Table 6.2 reviews the non-power-path component selection. The components in both phases are all the same, with some exceptions described in the table. For more details of each pin, refer to the LTC3777 datasheet.

[3] Refer to Appendix C for an explanation as to why the maximum input RMS current of a buck converter is equivalent to half the maximum output current.

Table 6.2. Pin descriptions and components connected to all pins of the LTC3777.

| Pin Name | Pin Description | Pin Configuration in Non-Isolated Design |
|---|---|---|
| V5 | Output of the internal 5.5 low dropout regulator (LDO) | Connected to MODE pin to enable pulse-skipping mode (unidirectional converter). A 5µF decoupling capacitor connects to ground to deter coupling from nearby traces. |
| VIN | Main supply pin. | Connected to the input source and VINSNS for voltage sensing purposes. Also connects to RUN and BRUN to turn on the IC and switching biasing supply, respectively. |
| VINSNS | Input voltage sense pin. | Connected to VIN to sense input voltage. |
| VINOV | Sets overvoltage lockout level. | Configured by a resistive divider such that the IC turns off if the input voltage exceeds 110V. |
| RUN | A voltage above 1.2V on this pin turns on the IC. | Connected to VIN to turn on the IC. The resistor connected to RUN prevents RUN from drawing excessive current. |
| PGOOD | Fault indicator output. | Connected to a pull-up resistor which limits the amount of current drawn into the PGOOD pin in case the voltage on the VFB pin is not within 10% of its set point. |
| DRVCC | Output of the internal or external LDO. | Connected to BOOST1 and BOOST2 to assist in powering the internal gate drivers. A 10µF decoupling capacitor connects to ground to deter coupling from nearby traces. |
| BOOST1, BOOST2 | Boosted floating driver supplies. | The bootstrap diode and capacitors connected to these pins allows the voltage on these pins to swing below DRVCC up to VIN+DRVCC. |
| TG1(A), TG2(D) | High current gate drivers for top NMOS devices. | Connected to the top AOTL66518 MOSFETs. |
| SW1, SW2 | Switch node connections to the inductors. | Connected to both terminals of the 450µH inductor. |
| BG1(B), BG2(C) | Bottom NMOS gate driver outputs. | Connected to the bottom AOTL66518 MOSFETs. |
| SS | Soft-start input. | Configured for a soft-start of approximately $t_{ss} =$ |

| | | |
|---|---|---|
| | | $(5n)(1.2V)/(5\mu A) = 1.2ms.$ |
| ITH | Error amplifier output. Can be used to control input power. | Compensation on the ITH pin ensures sufficient damping of undesired oscillations. |
| SGND | Signal ground. All feedback and soft-start connections return to this ground. | Connected to ground. |
| SENSE+, SENSE- | The positive and negative inputs to the differential current comparator. | Connected to the sense resistor in the neighborhood of the inductor. |
| PGND | Power ground (return current path for high-power components). | Connects to ground of all input capacitors, output capacitors, and sense resistors. |
| PLLIN | External synchronization input to phase detector. | Floating because a synchronization feature was not implemented. |
| DRVSET | Sets DRVCC voltage. | Left floating to set DRVCC to 8V. |
| MODE | Selects the ICs mode of operation. | Tied to V5 to enable pulse-skipping mode. |
| IOSENSE+, IOSENSE- | The positive and negative inputs to the input/output average current sense amplifier. | Connected to the sense resistor at the output of the buck-boost stage. The capacitors reduce the susceptibility of the pin to noise. The resistors limit the current flowing out of the pin. |
| VOUTSNS | Output voltage sense pin. | Connected to the output through a 1kΩ resistor to prevent excessive current from entering the pin. |
| EXTVCC | External power input to an internal LDO connected to DRVCC. | Tied to ground because it was not needed. |
| BVFB | The feedback pin to the low quiescent current switching bias supply. | The top phase of the buck-boost stage is configured by a resistive divider so that the switching bias supply produces approximately 3.3VDC. The biasing supply of the bottom phase produces approximately 11VDC. |
| BSW | Bias supply switch node connection to | As the pin description suggests, BSW connects to an inductor. |

| | | |
|---|---|---|
| | inductor. | |
| BRUN | A voltage above 1.21V on this pin turns on the switching bias supply. | Connects to VIN to turn on the switching bias supply. A 0.1µF decoupling capacitor connects to ground to deter coupling from nearby traces. |
| BOV | Sets overvoltage lockout level of the switching bias supply. | Tied to ground because it was not needed. |
| BVIN | Main bias supply pin. | Connected to the input source and VINSNS for voltage sensing purposes. |

### 6.2.2 DC/AC Stage Design

The MOSFETs in the DC/AC stage of the non-isolated converter were selected based on reasoning similar to that presented in Section 6.2.1: If it is assumed that the junction-to-ambient thermal resistance of a MOSFET, $\theta_{JA}$, is 30ºC/W and the maximum junction temperature, $T_J$, is 175ºC, the maximum power dissipated in the MOSFETs is 4.17W. Subsequently, $R_{DS(ON)} < 3.2m\Omega$ because the current passing through the MOSFET directly connected to the main power-path of the buck-boost stage is approximately 36A (assuming 100% efficiency).[4] Additionally, the drain-source voltage rating of the MOSFET should be at least 150VDC to tolerate the output voltage of the buck-boost stage. Also, the gate-source voltage rating cannot be less than +30VDC, as shown in Figure 6.5. According to electronic component distribution companies such as Mouser and DigiKey, a MOSFET which satisfies all the aforementioned criteria did not exist at the time of writing. However, this issue is circumvented if a method of limiting the voltage spikes across the high-side MOSFET is developed, such as implementing a MOSFET with a smaller miller capacitance, or replacing the current MOSFET driver with a driver with a weaker gate drive. Neither approach was further investigated in the non-isolated design due to larger design issues discussed in Section 6.3 which prevented the design from progressing.

[4] The drain-to-source resistance in the triode region was calculated using $P=(I)^2*R$.

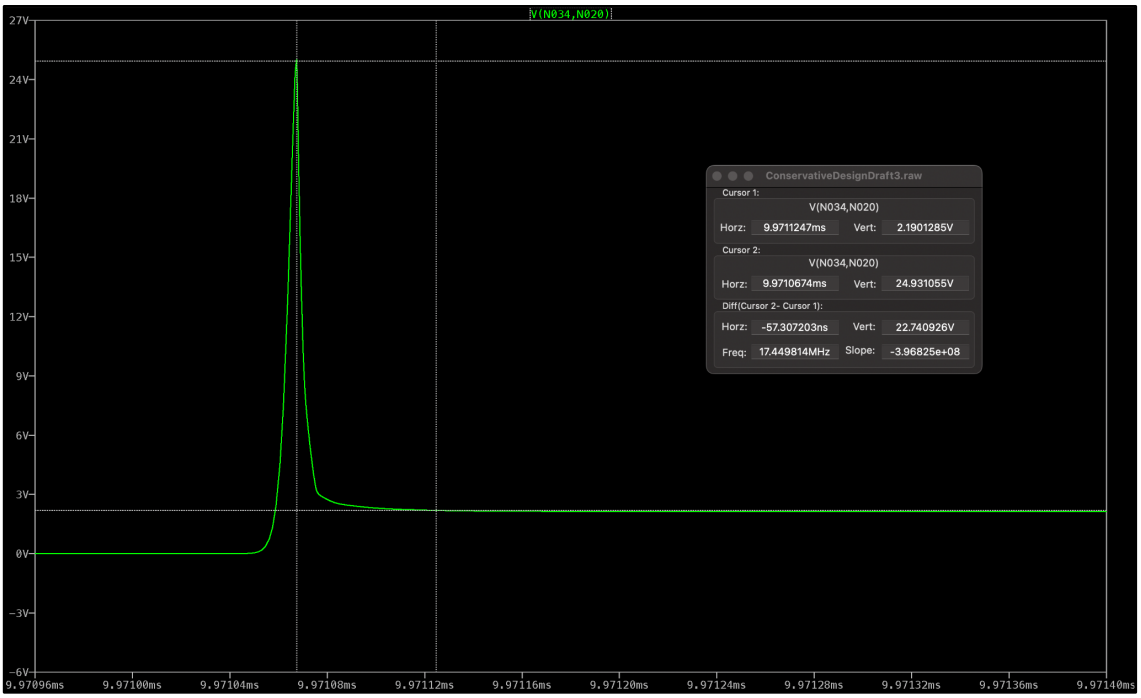


Figure 6.5. Simulation of the voltage spike present in the gate-to-source signal of the AOTL66518 when the signal from the TG pin of the LTC4440A-5 transitions from low-to-high.

The MOSFET connected to ground would warrant a more constrictive $R_{DS(ON)} \ll 3.2m\Omega$. In turn, the current passing from the drain-to-source of this MOSFET would become larger, further restricting the $R_{DS(ON)}$ value until it is sufficiently small. Once again, at the time of this writing, such a MOSFET does not exist. This is another design shortcoming elaborated in Section 6.3.

### 6.2.3 MOSFET Driver Stage Design

All of the components connected to the LTC4440A-5 and ADP3654 were selected according to constraints associated with each pin of the ICs. Table 6.3 and 6.4 concisely summarize the component selection for the MOSFET drivers.

Table 6.3. Pin descriptions and components connected to each pin of the LTC4440A-5.

| Pin Name | Pin Description | Pin Configuration in Non-Isolated Design |
|---|---|---|
| VCC | Chip supply (requires anywhere between -0.3VDC to 15VDC). | The biasing supply of the top phase of the buck-boost stage biases VCC at about 11VDC. A 0.1µF decoupling capacitor connects to ground to deter coupling from nearby traces. |
| INP | Input reference signal to the LTC4440A-5. | The LTC6902 provides a 50% duty cycle 560kHz square wave as a reference to the INP pin. |
| GND | Ground. | Connected to ground. |

| | | |
|---|---|---|
| TS | Top high side source connection. Can be connected to ground in ground-referenced applications. | Connected to ground to maximize the voltage gain of the non-isolated converter. |
| TG | High current gate driver output. | Connected to the gate of the MOSFET in the DC/AC stage which does not have its source connected to ground. |
| BOOST | Highside bootstrapped supply. | Connected to the output of the buck-boost stage to supply bias the high-side MOSFET in the DC/AC stage. The 0.1μF capacitor connected from the BOOST to the TS pin. |

Table 6.4. Pin descriptions and components connected to each pin of the ADP3654.

| **Pin Name** | **Pin Description** | **Pin Configuration in Non-Isolated Design** |
|---|---|---|
| INA | Input reference signal to the ADP3654. | The LTC6902 provides a 50% duty cycle 560kHz square wave as a reference to the INA pin. |
| INB | Input reference signal to the ADP3654. | Floating because it was not needed. |
| VDD | Power supply voltage (requires anywhere between -0.3VDC to 20VDC). | The biasing supply of the top phase of the buck-boost stage biases VCC at about 11VDC. A 5μF decoupling capacitor connects to ground to deter coupling from nearby traces. |
| PGND | Power ground (return current path for high-power components). | Connected to ground. |
| OUTB | Output signal which drives the low-side MOSFET. | Floating because not needed. |
| OUTA | Output signal which drives the low-side MOSFET. | Connected to the gate of the MOSFET in the DC/AC stage which has its source connected to ground. |

### 6.2.4 AC/DC Stage Design

The design of the AC/DC stage was dictated by the requirements of the capacitors and diodes in the charge pump. Flying capacitor C31 in the charge pump of Figure 6.1 is responsible for maintaining the switching voltage at the drain of the MOSFET whose source is connected to ground in the DC/AC stage. Similarly, flying capacitor C32 maintains the switching voltage at the cathode of D6. As such, the flying capacitors should be selected so that they are sufficiently small. Otherwise, the larger ESR typically associated with larger capacitors could potentially cause significant power losses in the presence of a sufficiently large current [27]. If it is possible to procure large capacitors with negligible ESRs, the largest of such a capacitor variety can be implemented to reduce the equivalent impedance of the charge pump stage, thereby alleviating the load dependency issue discussed in Section 6.3. Equation (6.10) can be manipulated to estimate the capacitance of the flying capacitor:

$$\Delta V_{RIPPLE(PUMP)} = \left(\frac{(I_{OUT})(D)}{(C)(f)}\right) + (I_{OUT})(ESR) \approx \frac{(I_{OUT})(D)}{(C)(f)} \qquad \text{(eq. 6.10)}$$

as shown in [27]. It is important to note this equation was derived for the charge pump doubler circuit. For the charge pump tripler circuit constructed in the non-isolated design, Equation (6.10) can be utilized to qualitatively understand how to select the flying capacitors. For example, Equation (6.10) demonstrates that the flying capacitors will decrease with higher frequencies and smaller duty cycles of the applied waveforms. It was from this qualitative understanding, as well as several iterations of the charge pump design in LTspice, that the flying capacitors were selected to be 6µF. The storage capacitors (C34, C35, and C36) were selected based on the allowable output voltage ripple (design criterion 6). Through several iterations of the charge pump design in LTspice, it was found that a value of 50µF for each storage capacitor sufficed. Specific capacitor components were not selected due to larger design issues discussed in Section 6.3 which prevented the non-isolated design from progressing.

To reduce losses, the diodes in the charge pump were selected such that the forward voltage drop was minimized for a reverse voltage rating higher than 400VDC, the maximum output voltage in our unmanned autonomous vehicle application. Evidently, the diodes should also be rated to handle at least 15A of current (11.6A is the maximum output current of our unmanned autonomous vehicle application). As a result, the VS-E5PX7506 diode was selected in the first draft of the design.[5] Figure 6.6 shows that the VS-E5PX7506 diode satisfies all the previously mentioned requirements, but still suffers from high power dissipation in some circumstances. For example, at instantaneous forward currents as large as 10A, the forward voltage drop at a junction temperature of 125ºC is approximately 0.75V, yielding 7.5W of dissipation. A quick solution to this issue would involve paralleling several diodes.

[5] Refer to the VS-E5PX7506 datasheet if desired.

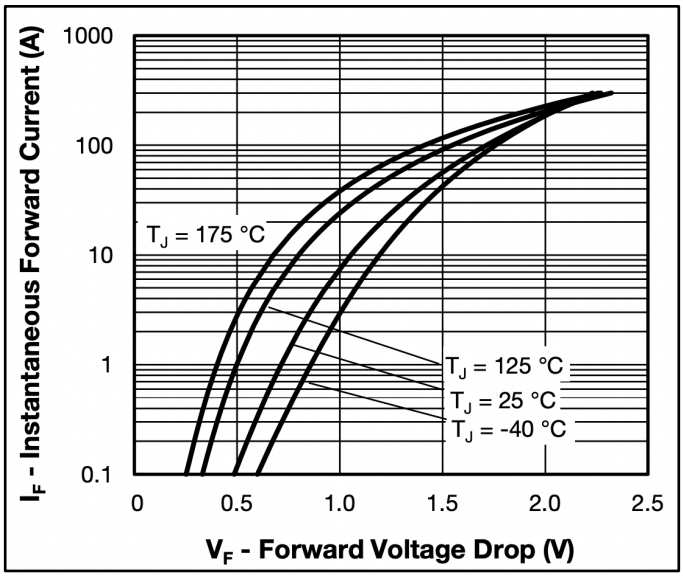

Figure 6.6. Forward voltage drop characteristics for the VS-E5PX7506 diode [28].

### 6.2.5 Oscillator Stage Design

Similar to Section 6.2.3, the components connected to the LTC6902 were selected based on pin descriptions and other constraints. Table 6.5 summarizes the component selection for the oscillator.

Table 6.5. Pin descriptions and components connected to each pin of the LTC6902.

| Pin Name | Pin Description | Pin Configuration in Non-Isolated Design |
|---|---|---|
| $V^+$ | Supply voltage pin (requires anywhere between 2.7VDC to 5.5VDC). | The biasing supply of the bottom phase of the buck-boost stage biases $V^+$ at 3.3VDC. A 0.1µF decoupling capacitor connects to ground to deter coupling from nearby traces. |
| DIV | Frequency divider setting input. | Tied to ground for the division by 1 setting of the frequency (corresponds to $N = 1$ in frequency equation). |
| PH | Sets the outputs to produce 2-phase, 3-phase, or 4-phase signals. | Tied to ground for the 2-phase setting since there are only two MOSFET drivers that the LTC6902 connects to. |
| OUT1 | Oscillator output. | Feeds a 50% duty cycle 560kHz square wave to the LTC4440A-5. |
| OUT2 | Oscillator output. | Feeds a 50% duty cycle 560kHz square wave to the ADP3654. This square wave is 180º out-of-phase |

| | | |
|---|---|---|
| | | with respect to the OUT1 square-wave. |
| OUT3 | Oscillator output. | Floating because it was not needed. |
| OUT4 | Oscillator output. | Floating because it was not needed. |
| GND | Ground. | Connected to ground. |
| MOD | Spread spectrum frequency modulation setting resistor pin. | Connected to ground to disable modulation (corresponds to $M = 1$ in frequency equation). |
| SET | Frequency setting resistor pin. | 357kΩ resistor connected to achieve an oscillation frequency of about 560kHz. Resistor selection is based on the following equation: $f_{OUT} = \frac{10MHz}{N \cdot M}(\frac{20k\Omega}{R_{SET}})$, where $N = M = 1$ for this design. |

## 6.3 Drawbacks & Concerns

The non-isolated design can attain an output voltage of 400VDC in LTspice, but not without exceeding the absolute maximum rating of the BOOST pin of the LTC4440A-5.[6] The design has several other problems that prevent it from being immediately adopted. In particular, the load dependency and low efficiency of the non-isolated design are what prevented it from progressing to the next design phase.

### 6.3.1 Load Dependency

The non-isolated design can attain an output voltage of 400V, but this can only be achieved when the load resistance and resistors R2 and R13 are sufficiently large. If R2 and R13 are maintained as constant while the load resistance is decreased, the output voltage reduces. For example, if $R2 = R13 = 1.1M\Omega$ and the load resistor value is 77Ω, the maximum output voltage of the non-isolated boost converter is approximately 420VDC. If the load resistance is then reduced to 43Ω and $R2 = R13 = 1.1M\Omega$, the maximum output voltage reduces to 320VDC.

The load dependence of the non-isolated boost converter can be attributed to the AC/DC stage. The ESR of the flying capacitors, in conjunction with large currents, conjure voltage drops in the charge pump stage which change as the current varies. Moreover, the three 50μF capacitors in the AC/DC stage cannot withstand sufficiently large currents, further reducing the gain of this stage. It may be possible to make the capacitors in the AC/DC stage sufficiently large to reduce the equivalent impedance of the charge pump, but the ESR of a capacitor is typically proportional to its size. Alternatively, we can solve the load dependence problem by creating our own control

[6] By altering R2 and R13 in Figure 6.1 to 1.35MΩ, the output voltage of the non-isolated converter can become as large as 450VDC with negligible ripple.

system to regulate the output voltage. However, this idea was abandoned because of the low efficiency of the non-isolated design, described in the next section.

### 6.3.2 Low Efficiency

Another problem with the non-isolated design is low efficiency. Different load resistances were simulated with the following parameters:

- $R2 = R13 = 1.1M\Omega$
- Input voltage is 50VDC
- Input current is 62.5A

With a load resistance of 77Ω, the output power is about 2.31kW, yielding an efficiency of 73.92%. When the load resistance is 43Ω, the output power is nearly 2.2kW and the efficiency 70.4%. These efficiencies are lower than the desired minimum efficiency of 80%.

A substantial reason for the low efficiency of this design is the DC/AC stage. The two MOSFETs in this stage–Q3 and Q4–generate considerable power losses when converting the DC voltage of the buck-boost stage into an AC voltage waveform. In particular, when the load resistance value is 77Ω, the average power losses of the MOSFETs in the DC/AC stage are about 100W and 150W, respectively. In addition, MOSFETs with lower drain-to-source on-resistances were experimented with in LTspice to rectify the issue. However, calculations performed in Section 6.2.2 indicated that the MOSFETs which would be required to resolve the low-efficiency of the DC/AC stage would need to have impractically small on-resistances for the given gate-to-source and drain-to-source voltage ratings. Thus, the low efficiency issue prompted us to design a new converter.

# 7. Final Design: Isolated Push-Pull Boost Converter

Contrary to our non-isolated design, our isolated design relied upon well-established techniques to satisfy the design criteria.

## 7.1 Block Diagram Description

A schematic of the isolated design can be observed in Figure 7.1.

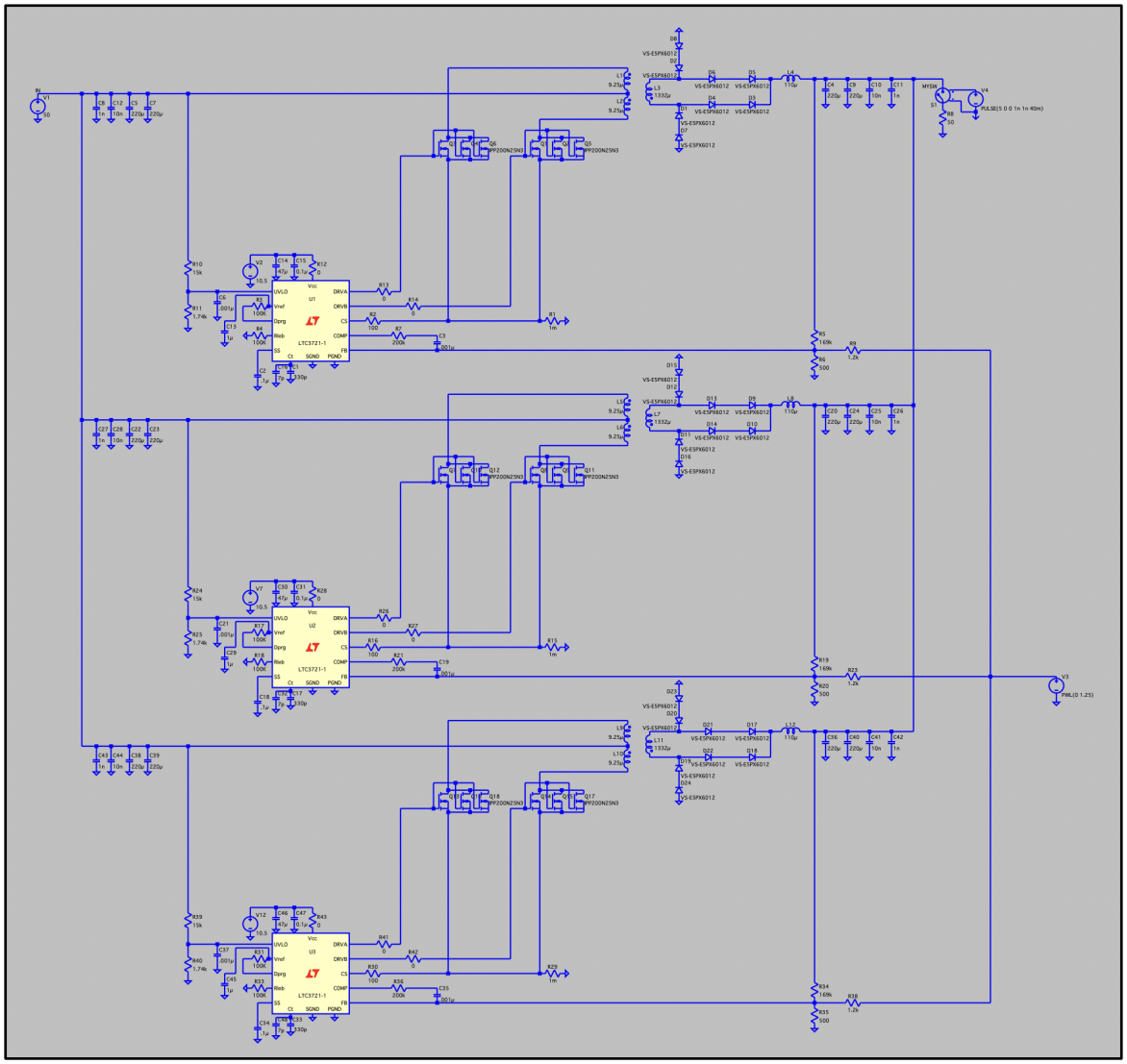

Figure 7.1. Schematic for the isolated design.

Each of the three phases of the design are identical. Consequently, an understanding of the design can be acquired through the analysis of a single-phase. A single-phase rendering of the isolated design and a description of each block within the rendering can be reviewed below.

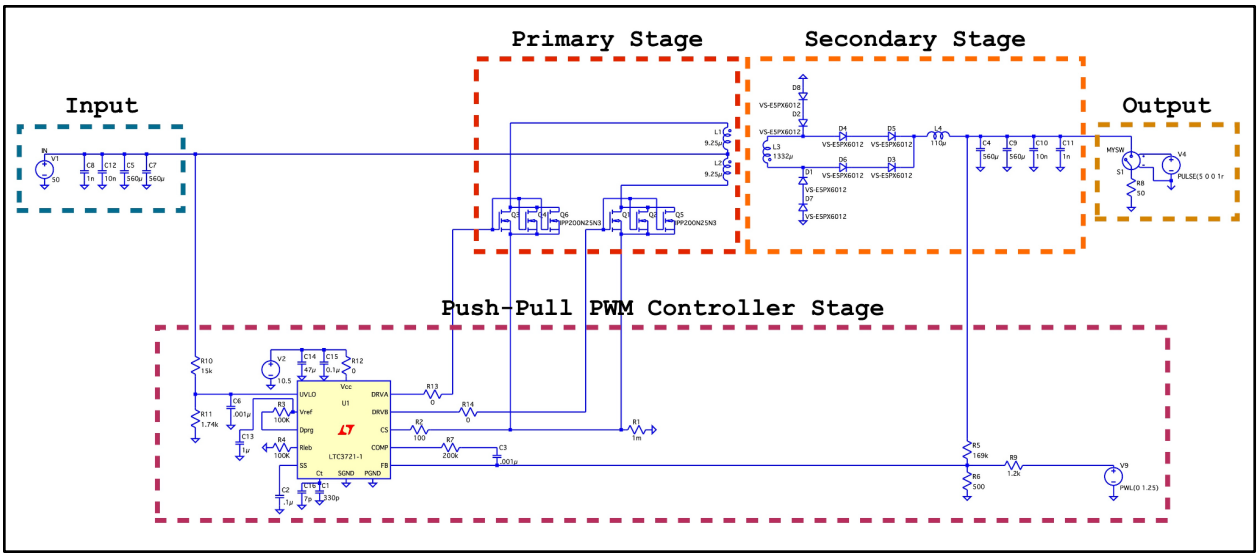


Figure 7.2. Schematic for the single-phase rendition of the isolated design with delineated blocks.

### 7.1.1 Primary Stage Description

The primary stage for all phases of the isolated push-pull boost converter consists of three NMOS devices on each side of the primary center-tapped winding of the DCDC2400-001 transformer from Premo, a magnetics company. Three MOSFETs are utilized on each side of the primary stage to manage the power dissipated per MOSFET. The MOSFETs are controlled such that when three MOSFETs on one side of the primary stage are operating in the triode region, the three MOSFETs on the other side of the primary stage are off. For example, when the left side MOSFETs are in the triode region the right side MOSFETs are off. As a result, the current in the primary stage traverses from the input source, out from the top-half of the primary winding, and from the drain to the source of the left side MOSFETs. Contrarily, when the right side MOSFETs are in the triode region the left side MOSFETs are off. As such, the current in the primary stage travels from the input source, into the bottom-half of the primary winding, and from the drain to the source of the right side MOSFETs. There also exists an interval of time where all six MOSFETs in the primary stage are off and current from the input source is pushed into the magnetizing inductance of the transformer. From these insights on the current behavior in the primary stage, it can be discerned that current is always “pushed” into the primary winding of the transformer from the input source for the described PWM scheme, which is summarized in the Figures 7.3 and 7.4.

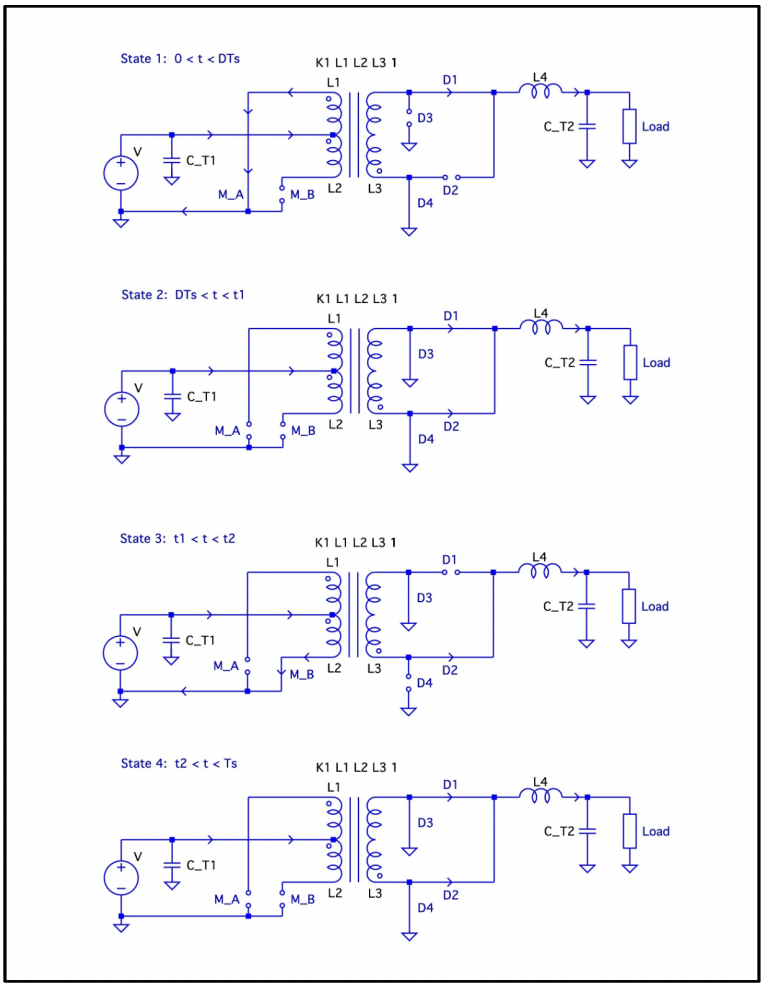


Figure 7.3. The four states the converter cycles through every switching period, $T_s$.

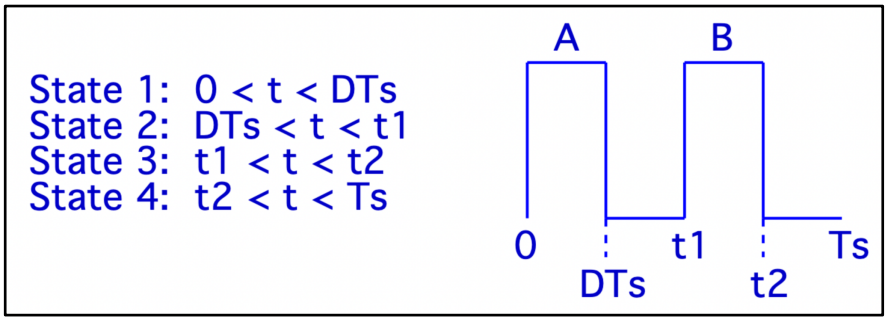


Figure 7.4. Superimposed PWM waveforms for the isolated design, where $t_1 = \frac{T_s}{2}$ and $t_2 = \frac{T_s}{2} + DT_s$ if $D = 0.5$. Observe that this figure suggests that the frequency of the current waveform through the output inductor is $\frac{1}{t_1} = \frac{2}{T_s}$.

### 7.1.2 Secondary Stage Description

For all phases of the isolated push-pull boost converter, the secondary stage contains the secondary side of the DCDC2400-001 transformer, eight fast rectifier diodes, and an output filter. The diodes connected directly to the output inductor rectify the current waveform which travels through the output inductor, whereas the diodes connected to ground rectify the pulsating voltage waveform applied to the anodes of D4-D5 and D6-D3 in Figure 7.2. Afterwards, the output filter attenuates nearly all AC frequency components of the pulsating voltage waveform from the diode juncture.

The following example demonstrates the behavior of the secondary stage: Suppose that the MOSFETs on the left side of the primary stage are in the triode region and the MOSFETs on the right side are off. From Section 7.1.1, it can be inferred that a current through the secondary side of the transformer is induced such that it enters the bottom half of the secondary winding. Hence, D6-D3 in Figure 7.2 becomes reverse biased, while D4-D5 becomes forward biased. Without D8-D2 or D7-D1, D6-D3 and D4-D5 would always remain reverse biased because of the -600VAC to -1200VAC pulsating voltage waveform applied to their anodes. Instead, this mishap is circumvented because D7-D1 becomes forward biased and D8-D2 becomes reverse biased, shorting the positive terminal of the secondary winding to ground. In turn, this implies that a +600VAC to +1200VAC pulsating voltage waveform appears at the negative terminal of the secondary winding, which is consistent with D4-D5 being forward biased. Thereafter, the output filter attenuates nearly all AC components of the +600VAC to +1200VAC pulsating voltage waveform. A similar pattern of reasoning can be employed when the MOSFETs on the right side of the primary stage are in the triode region and the MOSFETs on the left side are off. From these conceptual analyses, it can be concluded that the secondary stage always “pulls” current into the load for the PWM scheme described in Section 7.1.1.

### 7.1.3 Push-Pull PWM Controller Stage Description

The push-pull PWM controller stage consists of the LTC3721 and a DAC modeled as a PWL voltage source for output voltage control. The LTC3721 is a push-pull PWM controller which employs peak current mode control with programmable slope compensation, leading edge blanking, and protection features necessary for high density power modules [29]. In short, it is responsible for driving the MOSFETs as described in Sections 7.1.1 and 7.1.2. Within the isolated design, the LTC3721 is configured to have a switching frequency of 100kHz, a soft-start of approximately 3.8ms, 310ns of leading edge blanking, and a deadtime of nearly 115ns. Moreover, the UVLO pin has been configured to turn on the IC when the input voltage is about 50VDC, but can also be configured through digital means, as explored in Section 7.4. Lastly, when the output voltage of the DAC is 2.1V, the output voltage of the converter is set to 280VDC; when the output voltage of the DAC is 1.25V, the output voltage of the DAC is set to 400VDC. The operation of the DAC is explored in Section 7.3.2.

## 7.2 Design Process

Before any of the resistor, inductor, or capacitor values in the isolated design were selected, a suitable transformer was selected: The DCDC2400-001 transformer. According to the datasheet, the DCDC2400-001 is a 2kW 100kHz 1+1:12 push-pull topology transformer. As a result, all components in the isolated design were selected to be compatible with the DCDC2400-001 transformer. A 3D rendering of the transformer is shown in Figure 7.5.

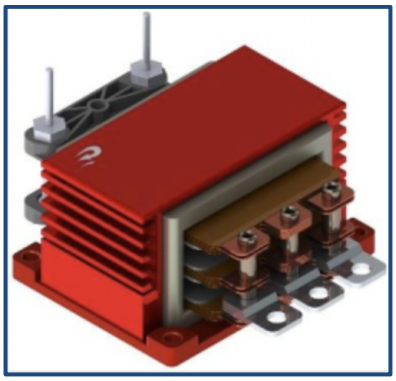

Figure 7.5. Render of the DCDC2400-001 transformer. The three metal contacts shown in the figure connect to the converter as follows: left contact to the DRVA MOSFETs, center to the PEMFC, and right to the DRVB MOSFETs [30].

### 7.2.1 Primary Stage Design

The design of the primary stage mainly involved the selection of appropriate MOSFETs. The maximum drain to source voltage rating for the MOSFETs needed to be at least 250V because the maximum voltage stress on each MOSFET is approximately twice the maximum input voltage (100VDC). For example, at an input voltage of 100VDC, when the MOSFETs on the left side of the primary stage are in the triode region, the MOSFETs on the right side are off. Kirchoff's voltage law can be applied through the source, L1 in Figure 7.2, and the drain-source voltage across the left side MOSFETs. As a result, the maximum electric potential difference across L1 is 100V. Consequently, the electric potential difference across L3 is 1200V. Reflecting this voltage back to L2 suggests the electric potential difference across L2 is 100V, so the maximum voltage drop across the right side MOSFETs is 200V. A similar pattern of reasoning can be applied to the other states of the converter.

Next, it was important to select a MOSFET with a drain-to-source voltage rating of at least 250V, a positive gate voltage rating of at least 15V, and sufficiently low drain-to-source resistance; however, the drain-to-source resistance should not be so low that the overcurrent comparator within the LTC3721, shown in Figure 7.6, exceeds its 650mV threshold for a sufficiently long interval of time. Otherwise, the PWM operation of the LTC3721 will be terminated until the capacitor on the SS pin charges back to 4V when the converter is in steady-state (the capacitor discharges when PWM operation is terminated). If the overcurrent comparator limit is still exceeded by the time the capacitor on the SS pin charges back to 4V, PWM operation will cease

again. This operation is referred to as "hiccup mode operation" [29].[7] For these reasons, the IPP20 0N25N3 20mΩ MOSFET was selected.[8] To further reduce the power dissipated in each MOSFET, three MOSFETs were put in parallel for each side of the primary stage. This is effective to having one 6.7mΩ on each side of the primary stage (since $20m\Omega \,||\, 20m\Omega \,||\, 20m\Omega \approx 6.7m\Omega$).[9]

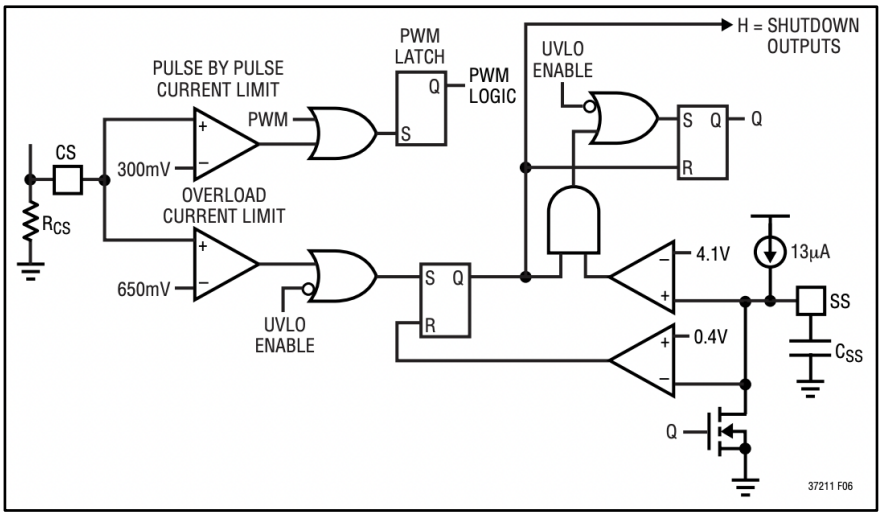


Figure 7.6. Internal circuitry of the LTC3721 that enables hiccup mode operation [29].

For an effective 6.7mΩ MOSFET on each side of the primary stage, hiccup mode operation was not triggered during the start-up of the converter when the input voltage is 50VDC, as presented in Figure 7.7. Any lower effective MOSFET resistance could cause hiccup mode operation to trigger for an input of 50VDC. When the input voltage is 100VDC, the overcurrent limit is exceeded four times during start-up. In other words, hiccup mode operation occurred, as can be observed in Figure 7.8. This strongly suggests that an effective 6.7mΩ MOSFET on each side of the primary stage may be the lower drain-to-source limit for the component values in Figure 7.2.

[7] Note that it is primarily the overload current comparator which enables hiccup mode operation. Under most abnormal conditions, the pulse-by-pulse comparator is fast enough to prevent hiccup operation.

[8] Refer to Appendix J for the IPP200N25N3 datasheet.

[9] If it is desired to implement a single MOSFET rather than three in parallel, the IXFN240N25X3 MOSFET appears to be a suitable candidate: it has a maximum drain-to-source voltage of 250V, drain currents of up to 240A, gate-source voltages up to 30V, and a maximum drain-to-source resistance of 4.5mΩ. If hiccup mode becomes more prevalent, the inductance of the output inductor may be increased or the input and output capacitance could be decreased. A possible consequence of increasing the output inductance is a considerable gain in converter weight.

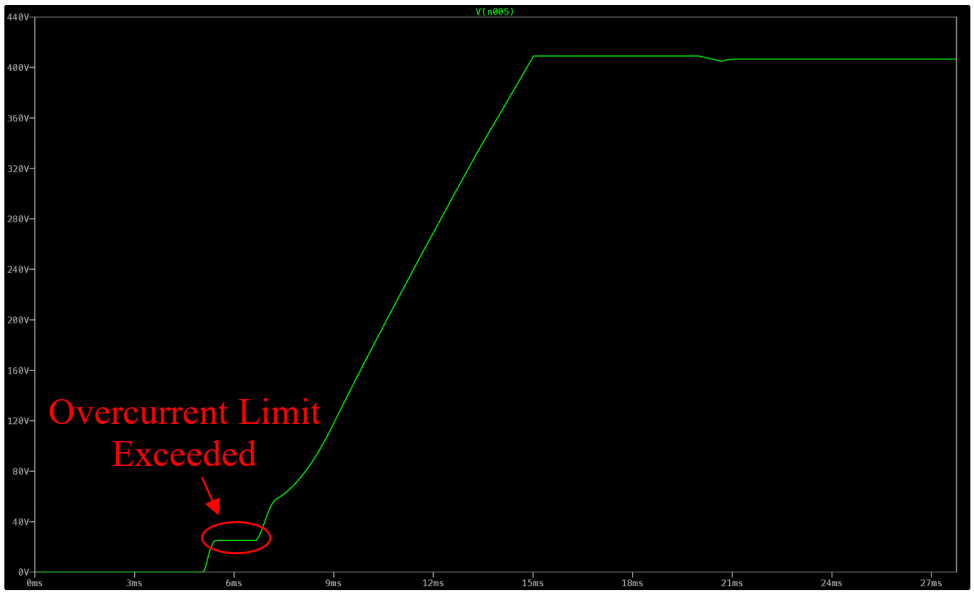


Figure 7.7. Simulation displaying excession of the overcurrent limit at an input voltage of 50VDC. From 5.5ms to 7ms, the soft-start capacitor recharges to its value before the overcurrent limit was exceeded.

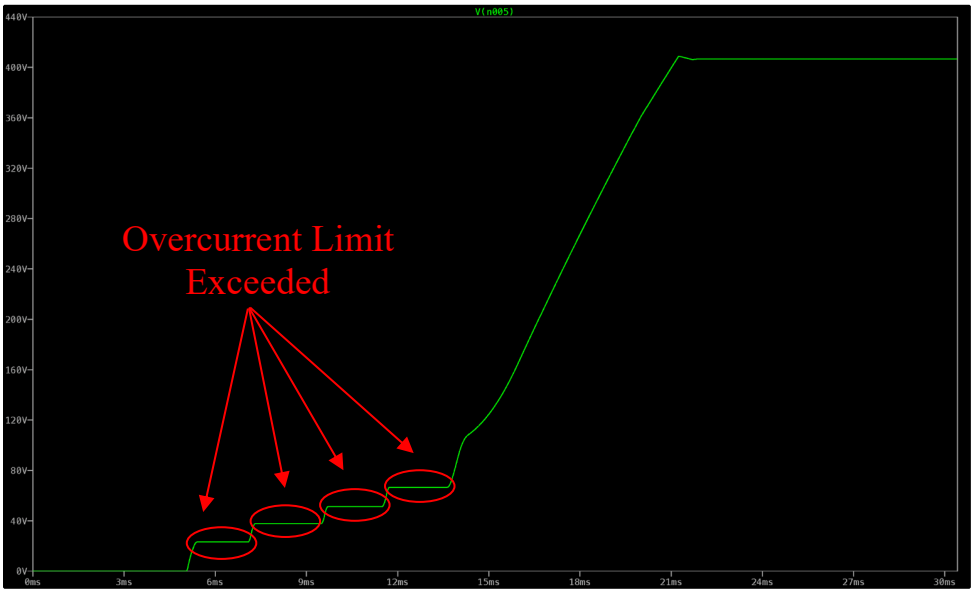


Figure 7.8. Simulation displaying excession of the overcurrent limit four times from 5.5ms to 14ms at an input voltage of 100VDC. Each time the overcurrent limit is exceeded, the soft-start capacitor recharges to its value before the overcurrent limit was exceeded, creating a sawtooth waveform on the SS pin from 5.5ms to 14ms.

In addition to preventing hiccup mode operation at the primary operating input voltage of 50VDC, three IPP200N25N3 MOSFETs in parallel on each side of the primary stage are also suitable for power management in steady-state. According to its datasheet, the maximum junction temperature of the IPP200N25N3 is 175ºC, and the junction-to-ambient resistance is a maximum

of 62K/W. Assuming the ambient temperature is 50ºC, Equation (6.6) suggests that the maximum power dissipated in each MOSFET in steady-state can be no more than approximately 2W without a heat sink. Since there are three phases in the isolated design and three MOSFETs in parallel on each side of the primary stage, the maximum current through an individual MOSFET is 7.22A. Hence, the maximum power dissipated in an individual MOSFET is approximately 1W in steady-state in the triode region. In reality, the power dissipated will likely deviate from this calculated value due to various losses such as power dissipated in the gate or switching loss, suggesting that a 1W fan or appropriate heatsink may be needed in practice.

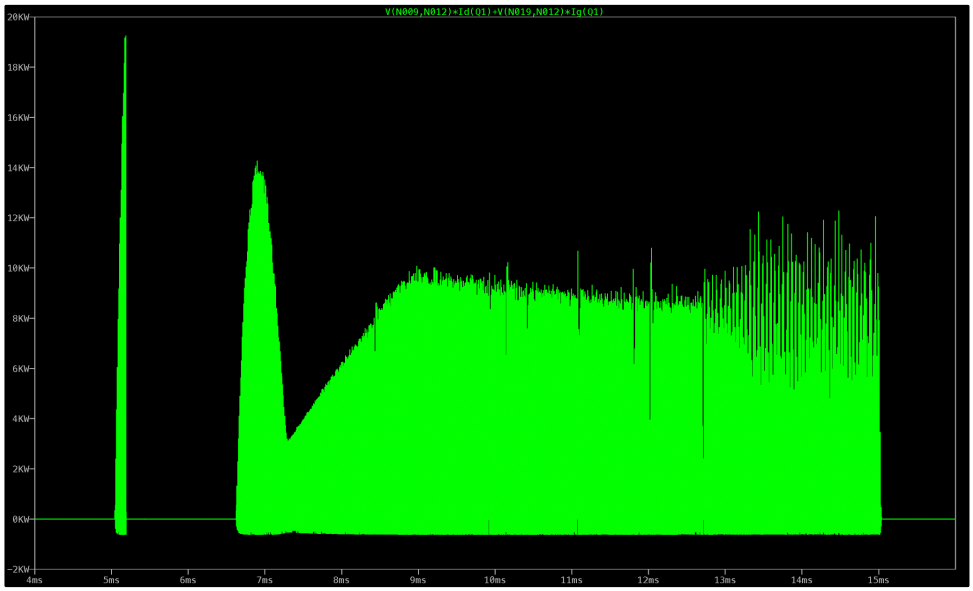

Figure 7.9. Simulation showing pulses of power experienced by an individual MOSFET during startup of the isolated design at full power (3.25kW).

During startup, LTspice predicts that an individual MOSFET in the isolated design will experience large pulses of power, as shown in Figure 7.9. Such large pulses of power may not occur in practice due to the inclusion of parasitics from each component and simplified models employed in LTspice (described in Chapter 5). However, the power pulses were still examined in LTspice to discern if the safe operating area curve of the IPP200N25N3 was being violated using Figure 7.10. The current through an individual MOSFET during startup is shown in Figure 7.11.

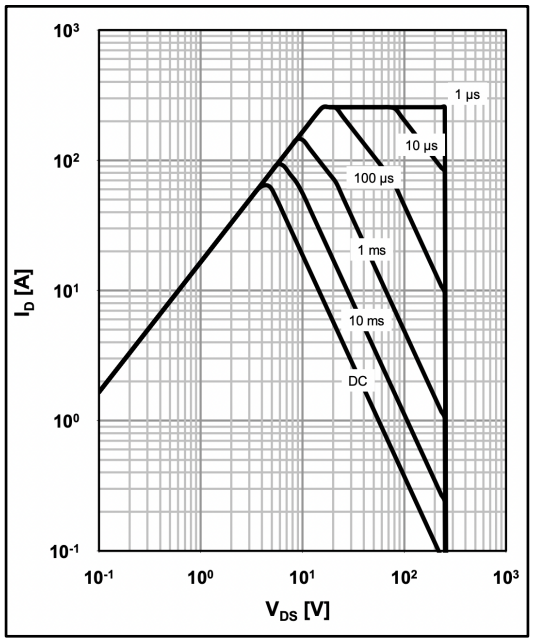


Figure 7.10. Safe operating area curve of the IPP200N25N3 MOSFET [31].

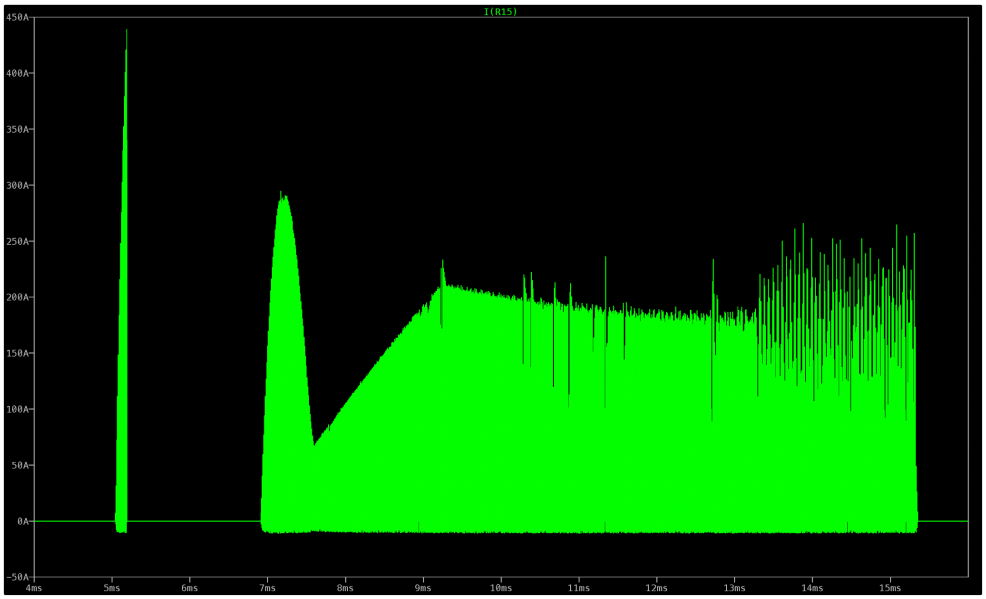


Figure 7.11. Simulation showing pulses of current experienced by an individual MOSFET during startup of the isolated design at full power (3.25kW).

The largest pulse with respect to area in the 5ms to 5.2ms interval in Figure 7.11 achieves a current magnitude of 200A for 269ns, which is significantly less than 1µs. This is further evidenced by Figure 7.12. All other pulses within the 5ms to 5.2ms also persist for less than 1µs. Moreover, all pulses from 7ms to 15ms remain within the specified time limits of the safe operating area curve. If it is desired to reduce the magnitude of the spike, the capacitance on the SS pin of

the LTC3721 can be increased. Appendix H provides the SPICE netlist of the isolated design to verify these results.

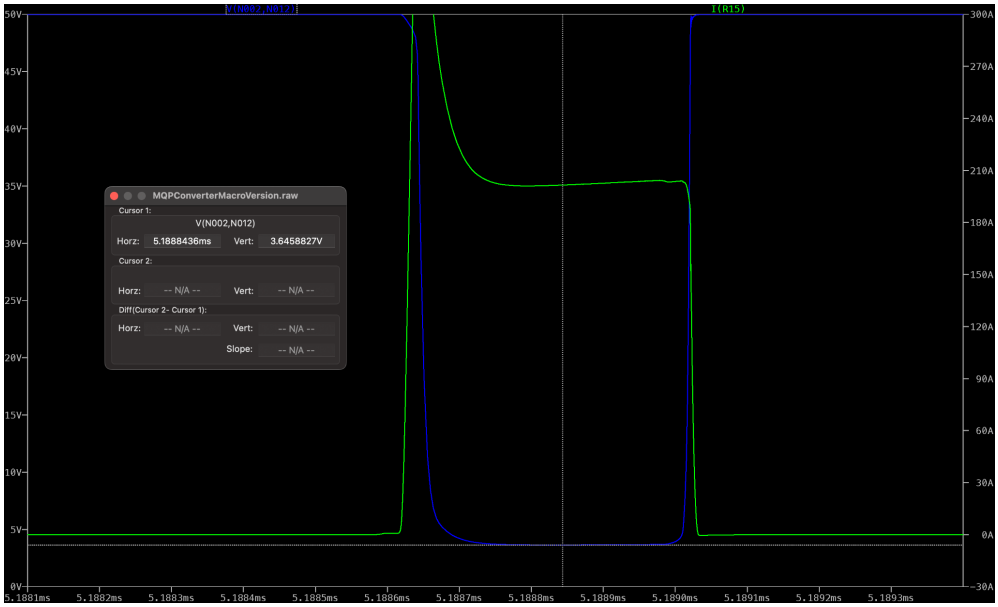


Figure 7.12. Simulation showing the largest pulse in terms of area in the 5ms to 5.2ms interval.

The IPP200N25N3 also possesses sufficient switching and drain-to-source resistance characteristics, as seen in Figure 7.13 and Table 7.1 below. For example, Figure 7.13 shows that when the gate-source voltage is 10V, the on-resistance remains less than 20mΩ for $T_j = 25ºC$.

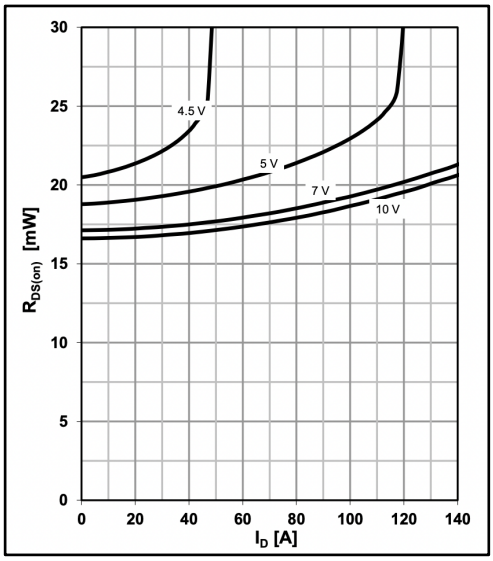


Figure 7.13. IPP200N25N3 MOSFET on-resistance vs. drain-current and gate-source voltage for $T_j = 25ºC$ [31].

Table 7.1. Switching characteristics for the IPP200N25N3 MOSFET. For all parameters in the table, $(t \cdot f_{SW})100 \approx 4.5\%$ at maximum [31].

| | | | | | | |
|---|---|---|---|---|---|---|
| Turn-on delay time | $t_{d(on)}$ | $V_{DD}$=100 V, $V_{GS}$=10 V, $I_D$=25 A, $R_{G,ext}$=1.6 Ω | - | 18 | - | ns |
| Rise time | $t_r$ | | - | 20 | - | |
| Turn-off delay time | $t_{d(off)}$ | | - | 45 | - | |
| Fall time | $t_f$ | | - | 12 | - | |

As a consequence of the analysis shown in Table 7.1, the 20mΩ rating of the IPP200N25N3 was deemed sufficient. Other seemingly viable MOSFET candidates lacked LTspice models and were not explored further in simulation. Such MOSFETs would likely need to be explored in a laboratory setting, as discussed in Chapter 10.

### 7.2.2 Secondary Stage Design

The design of the secondary stage centered on fast diode selection and sufficient filtering of the waveform following the diode juncture in the secondary stage. To properly select the diodes in the secondary stage, the peak current through the diodes must be discerned. The peak current through the diodes occurs when the output voltage is 280VDC and the output current is approximately 11A. Through LTspice, it was found that the peak current through the diodes in steady-state is about 7.2A, as Figure 7.14 suggests.

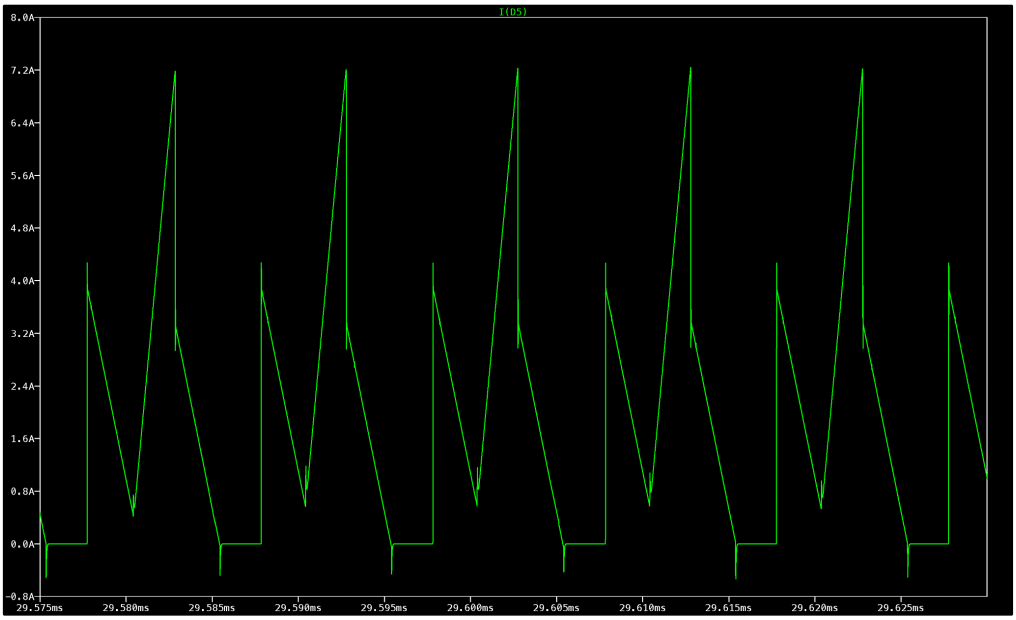


Figure 7.14. Waveform morphology of the current through each diode in the secondary stage when the output current is 11A.

The diodes must be selected to minimize the voltage drop at a peak steady-state current of 7.2A while withstanding reverse voltages of up to 1200V, as insinuated in Section 7.2.1. Furthermore, the diodes must be fast due to the 100kHz voltage waveform applied to the diodes from the secondary side of the transformer. To satisfy the reverse voltage criterion, either a fast diode with a reverse voltage rating of greater than 1200V can be selected, or two appropriate fast diodes can be placed in series to increase the reverse voltage rating beyond 1200V. Given these constraints, the VS-E5PX6012 diode was selected, which can average currents up to 60A.[10] Two VS-E5PX6012 in series can withstand up to 2400V.[11] Figure 7.15 shows that the VS-E5PX6012 diode satisfies all the previously mentioned requirements, but may still experience power dissipation as large as 12W in steady-state according to LTspice. However, as explored in Section 7.4.2, the package of the VS-E5PX6012 may be large enough to withstand such large power dissipation. Based on the forward voltage drop characteristics, it is reasonable to assume the designers of the diode may have anticipated such large power dissipation, hence the package size.

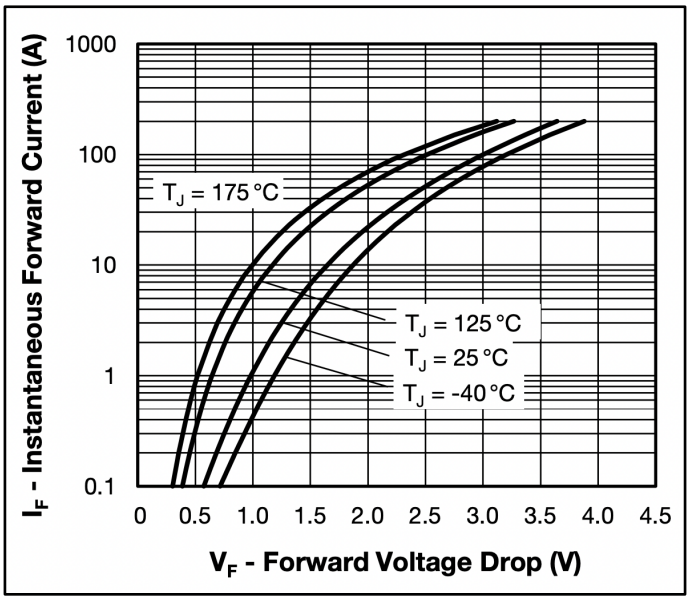


Figure 7.15. Forward voltage drop characteristics of the VS-E5PX6012 diode [32].

The second-order low pass filter in the secondary stage possesses a resonant frequency, $f_O$, given by the following equation:

$$f_O = \frac{1}{2\pi\sqrt{L_{eq}C_{eq}}} \quad \text{(eq. 7.1)}$$

[10] Refer to Appendix J for the VS-E5PX6012 datasheet.

[11] If it is desired to implement one fast recovery diode rather than two in series, the QRS1420T30 diode is a suitable candidate which was in-stock as of the time of this writing. However, it lacks an LTspice model, so it was not investigated in LTspice.

$L_{eq} = 110\mu H$ is the equivalent inductance of the filter and $C_{eq} = 440\mu F$ is the equivalent capacitance of the filter, yielding $f_O = 723\ Hz$.[12] Consequently, the output voltage waveform of the isolated design consists of a DC signal imposed upon an AC signal with sufficiently small perturbations about the DC output, as shown below (when the DC output of the converter is 280VDC and 400VDC). It is important to note that sufficient filtering could have been accomplished with a smaller inductor. However, a smaller inductor will warrant a larger change in current over the time interval that energy is being stored within it. In turn, the LTC3721 may enter hiccup mode operation to compensate for this larger change in current. Moreover, a lower inductor value would change the magnitude of the ripple of the current waveform from 8A to a larger value.[13] The inductor current ripple for $L_{eq} = 110\mu H$ is shown in Figure 7.16. In reality, the current ripple may be less than predicted by the calculations and simulation because the magnetizing inductance of the transformer was not modeled, so the inductance of the output inductor was not reduced.

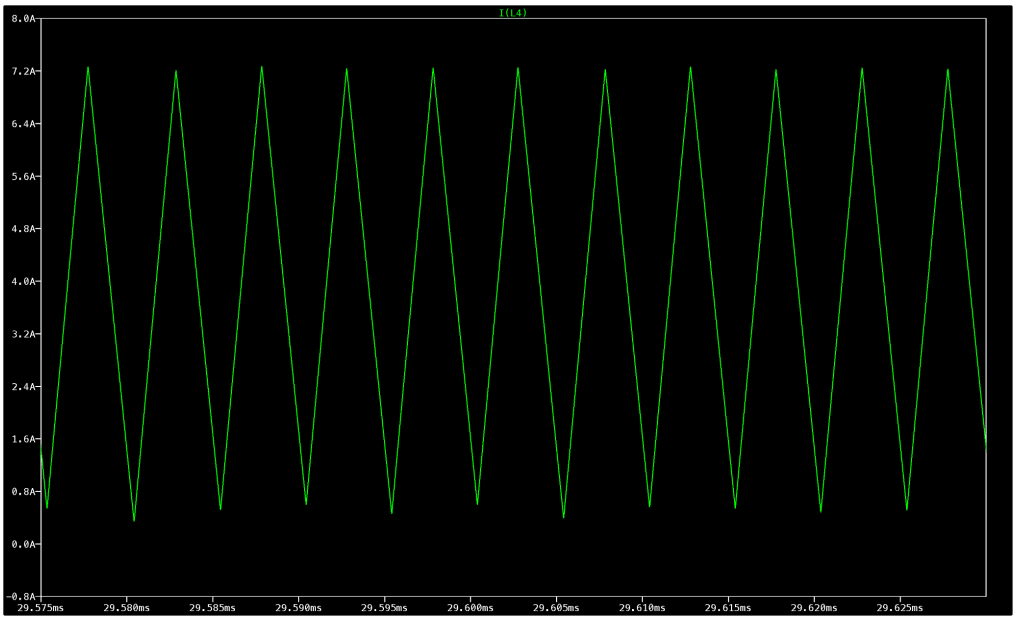

Figure 7.16. Waveform morphology of the current through the output inductor when the output current is 11A.

The inductor component was selected based on the frequency rating (100kHz), maximum DC-bias current through the inductor in steady-state (3.9A), maximum peak current in steady-state (8A), and voltage rating (at least 1000V). The ESR of the inductor also had to be less than 10mΩ to minimize power dissipation. As such, the CPEX3635L-111MC inductor from CODACA was selected. The CPEX3635L-111MC was designed for frequencies as large as 1MHz (as evidenced by Figure 7.17), currents as large as 24A before saturation, and a maximum DC resistance of

[12] Refer to Appendix D for the output inductor and total output capacitance equations.

[13] The 8A ripple current value can be solved by using the inductance equation in Appendix D.

7.41mΩ. However, the voltage rating of the CPEX3635L-111MC was not specified. If desired, a choke rated for 1000V can be implemented instead, as discussed in Section 7.4.2.

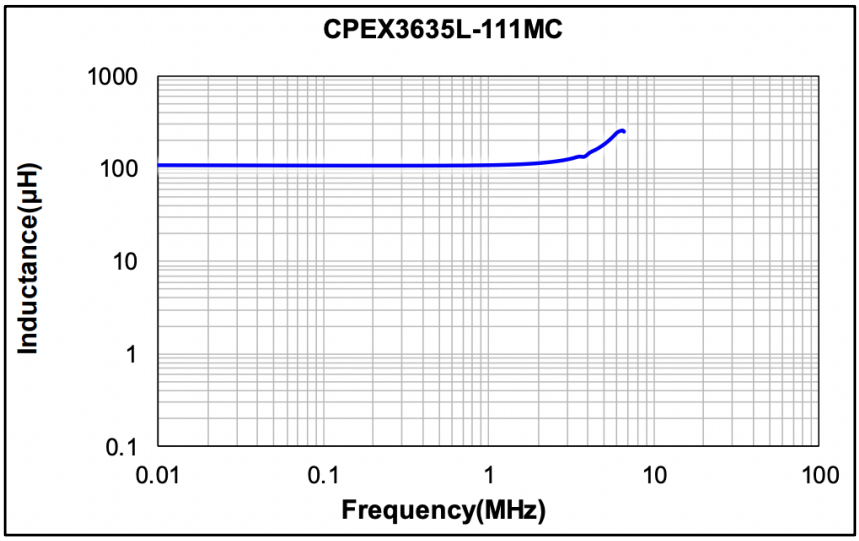


Figure 7.17. Inductance as a function of frequency for the CPEX3635L-111MC inductor [33].

As a consequence of the duty cycle being nearly 0.5, the total output capacitance can be selected to be as low as 100μF to attain a negligible output voltage ripple.[14] Larger capacitor values also suffice, so long as the inrush current during startup doesn't compromise the performance of a component. Thus, two 220μF E91D501VND561MA80U aluminum electrolytic capacitors in the secondary stage were implemented, along with two ceramic capacitors with smaller capacitance values. The aluminum capacitors were needed to store the bulk of the electric field energy and suppress voltage ripple (observe Figures 7.18 and 7.19 for the voltage ripple), and were selected based upon the output voltage rating (at least 450V) and ripple current handling capabilities (4A at 200kHz for two aluminum capacitors in parallel). For the E91D501VND561MA80U capacitor in particular, the ripple current rating at 120Hz is 1.37A; at 10kHz, the ripple current rating is 1.918A. If the pattern is extrapolated to frequencies beyond 10kHz, these capacitors will be able to withstand more current at higher frequencies. It may also be possible to implement other capacitors, such as the 560μF E91D501VND561MA80U aluminum electrolytic capacitors, which promise to withstand ripple currents of up to 4.719A up to 100kHz.[15] Additionally, the ESR and ESL of the aluminum capacitors needed to be small to prevent discontinuities or oscillations in the output waveform.[16] The ceramic capacitors can significantly reduce the equivalent ESR and ESL of the output capacitor stage, in addition to responding to sufficiently fast transients. The same reasoning can be applied to the input capacitors in Figure 7.1.

[14] This can be verified with the capacitor equation in Appendix D.
[15] The simulation tests in Appendix F were not performed with this capacitor due to protracted simulation times.
[16] Refer to Appendix I for the bill of materials (BOM) for the isolated push-pull design.

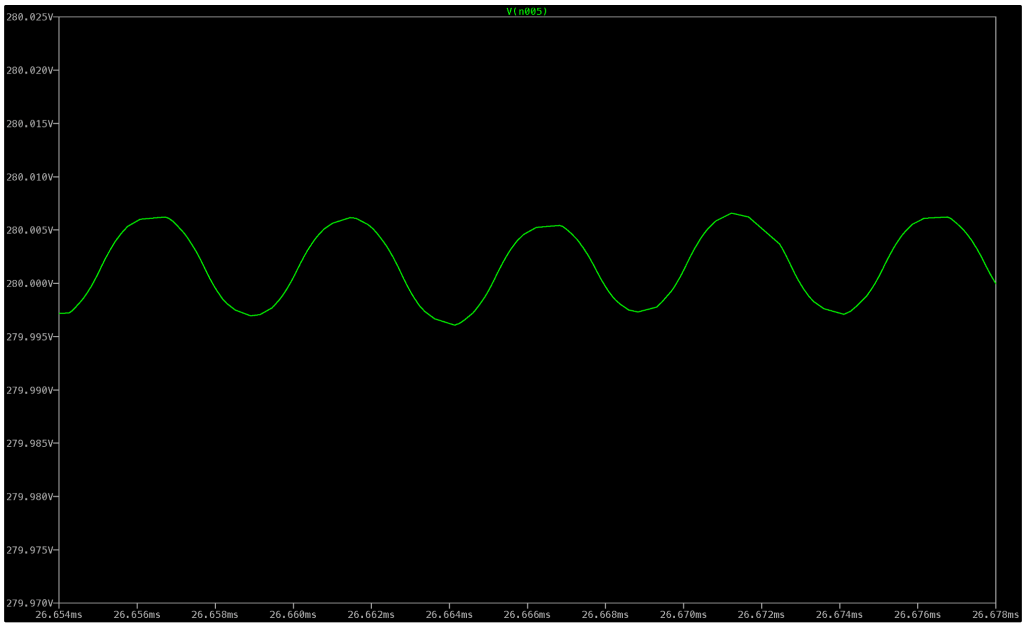


Figure 7.18. Simulation showing the output voltage ripple when the output voltage is 280VDC. The ESR of the output capacitors was assumed to be negligible.

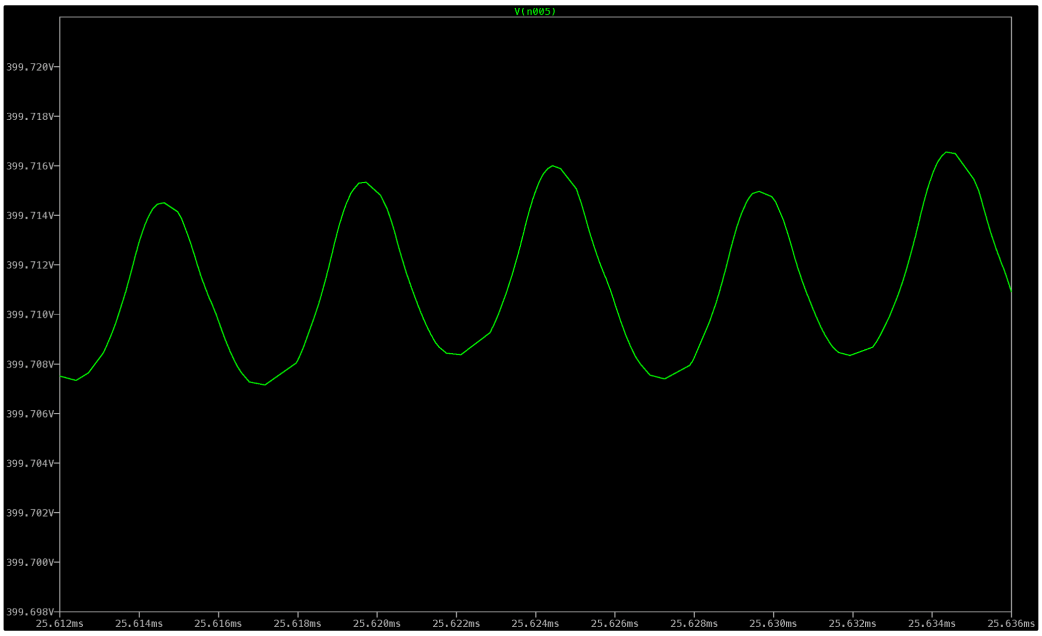


Figure 7.19. Simulation showing the output voltage ripple when the output voltage is 400VDC. The ESR of the output capacitors was assumed to be negligible.

### 7.2.3 Push-Pull PWM Controller Stage Design

The components connected to the LTC3721 were selected based on pin descriptions and other constraints. Table 7.2 summarizes the component selection for the controller. All capacitors connected to the IC were ceramic and selected based upon voltage rating. The resistors were

selected based upon power dissipation and voltage rating. Refer to Appendix I for the bill of materials (BOM) of the isolated design.

Table 7.2. The pin descriptions and components connected to each pin of the LTC3721.

| Pin Name | Pin Description | Pin Configuration in Non-Isolated Design |
|---|---|---|
| $V_{REF}$ | Output of the 5.0V reference. | Connected to DPRG through a 100kΩ resistor to program 115ns deadtime; decoupled to GND with a 1µF ceramic capacitor to deter coupling from nearby traces. |
| DRVA, DRVB | High Speed 1.5A sink, 1A source totem pole MOSFET driver. | Connected to gate pin of IPP200N25N3 MOSFETs. The zero ohm resistors may be supplanted with non-zero resistors to improve the signal integrity of the drive signals. |
| VCC | Supply voltage input to the LTC3721 and 10.25V shunt regulator. | Bypassed VCC to GND with 47µF and 0.1µF ceramic capacitors in parallel for suppressing the voltage ripple and response to fast transients, respectively. The zero ohm resistor may be supplanted with a non-zero resistor to improve the signal integrity of the drive signals. |
| SGND | Signal ground. All feedback and soft-start connections return to this ground. | Connected to ground. |
| PGND | Power ground (return current path for high-power components). | Connects to ground of all input capacitors, output capacitors, and sense resistors. |
| $C_T$ | Timing capacitor for the oscillator. | Connected a parallel circuit of 7pF and 330pF ceramic capacitors to set the switching frequency, $f_{SW}$, to 100kHz, where $f_{SW} = \frac{1}{2(C_T)(14.8k)}$. |
| DPRG | Programming input for Push-Pull dead-time. | Connected to $V_{REF}$ through a 100K ohm resistor. |
| CS | Input to pulse-by-pulse and overload current limit comparators; Output of internal slope compensation circuitry. | Connected to the source of each of the IPP200N25N3 MOSFET through a 100Ω slope compensation resistor. Also indirectly connected to a 1mΩ current sense resistor. It was found that a larger current sense resistor made the 3-phase converter load dependent. |
| COMP | Error amplifier output; | Connected to the FB pin through a compensation |

| | | |
|---|---|---|
| | Inverting input to phase modulator. | network consisting of a 200kΩ resistor and a 0.001µF ceramic resistor. |
| $R_{LEB}$ | Timing resistor for leading edge blanking. | Connected a 100k ohm resistor to ground to program a maximum of 310ns of leading edge blanking on the CS pin to prevent hiccup mode operation. |
| SS | Soft-start timing capacitor. | A 0.1µF ceramic capacitor connected to this pin programs a soft-start time of approximately 3.8ms. |
| FB | Error amplifier inverting input. | The resistors were sized with (6.1) such that the LTC3721 regulates the output voltage converter at 400V. $R2 = 500\Omega$ so that a change in current when the load is connected to the converter does not induce a large change in the output voltage. |
| UVLO | Input to program system turn-on and turn-off voltage. | The UVLO pin was configured such that, at input voltage of 50VDC, the LTC3721 turns on. In practice, it may suffice to utilize a controllable on-board voltage to turn on the IC in each phase. |

## 7.3 Converter Control

As described in Section 3.2.1, the converter must possess the ability to (1) limit the output voltage; (2) limit the input power; and (3) limit the output current per phase. The following subsections detail how these mechanisms were implemented in the isolated design. Before doing so, current mode control operation and its significance for the push-pull topology is discussed.

### 7.3.1 Current Mode Control Operation

Current mode control is a control scheme in which variations in the output voltage indirectly adjust the duty cycle of the converter through alterations of the control current, $i_C(t)$. Commonly, the control current is defined as a compensated version of the current from the output of an error amplifier, as shown in Figure 7.20. $i_C(t)$ is then compared to the instantaneous value of the current traversing through the MOSFETs, $i_S(t)$. In a myriad of applications, $i_S(t)$ is usually defined as the current through the current sense resistor, which was discussed in Section 7.2.3. Under the condition that $i_S(t) < i_C(t)$, the MOSFETs on one of the sides of the primary stage in Figure 7.2 are in the triode region. If $i_S(t) \geq i_C(t)$, the switching terminates, meaning all MOSFETs are off. The relationship between $i_S(t)$ and $i_C(t)$ indicates that current mode controlled converters compare these two currents. The comparison from a high-level block diagram perspective is illustrated in Figure 7.20.

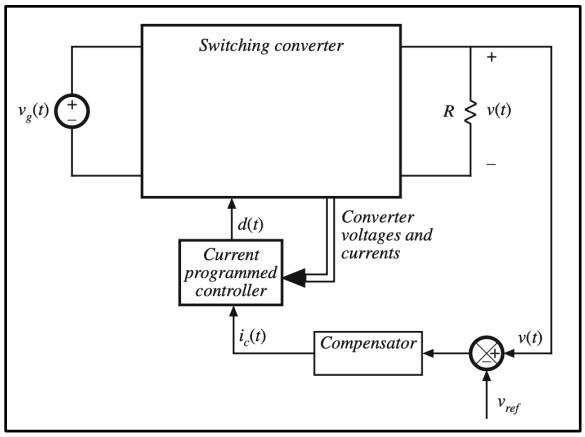


Figure 7.20. High-level block diagram of the current-programmed control. $i_S(t)$ travels through the path labeled "converter voltages and currents" [3].

In Figure 7.20, all blocks below the "switching converter" block and to the left of $v(t)$ can be implemented via an IC. The block diagram for the current mode control IC implemented in the isolated design—the LTC3721—is presented in Figure 7.21.

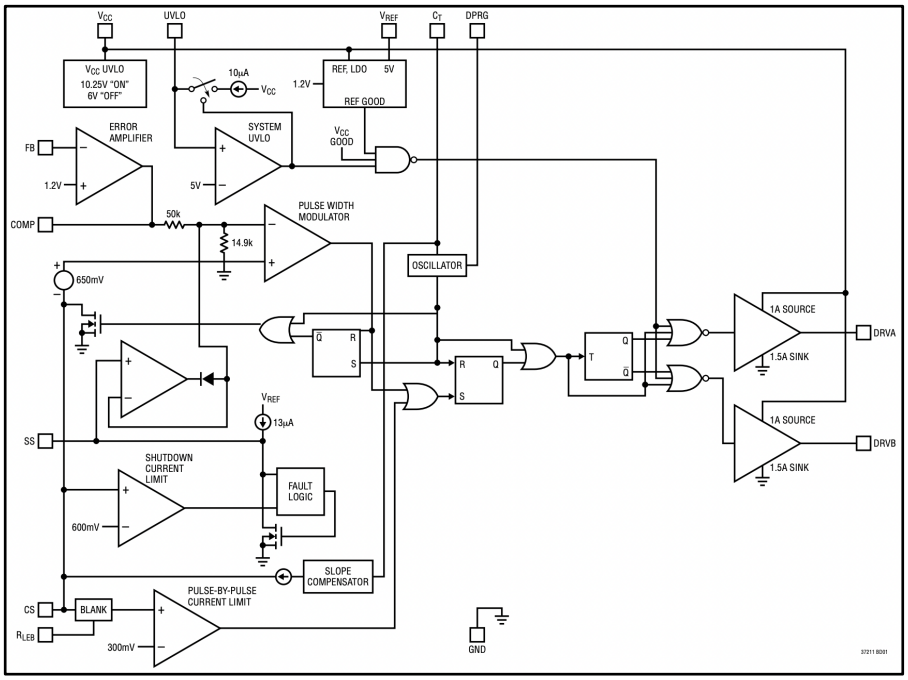


Figure 7.21. Block diagram for the LTC3721 [29].

The LTC3721 operates as follows: first, $i_S(t)$ is converted to a voltage and fed to the CS pin by the external current sense resistor, and the current traversing through the 500Ω FB resistor is converted to a voltage and fed to the FB pin. In steady-state, the voltage on the FB pin with respect to ground is equivalent to a voltage slightly less than 1.2V due to the current drawn from the FB pin. The error amplifier then amplifies the voltage difference between 1.2V and the voltage

on the FB pin, yielding an output voltage potentially as high as the positive supply of the error amplifier (5V). If the output of the shutdown current limit comparator the CS pin connects to corresponds to a logical 0, the output of the pulse width modulator following the error amplifier would also correspond to a logical 0. In turn, the output of the OR gate connected to the pulse width modulator would correspond to a logical 0 as well. Afterwards, the outputs of the edge-triggered SR and T flip-flops are determined by the internal oscillator clock, which outputs a logical 1 every switching period. In the case where $S = 0$ and $R = 1$, $Q$ of the SR flip-flop is 0, further suggesting the output of the OR gate following the SR flip-flop is a 1. Therefore, $T = 1$ and $Q$ and $\underline{Q}$ of the T flip-flop switch logical values. Immediately after, assuming no deadtime programming, the internal oscillator clock relaxes back to a logical 0, yielding $T = 0$, so $Q$ and $\underline{Q}$ retain their new logical values until the next switching period commences. This is why the PWM waveforms alternate as shown in Figure 7.4. With deadtime programming, the OR gates preceding the drivers output a logical 0 so that the duty cycle of the converter is less than 0.5. Similarly, if the 300mV limit is exceeded ($i_S(t) \geq i_C(t)$), switching action halts for the present cycle. If the 600mV limit is surpassed, all switching is terminated and a soft-start sequence is initiated (SS pin).

The importance of the current mode control operation of the LTC3721 for the push-pull converter can be emphasized through a discussion of the magnetizing inductance of the transformer. Due to manufacturing differences, it is highly unlikely that the drain-source voltage drops of the MOSFETs on each side of the primary stage will be equivalent, implying that $\frac{1}{T_s}\int_{T_s} v_T(t)dt \neq 0$, where $v_T(t)$ is the voltage waveform applied to each half of the primary winding and $T_s$ is the switching period [3]. As a result, there can be a net increase in the magnetizing current by the end of every switching period. Eventually, the transformer may saturate and the push-pull converter will no longer behave as intended. Current mode control prevents this from occurring by ensuring that $\frac{1}{T_s}\int_{T_s} v_T(t)dt = 0$ through the current comparison mechanism.

### 7.3.2 Limiting the Output Voltage, Input Power, & Output Current

The output voltage of the isolated converter can be controlled via a DAC connected to the FB pin of the LTC3721 through an appropriately sized resistor, as shown in Figure 7.2.[17] The resistor was sized through an iterative process in LTspice so a DAC output voltage of less than 2.5V–the maximum output of the DAC–could lower the output voltage of the isolated converter to 280V. In particular, for a resistor value of 1.2kΩ, the output voltage of the converter as a function of the DAC output is depicted in Figure 7.22.

[17] Recall that the DAC was modeled as a PWL voltage source in this project.

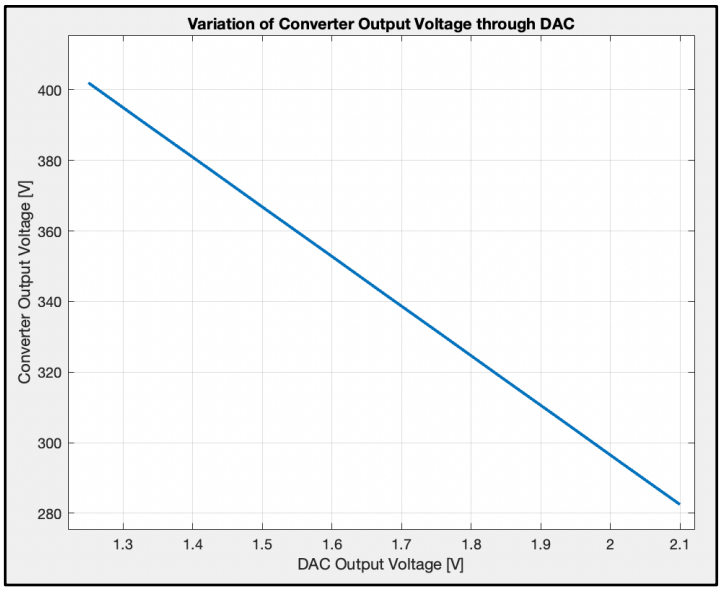


Figure 7.22. Output voltage as a function of the DAC output voltage for a resistor value of 1.2kΩ.

The block diagram of the LTC3721 in Section 7.3.1 reveals why this method is an effective way of controlling the output voltage. As the DAC output voltage increases from 1.25V to 2.1V, a large voltage difference is induced across the 1.2kΩ resistor. Thus, the current traversing through the 1.2kΩ and 500Ω resistors increases.[18] Note that the current from the DAC will be no more than 750µA. Consequently, as the DAC output voltage increases, the increase in current from the DAC through the 500Ω resistor raises the FB voltage slightly. The difference between the voltage on the FB pin and 1.2V is then amplified by the error amplifier in Figure 7.21, as described by the following equation:

$$(1.2V - V_{FB})A_0 = V_{COMP} \qquad \text{(eq. 7.2)}$$

Assuming $A_0$, the gain of the error amplifier, is sufficiently large, voltage differences on the scale of µV can cause the error amplifier to output voltages near its positive supply rail (5V). Thus, it can be inferred that the output of the error amplifier decreases as the DAC voltage increases. For this reason, the LTC3721 regulates at a smaller output voltage than the one set by the resistors connected to the FB pin.

When the output voltage is not being limited by the DAC, the output voltage of the error amplifier can be modified by an integrator cascaded with a comparator to regulate the current from the PEMFC; a current amplifier would precede the cascade. In turn, the output voltage of the converter shifts to the LiPo battery voltage. Limiting the input current in this manner limits the input power and protects the PEMFC from operating in undesirable conditions. To instead limit

[18] Ideally, 0A of current enters the FB pin since the input impedance of an operational voltage amplifier is ideally infinite.

the output current rather than the output voltage or input power to ensure the converter doesn't generate excessive heat, a similar process is followed.

## 7.4 Drawbacks & Concerns

Although the isolated design achieves much of the desired capabilities and specifications Honeywell hoped to achieve, there are a few limitations of the LTC3721 and component concerns that must be addressed.

### 7.4.1 LTC3721 Limitations

If the current waveforms at the output of each phase of the converter are identical and in-phase with one another, the sum of the output current waveforms of each phase will yield a current ripple three times the ripple of the output current from a single phase. This could induce a ripple in the output voltage waveform large enough to reduce the lifetime of the LiPo battery. If the LTC3721 had a synchronization pin that allowed the output current waveforms to be set 120º out of phase with each other, this issue could easily be bypassed. However, the LTC3721 does not possess such a pin. Alternative methods, such as controlling the time each LTC3721 turns on through the UVLO pin, might be too imprecise for this unmanned autonomous vehicle application due to time delays.

Another limitation of the LTC3721 are the transient currents through the VCC pin caused by the 100kHz switching of the MOSFETs and capacitive load on the totem pole drivers in Figure 7.21. The primary reason this phenomenon is a concern is because the VCC pin has an absolute maximum current limit of 40mA, and the current transients attain values as high as 2.5A, as shown in Figure 7.23. Consequently, the LTC3721 is at risk of failure. This issue could be circumvented by adding resistance to the DRVA, DRVB, and VCC pins. In Figure 7.2, 0Ω resistors were added to each of these pins so that when the PCB of the isolated design is constructed and the resistance of the PCB traces determined, the 0Ω resistors could be soldered off and replaced with appropriate resistor values to manage the current transients. Alternatively, the number of MOSFETs on each leg could be reduced to decrease the capacitive load on the totem pole drivers. If heat management becomes an issue after reducing the number of MOSFETs from three, MOSFETs with lower gate-source and gate-drain capacitances could be implemented instead of reducing the number of MOSFETs.

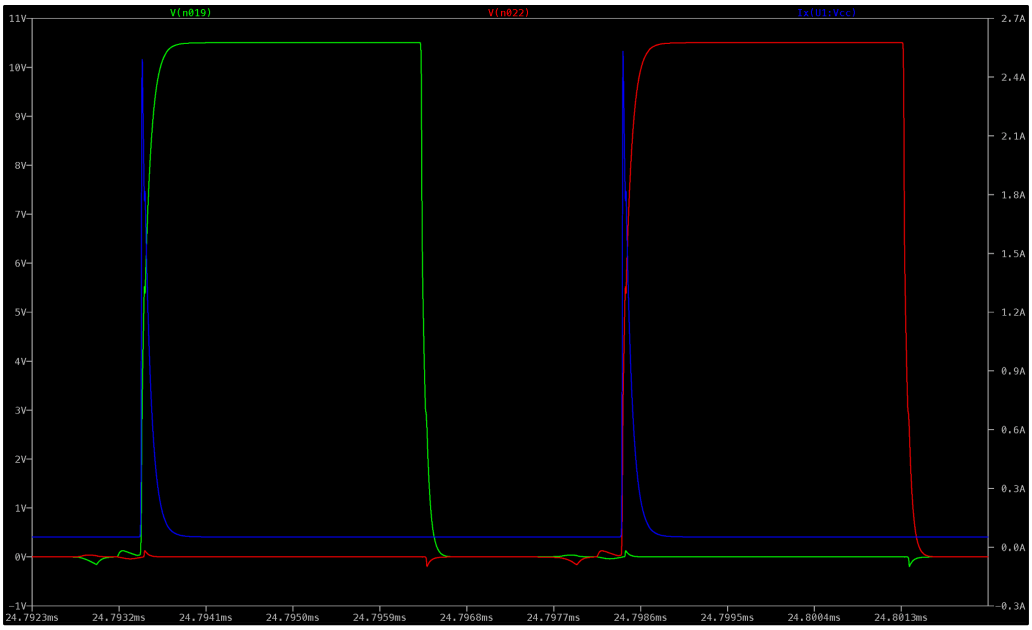


Figure 7.23. Simulation showing the current transients through the VCC pin as the MOSFETs on each leg of the primary stage switch on. The green waveform corresponds to the voltage waveform of DRVA; red to the voltage waveform of DRVB; and blue to the current fed into the VCC pin.

### 7.4.2 Component Ratings

To guarantee that the isolated design operates properly, it is necessary that the absolute maximum ratings of each component are never exceeded. Otherwise, the isolated design will no longer function as intended. One of the components of concern is the DCDC2400-001 transformer. According to the datasheet, the DCDC2400-001 transformer is recommended for DC/DC converter application where the input voltage of the converter ranges from 16VDC to 32VDC and the output is 400VDC. In our unmanned autonomous vehicle application, the input voltage ranges from 50VDC to 100VDC. Although the datasheet specifies that the transformer was designed based on AEC-Q200 standards–meaning the transformer was designed to withstand harsh temperature conditions–the transformer may yet saturate for input voltage sufficiently larger than the specified range.[19] If the transformer saturates, the reluctance of its core will become exceedingly large, and it will lose its ability to store magnetic field energy. Therefore, the push-pull converter will no longer behave as intended.

In addition to the DCDC2400-001 transformer, the ratings of the diodes, inductor, and MOSFETs may also be cause for concern. According to the datasheet of the VS-E5PX6012 diode, the maximum junction temperature is 175ºC, and the thermal resistance of its package, the TO-247AD 2L, is 0.4ºC/W; this implies the package can withstand up to 180W of power dissipation if the case temperature is 100ºC. In practice, the junction-to-ambient thermal resistance will

[19] To see why a sufficiently large DC input to the push-pull converter can cause the DCDC2400-001 to saturate, refer to Appendix E.

impose an upper limit on the power dissipation in the diode. If needed, this problem can quickly be resolved by placing at least two more diodes in parallel for each diode in Figure 7.1, or purchasing a suitable heat sink.

Of more concern is the output inductor. As shown in Appendix I, the output inductor selected was the CPEX3635L-111MC inductor from CODACA.[20] This inductor was designed for frequencies as large as 1MHz, currents as large as 24A before core saturation, and a maximum DC resistance of 7.41mΩ to minimize power losses; however, the maximum voltage rating was not specified. Since the maximum voltage applied to the inductor from the diode stage is 1200V and the minimum output voltage of the converter is 280V, the voltage rating of the inductor must be at least 1000V. Another inductor which could be implemented is the SCR25XV-350-2R4A003JV, a common-mode choke which is rated for voltages up to 1000V.[21] However, the properties of the choke deviate from the properties of an ordinary inductor, meaning the simulated results in LTspice may significantly deviate from waveforms observed in the laboratory unless an appropriate model is procured.

With regards to the MOSFETs, the large pulse of current shown in Figure 7.12 through a single MOSFET in the isolated design during startup may damage the MOSFET, despite the duration of the pulse being much less than 1µs. In practice, such a transient may not occur due to the discrepancies between reality and the models utilized for the components in LTspice; however, to ensure design robustness, the pulse still warrants attention.

## 7.5 Simulation Test Results

As explored in Chapter 8, the isolated design was judged as a more feasible design than the non-isolated design. Accordingly, the isolated design progressed to the next stage of the design process. Sixteen simulation tests were performed on the isolated design to evaluate its transient response, efficiency, and average component power dissipation in steady-state under various circumstances. The average power dissipation during transients was neglected due to discrepancies between the PEMFC and voltage source, as mentioned in Chapter 5.

The graphs of the transient response and setup for each test can be found in Appendix F. Table 7.3 provides a succinct description of each test, Table 7.4 a numerical summary of the transient behavior and stability for each test, and Table 7.5 a quantitative description of the power considerations for outputs of (280V, 11A) and (400V, 8A). The power dissipated in each component is less than the power dissipated in all other output operating points.

Table 7.3. Description for each test performed in LTspice.

| Test Number | Test Description |
|---|---|
| 1 | Load transient at 400VDC output – 8A to 0.5A load current. |

[20] Refer to Appendix J for the CPEX3635L-111MC datasheet.

[21] Refer to the datasheet of the MIC3808/9 for an example on how to implement a choke in a push-pull converter. Additionally, if desired, refer to the datasheet of the SCR25XV-350-2R4A003JV.

| | |
|---|---|
| 2 | Load transient at 400VDC output – 0.5A to 8A load current. |
| 3 | Load transient at 280VDC output – 11A to 0.5A load current. |
| 4 | Load transient at 280VDC output – 0.5A to 11A load current. |
| 5 | Output voltage transient for 50Ω load resistance – 400VDC to 280VDC output voltage. |
| 6 | Output voltage transient for 800Ω load resistance – 400VDC to 280VDC output voltage. |
| 7 | Output voltage transient for 50Ω load resistance – 280VDC to 400VDC output voltage. |
| 8 | Output voltage transient for 800Ω load resistance – 280VDC to 400VDC output voltage. |
| 9 | Input voltage variation for 50Ω load resistance and 400VDC output voltage – 50VDC to 100VDC input voltage. |
| 10 | Input voltage variation for 800Ω load resistance and 400VDC output voltage – 50VDC to 100VDC input voltage. |
| 11 | Input voltage variation for 50Ω load resistance and 400VDC output voltage – 100VDC to 50VDC input voltage. |
| 12 | Input voltage variation for 800Ω load resistance and 400VDC output voltage – 100VDC to 50VDC input voltage. |
| 13 | Input voltage variation for 25.45Ω load resistance and 280VDC output voltage – 50VDC to 100VDC input voltage. |
| 14 | Input voltage variation for 560Ω load resistance and 280VDC output voltage – 50VDC to 100VDC input voltage. |

| | |
|---|---|
| 15 | Input voltage variation for 25.45Ω load resistance and 280VDC output voltage – 100VDC to 50VDC input voltage. |
| 16 | Input voltage variation for 560Ω load resistance and 280VDC output voltage – 100VDC to 50VDC input voltage. |

Table 7.4. Numerical summary of the transient behavior for each test performed in LTspice.

| Test Number | Summary of Transient Behavior | Stability |
|---|---|---|
| 1 | When the load current transitioned from 0A to 8A, the transients decayed after 2ms and an undershoot of approximately 2V occurred. From 8A to 0.5A, the transients decayed after about 2ms and there was an overshoot of 230mV followed by an undershoot of 100mV. | Stable due to no ringing on the COMP pin. |
| 2 | When the load current transitioned from 0A to 0.5A, the transients decayed after 8ms and an undershoot of approximately 600mV occurred. From 0.5A to 8A, the transients decayed after about 1.2ms and there was an undershoot of 300mV. | Stable due to no ringing on the COMP pin. |
| 3 | When the load current transitioned from 0A to 11A, the transients decayed after 1.6ms and an undershoot of approximately 2.1V occurred. From 11A to 0.5A, the transients decayed after about 2ms and there was an overshoot of 300mV followed by an undershoot of 170mV. | Stable due to no ringing on the COMP pin. |
| 4 | When the load current transitioned from 0A to 0.5A, the transients decayed after 9ms and an undershoot of approximately 600mV occurred. From 0.5A to 11A, the transients decayed after about 1ms and there was an undershoot of 400mV. | Stable due to no ringing on the COMP pin. |
| 5 | When the 50Ω load was connected to the converter, the transients decayed after about 2ms and an undershoot of 1.8V occurred. After the output voltage transitioned from 400V to 280V, the transients decayed after 2ms and an undershoot of 1.6V transpired. | Stable due to no ringing on the COMP pin. |
| 6 | When the 800Ω load was connected to the converter, the transients decayed after about 8ms and an undershoot of 600mV occurred. After the output voltage transitioned from 400V to 280V, the transients decayed after 4ms and an undershoot of 500mV transpired. | Stable due to no ringing on the COMP pin. |
| 7 | When the 50Ω load was connected to the converter, the transients | Stable due to |

| | | |
|---|---|---|
| | decayed after about 2ms and an undershoot of 1.6V occurred. After the output voltage transitioned from 280V to 400V, the transients decayed after 1.5ms and an overshoot of 2V transpired. | no ringing on the COMP pin. |
| 8 | When the 800Ω load was connected to the converter, the transients decayed after about 12ms and an undershoot of 500mV occurred. After the output voltage transitioned from 280V to 400V, the transients decayed after 9ms and an overshoot of 2V transpired. | Stable due to no ringing on the COMP pin. |
| 9 | When the input voltage increased from 50V to 100V, there was no change in the output voltage waveform. | Stable due to no ringing on the COMP pin. |
| 10 | When the input voltage increased from 50V to 100V, there was no change in the output voltage waveform. | Stable due to no ringing on the COMP pin. |
| 11 | When the input voltage increased from 100V to 50V, there was no change in the output voltage waveform. | Stable due to no ringing on the COMP pin. |
| 12 | When the input voltage increased from 100V to 50V, there was no change in the output voltage waveform. | Stable due to no ringing on the COMP pin. |
| 13 | When the input voltage increased from 50V to 100V, there was no change in the output voltage waveform. | Stable due to no ringing on the COMP pin. |
| 14 | When the input voltage increased from 50V to 100V, there was no change in the output voltage waveform. | Stable due to no ringing on the COMP pin. |
| 15 | When the input voltage increased from 100V to 50V, there was no change in the output voltage waveform. | Stable due to no ringing on the COMP pin. |
| 16 | When the input voltage increased from 100V to 50V, there was no change in the output voltage waveform. | Stable due to no ringing on the COMP |

| | | |
|---|---|---|
| | | pin. |

Table 7.5. A quantitative summary of the power considerations for outputs of (280V, 11A) and (400V, 8A) in steady-state. Please note, the average power dissipation, not instantaneous power, was tabulated. The ESR of the aluminum capacitors was assumed to be 100mΩ. For the calculations, the RMS current was measured in LTspice.

| **Output Voltage & Load Current** | **Measured Efficiency** | **Measured Average Dissipation Per Diode** | **Measured Average Dissipation Per MOSFET** | **Calculated Current Sense Resistor Dissipation** | **Calculated Aluminum Input Capacitor Dissipation** | **Calculated Aluminum Output Capacitor Dissipation** |
|---|---|---|---|---|---|---|
| (400V, 8A) | 98% | 2.6W | 1.51W | 1.1W | 0W | 65mW |
| (280V, 11A) | 97% | 3.3W | 1.9W | 1.3W | 0W | 100mW |

# 8. Assessing the Designs

The two converters discussed in the previous two chapters were compared and contrasted to determine which converter is more suitable for our intended application.

## 8.1 Comparing the Designs

On their own, the non-isolated and isolated designs hold attributes which either enhance or diminish their feasibility for our intended application. Table 8.1 and 8.2 distinguish between the advantages and disadvantages of each converter for our application.

Table 8.1. Advantages and disadvantages of the non-isolated design with respect to our intended UAV application.

| **Non-Isolated Design** | |
|---|---|
| **Advantages** | **Disadvantages** |
| • Resistance to input voltage transients up to 40V<br>• Avoids bulky transformers<br>• Mechanism for limiting the input power and output current (Ith pin) | • Efficiency below 80%<br>• Load dependency<br>• Complexity<br>• Power dissipation in AC/DC diodes<br>• No mechanism for direct digital control of the output voltage<br>• Power dissipation in flying capacitors |

Table 8.2. Advantages and disadvantages of the isolated design with respect to our intended UAV application.

| **Isolated Push-Pull Design** | |
|---|---|
| **Advantages** | **Disadvantages** |
| • Efficiency of 98%<br>• Simplicity<br>• Less sensitive to noise<br>• Mechanism for direct digital control of the output voltage, output current, and input power<br>• Satisfactory transient behavior<br>• Compatibility with output chokes for EMI purposes | • Phases are not synchronized<br>• Use of transformer (substantially increases weight)<br>• Limitation to how small the drain-source resistance of a MOSFET can be<br>• Power dissipation in secondary stage diodes<br>• Output inductor voltage rating of 1000V |

## 8.2 Design Selection Rationale

The previous section made it apparent that both designs have advantages and disadvantages for the intended application. The severity of the drawbacks determined which design proceeded to the PCB layout and testing phases.

Although a distinguished advantage of the non-isolated design is its much lighter weight independent of any heat sinks, the low efficiency and load dependency make it a less practical choice. The low efficiency of the converter may cause components–such as the MOSFETs in the DC/AC stage–to fail, unless a sufficiently large heat sink or thermal paste can be attained. In some cases, the heat sink could be so large that the overall mass of the non-isolated design (mass of the converter plus cooling equipment) becomes larger than the isolated design. Thus, this disadvantage could cause the non-isolated design to partially fail design criterion 1 and completely fail criterion 9.

The load dependency disadvantage of the non-isolated design could be overcome through the construction of a control system which regulates the output of the charge pump. However, such a task may be unnecessary due to the vast array of ICs available which may be more feasible and robust for our application, such as the PWM controller of the isolated design.

Unlike the non-isolated design, most of the disadvantages of the isolated design can be resolved by practical methods. In the isolated design, for example, the lower limit on the drain-to-source resistance of an individual MOSFET can be decreased by increasing the inductance of the output inductor, or decreasing the input and output capacitance. Furthermore, the required voltage rating of the output inductor can be decreased to 600V by replacing the DCDC2400-001 transformer with a 1+1:8 push-pull transformer. Subsequently, the transformer weight would be reduced. Increasing the switching frequency of the converter would further reduce the weight of the transformer. The power dissipation in the secondary stage diodes can be managed through an appropriate heat sink, several VS-E5PX6012 diodes can be placed in parallel, or every two VS-E5PX6012 diodes in series can be replaced with a single QRS1420T30 diode. Lastly, if an adequate synchronization method is not designed, the phases could be synchronized by replacing the LTC3721 with a similar IC which allows for synchronization.

Due to the disadvantages of the non-isolated design described in Table 8.1, the isolated design was selected to proceed to the next phase of the design process.

## 8.3 Compliance of Selected Design with Design Criteria

After selecting the isolated design to proceed to the PCB layout and testing phases, it was crucial to determine if the design complied with the majority of the design criteria. Table 8.3 showcases the results. The satisfaction of each criterion is based on simulated results from LTspice.

Table 8.3. Compatibility of the isolated design for our intended UAV application.

| Criterion | Satisfaction | Justification |
|---|---|---|
| 1 | Satisfied | The isolated design is capable of supporting a digital control system through the manipulation of the voltage waveforms on the FB and COMP pins of the LTC3721 independently, not simultaneously. The input power–and thereby input current and |

| | | |
|---|---|---|
| | | voltage of the PEMFC–can be limited with an integrator cascaded with a comparator from the input to the COMP pin. A current amplifier would precede the cascade. Indirectly, this also limits the output current. The maximum output voltage can be limited through a DAC connected to the FB pin. At maximum power and a maximum output voltage of 400V, the converter has an efficiency of 98%. At 280V and at the MPP, the efficiency of the converter is 97%. However, some component ratings may be exceeded at the maximum input voltage and MPP (see Section 7.4). Despite this, other components which did not have LTspice models and mentioned in Chapter 7 are rated for voltages and currents beyond what is expected to occur in reality for our three-phase design. Hence, this criterion can be considered as satisfied. |
| 2 | Satisfied | The isolated design can be limited to the specified minimum values through the same manner described in the justification of criterion one. Evidently, the converter can also withstand all minimum values. |
| 3 | Satisfied | As shown in Figure 7.3, there is never a state in each switching period when the LiPo battery is delivering power to the PEMFC. Hence, the converter is unidirectional. |
| 4 | Satisfied | Based on the results in Appendix F, a 1ms change of the input voltage from 50V to 100V or vice versa elicits no observable change in the steady-state output voltage. Since a 1ms change is likely significantly quicker than what the PEMFC can tolerate before hydrogen starvation, this criterion is satisfied. |
| 5 | Further Investigation Required | According to LTspice, the input current waveform of the isolated design is a triangular waveform which ranges from 0A to 75A every half switching period, as alluded to by Figure 7.16. LTspice predicts 0A because it doesn't model the magnetizing inductance of the transformer. As such, during states two and four in Figure 7.3, the input current reduces to 0A. Testing the converter in the lab or developing a more realistic transformer model will allow for the determination of the satisfiability of this criterion. |
| 6 | Satisfied | As evidenced by the graphs in Appendix F, the output voltage ripple when steady-state is achieved is negligible for various load resistance or current values. As a result, the ripple of the current waveform must also be negligible in accordance with Ohm's law. If the E91D501VND561MA80U capacitors are simulated instead with their ESR, the output voltage ripple remains below 800mV for all operating conditions. |

| | | |
|---|---|---|
| 7 | Satisfied | The LTC3721 is capable of switching the MOSFETs at frequencies as high as 500kHz [29]. Any higher, and the gain of the internal error amplifier will diminish. Since the switching losses can become much larger than the conduction losses for frequencies larger than 500kHz, it is unlikely that the converter will need to be modified for frequencies beyond 500kHz. If the frequency of the converter is increased, components will need to be reselected. Additionally, soft-switching techniques can be implemented in the push-pull topology [34]. |
| 8 | Satisfied | The isolated design is capable of providing a maximum voltage gain of 12, but can be configured to provide smaller voltage gains by correctly selecting the resistors connected to the FB pin of the LTC3721. Table 7.5 displays that the minimum efficiency of the converter is 97%. |
| 9 | Not Satisfied | Predictably, the isolated design did not achieve the ideal power density of 62 kW/kg. Instead, it achieved a power density of approximately 1.8 kW/kg (3.25kW divided by 1800g). As a result, the converter is likely not suitable for a UAV application, but could still be appropriate for ground or undersea vehicles. |
| 10 | Further Investigation Required | Conducted and radiated emissions were not investigated in detail over the course of the project. Although the transformer may assist in suppressing EMI emissions, and the possible implementation of the SCR25XV-350-2R4A003JV choke may further curtail emissions, an analysis of the converter in a laboratory setting would be a more appropriate methodology for determining the satisfiability of this criterion. |

# 9. Altium Schematic & PCB Layout

After choosing the isolated push-pull converter design as our final design, we aimed to build a PCB prototype of our converter. Initially, we planned to fast track our converter design in order to have enough time to reach the PCB layout and testing phase of the project. However, our struggle to find a suitable PWM controller and reasonably sized transformer hindered our progress significantly. In the next few sections, we will discuss our PCB progress and provide recommendations for continued development of the board, while incorporating previously conducted research.

## 9.1 PCB Development of Our Unmanned Autonomous Vehicle Converter

The design of a PCB involves following four major steps:

1. Component Selection
2. Altium Schematic Design and Review
3. PCB Layout
4. Prototyping and Testing

We used Altium to design our PCB, as Honeywell was already familiar with the software program and provided us with training videos. We were able to complete steps 1 and 2, partially complete step 3, but did not complete step 4. With that said, having both the schematic and BOM at disposal gives engineers the ability to develop and test the board in any PCB design software. In the following sections, we will delve deeper into the component selection and schematic design.

### 9.1.1 Component Selection and Placement

As outlined, the first step was to select the components for our Altium schematic based on our simulations with LTspice. Section 2 of Chapter 7 extensively details the process used to select the components for our converter. DigiKey was mostly utilized due to its precise parameters and filtering options. However, we also relied on electronic part search engines like Octopart and Findchips to come across harder-to-find parts and to broaden the pool of parts to choose from.

To prevent significant changes in our converter's performance in real circumstances, we made a considerate effort to use the same components as our LTspice circuit, especially when dealing with high-power components such as MOSFETs, transformers, inductors, and diodes. For other components, such as fixed resistors and capacitors, we selected those with the largest inventory. This ensures most components will be in stock whenever the prototype is designed. In addition, these components were carefully selected to have a power rating of at least 20% higher than what was measured in the simulations for safety reasons.

After selecting all the components, we created a schematic library. Each component was imported through the built-in manufacturer part search and then drawn manually. This gave us all of the necessary components to start the construction of our Altium schematic.

### 9.1.2 Schematic Design and Review

The LTC3721-1 IC was drawn to match the LTspice chip layout to ensure consistency throughout our schematics and minimize errors. We also chose to use pads to represent our input, output, and DAC to clarify the external pins of our schematic. In addition, we thickened some of the wires to indicate the path of high-power flow, as shown in Figure 9.1. The BOM can be found in Appendix I.

Once we completed the construction of the schematic, we set up a schematic review with Honeywell, where we assessed and improved the schematic among experienced engineers before we progressed to the next design phase. We examined the schematic for errors and compliance with design requirements. Minor changes to the schematic were made, such as bolding the power flow path and certain components—C13 and R8. To give a more detailed overview of the design process to Honeywell, Chapter 7 was used to explain the reasoning behind many decisions, such as component selection and design choices.

After receiving approval from Honeywell, we moved onto creating the PCB footprint. Many of the component footprints were downloaded from Altium's built-in library to expedite the process. Although, we did manually create the through-hole ceramic capacitors and 110µH inductor. However, progress in this stage was limited due to time constraints. Therefore, we were unable to verify the accuracy of the footprints.

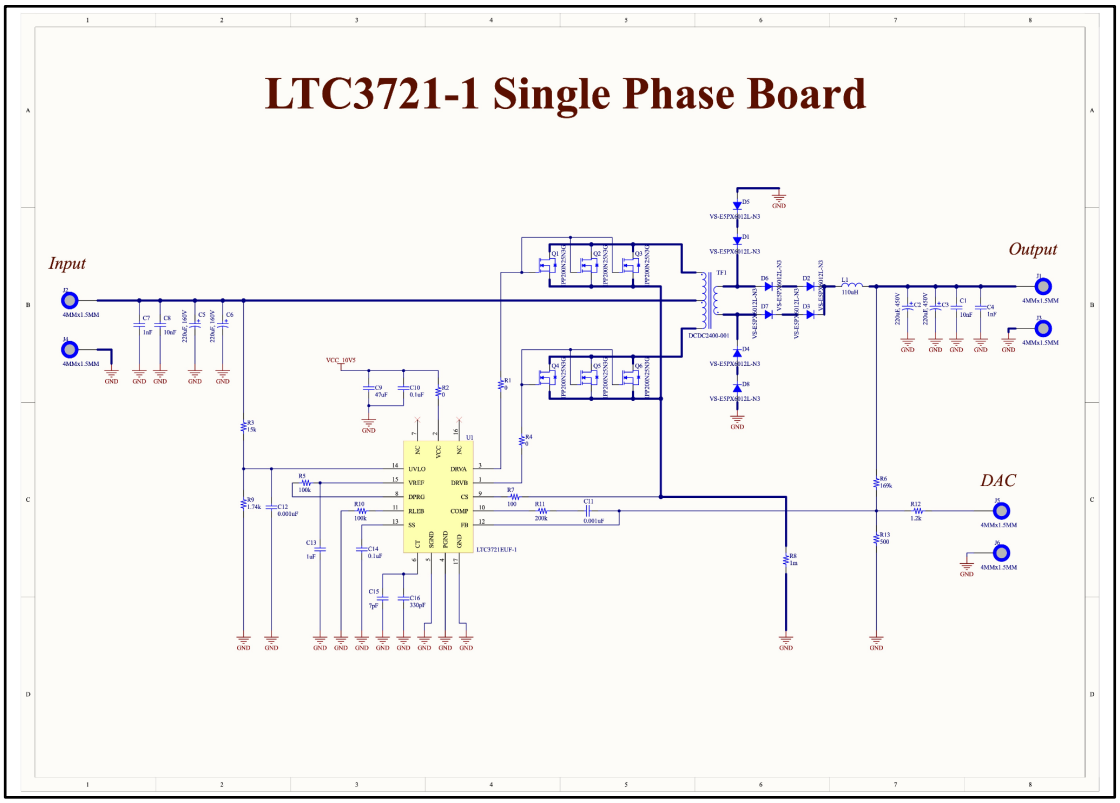


Figure 9.1. Schematic of the isolated push-pull boost converter in Altium for a single phase.

## 9.2 Research and Layout Considerations

In addition to converter size restrictions, we encountered two main issues to investigate,

relating to the PCB design: (1) the high current handling and (2) the effects of parasitic inductance and capacitance.

### 9.2.1 Issue One: High Current Handling

Failure to address high-current handling can lead to overheating, voltage drops, and component failures. Therefore, the implementation of proper design strategies to manage high currents is crucial for ensuring safe and efficient converter operation. To mitigate this issue, we learned about copper weight and area, as well as thermal limitations.

An efficient method to withstand higher currents is to widen the trace and increase the thickness of copper in the trace. In addition, the trace length should be as short as possible to reduce resistance and diminish power losses. Finally, multi-layer wiring can be utilized to shunt large currents, as suggested by Honeywell, avoiding the need for excessively thick copper wire.

To address thermal limitations, we found that most recommendations call for the PCBs temperature rising limit to be set between 10 and 20 degrees Celsius. However, this is not very realistic with large currents. Honeywell's prior experience designing PCBs for DC/DC converters indicates that these boards may tolerate temperatures rising as high as 80 degrees Celsius. Nevertheless, heat dissipation strategies are still necessary. Using a polygon pour to create a wide area of copper on one or both sides of the board is an effective way to dissipate heat. The copper acts as a heat sink, spreading and radiating heat away from the components, which also helps reduce EMI and improve electromagnetic compatibility (EMC) [21].

### 9.2.2 Issue Two: Effect of Parasitic Inductance & Capacitance

The fundamental problem with capacitance and parasitic inductance in high-current PCB designs is that they can lead to ringing, voltage spikes, and EMI. Parasitic inductance can lead to voltage spikes during high-current switching, while parasitic capacitance can worsen ringing, leading to noise and EMI problems. This can be mitigated by adding external circuitry, such as an EMI filter or a decoupling capacitor. The following techniques could also help improve the PCB design:

- Maximize ground area
- Increase the spacing of the trace to reduce interference caused by capacitive coupling
- Increase the width of the power and ground wires to reduce the resistance

## 9.3 Altium Schematic Recommendations & PCB Layout Plan

We have several recommendations regarding the Altium schematic and how to complete the PCB layout. These recommendations were derived from the LTC3721 and IPP200N25N3 datasheets, our previous experience in related fields, and our meetings with our sponsor, Honeywell.

### 9.3.1 Recommendations for Our Altium Schematic

The following is a list of recommendations for improvement of our schematic in Altium:

- The pads in Figure 9.1 are not suited to withstand large currents at the input and output. Therefore, we advise replacing these pads with PCB interfaces or binding posts.

- We recommend revisiting the PCB footprint for each component to ensure that they meet specifications, especially for the through-hole ceramic capacitors and 110µH inductor since these are made manually.
- Potentially integrate a fuse in the power path–the power path is bolded in Figure 9.1–to safeguard against possibly excessive currents during startup.
- If desired, implement a ballast resistor at the source of each MOSFET to approximately equalize the current sharing.

### 9.3.2 PCB Layout Plan for a Single Phase

The following is a list of recommendations for the PCB layout of a single phase of our converter:

- Strategically place the components to minimize current loop area, thus reducing EMI and the influence of parasitic inductance and capacitance (since trace length is kept minimum). Additionally, implementing a solid ground plane could minimize ground loop areas since currents travel along the path of least impedance.
- Keep the trace connecting the FB pin to the output of the converter as short as practical and route it away from potential noise sources, such as the MOSFETs, diodes, and the inductor. This could prevent instability and large fluctuations in the output voltage waveform of the converter.
- The voltage across the output inductor can be as large as 920V; the diode can ideally have a maximum of 600V; the MOSFETs can have a maximum of 200V. Consequently, creepage and clearance distances according to the Institute for Printed Circuit (IPC) standards should be strictly adhered to.
- To withstand the high voltages, PCB materials such as polyimide, grades of FR4, or other materials with high voltage breakdown ratings should be utilized.
- Make the PCB traces from the DRVA and DRVB pins to the gates of the MOSFETs as short as practical to preserve the integrity of the drive signals. Additionally, a short PCB trace should be used when connecting the 47µF (C9) and 0.1µF (C10) capacitors to VCC and GND.
- The influence of the parasitic trace inductances on the primary side of the DCDC2400-001 may reflect to the secondary side of the converter. Eliminate this behavior by putting a large copper plane–starting from the diodes–in parallel with a ground plane. The forward and return currents will then pass each other in opposite directions, eliminating the parasitic inductance on the secondary side and enabling equal current sharing among the output electrolytic aluminum capacitors.
- Utilize a sufficiently wide trace for the power path of each phase to withstand 22A of current (assuming 3 phases); however, the width should not be made so large as to inadvertently create an E-field antenna, particularly at the switching node.
- Dedicate a sufficiently large copper area drain connection to each MOSFET to lower the junction-to-ambient thermal resistance.[22] A cooling area of sufficient magnitude should also be reserved for each diode for the same reason. As a safety measure, thermal paste should also be applied.

[22] Assuming an epoxy PCB FR4, the copper area should be greater than or equal to $6cm^2$ since this halves the junction-to-ambient thermal resistance of the IPP200N25N3.

- Implement test points along the power path to facilitate testing and debugging. The same should be done for critical signals of the LTC3721, such as the DRVA, DRVB, CS, SS, VCC, and COMP pins.
- We also recommend adding a Kelvin connection, also known as four-terminal sensing (4T sensing), to achieve highly accurate measurements of smaller resistance values, such as the 1mΩ current sense resistor. Otherwise, the results from the equipment used to measure resistance in the laboratory will be corrupted by the resistance of the pads.

# 10. Conclusion & Recommendations

The following sections detail the conclusion and recommendations for future iterations of the project.

## 10.1 Conclusion

Throughout the course of this project, we explored various converter types, researched and simulated many components, and developed multiple schematics. Ultimately, the isolated push-pull converter design was selected. Our design process began with research into discrete components to build a converter from scratch, then moved into an investigation of different ICs to design around. The isolated push-pull converter, detailed in Chapter 7, was the more feasible design due to its higher efficiency, and overall better performance with our 16 simulation tests.

From this research and design process, we were able to provide Honeywell with a schematic of a three phase converter, a review of our design process, and a baseline for future research and development. Additionally, we performed a schematic review with Honeywell that focused on a single phase of our final design to fine-tune the converter as much as possible without lab-testing. Although our project did not make it to the PCB design and testing stage, we still researched PCB design and began a rough layout. More details on our progress in PCB layout can be found in Chapter 9.

Over the course of the year, we determined the most feasible converter option in the given timeframe was the isolated push-pull converter design, and provided detailed schematic and simulation test results to back up this claim. However, we recognize that with more time and resources, our converter could be improved, or different converter designs could be explored to develop a more feasible design. The following section provides more insight into our project's shortcomings, as well as opportunities for further improvement to the converter.

## 10.2 Recommendations

The final version of the isolated design produced satisfactory simulation results, as can be seen in Section 7.5 and Appendix F. Despite this, there are several improvements which could be made to strengthen the practicality of the converter.

### 10.2.1 Further Investigate Non-Isolated Topologies

Even though we ultimately chose the isolated push-pull boost converter topology as our final design, there are other design possibilities available, such as non-isolated converters. Our attempt at designing a non-isolated topology for the intended UAV application is discussed in Chapter 6. The key advantage of non-isolated converters is that they do not require transformers, making the product lighter and more compact. Non-isolated topologies may also have fewer power conversion stages and losses than isolated topologies.

Our brief investigation of a DC/DC converter controller served as an excellent illustration of an IC that can be designed as non-isolated topologies—the LT3758A. Four different topologies can be set up with the LT3758A: the boost, flyback, SEPIC (Single-Ended Primary Inductor Converter), and inverting converters. The controller has an input voltage range of 5.5V to 100V. We investigated the practicality of the LT3758A as an additional IC which could potentially satisfy the constraints of our application.

Even while the LT3758A displayed a number of positive qualities, particularly in terms of weight, we encountered significant problems with power dissipation. Questions concerning thermal management and overall efficiency were raised due to the noticeably high power dissipation of the inductor, diode, and MOSFETs. For example, in the circuit depicted in Figure 10.1, the power dissipation of one of the MOSFETs measured up to 29W. We chose the LTC3721 isolated design because it offered greater performance in terms of thermal characteristics and power efficiency, and more closely suited the objectives and constraints of our project.

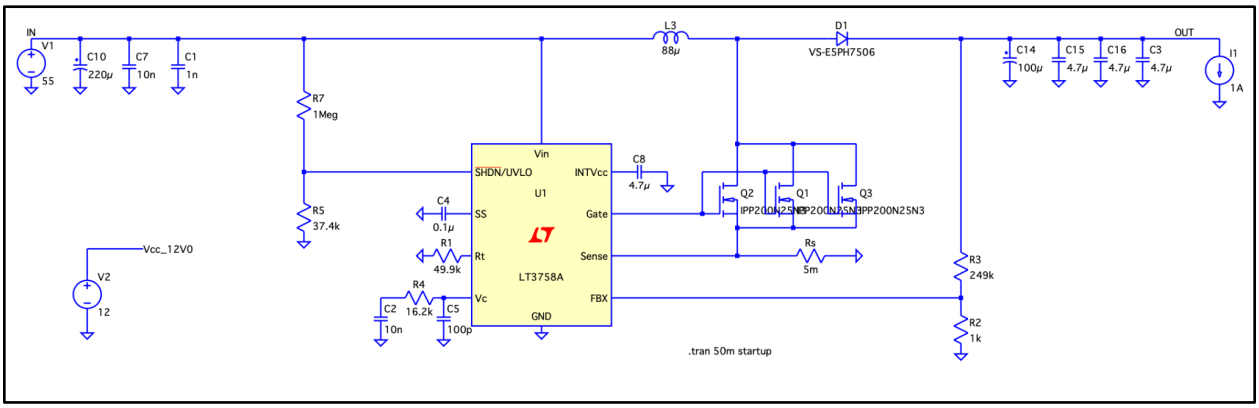

Figure 10.1. LTC3758A configured as a boost converter and delivering 400W of power.

Despite our IC choice, we suggest that future studies investigate developments in non-isolated topologies, such as the LT3758A, with an emphasis on addressing power dissipation issues. Looking into possible methods to improve efficiency and lessen heat stress in these components could reveal viable substitutes for similar applications.

### 10.2.2 Consult a Magnetics Company for a More Practical Transformer

Although the simulation results presented in Appendix F indicate that the DCDC2400-001 transformer is a suitable component for our UAV application, it has drawbacks which may degrade the functionality of the isolated design in practice. For instance, the 1+1:12 turns ratio of the DCDC2400-001 makes the maximum voltage across the output inductor 920V when the input voltage is 100VDC and the output is 280VDC (refer to Section 7.4.2 for more details). Thus, the output inductor must be capable of withstanding 1000V, and the diodes need to tolerate a reverse voltage of at least 1200V; this increases the difficulty of component selection and compliance with IPC standards. These challenges could be addressed by utilizing a transformer with a lower turns ratio. The minimum turns ratio for our application is 1+1:8 (see design criterion 8). A tradeoff to utilizing a 1+1:8 transformer is the current passing through each component on the secondary side of the transformer increases by a factor of 1.5, so the power dissipation in each secondary component increases by a factor of 2.25 (see Table 7.5 for the present part thermals). The excess power dissipation may be manageable by a heat sink of reasonable proportion.

The transformer ratings of the DCDC2400-001 may also limit the converter's practicality. The frequency rating of the DCDC2400-001 is 100kHz, which makes reducing component size or decreasing the inductor current ripple of the converter by increasing the switching frequency unlikely. For example, given the following parameters, the output inductor needs to be at least 1 mH (refer to Appendix D for the output inductor equation):

- Inductor current ripple of 1A

- Input voltage of 50VDC
- Output voltage of 400VDC
- Fixed frequency at 100kHz

Such a large inductance value could significantly increase the weight of the converter, further diminishing its practicality. Furthermore, any attempts to circumvent the tradeoffs of a 1mH inductor by reducing the number of phases of the isolated design to 1 can't be accomplished since the DCDC2400-001 is rated for 2kW, not up to 3.25kW. Lastly, as detailed in Section 7.4.2, the recommended rating of the DCDC2400-001 exceeds the input voltage specification of our application, suggesting that the transformer may saturate (see Appendix E).

As a result of the limitations described in this section, it is recommended that Honeywell consult a magnetics company that specializes in high-frequency, high-power density, and high-efficiency magnetics design. Thereafter, the magnetics company may be able to design a custom transformer tailored to the needs of this application.

### 10.2.3 Synchronize Each Phase of the Push-Pull Converter

Our team investigated the possibility of utilizing an integrated phase locked loop (PLL) circuit to synchronize the LTC3721 ICs in each phase of the isolated design with a 120º phase shift for each output current waveform. The PLL ensures that the phase of the waveform delivered to the converter does not change. This would minimize the ripple of the current delivered to the battery under various operating conditions, as described in Section 7.4.1. In theory, for every LTC3721 IC, there would be an external PLL IC that would connect to the UVLO pin of the LTC3721. Furthermore, an integrated oscillator circuit–such as the LTC6902 mentioned in Section 6.2.5—would provide a reference signal to each PLL so the waveforms in each phase are offset by 120º relative to one other. In practice, assuming the PCB traces which connect the oscillator to the PLL and the PLL to the LTC3721 are sufficiently long for 100kHz, the traces could exhibit transmission line behavior; this could cause undesired phase shifts due to delays. The delays nullify the purpose of the Oscillator-PLL system. More specifically, delays as small as 3µs are enough to cause the Oscillator-PLL system to deviate from its desired behavior because the switching period is 10µs. Consequently, multiple phases may simultaneously draw power for sufficiently large delays, yielding a potentially unacceptable output current ripple for some operating conditions. If this technique is utilized, the delay divided by the switching period should be less than 5%. Alternatively, an IC with an internal PLL can be procured, such as the LTC3777 explained in Section 6.2.1. The LTC6902 can then be used to synchronize each phase via the SYNC or PLLIN pins. This minimizes the length of PCB trace needed, and therefore reduces the delay. An example of synchronizing a DC/DC converter consisting of an IC with an internal PLL per phase is shown in Figure 10.2.

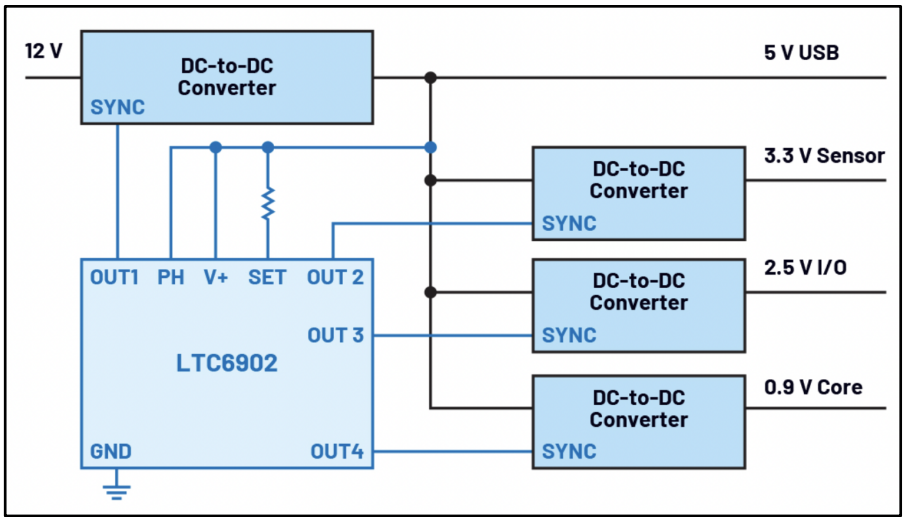


Figure 10.2. LTC6902 used to synchronize a DC/DC converter consisting of an IC with an internal PLL per phase [35].

### 10.2.4 Investigate Conducted & Radiated Emissions of the Push-Pull Converter

Since the PCB layout was not finalized the conducted and radiated EMI of the isolated design–which are highly dependent on the configuration of the layout–were not investigated. It is paramount to ensure both kinds of emissions are within acceptable limits so the performance of the isolated design is not degraded, the converter does not disrupt the performance of electronic equipment in its vicinity, and the lifetime of the PEMFC or LiPo battery is not reduced.

Through testing of the PCB, it can be discerned whether or not the conducted or radiated EMI is degrading the performance of the converter, PEMFC, or LiPo. Contrarily, because the regulatory framework for EMI in our intended UAV application is currently evolving, it is difficult to discern how disruptive the push-pull converter will be to the numerous types of electronic equipment it may pass by. Until the regulations are complete, the compliance of the push-pull converter with class A CISPR-22 standards, which are internationally accepted, can be verified.[23] Additionally, the most significant culprits of EMI in the converter could be identified so mitigation strategies could be implemented. For example, the diodes in the push-pull converter could prove to be a potent source of EMI. To minimize the emissions from each diode, an RC snubber could be placed in parallel for every diode at the expense of efficiency. Similar logic applies to the MOSFETs. Furthermore, an output common-mode choke, such as the SCR25XV-350-2R4A003JV, could replace the output inductor currently in the design to further attenuate EMI emissions.

### 10.2.5 Further Investigate MOSFET Selection for the Push-Pull Converter

In the initial research of this project, we investigated different semiconductor materials that could improve the power density and weight of our converter. Specifically, we researched wide band gaps in Silicon Carbide (SiC) and Gallium Nitride (GaN) semiconductors.

[23] Class A CISPR-22 standards correspond to commercial, industrial, and environmental applications [36].

When compared to the common Silicon (Si) semiconductor, the SiC and GaN had higher band gaps, lower leakage currents, and higher critical breakdown fields [37]. The higher voltage capabilities would make these semiconductors ideal for a high voltage application like our converter. They were also smaller in size and could withstand higher operating temperatures than Si semiconductors, which is ideal for our intended application and reduces the necessity of heavy heat sinks. Comparison between the GaN and SiC semiconductors demonstrated that GaN semiconductors performed better for high frequency applications, and their greater electron mobility gives them a greater switching capacity [37].

Due to their small dimensions, high power density, and high voltage capabilities, GaN semiconductors should be further investigated for their use in lightweight unmanned autonomous vehicle applications. For future iterations of this project, they should be investigated and tested for alternative versions of the converter design.

### 10.2.6 Explore the Feasibility of Reducing the Weight of the Push-Pull Converter

As discussed in Chapter 8, one of the major disadvantages of the latest rendition of the isolated design is its approximate mass of 1800g, which caused it to fail design criterion 9. As a consequence of failing design criterion 9, some characteristics of the flight performance of the intended UAV application could be partially compromised. This warrants an investigation into the practicality of reducing the weight of the isolated design.

A seemingly obvious method of reducing the weight of the isolated design involves decreasing the number of phases from three to two.[24] Moreover, one might also attempt to reduce the number of IPP200N25N3 MOSFETs in parallel from three to two. Subsequently, one may assume that the net change in the weight of the converter is a reduction due to a decrease in the number of components, particularly the transformer count. However, if the power dissipation in any one component exceeds its rated junction temperature as a result of decreasing the number of phases, cooling equipment of considerable proportion may have to be implemented. In turn, the overall weight of the converter could increase from the addition of the cooling equipment. For example, suppose the number of phases is reduced to two. This implies that, at the MPP of the PEMFC, the largest DC steady-state current which travels through an individual IPP200N25N3 MOSFET in the triode region is 17.5A, further suggesting the average conduction losses are approximately 6.125W. With the inclusion of the 100kHz switching losses and power dissipated in the gate, the average power dissipated in a single MOSFET may increase to 7W or higher. As such, the junction temperature of the MOSFET can rise to 484ºC if an ambient temperature of 50ºC and minimal footprint are assumed. A heat sink would need to be implemented in such a scenario. With a 6cm$^2$ copper area drain connection dedicated to each MOSFET on an epoxy PCB FR4, the junction temperature of an individual MOSFET decreases to 330ºC for an assumed ambient temperature of 50ºC, which is still impractical.

With a large enough cooling area or equipment for the PCB board, it may be possible to reduce the number of phases and IPP200N25N3 MOSFETs in parallel to two. However, it is unclear whether the weight reduction would be larger than the weight increase from the expanded PCB board or cooling equipment for the components. An alternative method for reducing weight involves replacing the DCDC2400-001 transformer with a transformer that has a turns ratio of 1+1:8 and can tolerate switching frequencies up to 500kHz (the maximum frequency of the

[24] Reducing the number of phases to one would exceed the 2kW rating of the DCDC2400-001 transformer.

LTC3721); however, switching losses in this scenario may induce the same issue described in the previous paragraph. The components can also be replaced with other components that minimize conduction and switching losses, but doing so introduces a new set of tradeoffs which could cause a net increase in the weight (see footnote 9).

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# Appendix A: Modeling Method for Chapter 4 Topologies

To simulate the topologies presented in Chapter 5, the PEMFC was treated as a variable voltage source in series with a variable resistor, and the LiPo battery as a variable resistor if the converter is operating in the continuous conduction mode (CCM). The value of the voltage source and the value of the resistor were varied depending on the region of the IV-characteristic the converter is operating in. For this model, it is paramount that the load resistor is sized correctly at a particular operating point. Otherwise, stack voltages and currents that are not on the characteristic curve will be obtained.

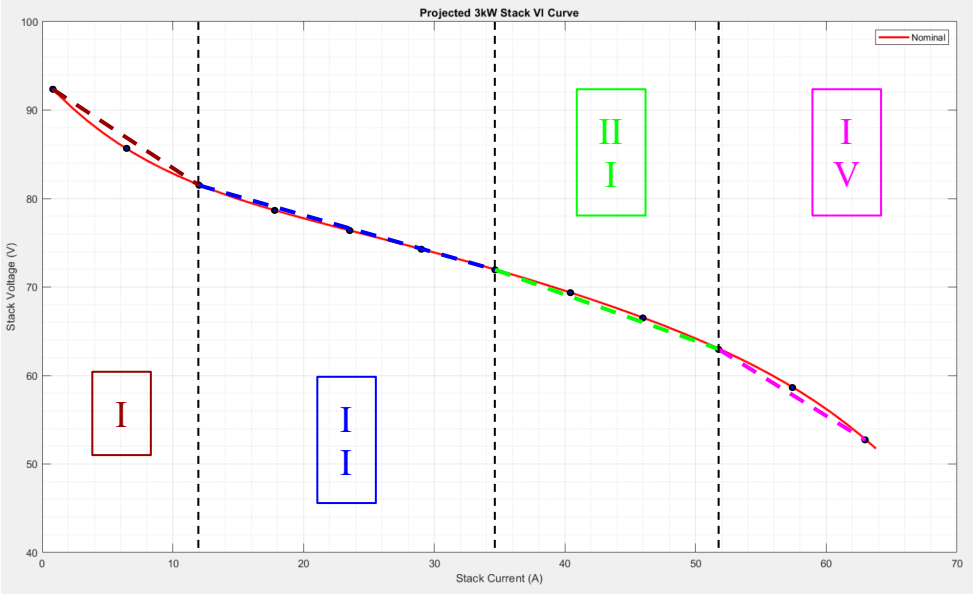


Figure A.1. IV-characteristic of the PEMFC split into linear regions for CCM modeling purposes.

In Region I, the fuel cell is modeled as a 93.17VDC independent voltage source in series with a 0.96 Ω resistor. In Region II, the fuel cell is modeled as a 86.67VDC independent voltage source in series with a 0.42 Ω resistor. In Region III, the fuel cell is modeled as a 88.74VDC independent voltage source in series with a 0.48 Ω resistor. Lastly, in Region IV, the fuel cell is modeled as a 114.58VDC independent voltage source in series with a 0.98 Ω resistor. If a point is on a boundary, then both models which the boundary separates will be appropriate. For when it is desired to evaluate the performance of the converter in DCM or CCM, the fuel cell is modeled as a 92.95VDC independent voltage source in series with a 0.45 Ω resistor. The load resistance (LiPo battery) is found by dividing the square of the expected output voltage by the input power.

To simulate the topologies presented in chapter five, the procedure below was followed:

1. Choose a switching frequency and duty cycle combination to simulate.
2. Select an operating point to simulate at and identify the corresponding region of operation.
3. Size the load resistor by dividing the square of the expected output voltage by the input power (100% efficiency is assumed at this step).
4. Add enough parasitics to the topology such that the efficiency of the topology is 92% at the MPP. It may take several attempts for this to occur.
5. Begin recording simulated parameter values for each operating point.

6. Repeat steps one through five for as many feasible frequency and duty cycle combinations.

# Appendix B: Simulation Results for Chapter 4 Topologies

The simulation results for some of the open-loop topologies discussed in chapter 4 are presented below.

## B.1 Quadratic Boost Converter Simulations

The quadratic boost converter was simulated at 500 kHz, with capacitor voltage ripple and inductor current ripple all set to 4%. The following inductor and capacitance values were calculated to be used in the simulation:

$$L1 = L2 = 2.31 \text{ mH}$$
$$C1 = C2 = 0.181 \text{ mF}$$

The simulation yielded the following results:

Table B.1. Simulated results for the quadratic boost converter at various operating points.

| **Fuel Cell Operating Points** | | | | **Li-Battery Values** | | |
|---|---|---|---|---|---|---|
| **Given Realistic Stack Voltage [V]** | **Given Realistic Stack Current [A]** | **Simulated Stack Voltage [V]** | **Simulated Stack Current [A]** | **Simulated Output Voltage [V]** | **Simulated Output Current [A]** | **Calculated Load Resistance [Ω]** |
| **92.5** | **0.7** | 92.5 | 0.6 | 364 | 0.158 | 2298 |
| **85.9** | **6.4** | 82.02 | 5.54 | 322.4 | 1.384 | 233 |
| **81.6** | **12** | 74.68 | 9.8 | 291.8 | 2.47 | 118 |
| **78.9** | **17.7** | 69.18 | 13.88 | 268.8 | 3.46 | 77.5 |
| **76.5** | **23.4** | 64.28 | 17.457 | 248.2 | 4.36 | 56.9 |
| **74.2** | **29** | 74.2 | 20.6 | 229.4 | 5.15 | 44.5 |
| **72** | **34.7** | 55.5 | 23.48 | 211.8 | 5.86 | 36.1 |
| **69.5** | **40.4** | 51.3 | 26 | 194.14 | 6.49 | 29.9 |
| **66.6** | **46** | 47 | 28 | 176.3 | 6.9 | 25.2 |
| **63.8** | **51.7** | 42.9 | 29.7 | 159.8 | 7.4 | 21.5 |
| **58.8** | **57.4** | 37.28 | 30.74 | 136.7 | 7.68 | 17.8 |
| **52.7** | **63** | 31 | 30.9 | 112 | 7.7 | 14.5 |

As demonstrated above, the quadratic boost converter failed at larger stack voltages.

## B.2 Double Cascade Boost Converter Simulations

The double cascaded boost converter was simulated in LTspice at a frequency of 500kHz for an output voltage of 280V and 400V. The duty cycles, input voltage, and load resistance were adjusted accordingly:

1. $@\ 280V, D2 = 0.75\ and\ D1\ varied. L2 = 536\mu H\ and\ L1 = 496\mu H$
2. $@\ 400V, D2 = 0.643\ and\ D1\ varied. L2 = 459\mu H\ and\ L1 = 493\mu H$

The reasoning behind using this method was to decrease the first-stage inductor L1 since the inductor current ripple was set at 4%. By setting D1 to the smallest possible value, the smallest inductor value could be achieved using these equations:

$$D1 = 1 - \frac{V_{in}}{V_{out}(1-D2)} \quad \text{(eq. B.1)}$$

$$L1 = \frac{D1\, V_{in}}{f\, \Delta i_{L1}} \quad \text{(eq. B.2)}$$

The results are summarized in Table 5.3 and 5.4 for an output voltage of 280V and 400V, respectively. The simulated output voltage for both varied for different operating points. This is likely due to the parasitics that were added to several components, such as the inductors and capacitors. At 280V, it dipped below the desired range. However, this could be fixed by resimulating for a higher output voltage in the range of 290-295V. At 400V, the output voltage stayed within the desired range.

Table B.2. Simulated results for the double cascade boost converter at various operating points for 280V.

| **Fuel Cell Operating Points** | | | | **Li-Battery Values** | | |
|---|---|---|---|---|---|---|
| **Given Realistic Stack Voltage [V]** | **Given Realistic Stack Current [A]** | **Simulated Stack Voltage [V]** | **Simulated Stack Current [A]** | **Simulated Output Voltage [V]** | **Simulated Output Current [A]** | **Calculated Load Resistance [Ω]** |
| **92.5** | **0.7** | 92.49 | 0.700 | 279.9 | 0.231 | 1211 |
| **85.9** | **6.4** | 86.96 | 6.470 | 282.1 | 1.97 | 143.2 |
| **81.6** | **12** | 81.69 | 11.96 | 277.3 | 3.47 | 79.92 |
| **78.9** | **17.7** | 79.27 | 17.62 | 276.9 | 4.94 | 56.05 |
| **76.5** | **23.4** | 76.94 | 23.16 | 275.5 | 6.29 | 43.80 |
| **74.2** | **29** | 74.69 | 28.53 | 273.8 | 7.52 | 36.41 |
| **72** | **34.7** | 72.47 | 33.90 | 272.1 | 8.67 | 31.39 |
| **69.5** | **40.4** | 69.93 | 39.18 | 269.9 | 9.67 | 27.91 |
| **66.6** | **46** | 67.37 | 44.52 | 269.5 | 10.5 | 25.59 |
| **63.8** | **51.7** | 65.37 | 50.22 | 270.7 | 11.4 | 23.81 |
| **58.8** | **57.4** | 60.31 | 55.37 | 268.0 | 11.6 | 23.18 |
| **52.7** | **63** | 54.87 | 60.92 | 269.0 | 11.4 | 23.60 |

Table B.3. Simulated results for the double cascade boost converter values at desired operating points for 400V.

| Fuel Cell Operating Points | | | | Li-Battery Values | | |
|---|---|---|---|---|---|---|
| **Given Realistic Stack Voltage [V]** | **Given Realistic Stack Current [A]** | **Simulated Stack Voltage [V]** | **Simulated Stack Current [A]** | **Simulated Output Voltage [V]** | **Simulated Output Current [A]** | **Calculated Load Resistance [Ω]** |
| **92.5** | **0.7** | 92.5 | 0.697 | 397.6 | 0.161 | 2470 |
| **85.9** | **6.4** | 87 | 6.42 | 401.2 | 1.38 | 290.8 |
| **81.6** | **12** | 81.78 | 11.87 | 394.8 | 2.42 | 163.1 |
| **78.9** | **17.7** | 79.34 | 17.44 | 394.3 | 3.44 | 114.6 |
| **76.5** | **23.4** | 77.03 | 22.96 | 392.6 | 4.39 | 89.42 |
| **74.2** | **29** | 74.8 | 28.27 | 390.4 | 5.25 | 74.37 |
| **72** | **34.7** | 72.57 | 33.7 | 388.1 | 6.06 | 64.05 |
| **69.5** | **40.4** | 70.08 | 38.88 | 385.4 | 6.76 | 57.01 |
| **66.6** | **46** | 67.49 | 44.26 | 384.7 | 7.37 | 52.20 |
| **63.8** | **51.7** | 65.55 | 50.03 | 387.0 | 7.98 | 48.50 |
| **58.8** | **57.4** | 60.57 | 55.11 | 384.0 | 8.1 | 47.41 |
| **52.7** | **63** | 55.12 | 60.68 | 385.0 | 7.99 | 48.19 |

## B.3 Interleaved N-Phase Boost Converter Simulations

Only the two-phase interleaved boost converter was simulated. This is primarily because, as the number of phases increases, the DC current, $I$, through each inductor, $L$, will become smaller. Eventually, for a certain number of phases $N$, the DC current through each inductor will be less than the ripple of the current waveform, $\Delta i_L$. In turn, the converter operates in DCM and the conversion ratio, $M(D)$, of the topology becomes load dependent, an undesirable outcome in this application[25]. To prevent DCM operation at $N$ phases, the inductors must be made sufficiently large so as to prevent the ripple current from exceeding the DC component of the current. However, doing so may significantly increase the mass of the converter, which is also undesirable in this application. Additionally, the cascaded two-phase interleaved boost converter was not simulated. This is largely because, for every subsequent stage of the cascaded interleaved boost converter, the inductance values must be increased by a factor as large as three. The inductance of the inductors must be increased to compensate for the decreased DC current through the inductors in

[25] Please note, it is likely that load dependence cannot be entirely avoided in reality as a consequence of the presence of parasitics.

the second and third stages, which puts the converter at higher risk of operating in DCM if the inductors aren't sufficiently large enough to suppress the ripple such that design criterion five is satisfied. Therefore, to minimize mass and reduce the risk of DCM operation, it may be desirable to investigate and optimize a design which utilizes the two-phase interleaved boost converter. Consequently, the focus of these simulation sets is on the single stage 2-phase interleaved boost converter as a constituent of more practical topologies. For example, by studying the single stage interleaved boost converter, the performance of a cascaded two-phase interleaved topology, driven at a duty cycle $D$, can more readily be understood.

Three sets of simulations were performed. The first set of simulations were performed on a single stage two-phase interleaved boost converter at $D = 0.5$, $f_s = 500\ kHz$, and $\eta = 0.92$ at the MPP. The second set of simulations were performed on a single stage two-phase interleaved boost converter at $D = 0.5$, $f_s = 100\ kHz$, and $\eta = 0.92$ at the MPP. The third set of simulations were performed on a single stage two-phase interleaved boost converter at $D = 0.5$, $f_s = 1\ kHz$, and $\eta = 0.92$ at the MPP. For each simulation set, the parasitic resistance of the inductors was increased to 130 m$\Omega$ to achieve an efficiency of 0.92 at the MPP and the model utilized was the more accurate CCM model.

The inductance of the inductors and capacitance of the capacitors were approximated using the following equations:

$$L = 1.2((V_{i,min}D)/(\Delta i_{L,min}f_s)) = 1.2L_{max} \quad \text{(eq. B.3)}$$

$$C = 1.2((I_{o,max}(1-D))/(f_s\Delta V_{o,min})) = 1.2C_{max} \quad \text{(eq. B.4)}$$

where, according to design criteria five and six, respectively

$$\Delta i_{L,min} = 0.04I_L \quad \text{(eq. B.5)}$$

$$\Delta V_{o,min} = 0.04V_o \quad \text{(eq. B.6)}$$

where

$$I_L = (0.5I_{o,min})/(1-D) \quad \text{(eq. B.7)}$$

The capacitance and inductance values were then increased or decreased accordingly to attain the proper operation in CCM with the inclusion of parasitics.

The simulated circuit and simulation results can be observed in figure B.1. An input capacitor was added to impede changes in the input voltage.

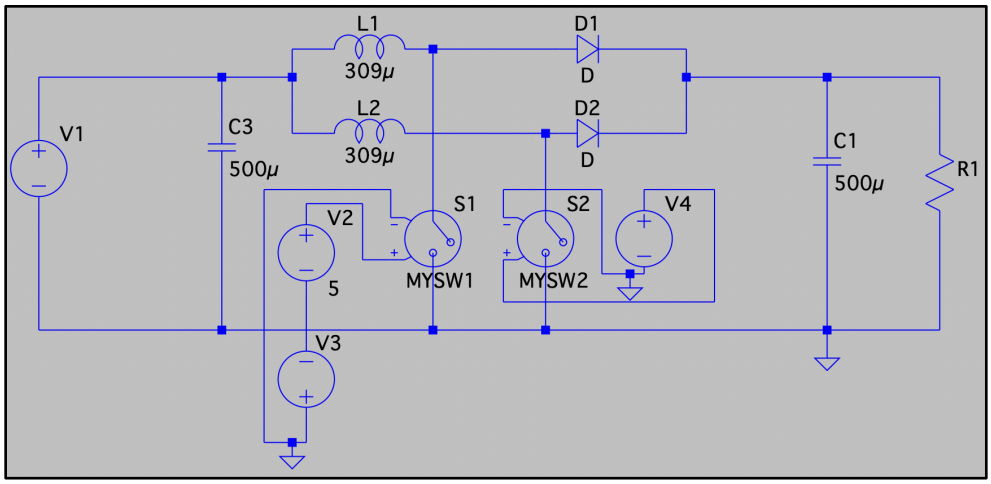

Figure B.1. Circuit diagram for the interleaved two-phase boost converter.

Table B.4. Simulated results for the fuel cell operating points and the corresponding LiPo battery values of a single-stage two-phase interleaved boost converter at $D = 0.5$, $f_s = 500\ kHz$, and $\eta \approx 0.92$ at the MPP.

| **Fuel Cell Operating Points** | | | | **Li-Battery Values** | | |
|---|---|---|---|---|---|---|
| **Given Realistic Stack Voltage [V]** | **Given Realistic Stack Current [A]** | **Simulated Stack Voltage [V]** | **Simulated Stack Current [A]** | **Simulated Output Voltage [V]** | **Simulated Output Current [A]** | **Calculated Load Resistance [Ω]** |
| 92.5 | 0.7 | 92.5 | 0.7 | 184 | 0.35 | 528.57 |
| 85.9 | 6.4 | 87 | 6.4 | 172.3 | 3.21 | 53.7 |
| 81.6 | 12 | 81.7 | 11.8 | 161 | 5.9 | 27.2 |
| 78.9 | 17.7 | 79.3 | 17.5 | 155.5 | 8.72 | 17.83 |
| 76.5 | 23.4 | 77 | 23 | 150 | 11.5 | 13.08 |
| 74.2 | 29 | 74.8 | 28.33 | 145 | 14.2 | 10.23 |
| 72 | 34.7 | 72.5 | 33.7 | 139 | 16.8 | 8.3 |
| 69.5 | 40.4 | 70 | 39 | 133.7 | 19.4 | 6.88 |
| 66.6 | 46 | 67.5 | 44.3 | 127.9 | 22.09 | 5.79 |
| 63.8 | 51.7 | 65.5 | 50 | 123 | 24.8 | 4.94 |
| 58.8 | 57.4 | 60.6 | 55.1 | 112.4 | 27.6 | 4.1 |
| 52.7 | 63 | 55.18 | 60.61 | 101 | 30.3 | 3.35 |

Table B.5. Criteria satisfaction for a single stage of the two-phase interleaved boost converter as the fuel cell operating point is varied at $D = 0.5$, $f_s = 500\ kHz$, and $\eta = 0.92$ at the MPP. Green corresponds to satisfied, red to not satisfied, dark yellow to partially satisfied, and gray to not currently measurable. These results were attained through LTspice simulations.

| **OP [V]** | **Criteria Satisfaction** | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** | **10** |
| 92.5 | | | | | | | | | | |
| 85.9 | | | | | | | | | | |
| 81.6 | | | | | | | | | | |
| 78.9 | | | | | | | | | | |
| 76.5 | | | | | | | | | | |
| 74.2 | | | | | | | | | | |
| 72 | | | | | | | | | | |
| 69.5 | | | | | | | | | | |
| 66.6 | | | | | | | | | | |
| 63.8 | | | | | | | | | | |
| 58.8 | | | | | | | | | | |
| 52.7 | | | | | | | | | | |

Table B.6. Fuel cell operating points and the corresponding LiPo battery values for a single-stage of the two-phase interleaved boost converter at $D = 0.5$, $f_s = 100\ kHz$, and $\eta \approx 0.92$ at the MPP. The simulated results were obtained from LTspice. Observe how the converter begins to "feel" DCM at a load resistance of 528.57 Ω at a frequency of 100 kHz.

| **Fuel Cell Operating Points** | | | | **Li-Battery Values** | | |
|---|---|---|---|---|---|---|
| **Given Realistic Stack Voltage [V]** | **Given Realistic Stack Current [A]** | **Simulated Stack Voltage [V]** | **Simulated Stack Current [A]** | **Simulated Output Voltage [V]** | **Simulated Output Current [A]** | **Calculated Load Resistance [Ω]** |
| 92.5 | 0.7 | 91.9 | 1.2 | 240.4 | 0.45 | 528.57 |

| | | | | | | |
|---|---|---|---|---|---|---|
| 85.9 | 6.4 | 87 | 6.42 | 172.3 | 3.2 | 53.7 |
| 81.6 | 12 | 81.7 | 11.8 | 161 | 5.92 | 27.2 |
| 78.9 | 17.7 | 79.3 | 17.5 | 155.5 | 8.72 | 17.83 |
| 76.5 | 23.4 | 77 | 23 | 150.2 | 11.5 | 13.08 |
| 74.2 | 29 | 74.8 | 28.3 | 145 | 14.2 | 10.23 |
| 72 | 34.7 | 72.6 | 33.7 | 140 | 16.8 | 8.3 |
| 69.5 | 40.4 | 70 | 39 | 134.1 | 19.5 | 6.88 |
| 66.6 | 46 | 67.5 | 44.3 | 128.3 | 22.15 | 5.79 |
| 63.8 | 51.7 | 65.5 | 50 | 123.6 | 25 | 4.94 |
| 58.8 | 57.4 | 60.6 | 55.1 | 112.5 | 27.6 | 4.1 |
| 52.7 | 63 | 55.2 | 60.6 | 101.5 | 30.3 | 3.35 |

Table B.7. Criteria satisfaction for a single stage two-phase interleaved boost converter as the fuel cell operating point is varied at $D = 0.5$, $f_s = 100\ kHz$, and $\eta = 0.92$ at the MPP. Green corresponds to satisfied, red to not satisfied, dark yellow to partially satisfied, and gray to not currently measurable. These results were attained through LTspice simulations.

| **OP [V]** | **Criteria Satisfaction** | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** | **10** |
| 92.5 | | | | | | | | | | |
| 85.9 | | | | | | | | | | |
| 81.6 | | | | | | | | | | |
| 78.9 | | | | | | | | | | |
| 76.5 | | | | | | | | | | |
| 74.2 | | | | | | | | | | |
| 72 | | | | | | | | | | |
| 69.5 | | | | | | | | | | |
| 66.6 | | | | | | | | | | |

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 63.8 | | | | | | | | | | |
| 58.8 | | | | | | | | | | |
| 52.7 | | | | | | | | | | |

Table B.8. Fuel cell operating points and the corresponding Li-Battery values for a single-stage of the two-phase interleaved boost converter at $D = 0.5$, $f_s = 1\ kHz$, and $\eta \approx 0.92$ at the MPP. Observe how the converter operates in the DCM for most operating points on the IV-characteristic at $f_s = 1\ kHz$. The simulated results were obtained from LTspice.

| **Fuel Cell Operating Points** | | | | **Li-Battery Values** | | |
|---|---|---|---|---|---|---|
| **Given Realistic Stack Voltage [V]** | **Given Realistic Stack Current [A]** | **Simulated Stack Voltage [V]** | **Simulated Stack Current [A]** | **Simulated Output Voltage [V]** | **Simulated Output Current [A]** | **Calculated Load Resistance [Ω]** |
| 92.5 | 0.7 | 52.3 | 42.9 | > 950 | 2 | 528.57 |
| 85.9 | 6.4 | 50.5 | 44.8 | 315.15 | 5.87 | 53.7 |
| 81.6 | 12 | 62.3 | 58 | 284.66 | 10.5 | 27.2 |
| 78.9 | 17.7 | 61.6 | 59.9 | 232.4 | 13 | 17.83 |
| 76.5 | 23.4 | 60.9 | 61.5 | 200.5 | 15.3 | 13.08 |
| 74.2 | 29 | 60.3 | 63 | 178.5 | 17.5 | 10.23 |
| 72 | 34.7 | 58.5 | 63.15 | 158.9 | 19.15 | 8.3 |
| 69.5 | 40.4 | 57.8 | 64.5 | 145.5 | 21.1 | 6.88 |
| 66.6 | 46 | 57 | 66 | 134.5 | 23.2 | 5.79 |
| 63.8 | 51.7 | 52.8 | 63 | 116.8 | 23.6 | 4.94 |
| 58.8 | 57.4 | 51.5 | 64.4 | 106.2 | 25.9 | 4.1 |
| 52.7 | 63 | 50 | 66 | 95.7 | 28.6 | 3.35 |

Table B.9. Criteria satisfaction for a single stage two-phase interleaved boost converter as the fuel cell operating point is varied at $D = 0.5$, $f_s = 1\ kHz$, and $\eta = 0.92$ at the MPP. Green corresponds to satisfied, red to not satisfied, dark yellow to partially satisfied, and gray to not currently measurable. These results were attained through LTspice simulations.

| **OP [V]** | **Criteria Satisfaction** | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** | **10** |
| 92.5 | | | | | | | | | | |
| 85.9 | | | | | | | | | | |
| 81.6 | | | | | | | | | | |
| 78.9 | | | | | | | | | | |
| 76.5 | | | | | | | | | | |
| 74.2 | | | | | | | | | | |
| 72 | | | | | | | | | | |
| 69.5 | | | | | | | | | | |
| 66.6 | | | | | | | | | | |
| 63.8 | | | | | | | | | | |
| 58.8 | | | | | | | | | | |
| 52.7 | | | | | | | | | | |

# Appendix C: Maximum Input RMS Current of a Buck Converter

According to the LTC3777 datasheet, the RMS input current of a buck converter can be approximated by the following equation:

$$I_{RMS} \approx (I_{OUT(MAX)})(\frac{V_{OUT}}{V_{IN}})\sqrt{\frac{V_{IN}}{V_{OUT}} - 1} \qquad \text{(eq. C.1)}$$

Taking the partial derivative of Equation (C.1) with respect to $V_{IN}$ yields:

$$\frac{\partial I_{RMS}}{\partial V_{IN}} = (I_{OUT(MAX)})((\frac{-V_{OUT}}{(V_{IN})^2})(\sqrt{\frac{V_{IN}}{V_{OUT}} - 1}) + (\frac{V_{OUT}}{V_{IN}})\frac{1}{2}(\frac{V_{IN}}{V_{OUT}} - 1)^{-1/2}(\frac{1}{V_{OUT}}))$$

setting $\frac{\partial I_{RMS}}{\partial V_{IN}} = 0$ and simplifying gives:

$$(\frac{V_{IN}}{V_{OUT}} - 1) = \frac{1}{2}(\frac{V_{IN}}{V_{OUT}}) \Leftrightarrow 1 = \frac{1}{2}(\frac{V_{IN}}{V_{OUT}}) \Leftrightarrow V_{IN} = 2V_{OUT}$$

Perturbing the $\frac{\partial I_{RMS}}{\partial V_{IN}}$ equation by $\pm\varepsilon$, where $\varepsilon > 0$, about $V_{IN} = 2V_{OUT}$ suggests that $2V_{OUT}$ is a global maximum. Hence, the maximum RMS current occurs when:

$$I_{RMS,MAX} \approx (I_{OUT(MAX)})(\frac{V_{OUT}}{2V_{OUT}})\sqrt{\frac{2V_{OUT}}{V_{OUT}} - 1} = \frac{I_{OUT(MAX)}}{2}$$

# Appendix D: Isolated Design Output Voltage, Output Capacitance, & Inductor Equations

To begin, the equation for the output inductance of the isolated design is derived by application of the principle of inductor volt-second balance. It is important to note that, in this derivation, the negative terminal of the inductor is assumed to be the terminal connected directly to the output capacitance. Furthermore, the number of turns for the top-half of the primary winding is delineated by $N_{P1}$, the bottom-half by $N_{P2} = N_{P1}$, and the secondary winding by $N_S$. The output voltage and source voltage are given by $V_O$ and $V_S$, respectively.

In state one of Figure 7.3, the voltage across the inductor is given by:

$$V_S(\frac{N_S}{N_{P1}}) - V_O = V_S(\frac{N_S}{N_{P2}}) - V_O.$$

As a result, the inductance, $L_{eq}$, of the output inductor is given by:

$$L_{eq} = (V_S(\frac{N_S}{N_{P1}}) - V_O)\frac{DT_s}{\Delta i} \quad \text{(eq. D.1)}$$

where $\Delta i$ is the ripple of the current waveform and $D$ is the duty cycle of the converter.

In state two, the voltage across the inductor is $-V_O$. In states three and four, the voltage across the output inductor is the same as in states one and two, respectively. Consequently, from the application of the principle of inductor volt-second balance:

$$\frac{1}{T_s}\int_{T_s} v_L(t)dt = 2(V_S(\frac{N_S}{N_{P1}}) - V_O)DT_s - 2V_O(\frac{1}{2} - D)T_s = 0$$

$$(V_S(\frac{N_S}{N_{P1}}) - V_O)D = V_O(\frac{1}{2} - D)$$

$$V_O = 2V_S(\frac{N_S}{N_{P1}})D = 2V_S\sqrt{\frac{L_S}{L_{P1}}}D \quad \text{(eq. D.2)}$$

which is the equation for the voltage gain of the isolated design. Please note that the gain of the isolated design is limited by the FB pin of the LTC3721: once the voltage on the FB pin becomes 1.2V with respect to ground, the output voltage will no longer increase.

The voltage gain equation, paired with the analysis below, will allow for the derivation of the output capacitance. Since the output filter of the isolated design contains two poles in its pole-zero plot, the principle of capacitor charge-balance cannot be employed to derive the output capacitance. Instead, graphical methods will be utilized.

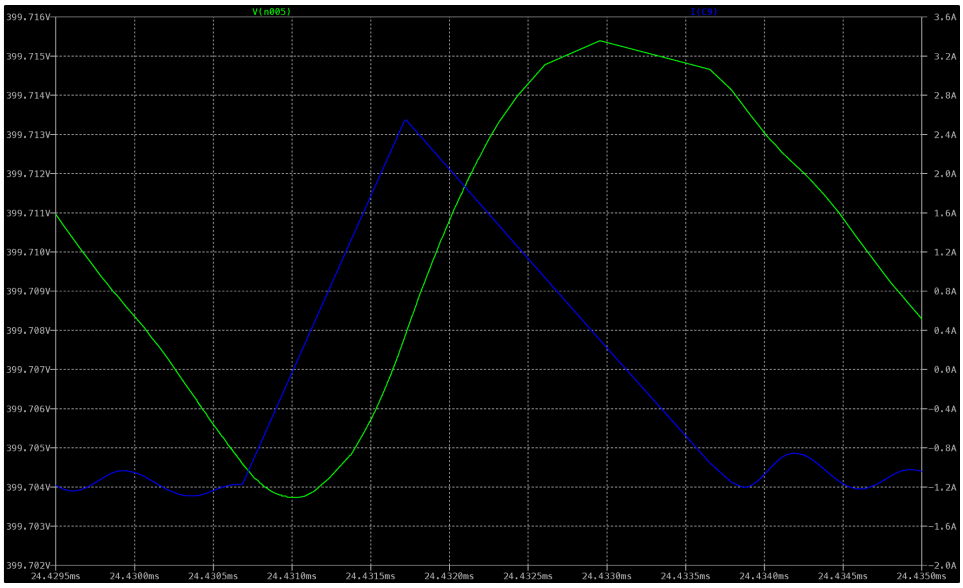

Figure D.1. Output capacitor voltage (green) and current (blue) for the isolated design.

From Figure D.1, it can be discerned that for the entire time interval that the current waveform is greater than zero, the capacitor voltage waveform increases by $2\Delta v$, where $\Delta v$ is half the pk-pk magnitude of the voltage waveform. Hence, the charge, $q$, imparted to the total output capacitance, $C_{eq}$, during this interval is:

$$q = C_{eq}(2\Delta v)$$

Since the current waveform is a triangular wave and persists for a quarter of the switching period when it is greater than zero and $D = 0.5$, the equation above may be equated to the area of a triangle:

$$\frac{1}{2}\left(\frac{T_s}{4}\right)\Delta i = C_{eq}(2\Delta v)$$

$$\Delta v = \frac{(\Delta i)(T_s)}{16C_{eq}}$$

Therefore:

$$\Delta v = \frac{T_s}{16C_{eq}}\left(\left(V_S\left(\frac{N_S}{N_{P1}}\right) - V_O\right)\frac{DT_s}{L_{eq}} = \frac{T_s}{16C_{eq}}\left(\left(V_S\left(\frac{N_S}{N_{P1}}\right) - 2V_S\left(\frac{N_S}{N_{P1}}\right)\right)\frac{DT_s}{L_{eq}}\right.\right.$$

$$\Delta v = \left(V_S\left(\frac{N_S}{N_{P1}}\right)D\right)(1-2D)\left(\frac{D(T_s)^2}{16C_{eq}L_{eq}}\right) = \left(\frac{V_O}{2}\right)(1-2D)\left(\frac{D(T_s)^2}{16C_{eq}L_{eq}}\right)$$

$$C_{eq} = \left(\frac{V_O}{\Delta v}\right)(1-2D)\left(\frac{D(T_S)^2}{32L_{eq}}\right) \qquad \text{(eq. D.3)}$$

# Appendix E: Input Voltage & Transformer Saturation

Suppose a DC input voltage from the PEMFC, $V_S$, is applied to the isolated design. As explained in Section 7.1.1, the control scheme of the isolated design will cause a voltage waveform, $v_T(t)$, to be induced across each half of the primary winding, where $v_T(t)$ is a squarewave which oscillates between $+V_S$ and $-V_S$ with switching period $T_s$. If the exact waveform morphology of $v_T(t)$ is known, the magnetizing current waveform through the magnetizing inductance, $L_M$, of one half of the primary can be derived through the following equation:

$$i_M(t) = \frac{1}{L_M}\int v_T(t)dt \qquad \text{(eq. E.1)}$$

where

$$L_M = \frac{(N_{P1})^2}{\Re} = \frac{(N_{P2})^2}{\Re}$$

$N_{P1}$ denotes the number of turns for the top-half of the primary winding and $N_{P2}$ the bottom-half. $\Re$ denotes the reluctance of the transformer, and can be approximated by:

$$\Re = \frac{l_m}{\mu A_C}$$

where $l_m$ is the mean-path length of the core, $A_C$ is the cross-sectional area of the core, and $\mu$ is the permeability of the core.

Using this information:

$$i_M(t) = \frac{\Re}{(N_{P1})^2}\int v_T(t)dt = \frac{l_m}{\mu A_C (N_{P1})^2}\int v_T(t)dt$$

If is assumed the magnetic flux density, $\overrightarrow{B(t)}$, is related to the magnetic field strength, $\overrightarrow{H(t)}$, through the following equation:

$$\overrightarrow{B(t)} = \mu(\overrightarrow{H(t)})$$

where $\overrightarrow{H(t)}$ can be calculated as:

$$\mu(\oint \overrightarrow{H(t)} \cdot \overrightarrow{dl}) \approx \mu(|H(t)|)l_m = \mu(N_{P1})i_M(t)$$

$$|H(t)| = \frac{(N_{P1})i_M(t)}{l_m}$$

$$|B(t)| = \mu(|H(t)|) = \mu(\frac{N_{P1}i_M(t)}{l_m})$$

then it must be the case that:

$$B(t) = \frac{1}{A_C N_{P1}} \int v_T(t) dt \qquad \text{(eq. E.2)}$$

as can be derived through Equation (E.1).

Hence, if the integral of the applied voltage waveform to the transformer from an interval of $t_1$ to $t_1 + \Delta t$ is sufficiently large, $B(t)$ can become so large in magnitude that the transformer saturates. This is evidenced through Figure E.1.

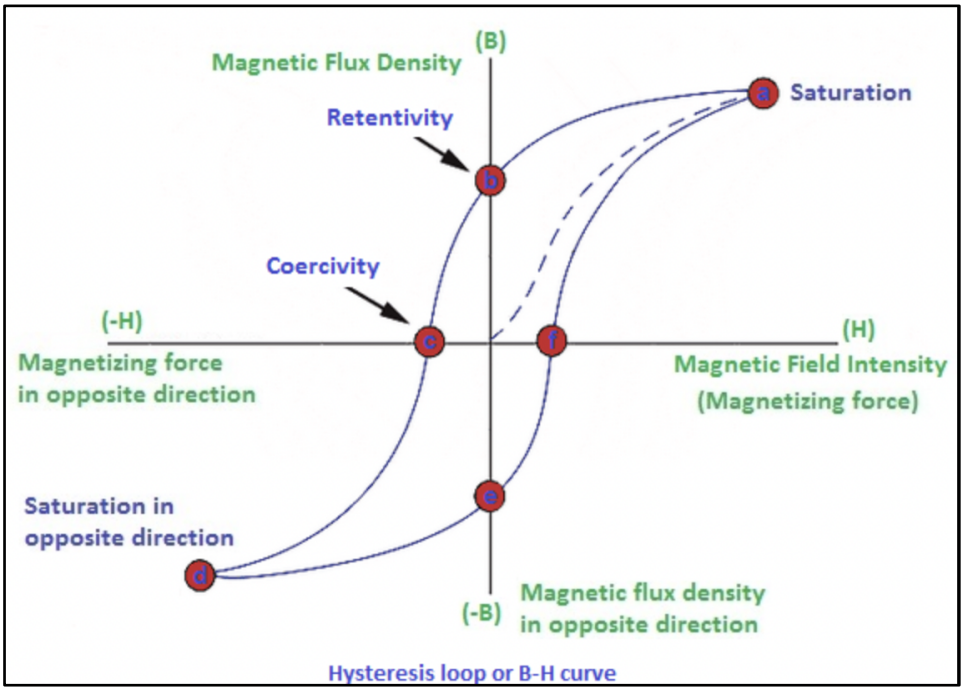


Figure E.1. B-H curve of a transformer. The saturation point on both ends of the loop have been labeled [38].

# Appendix F: Simulation Test Graphs & Setup

The graphs and setups for 16 simulation tests performed in LTspice on the three-phase push-pull converter are presented. Simulation tests 1 through 8 were created by engineers from Honeywell International Incorporated. The other simulation tests were composed by the students. It is important to note that, unlike in Figure 7.1, the simulation tests were performed with one VS-E5PX6012 diode rather than two in series as a consequence of a simulation glitch that prevented the simulation from progressing beyond a certain time. Since the voltage drop across a single VS-E5PX6012 diode is no more than 1.5V and likely has negligible influence on the overall dynamics of the converter, it is reasonable to assume that the results below are approximately equivalent to the results with two VS-E5PX6012 diodes in series. Additionally, the ESR of the aluminum capacitors was assumed to be negligible for these simulation tests. The version of the isolated design which was simulated is shown in Figure F.1.

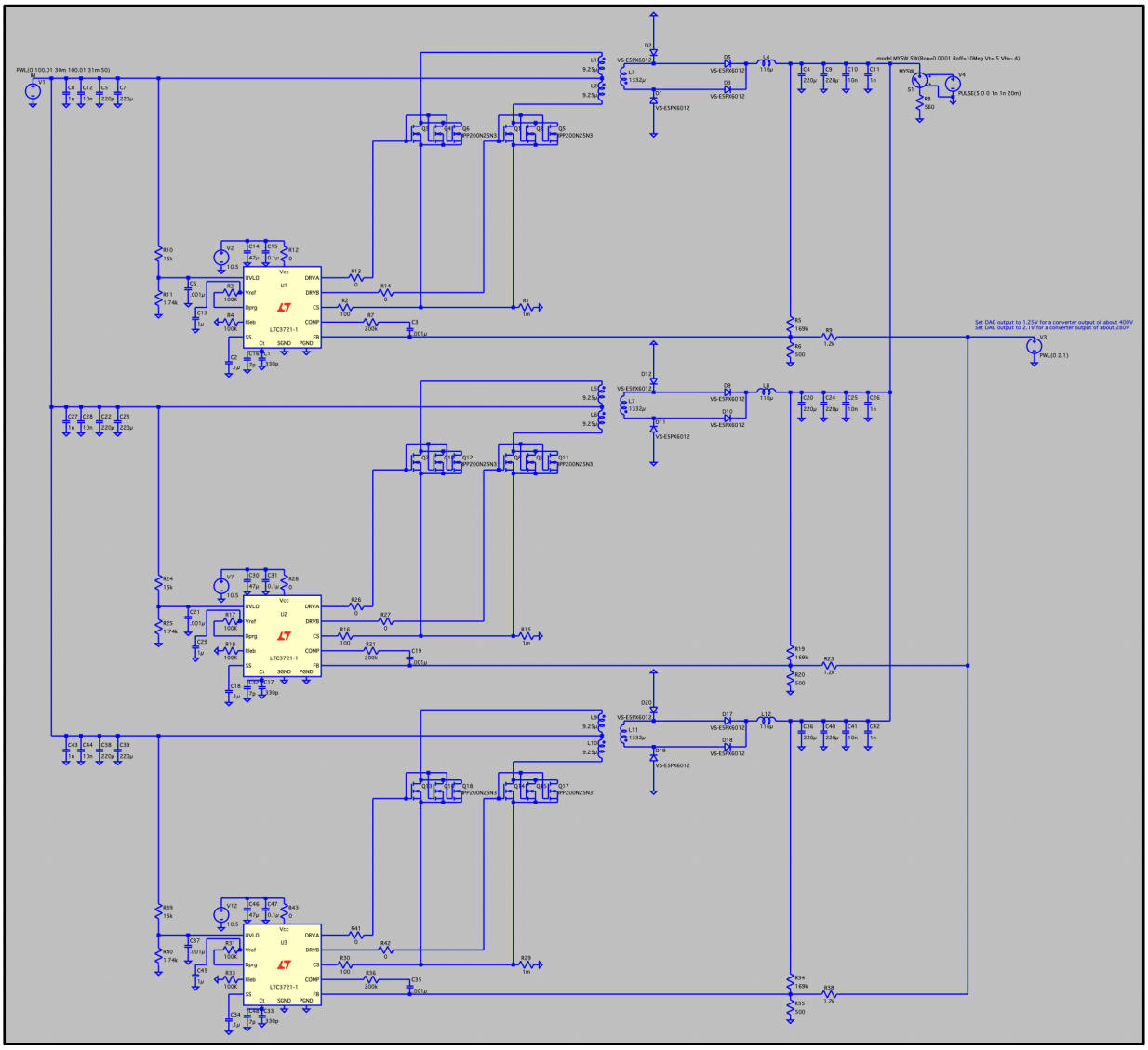

Figure F.1. Schematic for the simulated isolated design. The source and load were altered depending on the requirements of each simulation test.

# F.1 Simulation Test One

Test Description:

To properly perform this test, apply an input voltage of 50V to the converter and allow the output to settle to 400V before applying any load. After the output voltage settles, apply an 8A load. Once the voltage settles again, change the load to 0.5A.

Test Setup:

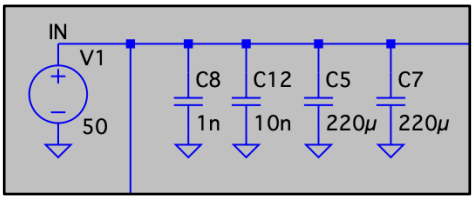


Figure F.2. Input of the three-phase push-pull converter for simulation test one.

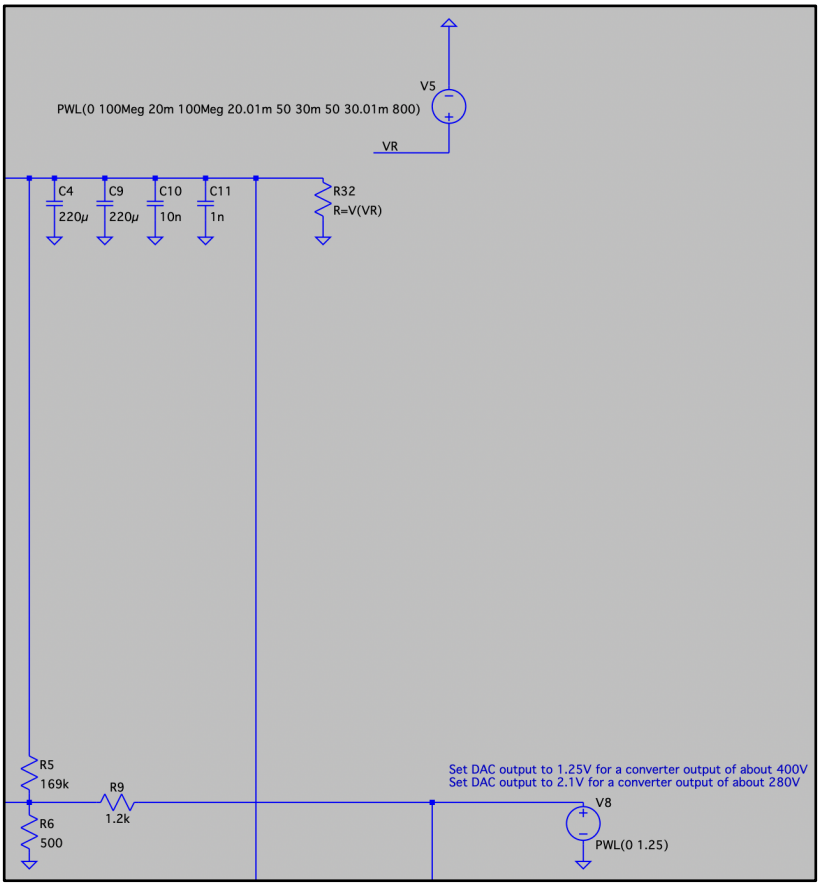


Figure F.3. Output and DAC of the three-phase push-pull converter for simulation test one. A variable resistor was utilized to perform this test. If the output voltage does not significantly vary, a PWL current source could be used to produce nearly equivalent results.

Test Results:

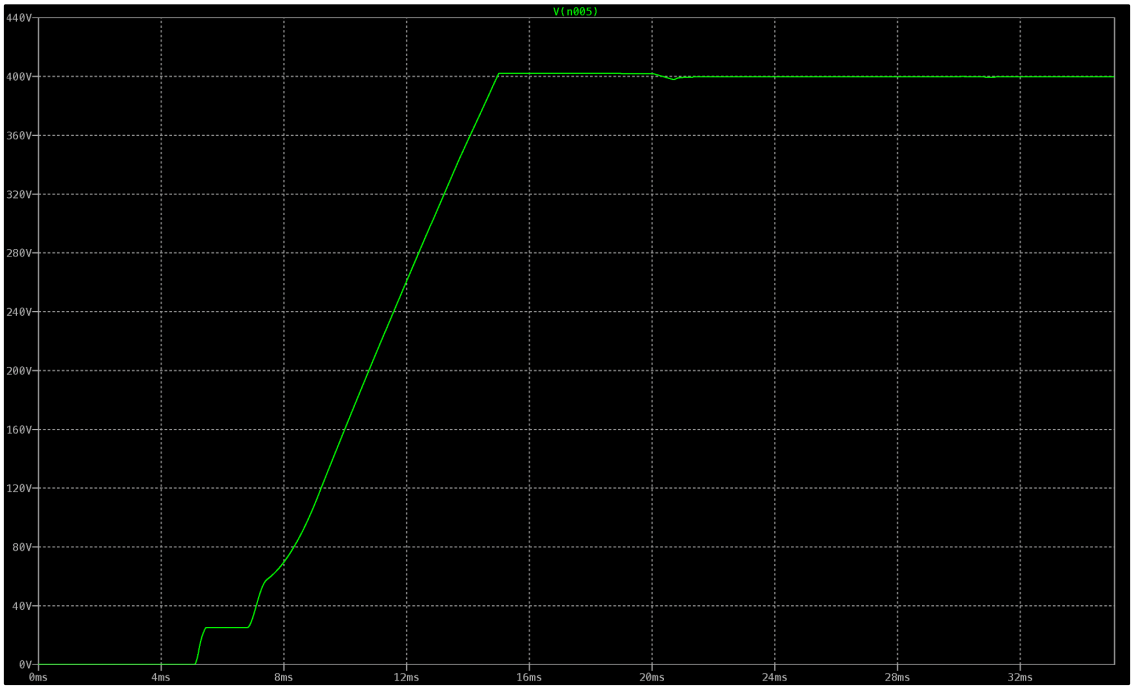


Figure F.4. Output voltage as a function of time for simulation test one. At approximately 15ms, the output voltage settled to 400V. Afterwards, at 20ms an 8A load was applied to the output. Lastly, at 30ms, the load transitioned from 8A to 0.5A.

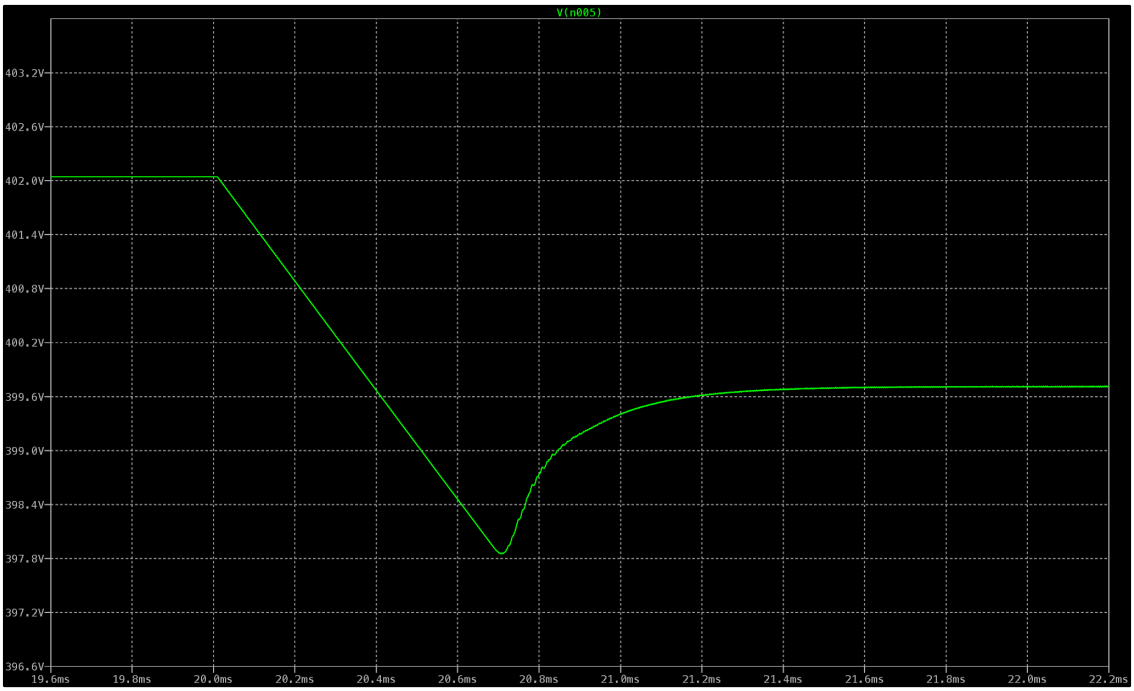


Figure F.5. Response to the application of the 8A load from 0A for simulation test one. The transients decayed after approximately 2ms. Additionally, the undershoot is nearly 2V and the ripple once steady-state is achieved is negligible.

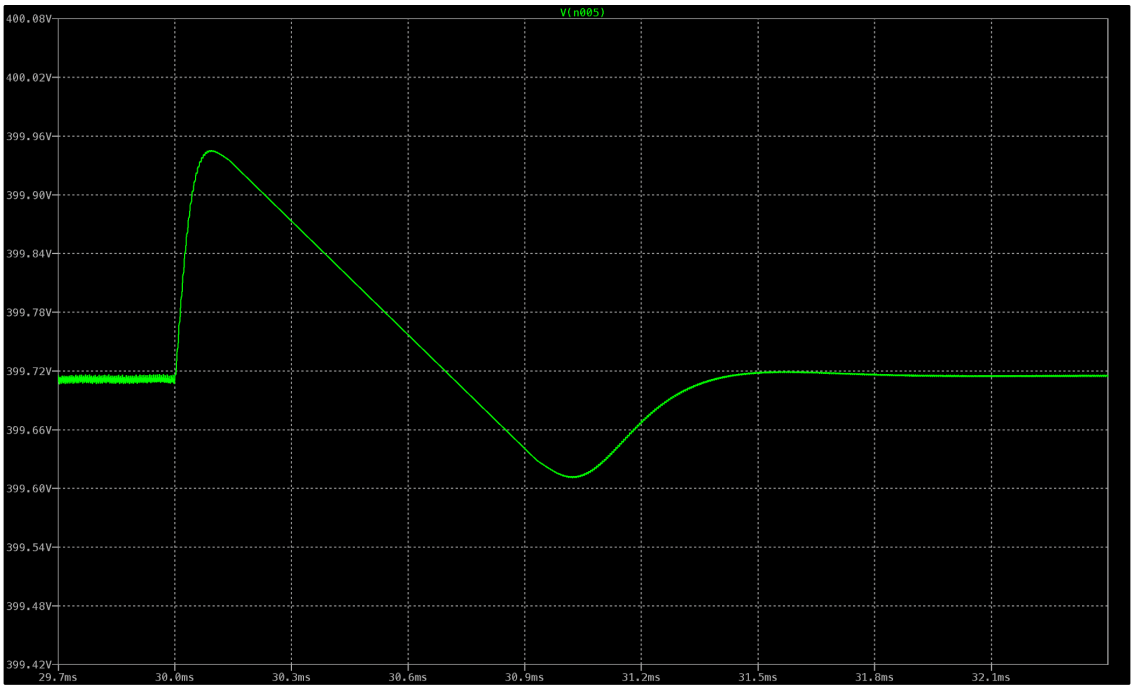


Figure F.6. Response to the application of the 0.5A load from 8A for simulation test one. The transients decayed after approximately 2ms. Additionally, the overshoot is 230mV, undershoot 100mV, and the ripple once steady-state is achieved appears negligible.

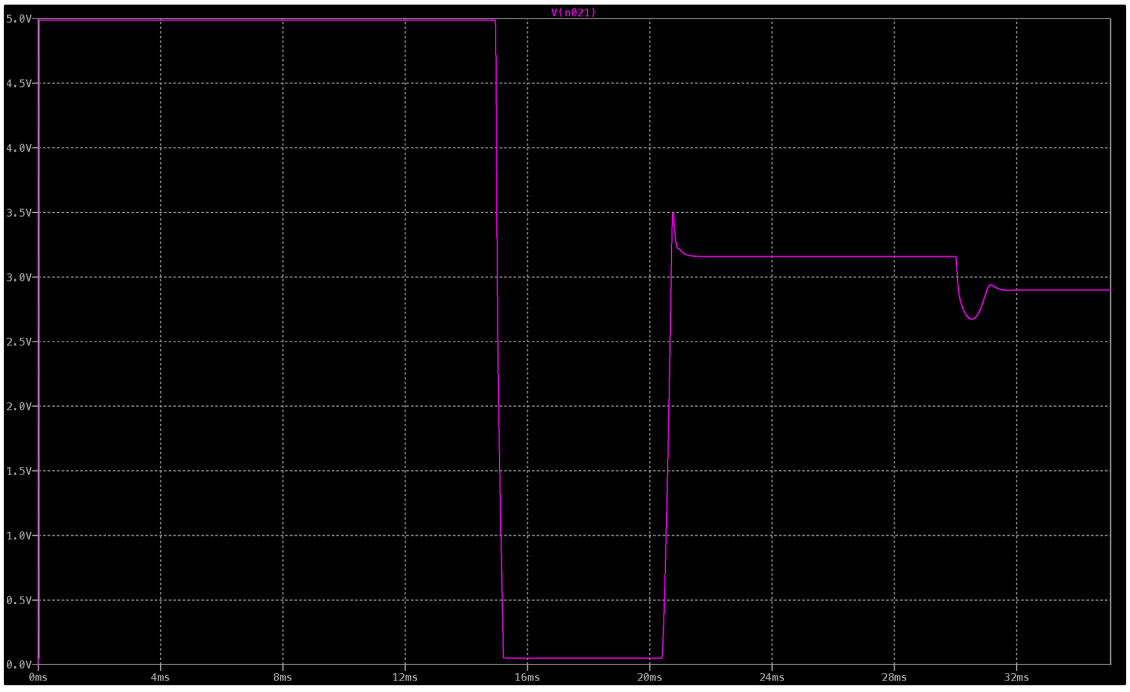


Figure F.7. Voltage waveform on the COMP pin with respect to ground for simulation test one. Compare this figure with Figure F.4 to discern what each nearly constant voltage interval corresponds to.

## F.2 Simulation Test Two

Test Description:

To properly perform this test, apply an input voltage of 50V to the converter and allow the output to settle to 400V before applying any load. After the output voltage settles, apply an 0.5A load. Once the voltage settles again, change the load to 8A.

Test Setup:

The input of the three-phase push pull converter in simulation test two is the same as shown in Figure F.2. On the contrary, the output setup is different.

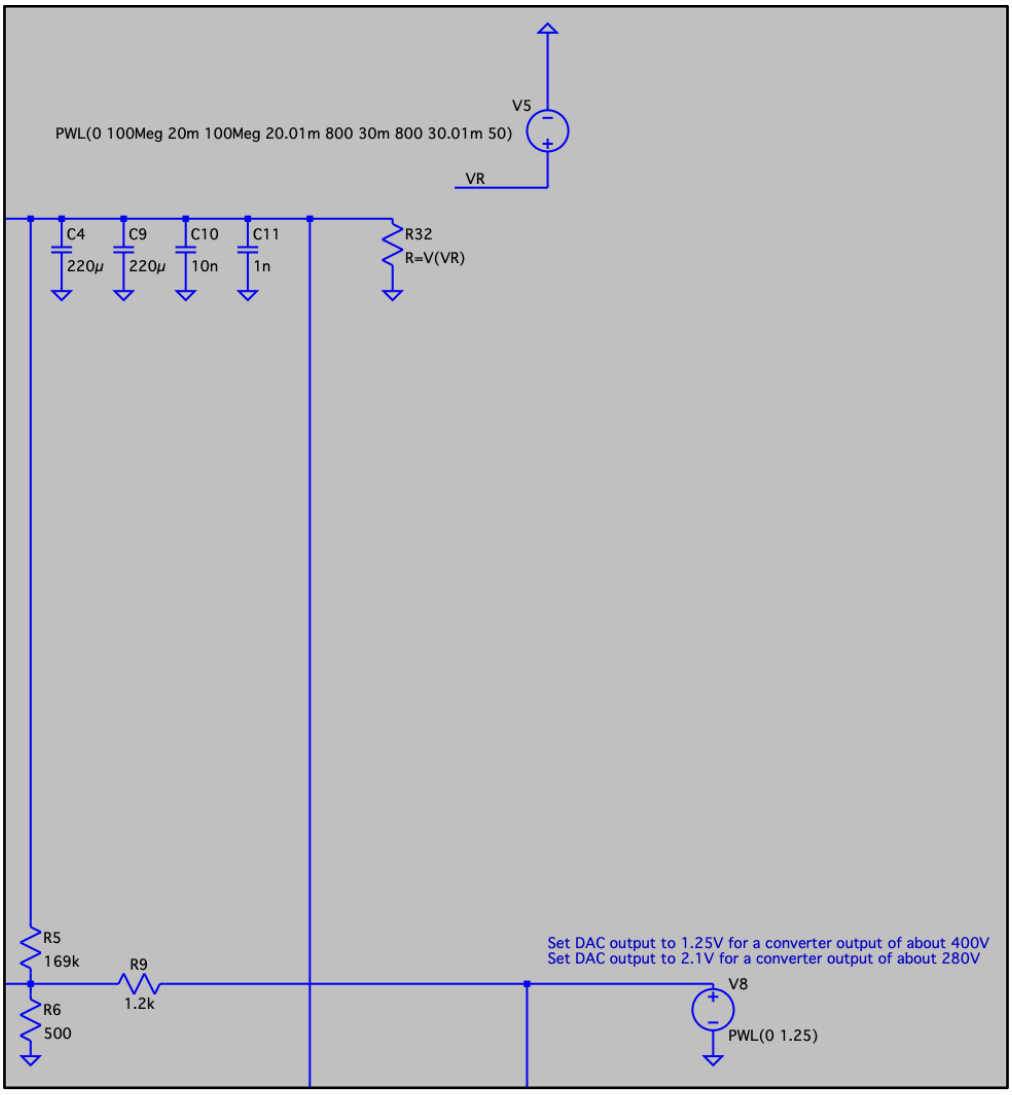


Figure F.8. The output and DAC of the three-phase push-pull converter for simulation test two. A variable resistor was utilized to perform this test. If the output voltage does not significantly vary, a PWL current source could be used to produce nearly equivalent results.

Test Results:

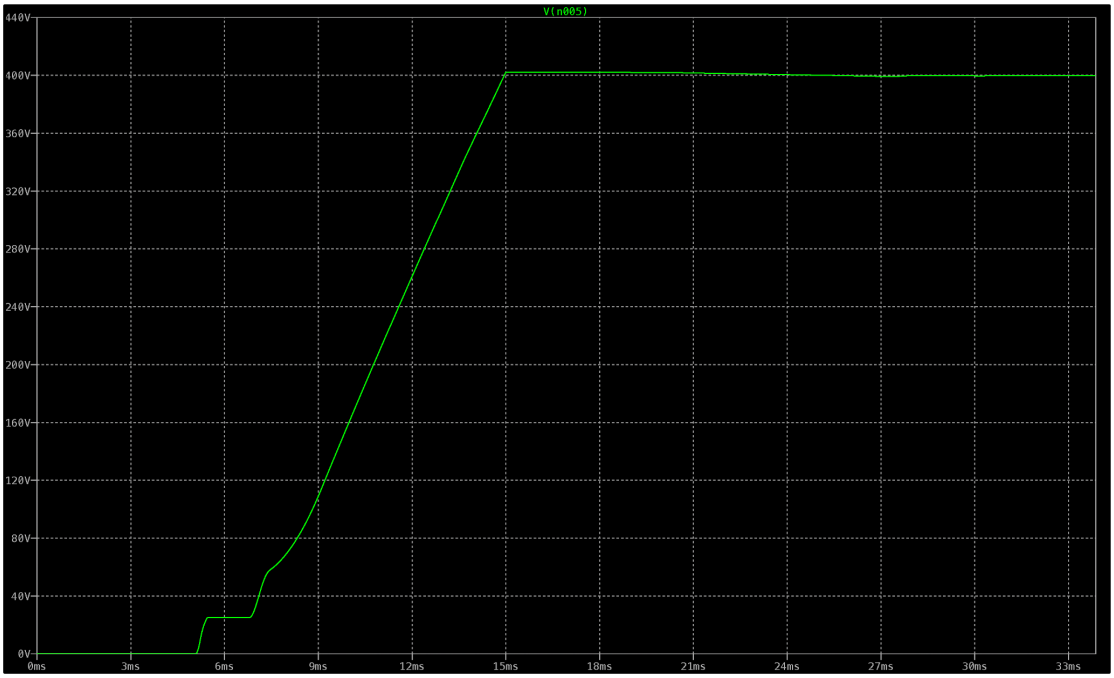


Figure F.9. Output voltage as a function of time for simulation test two. At approximately 15ms, the output voltage settled to 400V. Afterwards, at 20ms a 0.5A load was applied to the output. Lastly, at 30ms, the load transitioned from 0.5A to 8A.

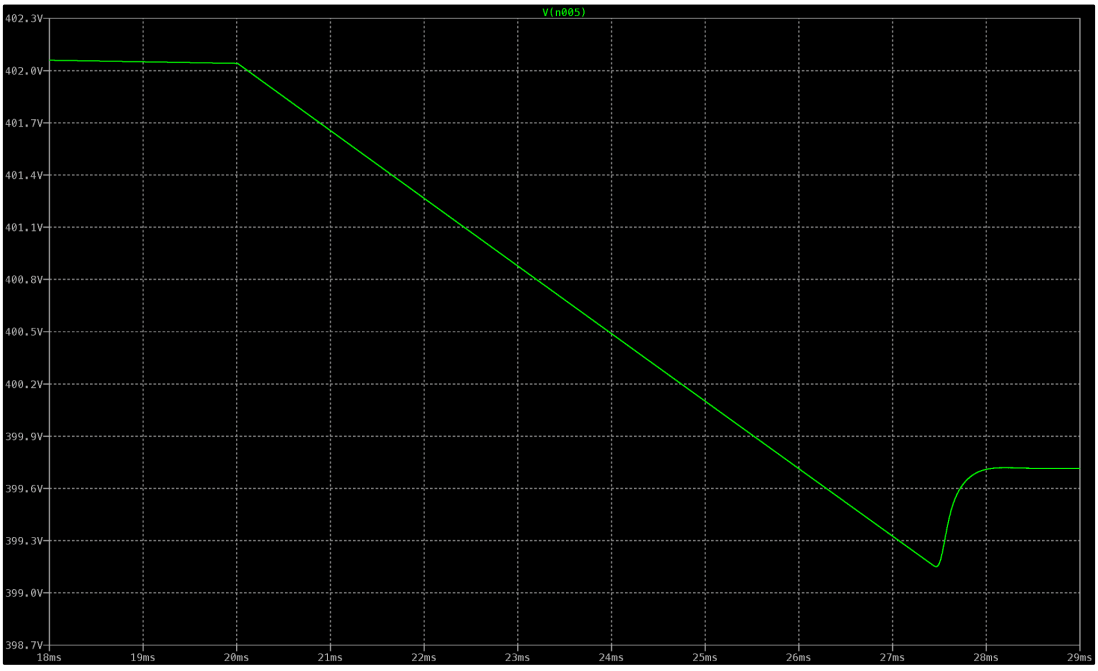


Figure F.10. Response to the application of the 0.5A load from 0A for simulation test two. The transients decayed after approximately 8ms. Additionally, the undershoot is nearly 600mV and the ripple once steady-state is achieved appears negligible.

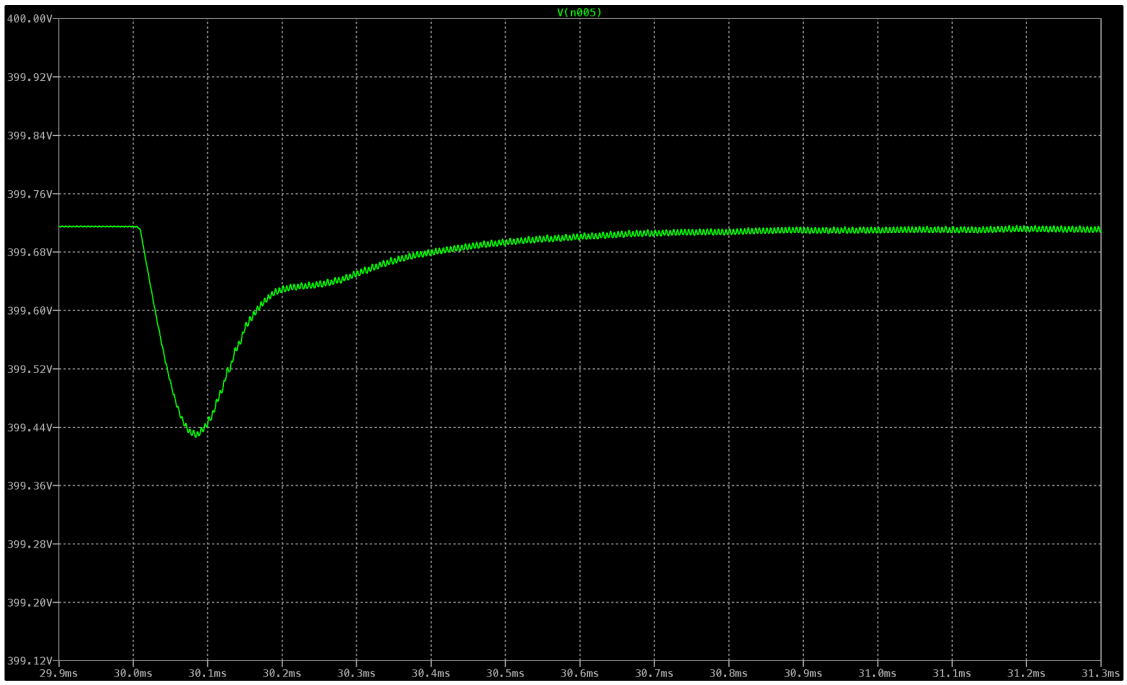


Figure F.11. Response to the application of the 8A load from 0.5A for simulation test two. The transients decayed after approximately 1.2ms. Additionally, the undershoot is nearly 300mV and the ripple once steady-state is achieved appears negligible.

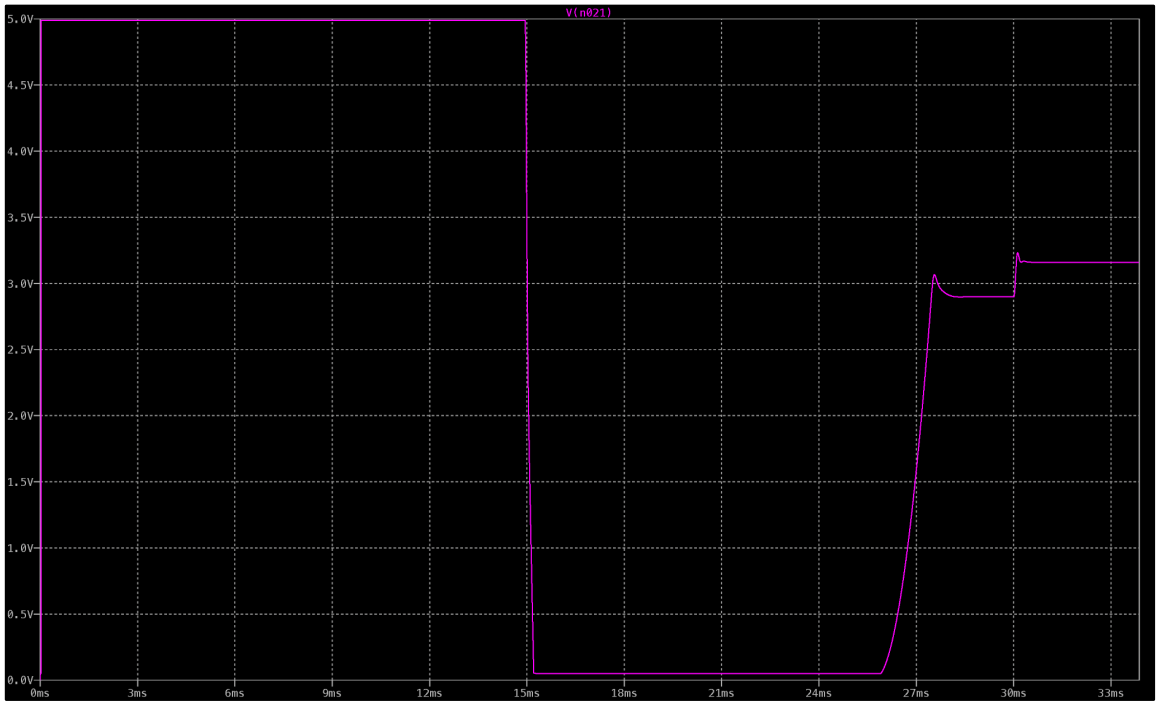


Figure F.12. Voltage waveform on the COMP pin with respect to ground for simulation test two. Compare this figure with Figure F.9 to discern what each nearly constant voltage interval corresponds to.

## F.3 Simulation Test Three

Test Description:

To properly perform this test, apply an input voltage of 50V to the converter and allow the output to settle to 280V before applying any load. After the output voltage settles, apply an 11A load. Once the voltage settles again, change the load to 0.5A.

Test Setup:

The input of the three-phase push pull converter in simulation test three is the same as shown in Figure F.2. On the contrary, the output setup is different.

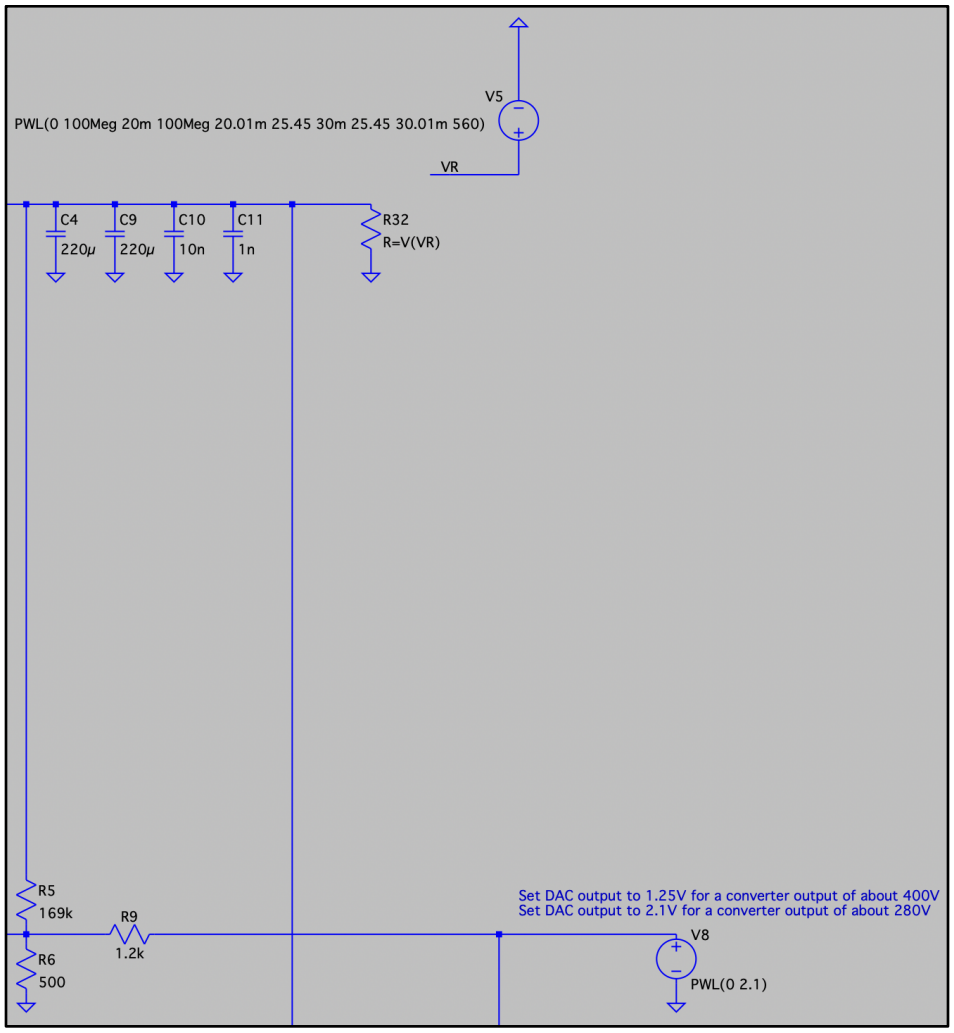


Figure F.13. Output and DAC of the three-phase push-pull converter for simulation test three. A variable resistor was utilized to perform this test. If the output voltage does not significantly vary, a PWL current source could be used to produce nearly equivalent results.

Test Results:

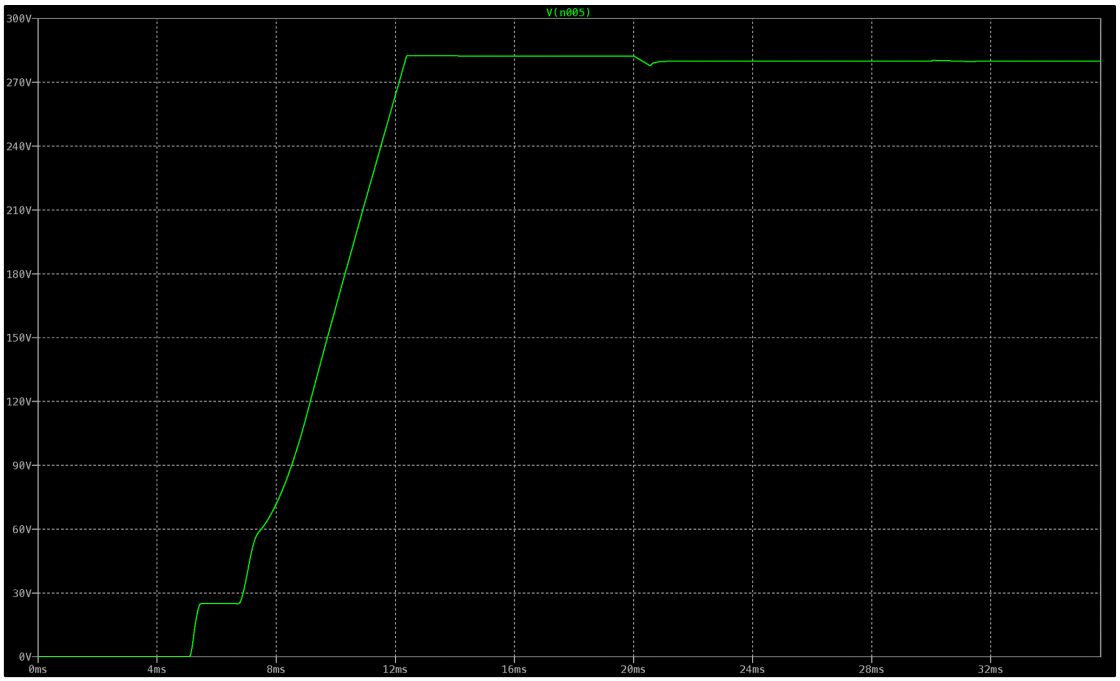


Figure F.14. Output voltage as a function of time for simulation test three. At approximately 12.5ms, the output voltage settled to 280V. Afterwards, at 20ms an 11A load was applied to the output. Lastly, at 30ms, the load transitioned from 11A to 0.5A.

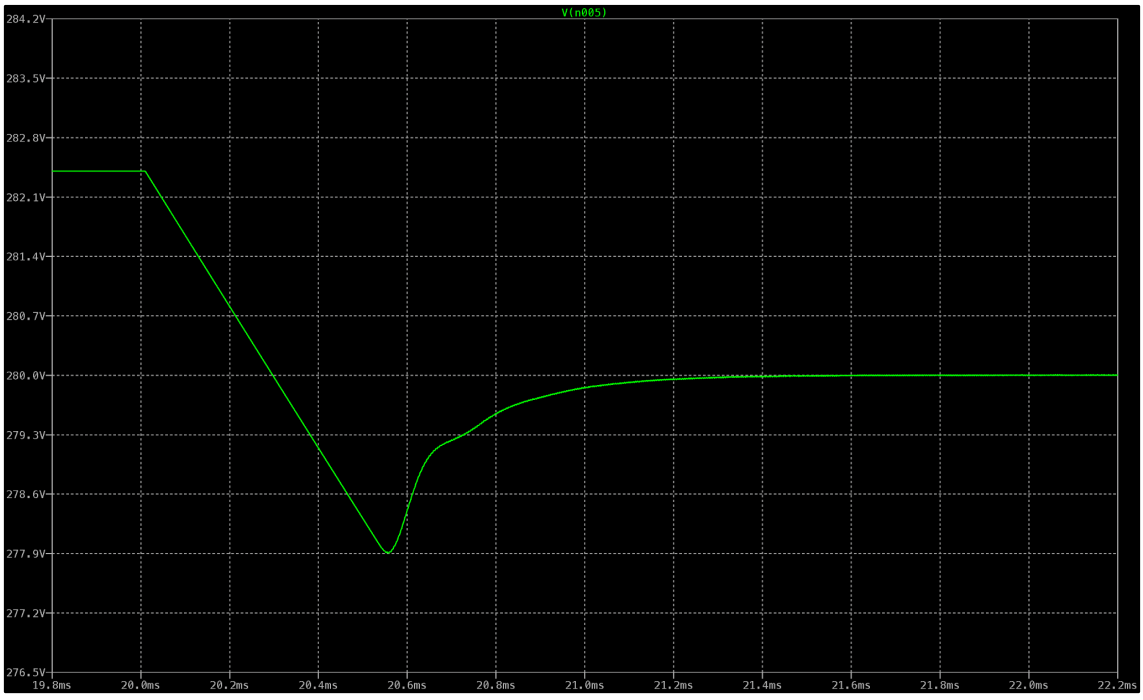


Figure F.15. Response to the application of the 11A load from 0A for simulation test three. The transients decayed after approximately 1.6ms. Additionally, the undershoot is approximately 2.1V and the ripple once steady-state is achieved appears negligible.

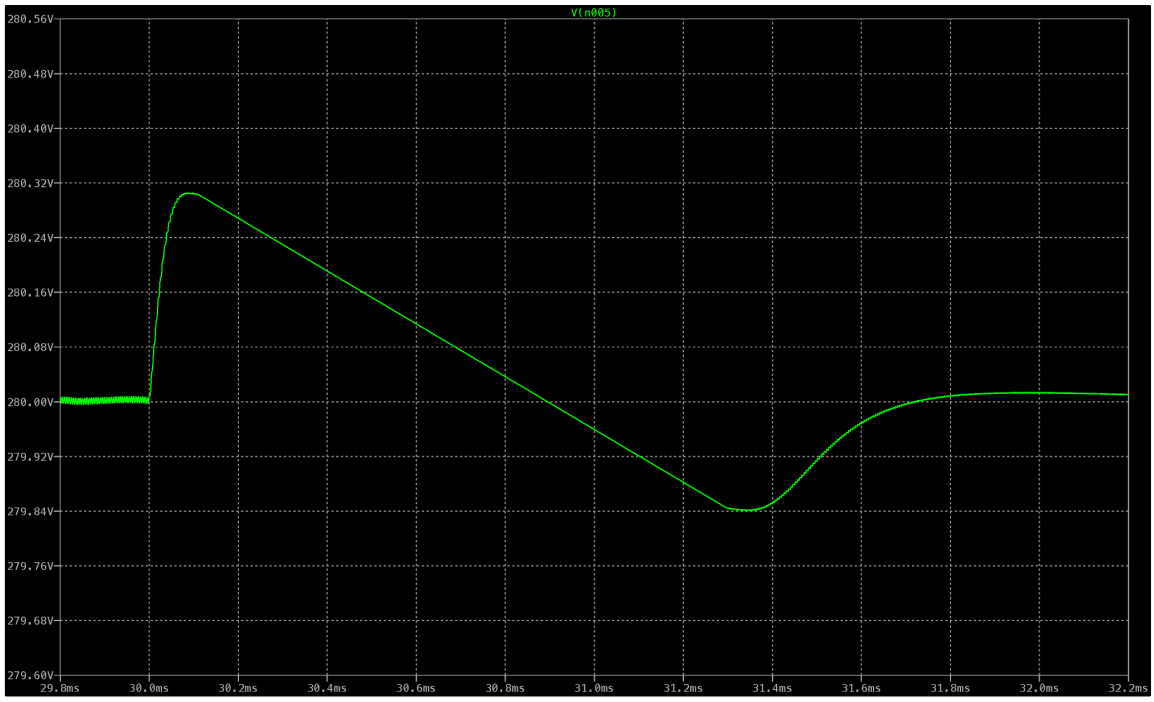


Figure F.16. Response to the application of the 0.5A load from 11A for simulation test three. The transients decayed after 2ms. Additionally, the overshoot is 300mV, undershoot 170mV, and the ripple once steady-state is achieved appears negligible.

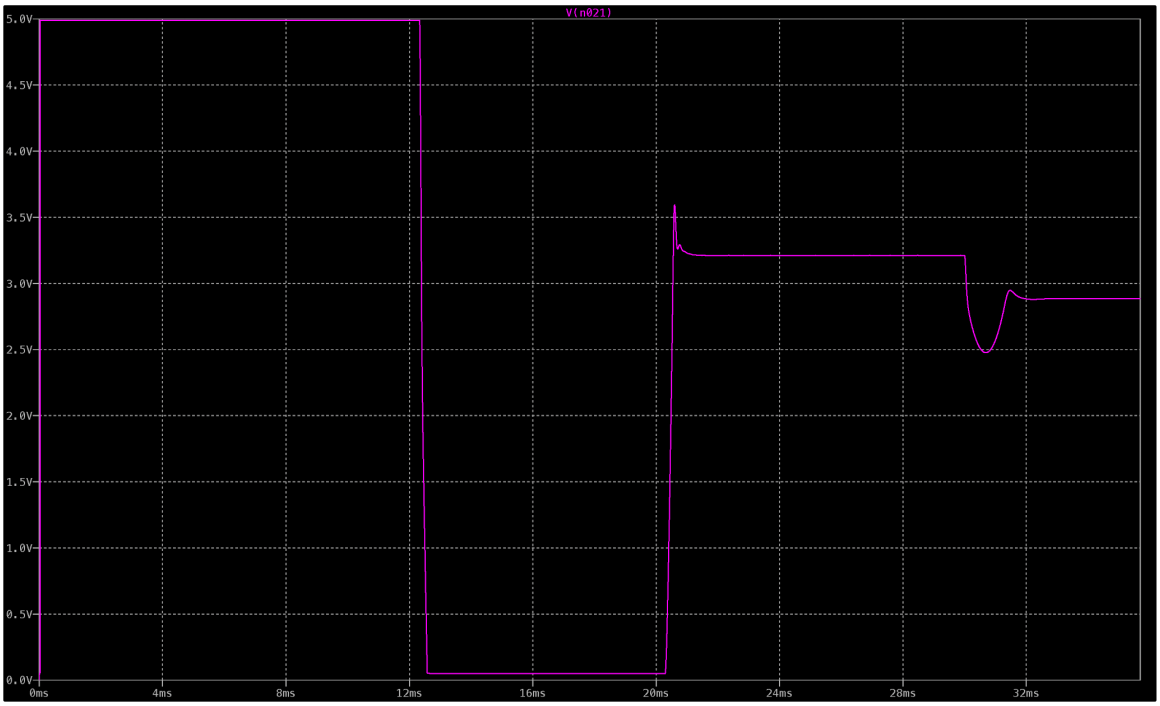


Figure F.17. Voltage waveform on the COMP pin with respect to ground for simulation test three. Compare this figure with Figure F.14 to discern what each nearly constant voltage interval corresponds to.

## F.4 Simulation Test Four

Test Description:

To properly perform this test, apply an input voltage of 50V to the converter and allow the output to settle to 280V before applying any load. After the output voltage settles, apply an 0.5A load. Once the voltage settles again, change the load to 11A.

Test Setup:

The input of the three-phase push pull converter in simulation test four is the same as shown in Figure F.2. On the contrary, the output setup is different.

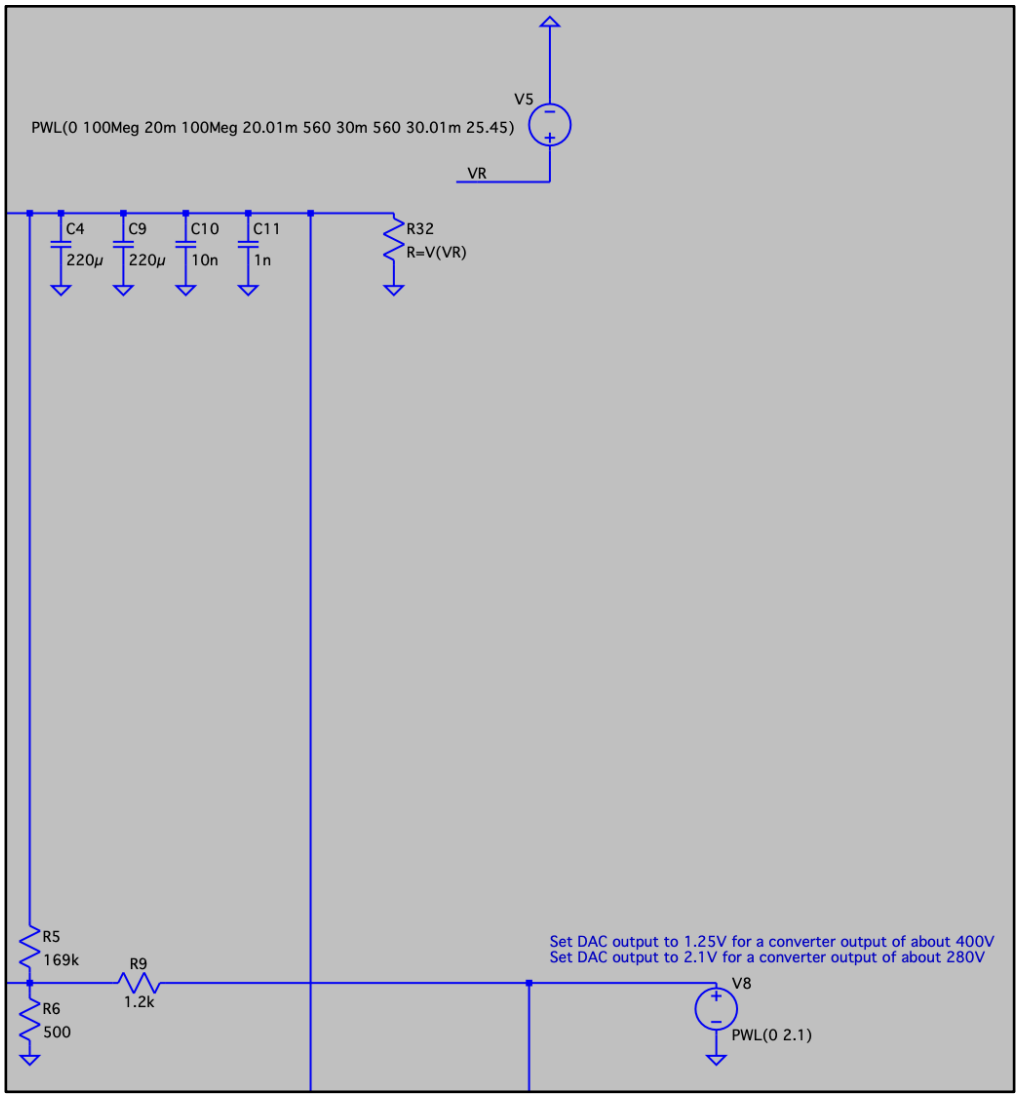


Figure F.18. Output and DAC of the three-phase push-pull converter for simulation test four. A variable resistor was utilized to perform this test. If the output voltage does not significantly vary, a PWL current source could be used to produce nearly equivalent results.

Test Results:

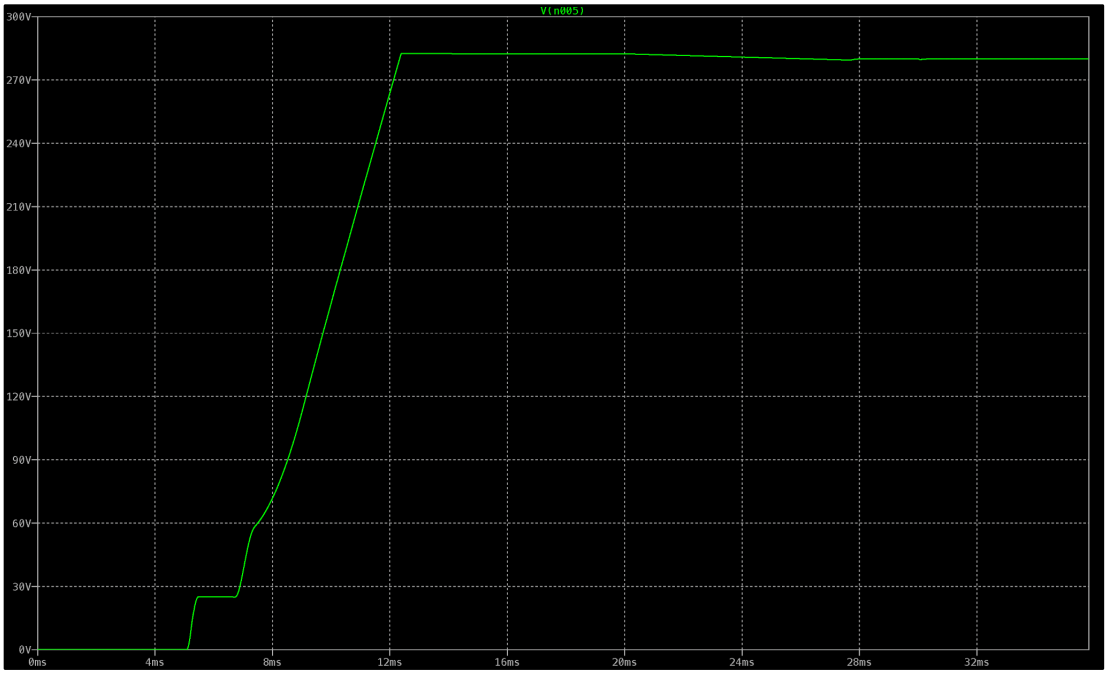


Figure F.19. Output voltage as a function of time for simulation test four. At approximately 12.5ms, the output voltage settled to 280V. Afterwards, at 20ms a 0.5A load was applied to the output. Lastly, at 30ms, the load transitioned from 0.5A to 11A.

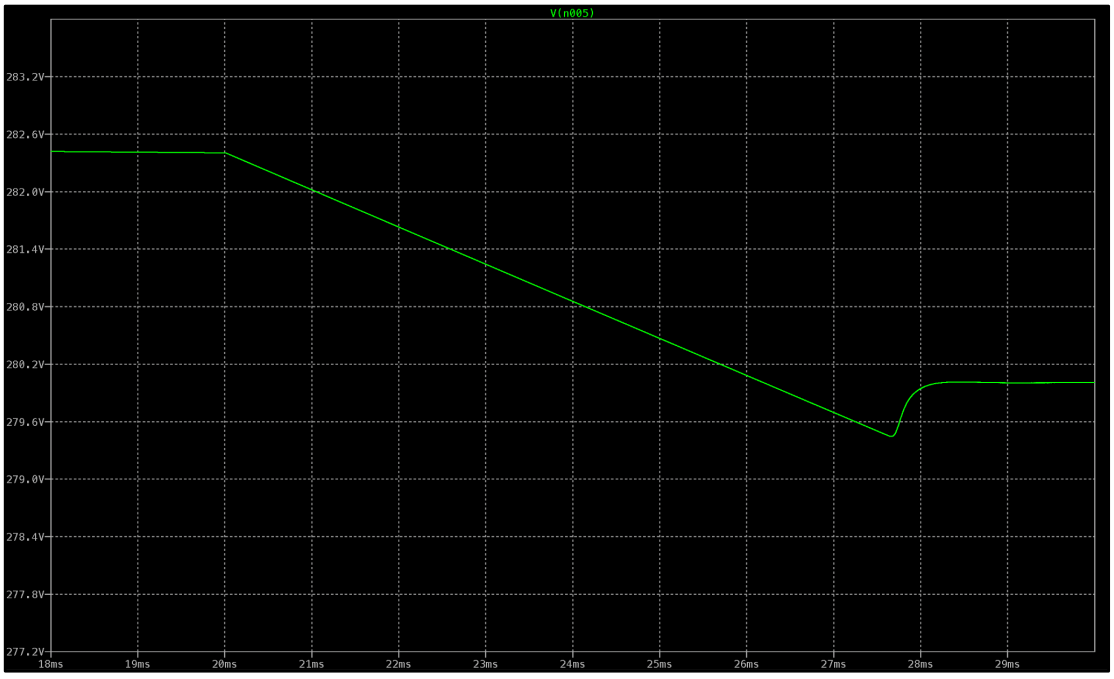


Figure F.20. Response to the application of the 0.5A load from 0A for simulation test four. The transients decayed after approximately 9ms. Additionally, the undershoot is about 600mV and the ripple once steady-state is achieved appears negligible.

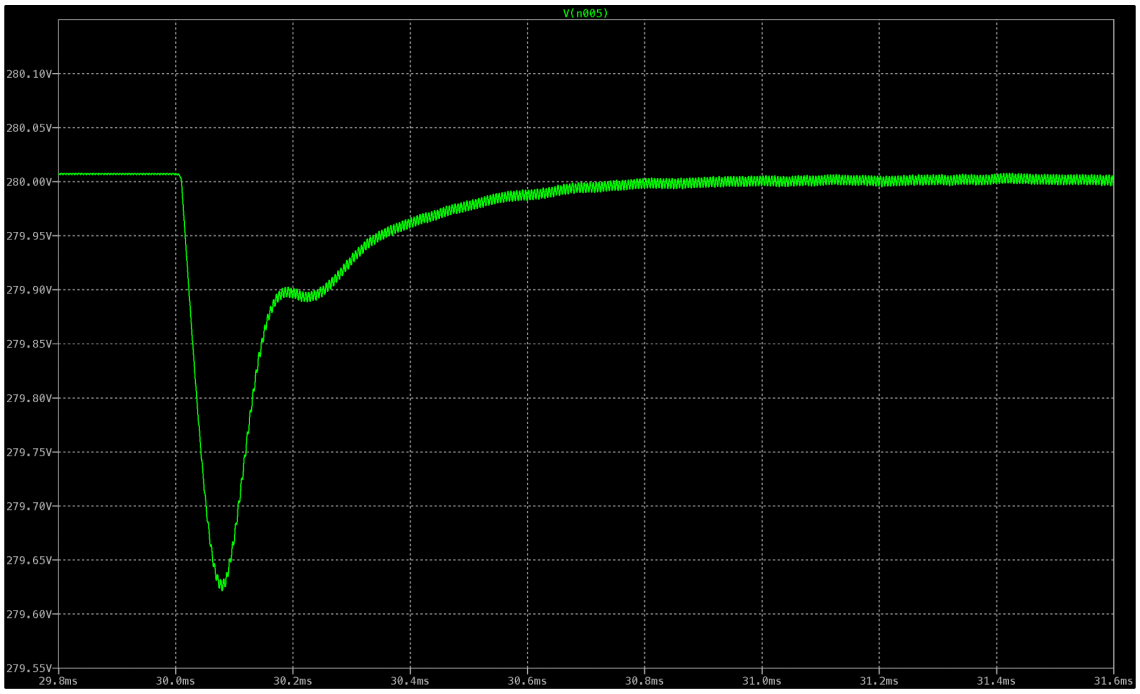


Figure F.21. Response to the application of the 11A load from 0.5A for simulation test four. The transients decayed after approximately 1ms. Additionally, the undershoot is nearly 400mV and the ripple once steady-state is achieved appears negligible.

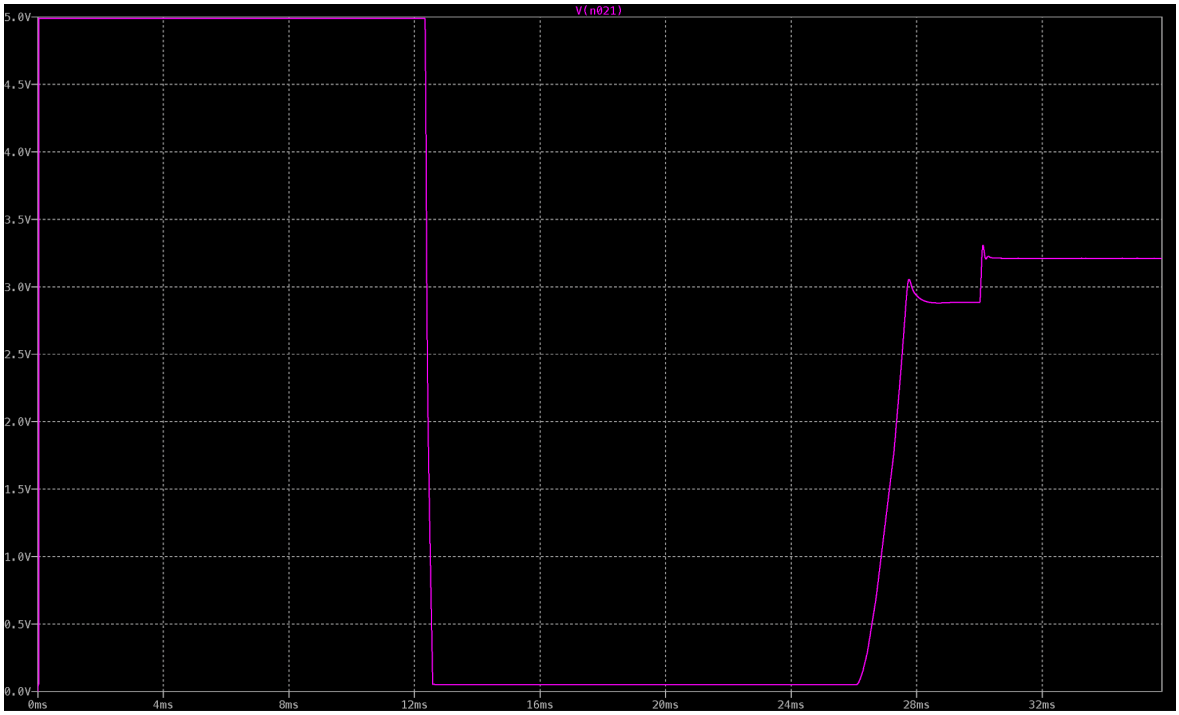


Figure F.22. Voltage waveform on the COMP pin with respect to ground for simulation test four. Compare this figure with Figure F.19 to discern what each nearly constant voltage interval corresponds to.

## F.5 Simulation Test Five

Test Description:

To properly perform this test, apply an input voltage of 50V to the converter and allow the output to settle to 400V before applying any load. After the output voltage settles, apply a resistance of 50Ω to the output. Once the voltage settles again, use the DAC to change the output voltage from 400V to 280V.

Test Setup:

The input of the three-phase push pull converter in simulation test five is the same as shown in Figure F.2. On the contrary, the output setup is different.

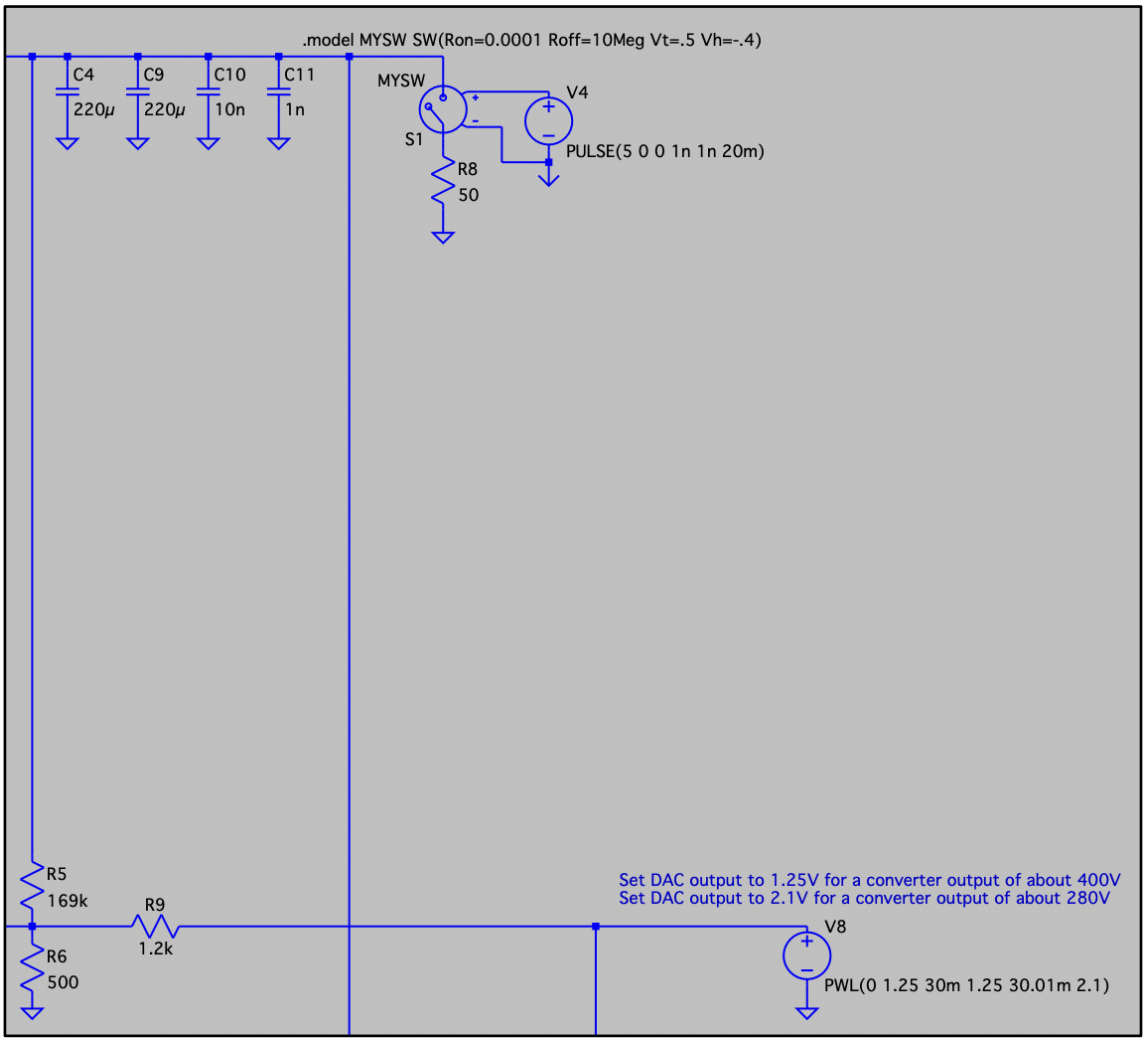


Figure F.23. Output and DAC of the three-phase push-pull converter for simulation test five. A resistor in series with an ideal switch was utilized to perform this test. Please note that the DAC transitions from 1.25V to 2.1V in 0.01ms.

Test Results:

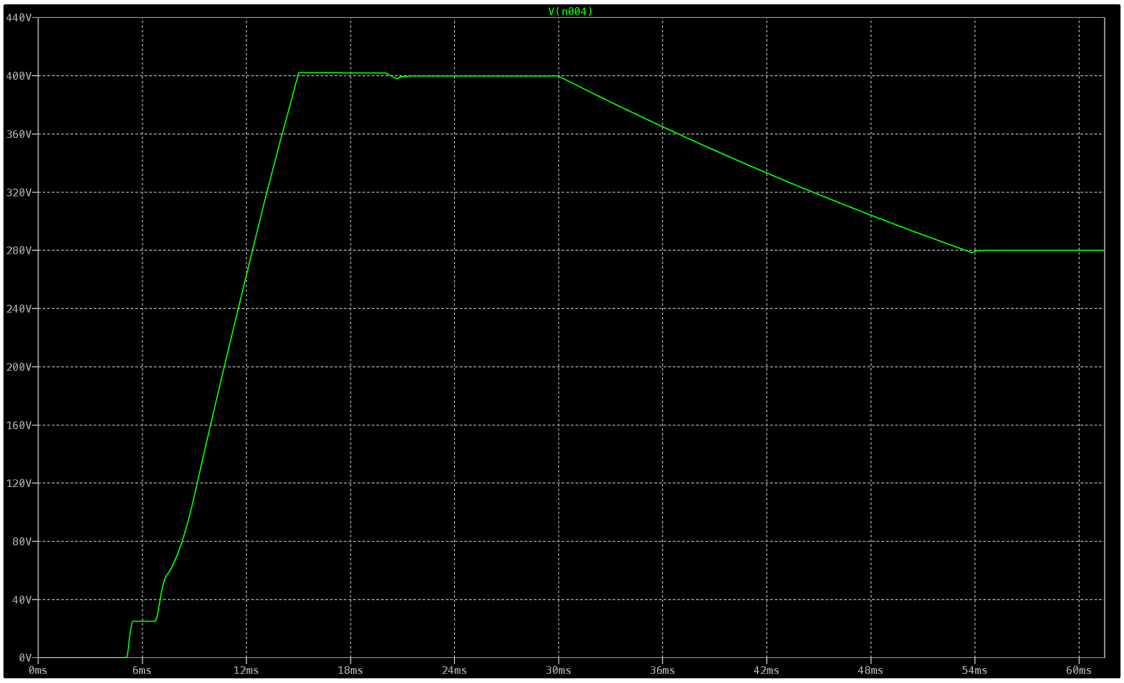


Figure F.24. Output voltage as a function of time for simulation test five. At approximately 15ms, the output voltage settled to 400V. Afterwards, at 20ms a resistor of 50Ω was applied to the output. Lastly, from 30ms to 54ms, the output voltage transitioned from 400V to 280V.

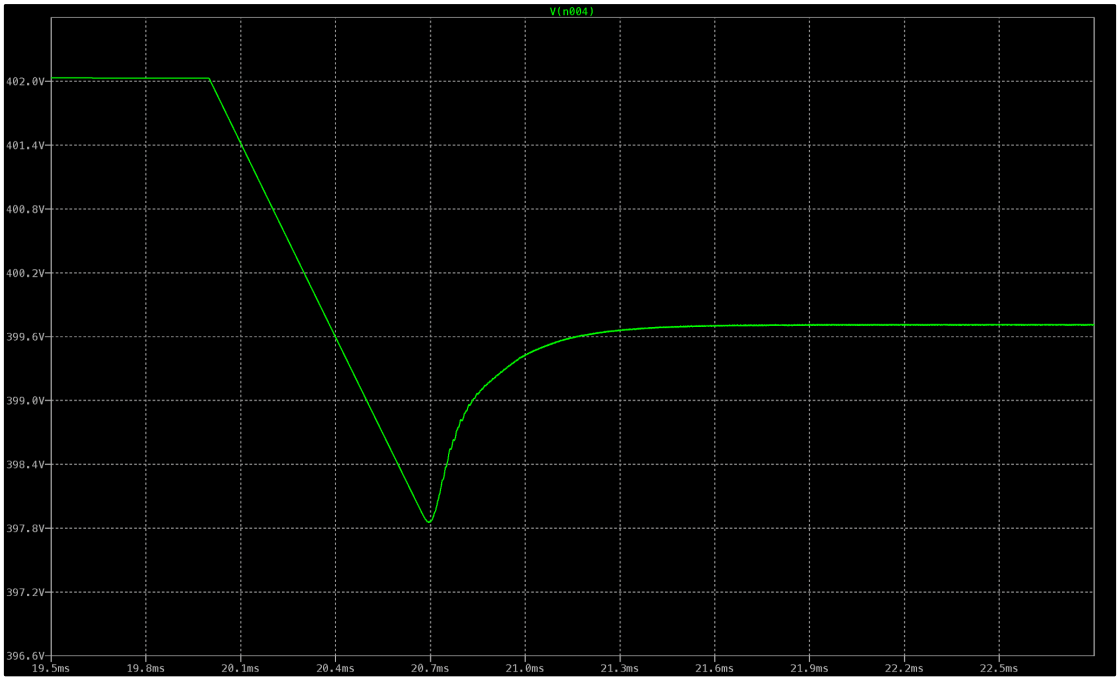


Figure F.25. Response to the application of the resistor of 50Ω for simulation test five. The transients decayed after approximately 2ms. Additionally, the undershoot is about 1.8V and the ripple once steady-state is achieved appears negligible.

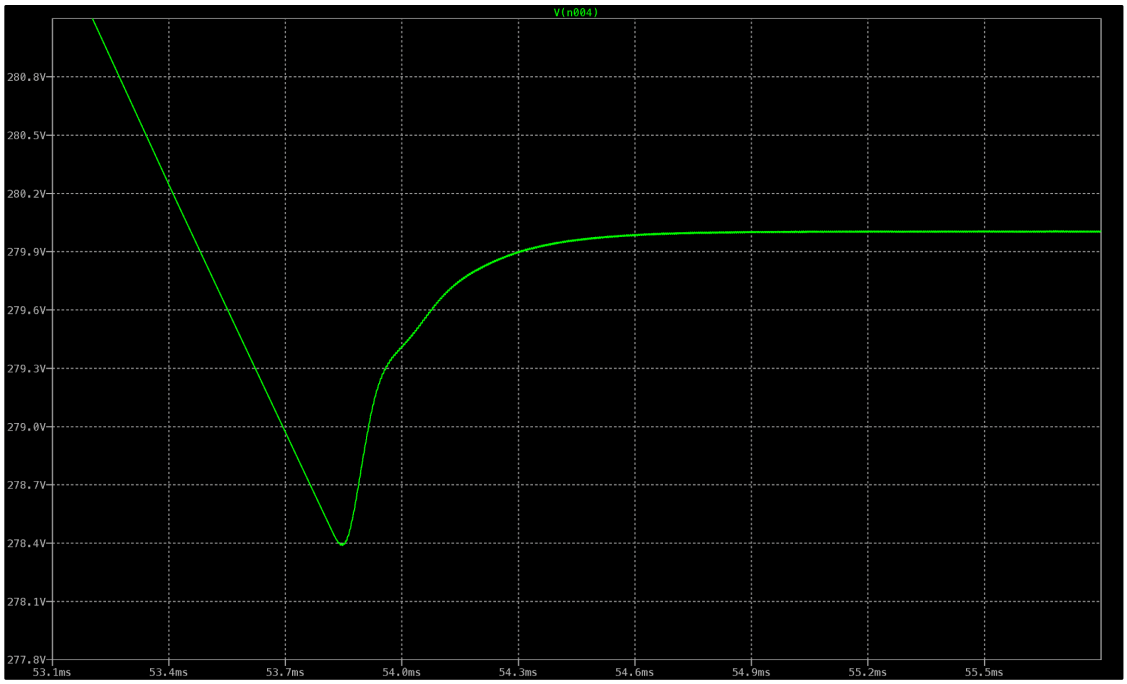


Figure F.26. Response to transitioning from 400V to 280V. When the output first attained 280V, the transients decayed after approximately 2ms. Additionally, the undershoot is nearly 1.6V and the ripple once steady-state is achieved appears negligible.

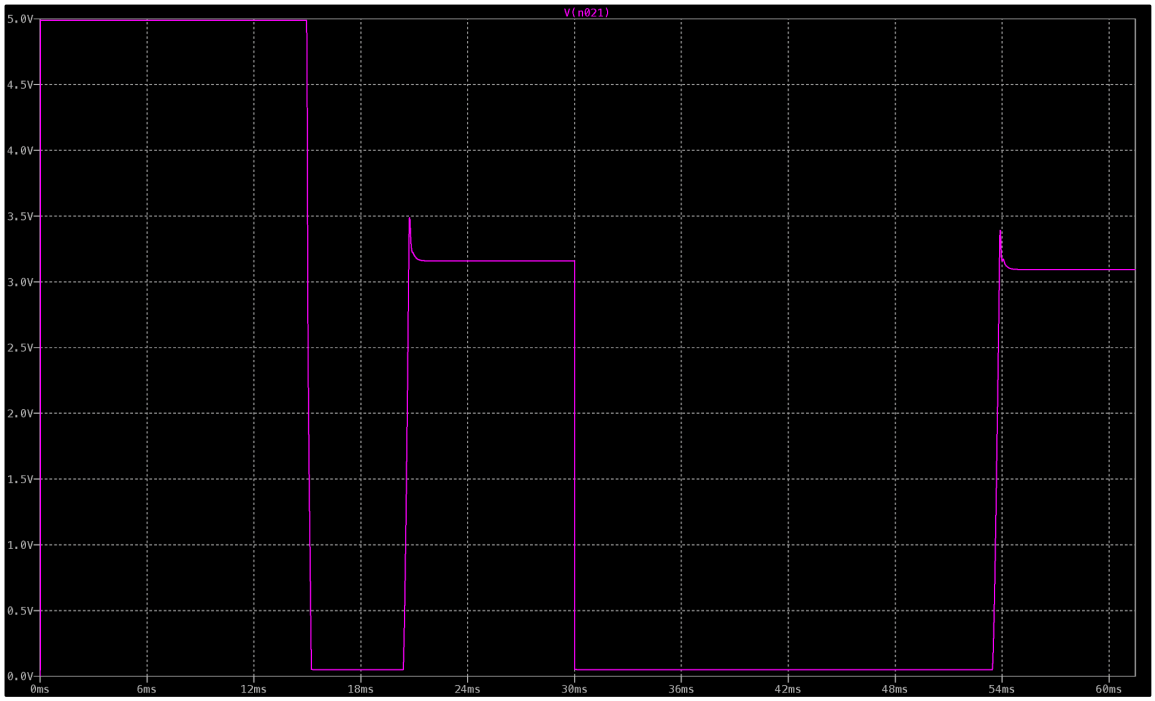


Figure F.27. Voltage waveform on the COMP pin with respect to ground for simulation test five. Compare this figure with Figure F.24 to discern what each non-zero voltage interval corresponds to.

## F.6 Simulation Test Six

Test Description:

To properly perform this test, apply an input voltage of 50V to the converter and allow the output to settle to 400V before applying any load. After the output voltage settles, apply a resistance of 800Ω to the output. Once the voltage settles again, use the DAC to change the output voltage from 400V to 280V.

Test Setup:

The input of the three-phase push pull converter in simulation test six is the same as shown in Figure F.2. On the contrary, the output setup is different.

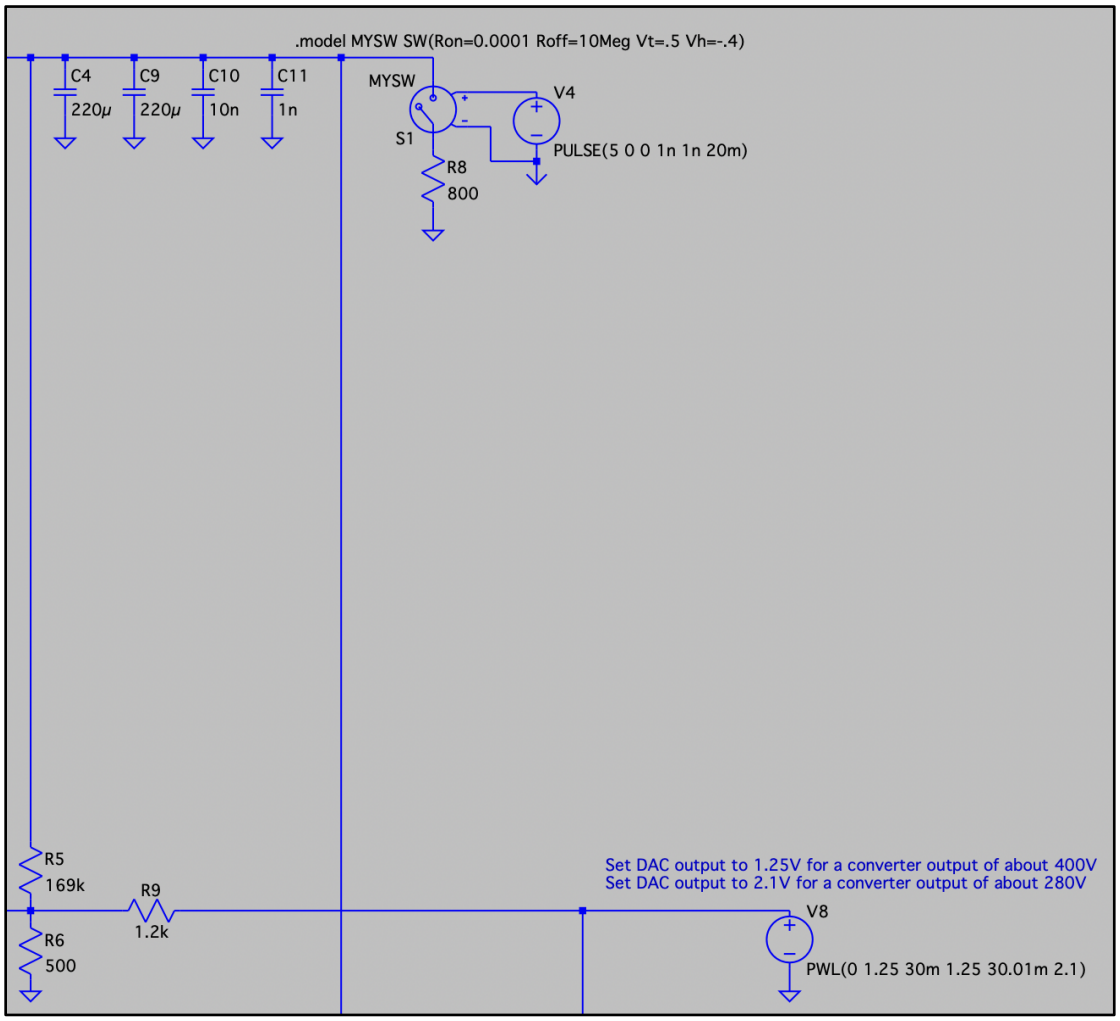


Figure F.28. Output and DAC of the three-phase push-pull converter for simulation test six. A resistor in series with an ideal switch was utilized to perform this test. Please note that the DAC transitions from 1.25V to 2.1V in 0.01ms.

Test Results:

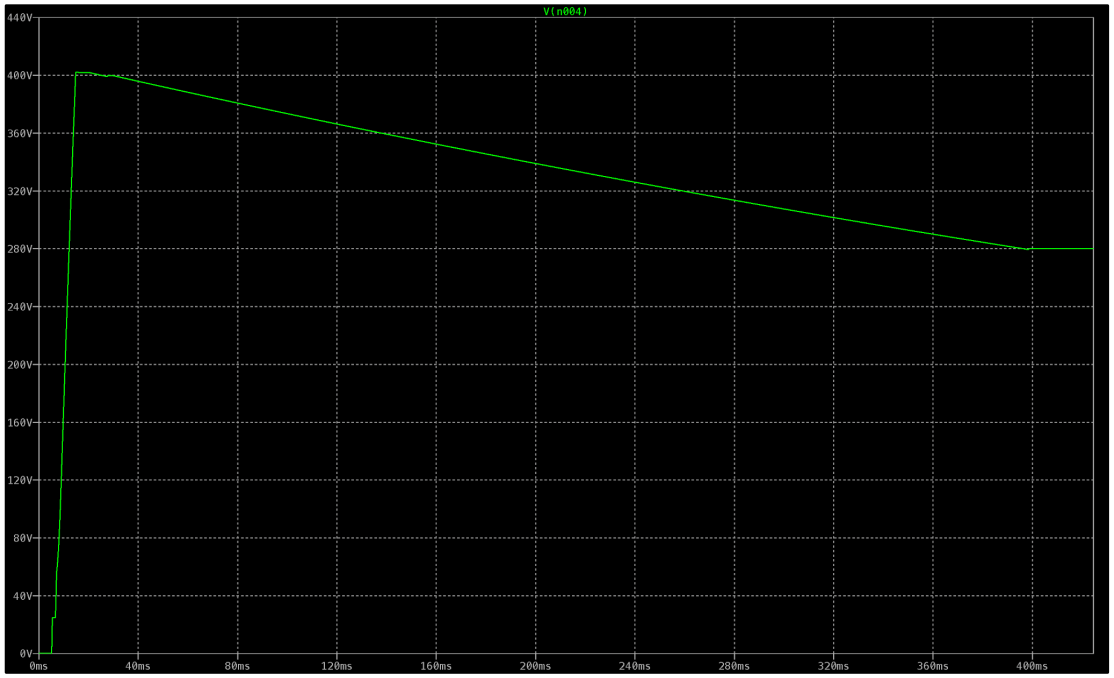


Figure F.29. Output voltage as a function of time for simulation test six. At approximately 15ms, the output voltage settled to 400V. Afterwards, at 30ms a resistor of 800Ω was applied to the output. Lastly, from 30ms to 400ms, the output voltage transitioned from 400V to 280V.

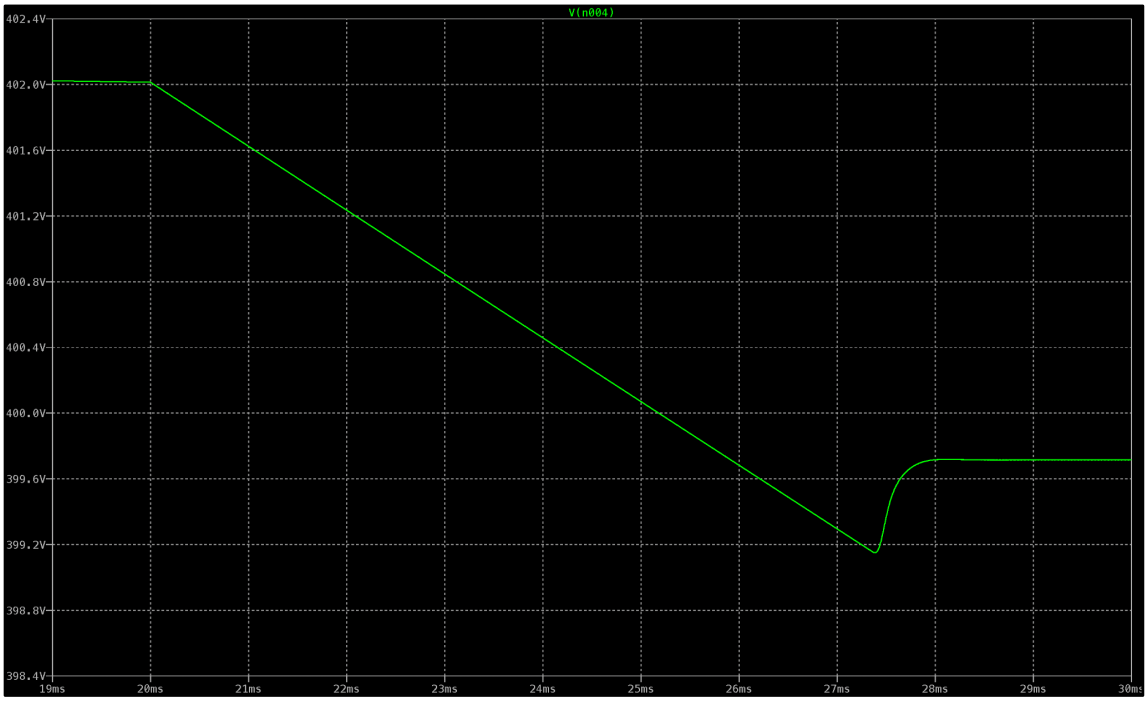


Figure F.30. Response to the application of the resistor of 800Ω for simulation test six. The transients decayed after approximately 8ms. Additionally, the undershoot is about 600mV and the ripple once steady-state is achieved appears negligible.

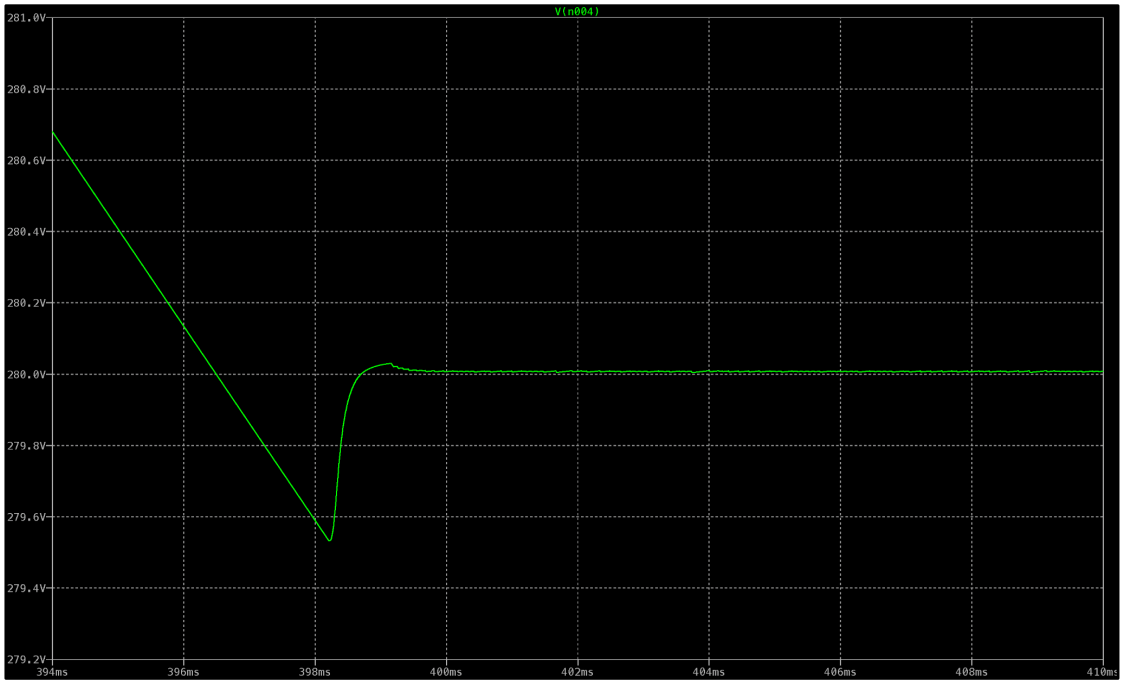


Figure F.31. Response to transitioning from 400V to 280V. When the output first attained 280V, the transients decayed after approximately 4ms. Additionally, the undershoot is approximately 500mV and the ripple once steady-state is achieved appears negligible.

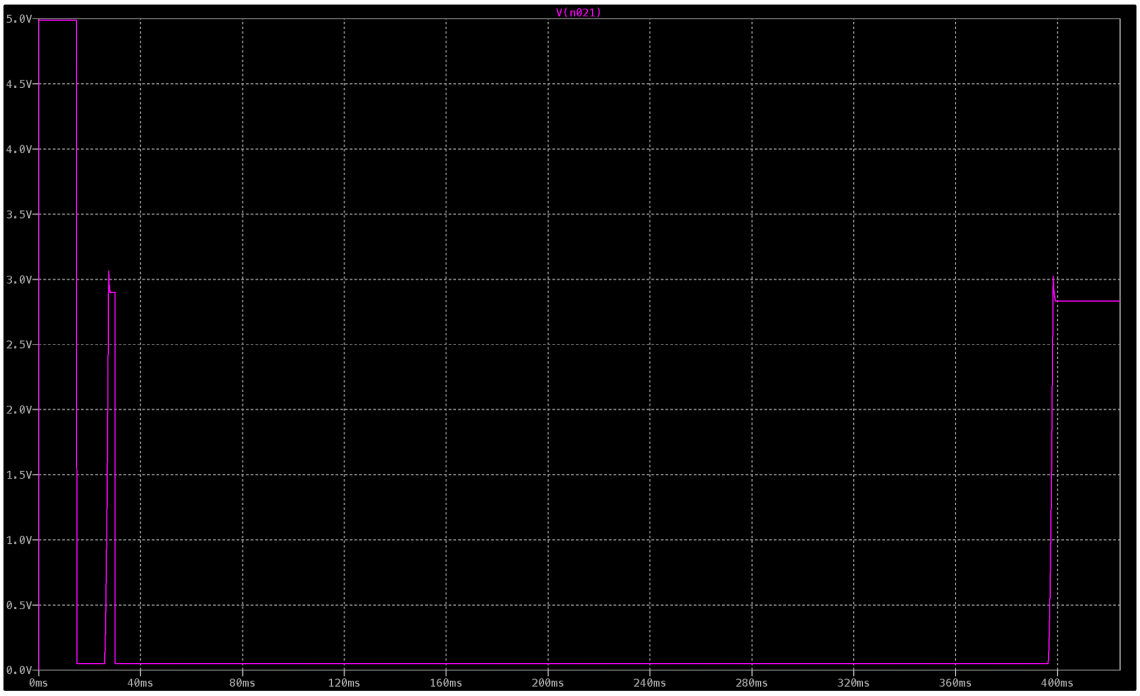


Figure F.32. Voltage waveform on the COMP pin with respect to ground for simulation test six. Compare this figure with Figure F.29 to discern what each non-zero voltage interval corresponds to.

## F.7 Simulation Test Seven

Test Description:

To properly perform this test, apply an input voltage of 50V to the converter and allow the output to settle to 280V before applying any load. After the output voltage settles, apply a resistance of 50Ω to the output. Once the voltage settles again, use the DAC to change the output voltage from 280V to 400V.

Test Setup:

The input of the three-phase push pull converter in simulation test seven is the same as shown in Figure F.2. On the contrary, the output setup is different.

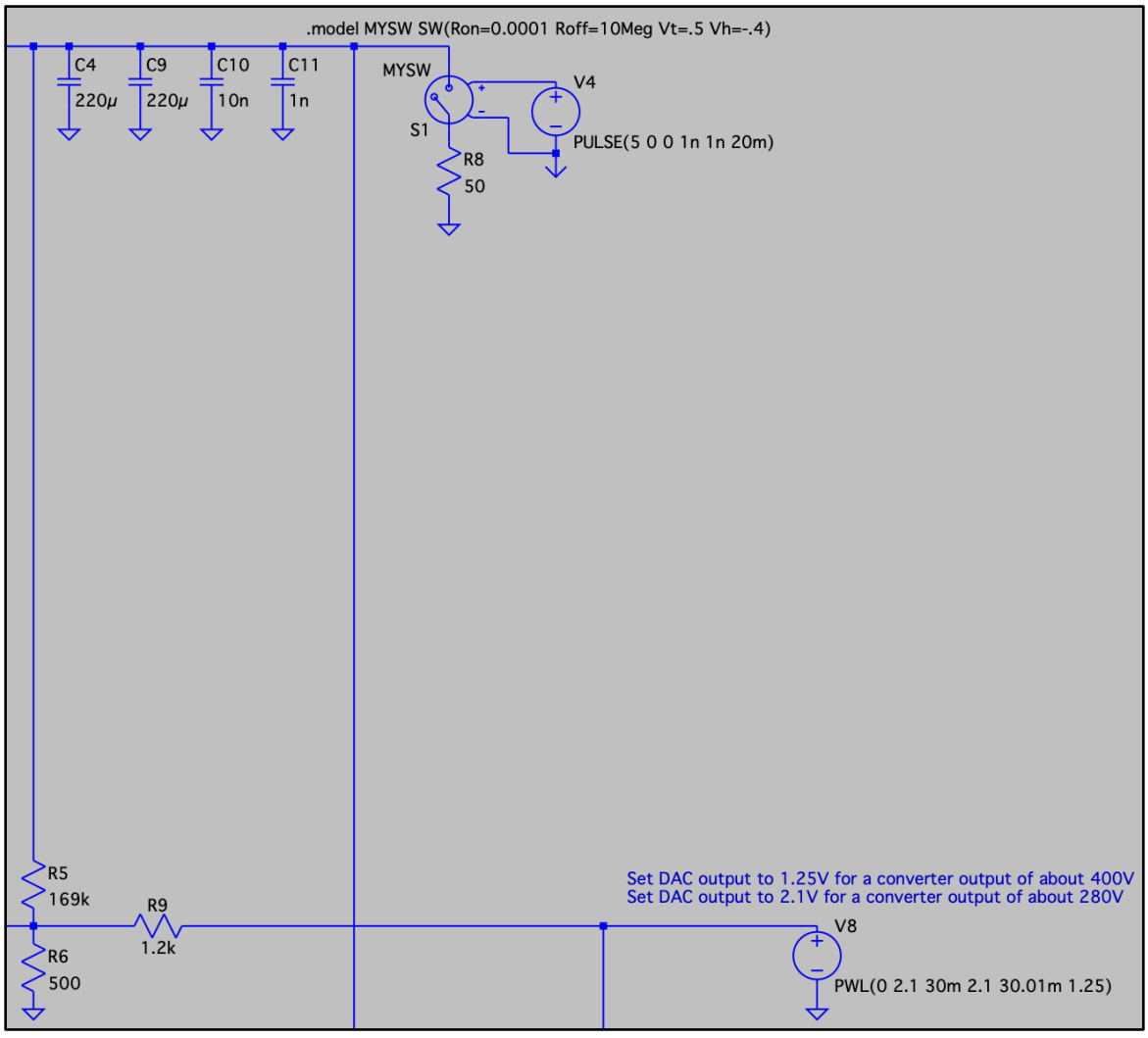


Figure F.33. Output and DAC of the three-phase push-pull converter for simulation test seven. A resistor in series with an ideal switch was utilized to perform this test. Please note that the DAC transitions from 2.1V to 1.25V in 0.01ms.

Test Results:

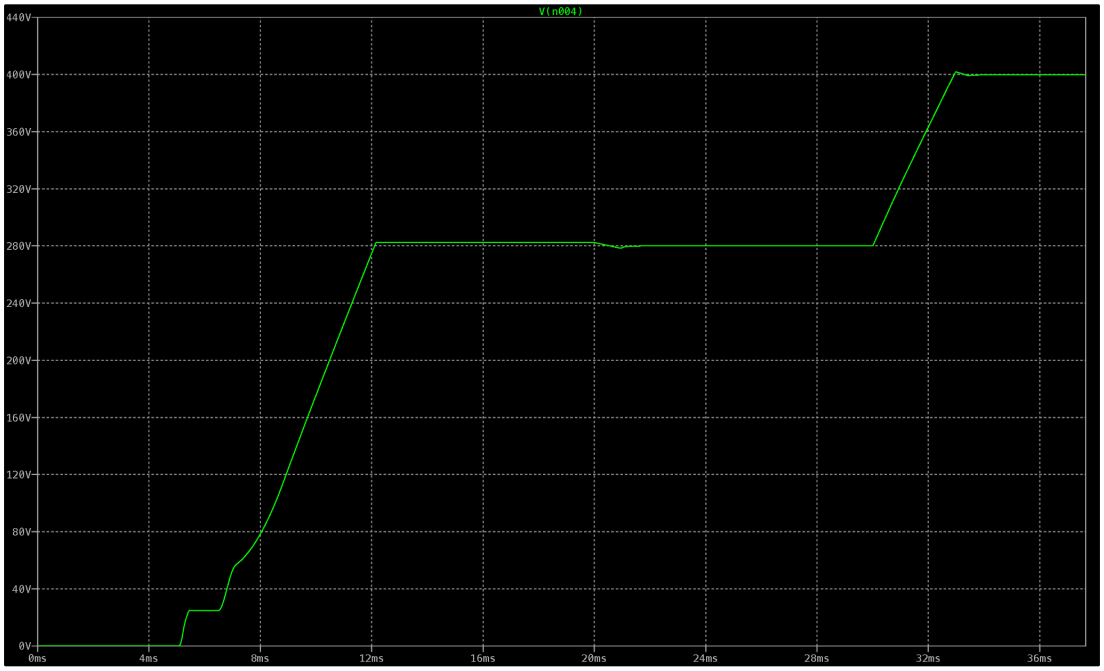


Figure F.34. Output voltage as a function of time for simulation test seven. At approximately 12.5ms, the output voltage settled to 280V. Afterwards, at 30ms a resistor of 50Ω was applied to the output. Lastly, from 30ms to 33ms, the output voltage transitioned from 280V to 400V.

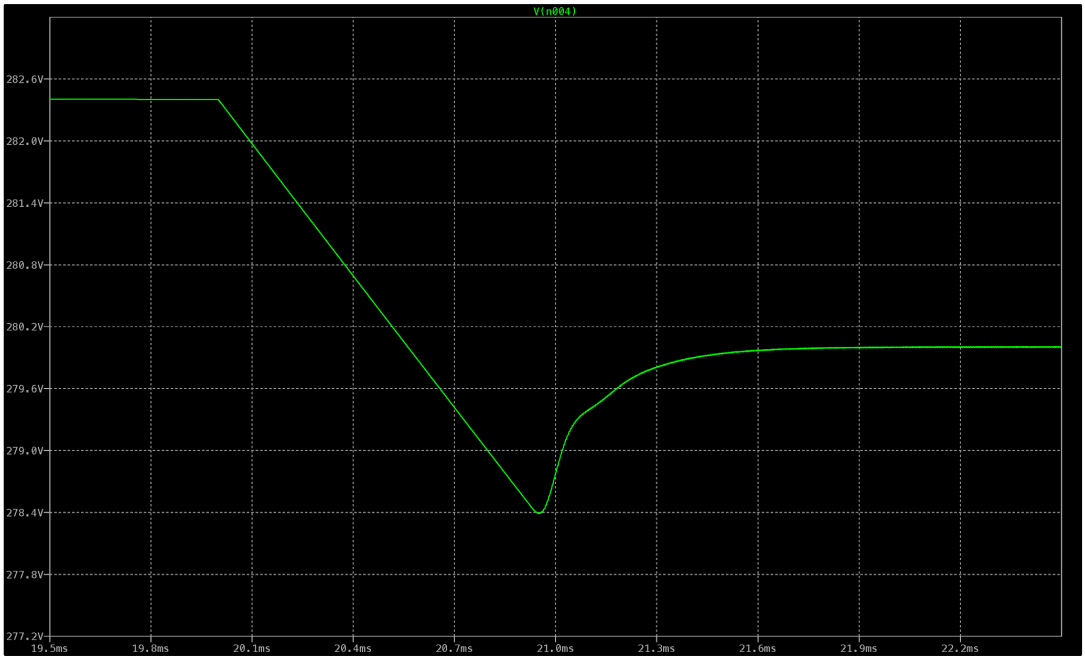


Figure F.35. Response to the application of the resistor of 50Ω for simulation test six. The transients decayed after approximately 2ms. Additionally, the undershoot is about 1.6V and the ripple once steady-state is achieved appears negligible.

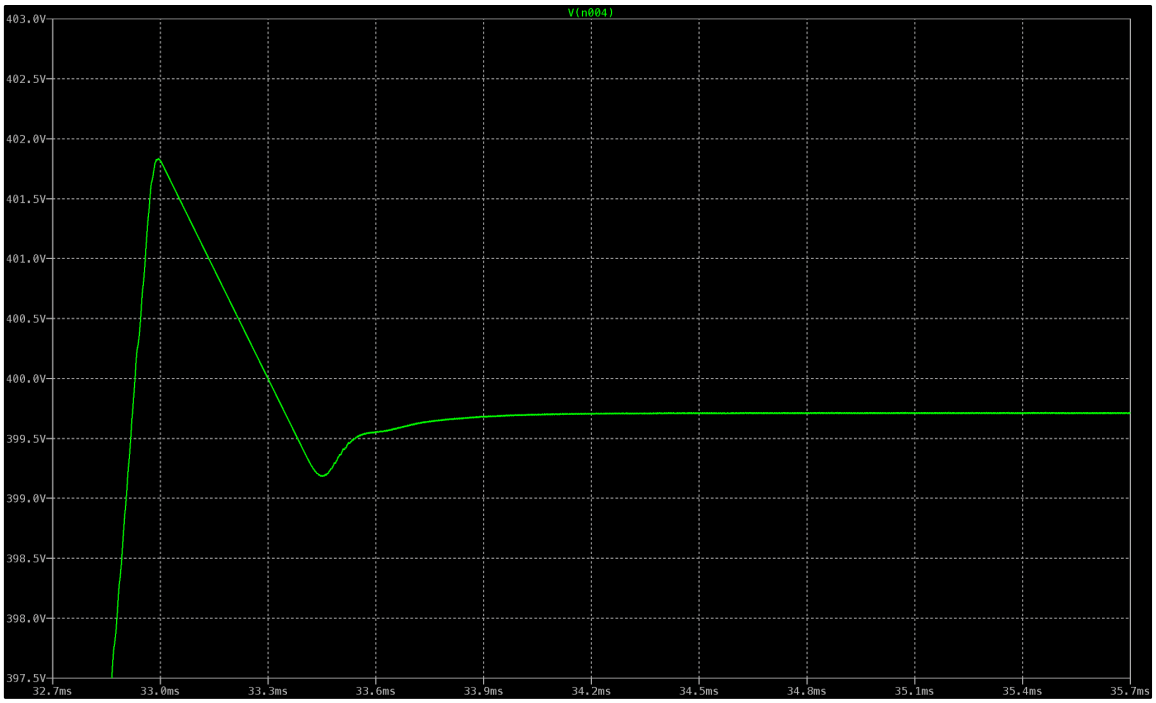


Figure F.36. Response to transitioning from 280V to 400V. When the output first attained 400V, the transients decayed after approximately 1.5ms. Additionally, the overshoot is about 2V and the ripple once steady-state is achieved appears negligible.

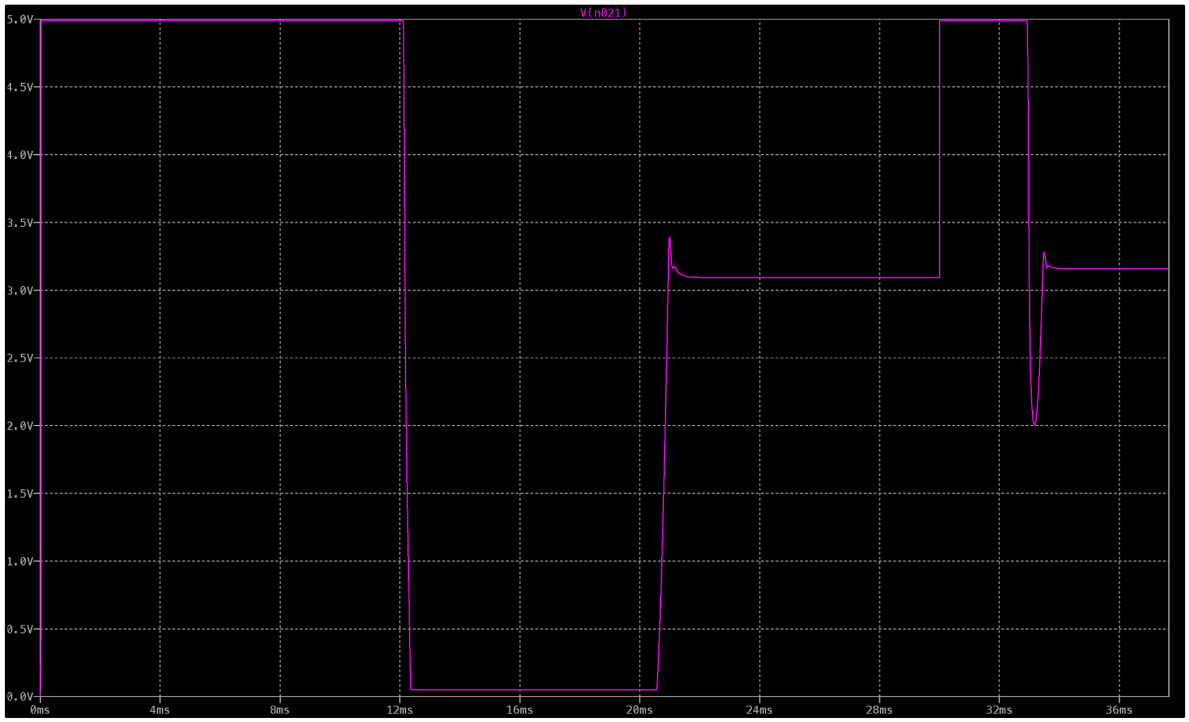


Figure F.37. Voltage waveform on the COMP pin with respect to ground for simulation test seven. Compare this figure with Figure F.34 to discern what each non-zero voltage interval corresponds to.

## F.8 Simulation Test Eight

Test Description:

To properly perform this test, apply an input voltage of 50V to the converter and allow the output to settle to 280V before applying any load. After the output voltage settles, apply a resistance of 800Ω to the output. Once the voltage settles again, use the DAC to change the output voltage from 280V to 400V.

Test Setup:

The input of the three-phase push pull converter in simulation test seven is the same as shown in Figure F.2. On the contrary, the output setup is different.

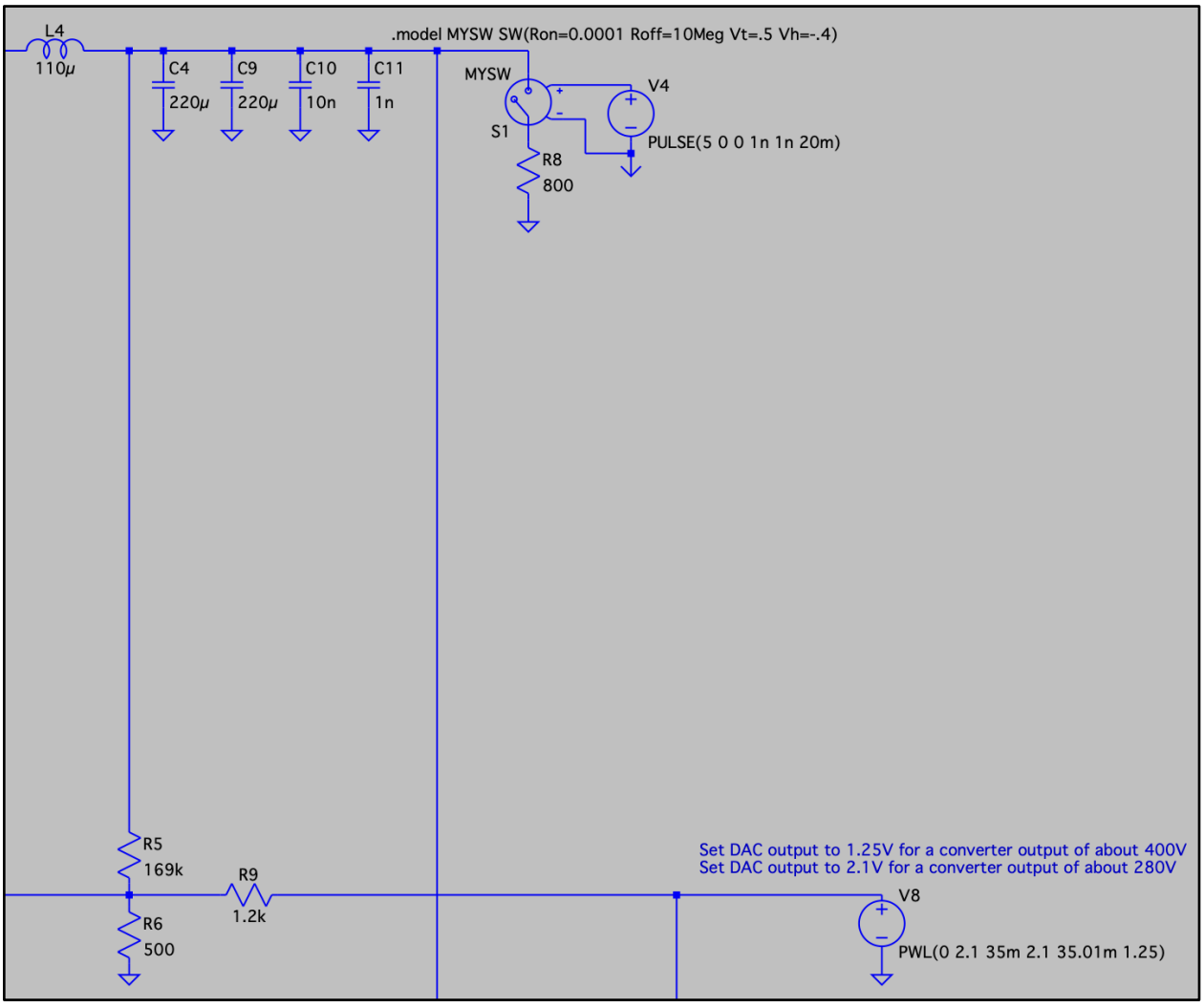


Figure F.38. Output and DAC of the three-phase push-pull converter for simulation test eight. A resistor in series with an ideal switch was utilized to perform this test. Please note that the DAC transitions from 2.1V to 1.25V in 0.01ms.

Test Results:

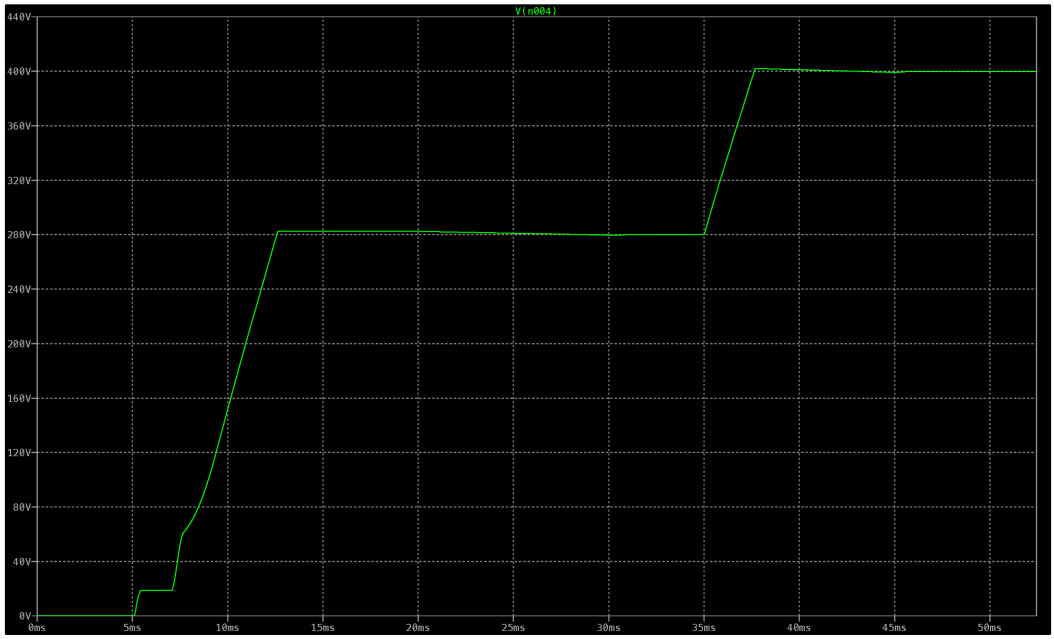


Figure F.39. Output voltage as a function of time for simulation test eight. At approximately 12.5ms, the output voltage settled to 280V. Afterwards, at 35ms a resistor of 800Ω was applied to the output. Lastly, from 35ms to 38ms, the output voltage transitioned from 280V to 400V.

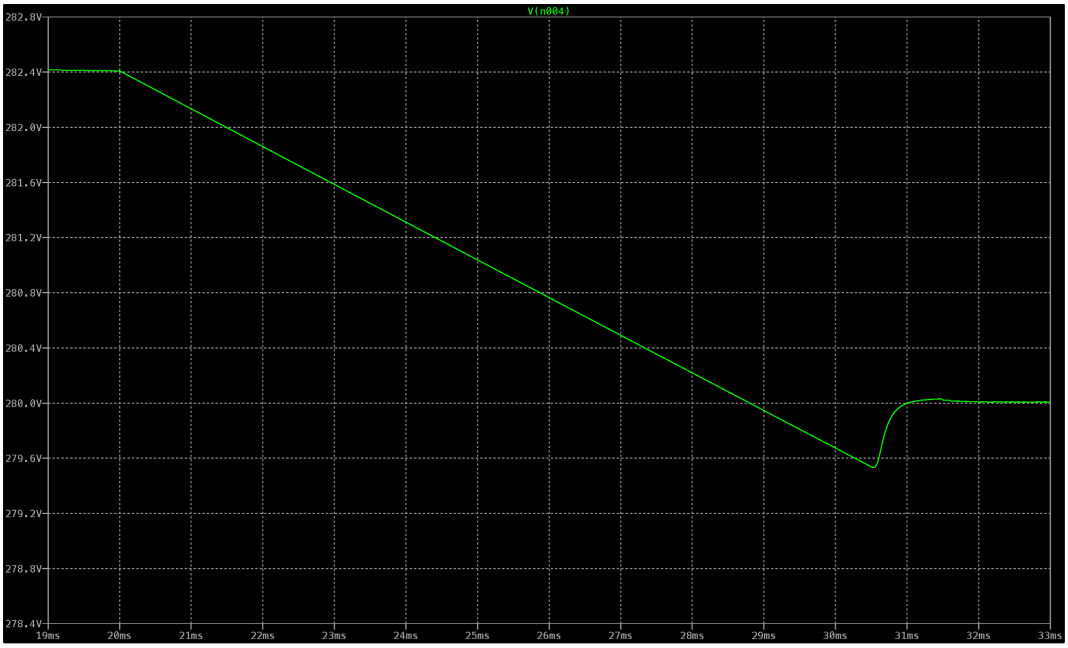


Figure F.40. Response to the application of the resistor of 800Ω for simulation test eight. The transients decayed after approximately 12ms. Additionally, the undershoot is approximately 500mV and the ripple once steady-state is achieved appears negligible.

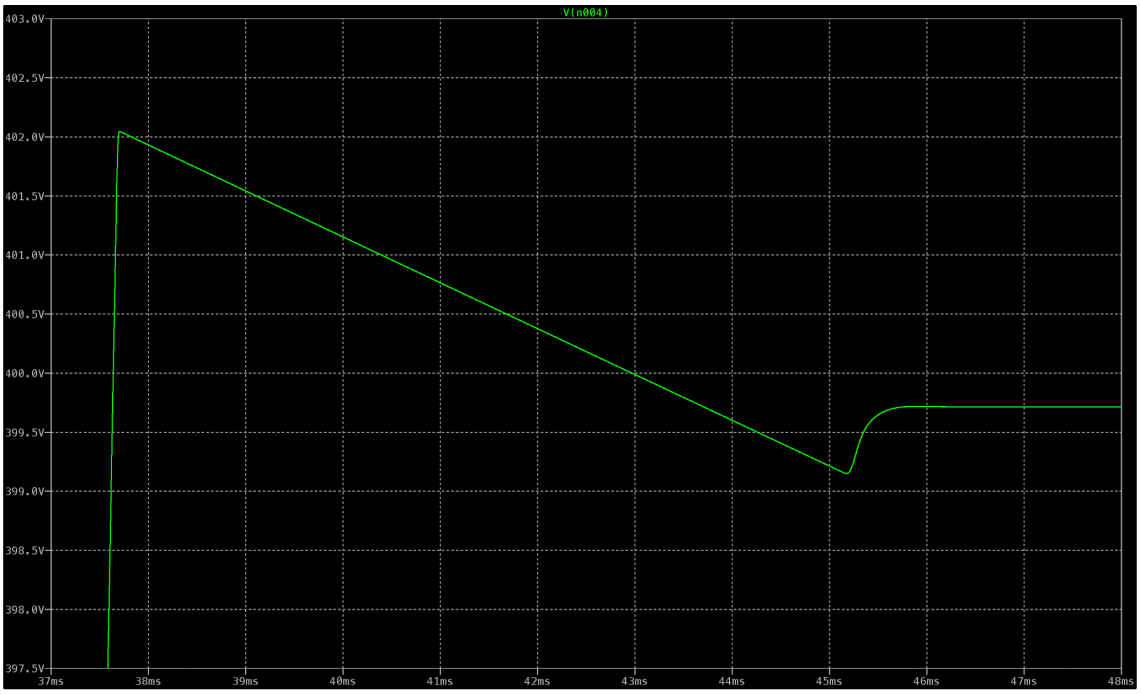


Figure F.41. Response to transitioning from 280V to 400V. When the output first attained 400V, the transients decayed after approximately 9ms. Additionally, the overshoot is about 2V and the ripple once steady-state is achieved appears negligible.

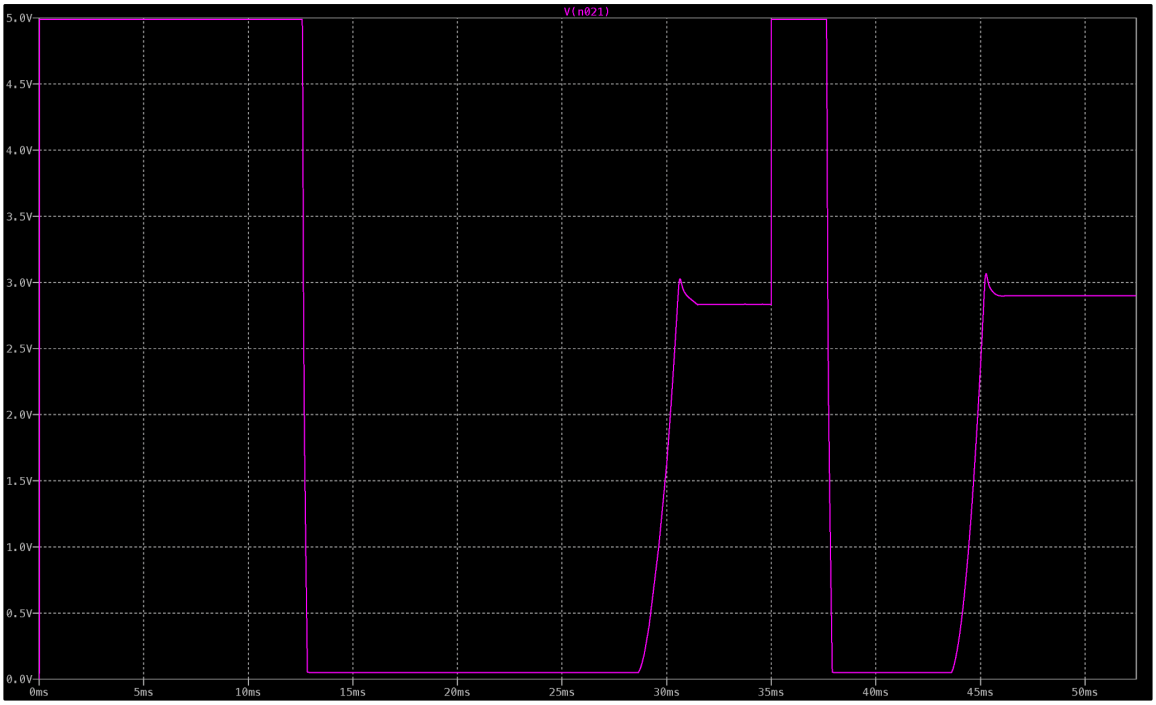


Figure F.42. Voltage waveform on the COMP pin with respect to ground for simulation test eight. Compare this figure with Figure F.39 to discern what each non-zero voltage interval corresponds to.

## F.9 Simulation Test Nine

Test Description:

To properly perform this test, apply an input voltage of 50V to the converter and allow the output to settle to 400V before applying any load. After the output voltage settles, apply a resistance of 50Ω to the output. Once the voltage settles again, vary the input voltage from 50V to 100V in 1ms.

Test Setup:

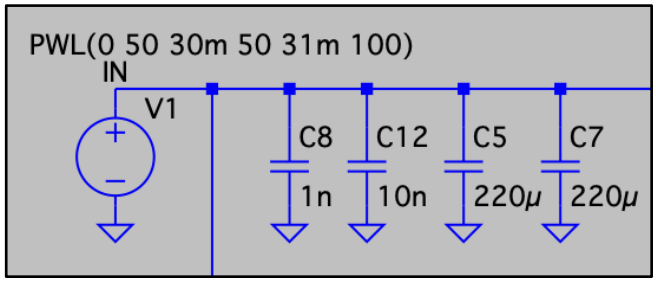


Figure F.43. Input of the three-phase push-pull converter for simulation test nine.

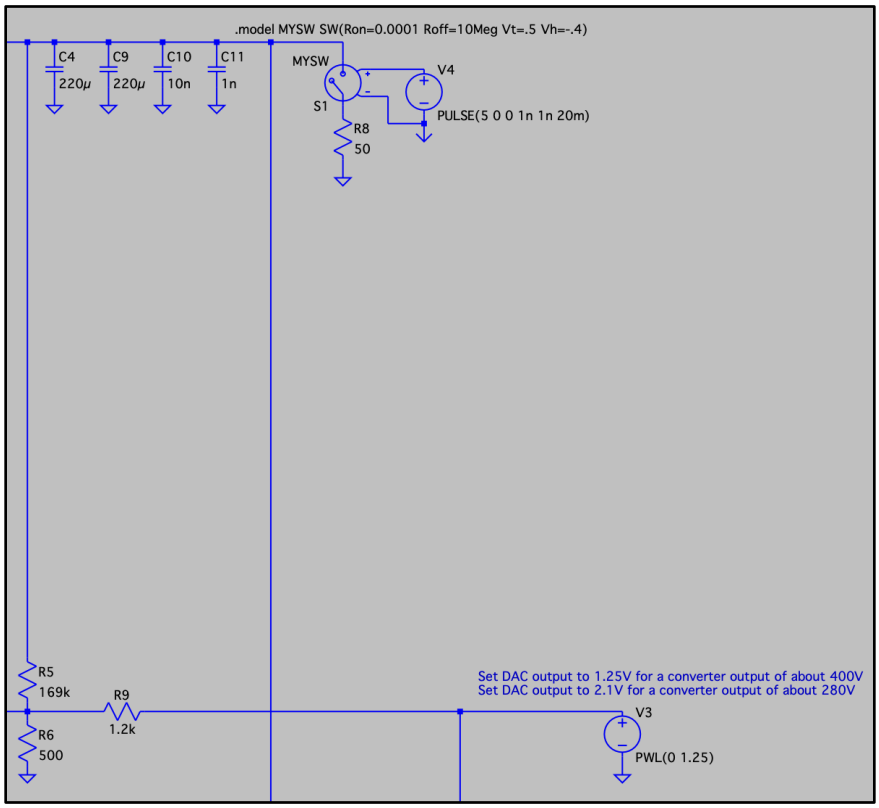


Figure F.44. Output and DAC of the three-phase push-pull converter for simulation test nine. A resistor in series with an ideal switch was utilized to perform this test.

Test Results:

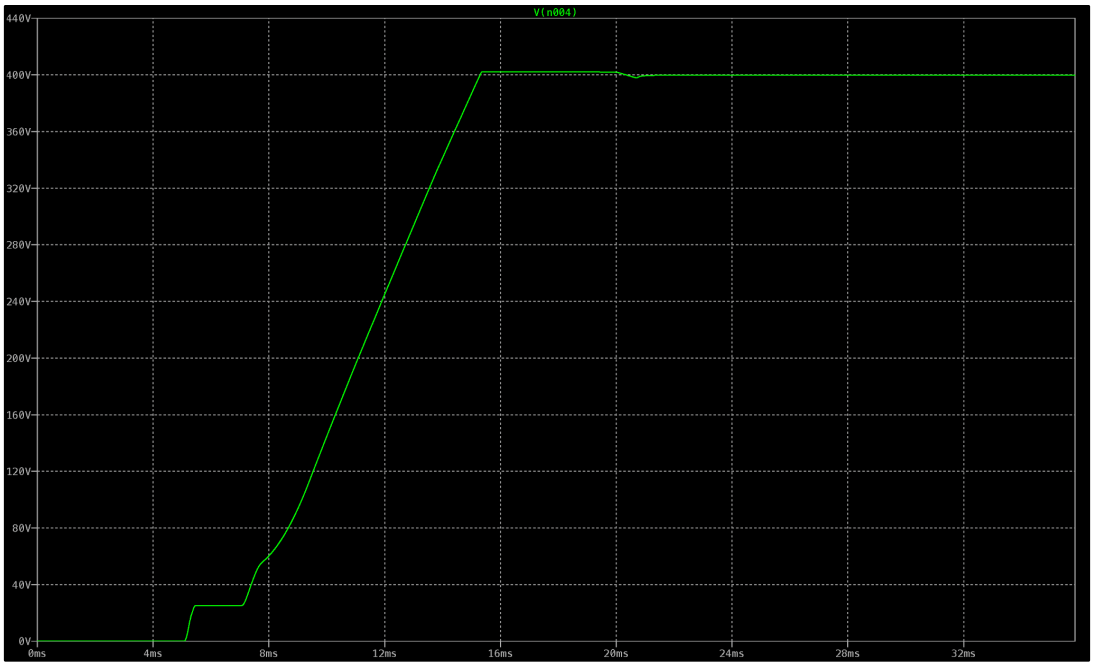

Figure F.45. Output voltage as a function of time for simulation test nine. At approximately 15ms, the output voltage settled to 400V. Afterwards, at 20ms a resistor of 50Ω was applied to the output. From 30ms to 31ms, the input voltage transitioned from 50V to 100V.

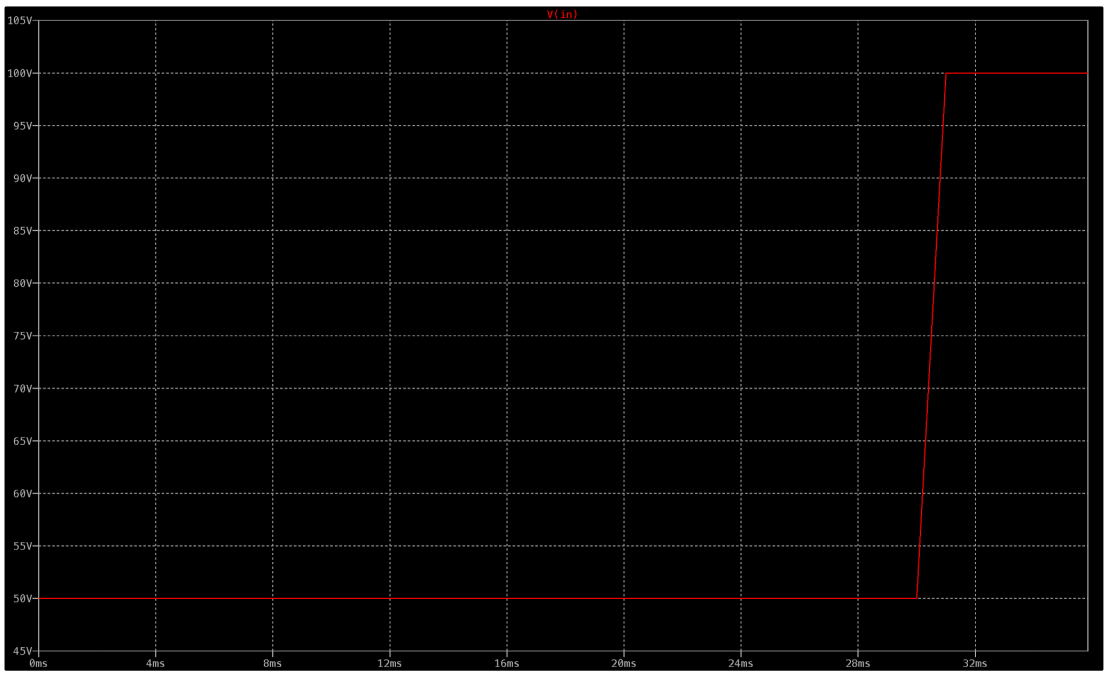

Figure F.46. Input voltage as a function of time for simulation test nine.

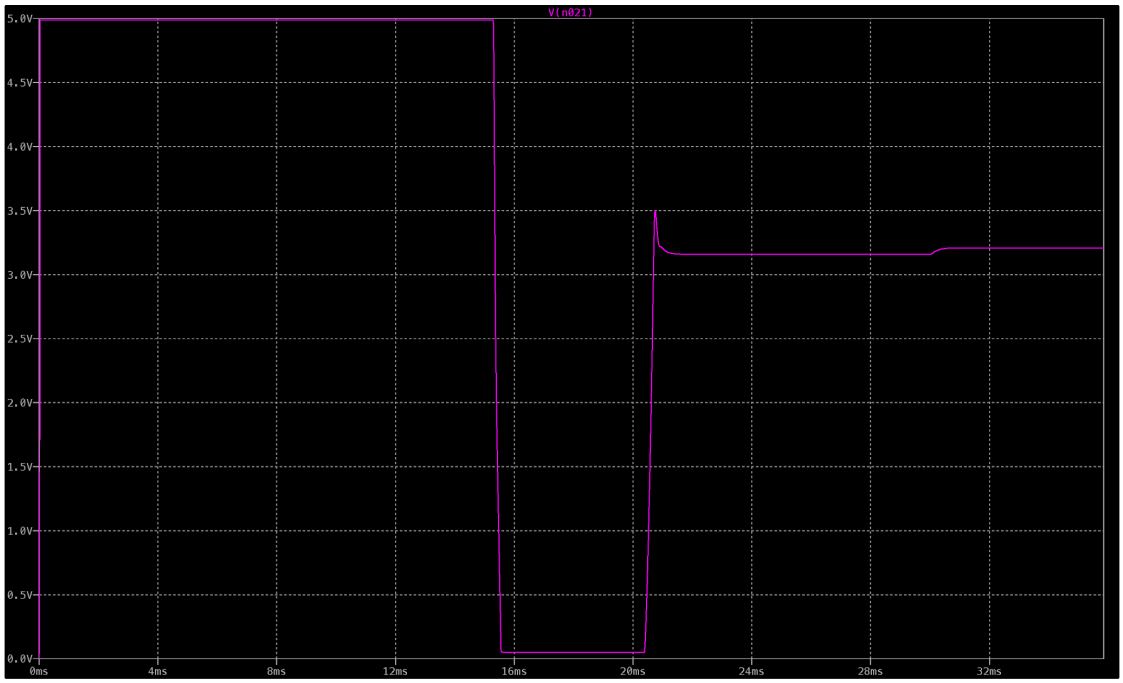

Figure F.47. Voltage waveform on the COMP pin with respect to ground for simulation test nine. Compare this figure with Figure F.45 to discern what each non-zero voltage interval corresponds to.

## F.10 Simulation Test Ten

Test Description:

To properly perform this test, apply an input voltage of 50V to the converter and allow the output to settle to 400V before applying any load. After the output voltage settles, apply a resistance of 800Ω to the output. Once the voltage settles again, vary the input voltage from 50V to 100V in 1ms.

Test Setup:

The input of the three-phase push pull converter in simulation test ten is the same as shown in Figure F.43. On the contrary, the output setup is different.

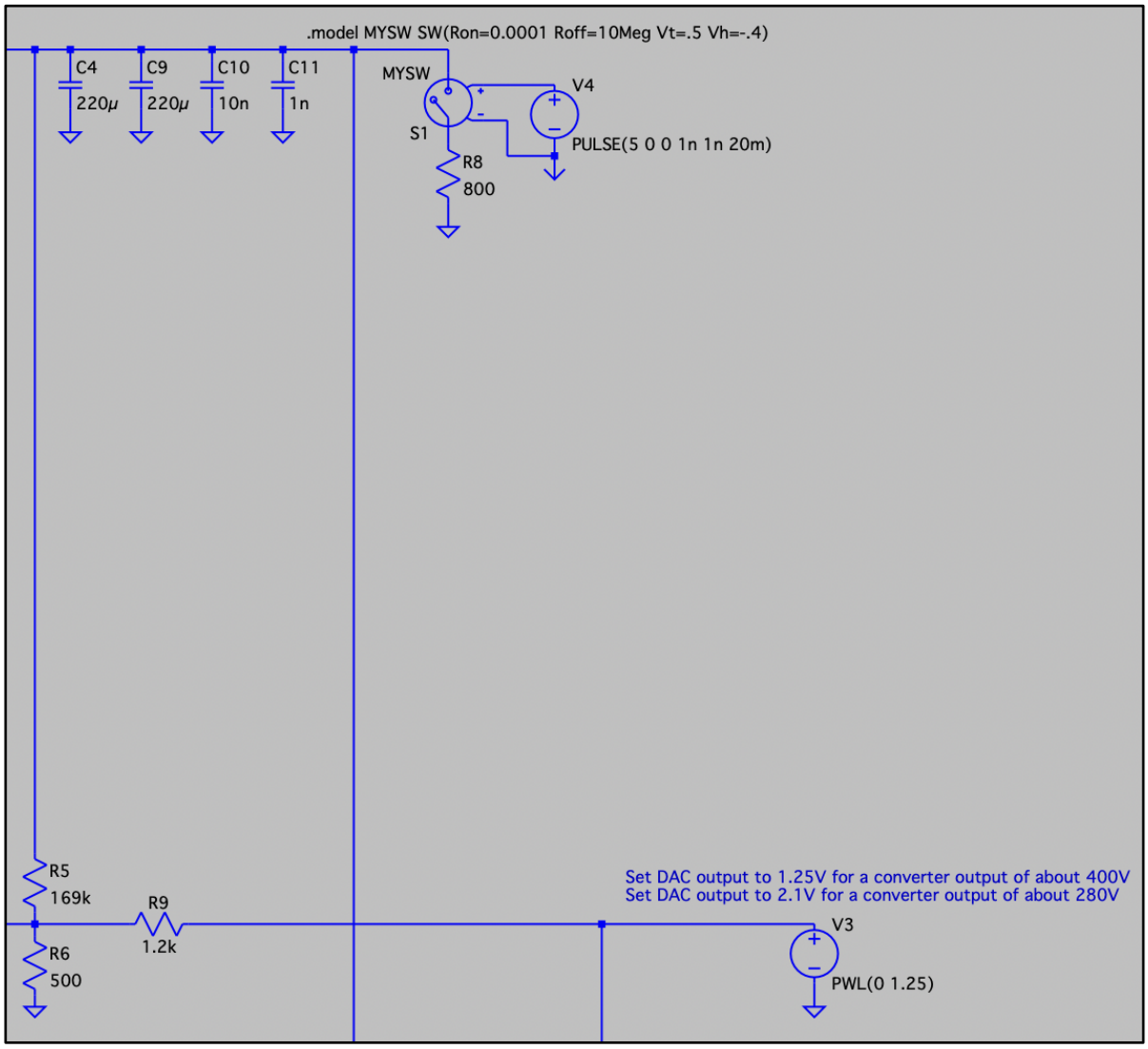


Figure F.48. Output and DAC of the three-phase push-pull converter for simulation test ten. A resistor in series with an ideal switch was utilized to perform this test.

Test Results:

The input voltage waveform is the same as in Figure F.46.

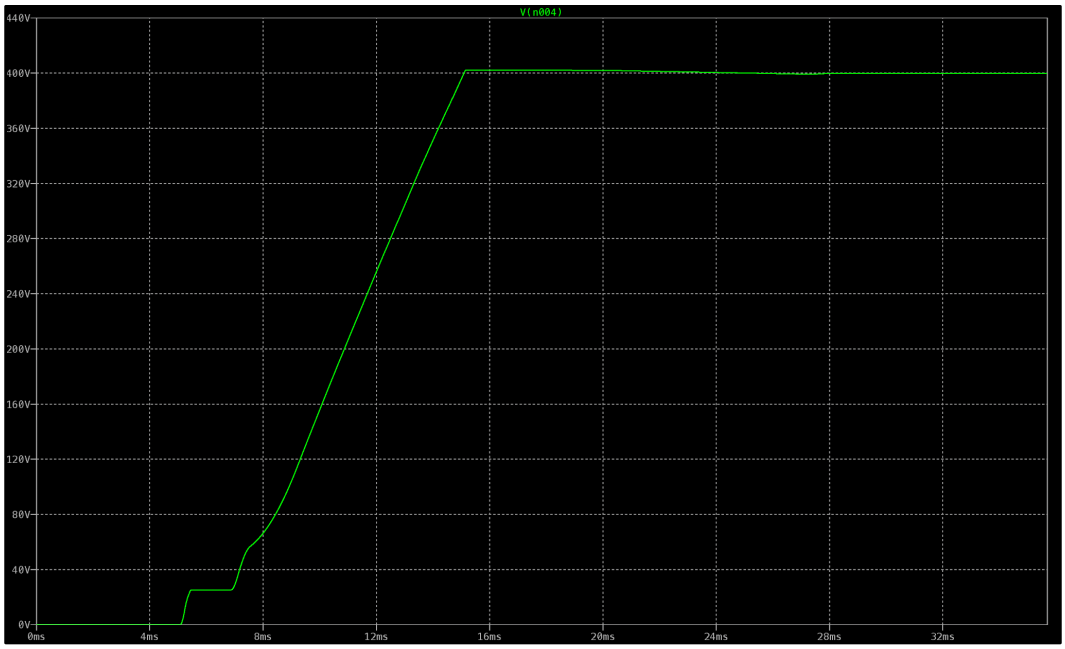


Figure F.49. Output voltage as a function of time for simulation test ten. At approximately 15ms, the output voltage settled to 400V. Afterwards, at 20ms a resistor of 800Ω was applied to the output. From 30ms to 31ms, the input voltage transitioned from 50V to 100V.

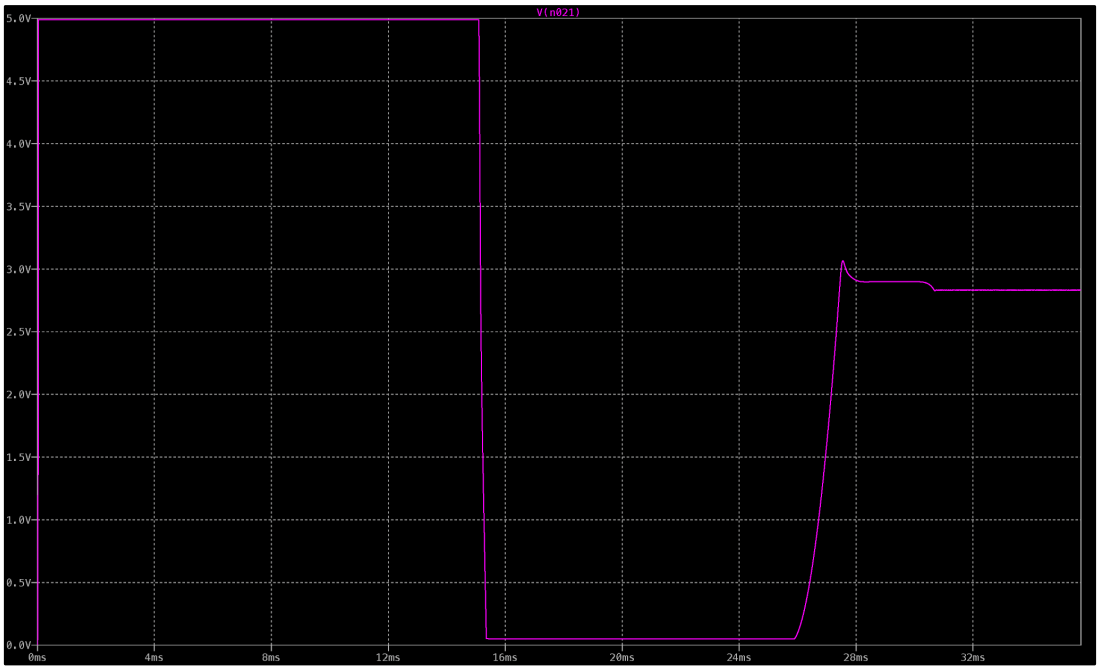


Figure F.50. Voltage waveform on the COMP pin for simulation test ten. Compare this figure with Figure F.49 to discern what each non-zero voltage interval corresponds to.

## F.11 Simulation Test Eleven

Test Description:

To properly perform this test, apply an input voltage of 100V to the converter and allow the output to settle to 400V before applying any load. After the output voltage settles, apply a resistance of 50Ω to the output. Once the voltage settles again, vary the input voltage from 100V to 50V in 1ms.

Test Setup:

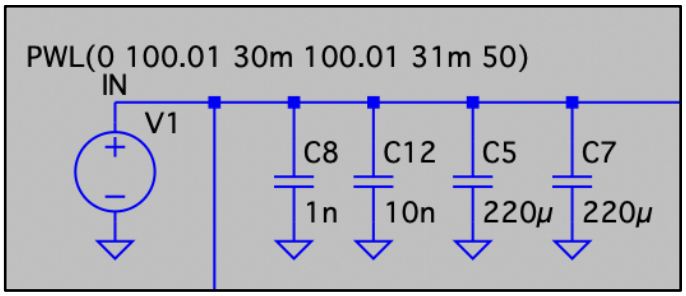


Figure F.51. Input of the three-phase push-pull converter for simulation test eleven. The input decreases from 100.01V rather than 100V to avoid undesired simulation termination.

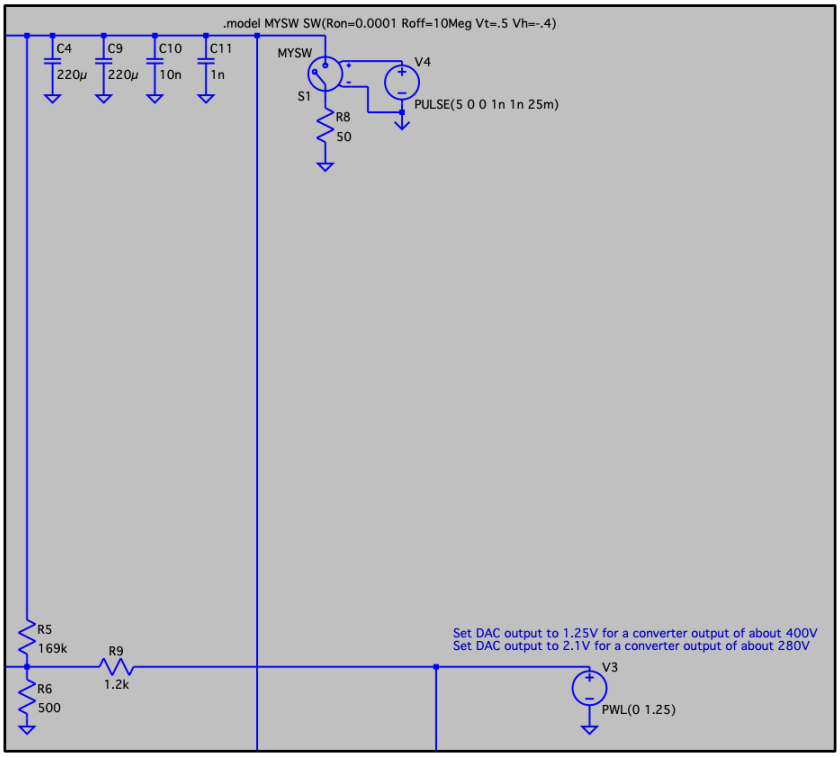


Figure F.52. Output and DAC of the three-phase push-pull converter for simulation test eleven. A resistor in series with an ideal switch was utilized to perform this test.

Test Results:

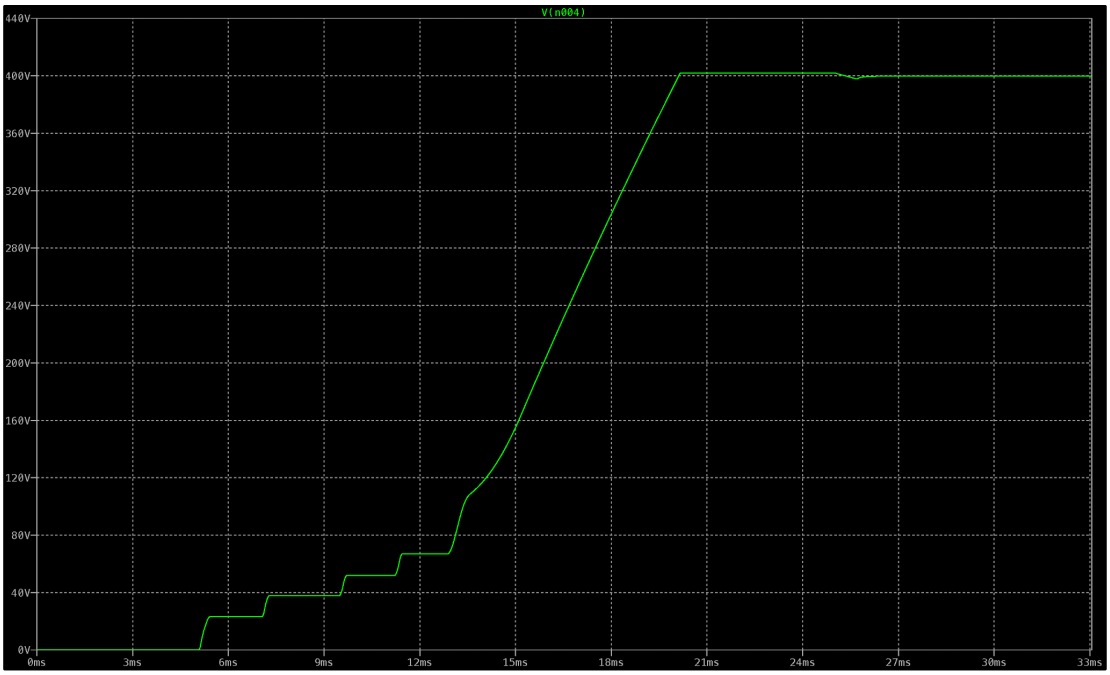


Figure F.53. Output voltage as a function of time for simulation test eleven. At approximately 20ms, the output voltage settled to 400V. Afterwards, at 25ms a resistor of 50Ω was applied to the output. From 30ms to 31ms, the input voltage transitioned from 100V to 50V.

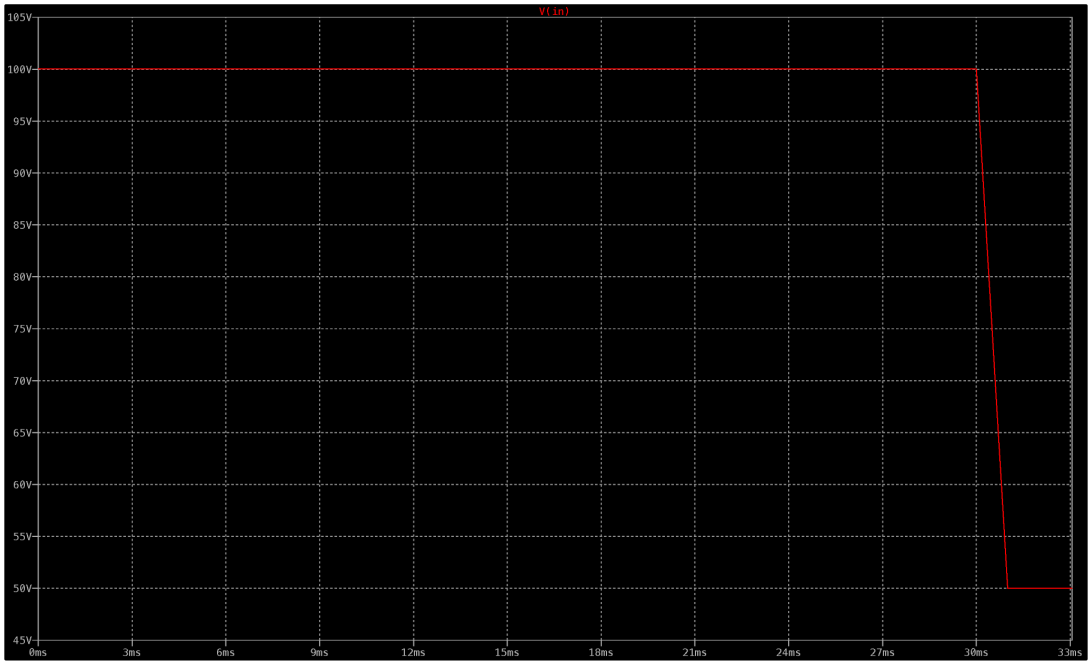


Figure F.54. Input voltage as a function of time for simulation test eleven.

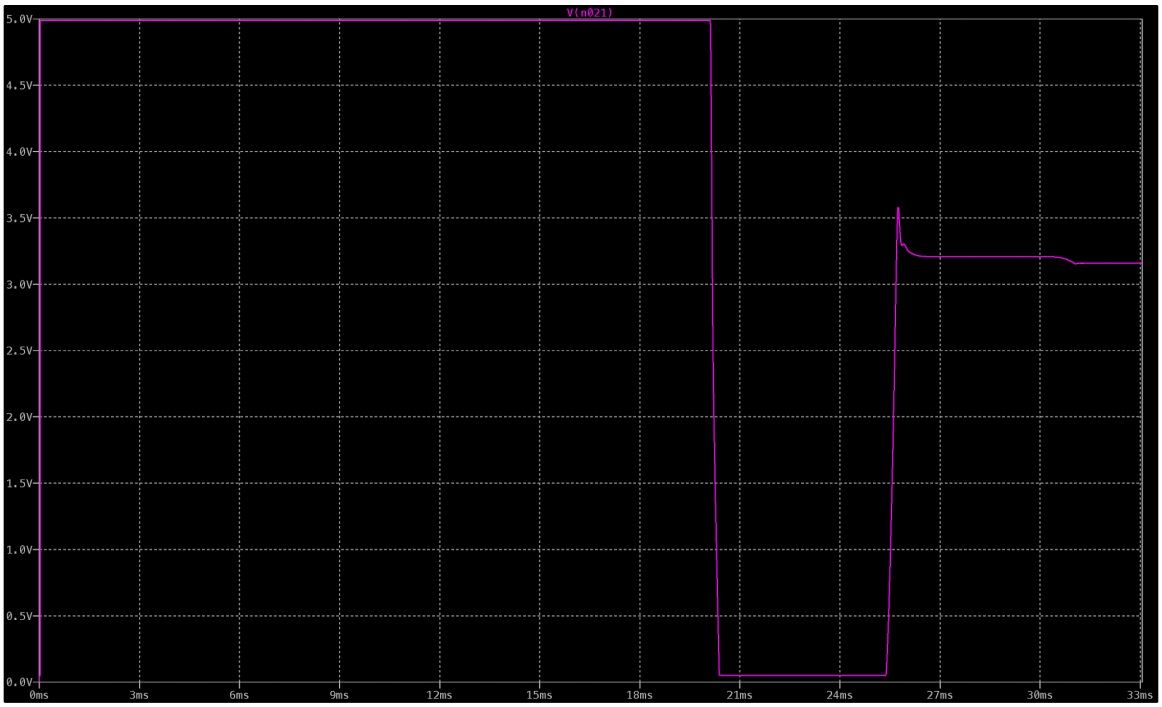

Figure F.55. Voltage waveform on the COMP pin with respect to ground for simulation test eleven. Compare this figure with Figure F.53 to discern what each non-zero voltage interval corresponds to.

## F.12 Simulation Test Twelve

Test Description:

To properly perform this test, apply an input voltage of 100V to the converter and allow the output to settle to 400V before applying any load. After the output voltage settles, apply a resistance of 800Ω to the output. Once the voltage settles again, vary the input voltage from 100V to 50V in 1ms.

Test Setup:

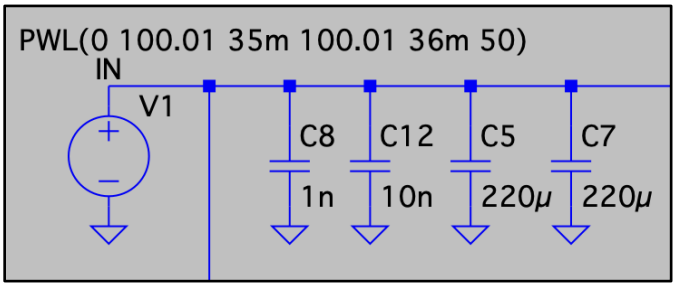


Figure F.56. Input of the three-phase push-pull converter for simulation test twelve. The input decreases from 100.01V rather than 100V to avoid undesired simulation termination.

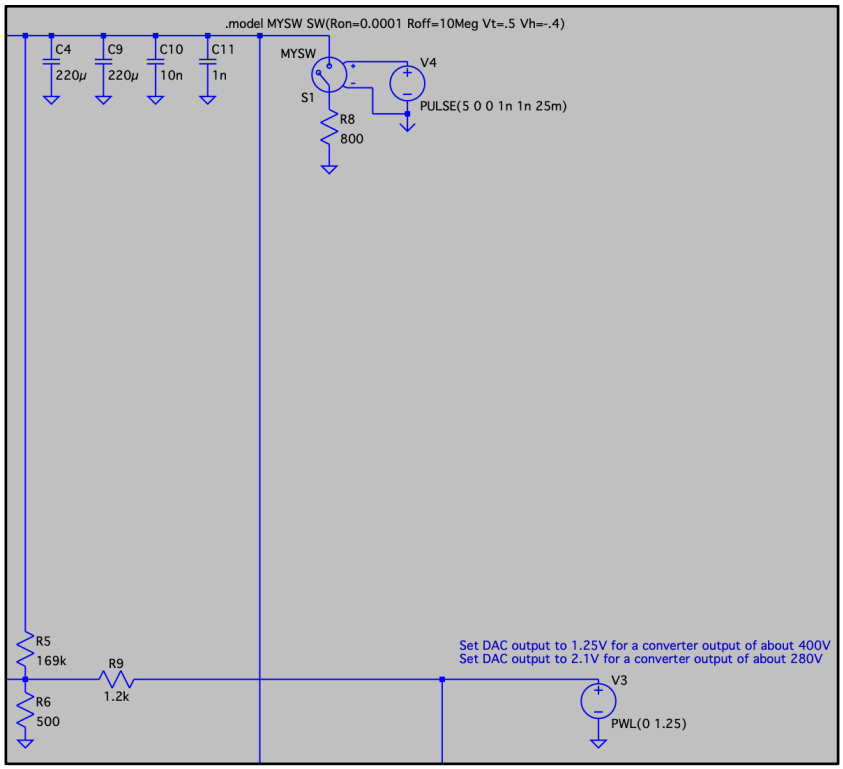


Figure F.57. Output and DAC of the three-phase push-pull converter for simulation test twelve. A resistor in series with an ideal switch was utilized to perform this test.

Test Results:

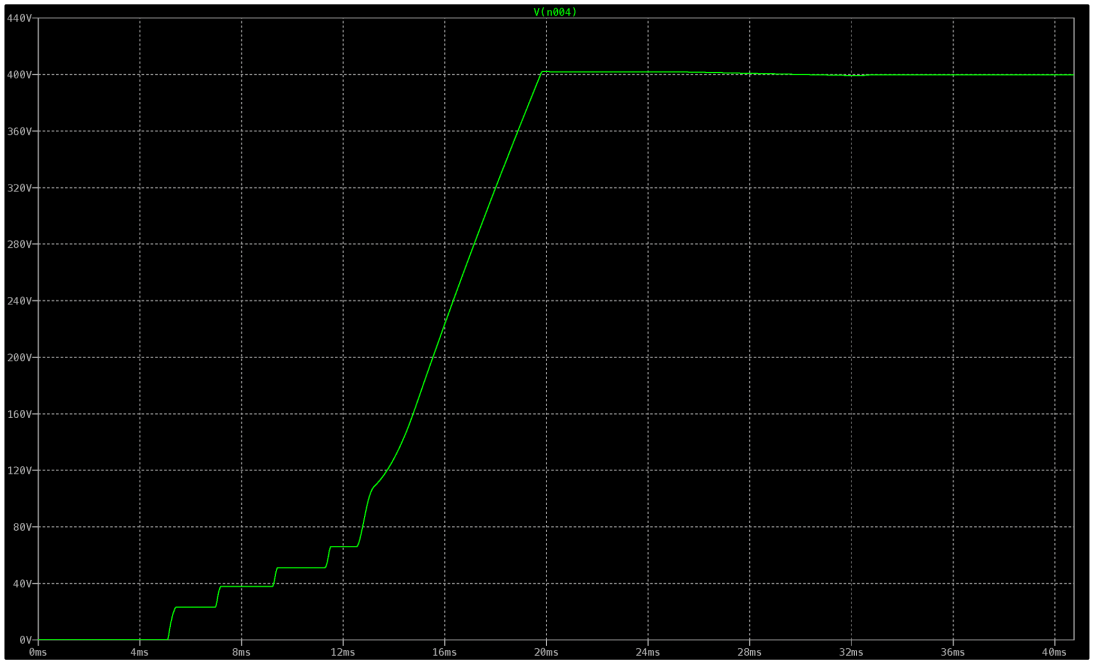


Figure F.58. Output voltage as a function of time for simulation test eleven. At approximately 20ms, the output voltage settled to 400V. Afterwards, at 25ms a resistor of 50Ω was applied to the output. From 35ms to 36ms, the input voltage transitioned from 100V to 50V.

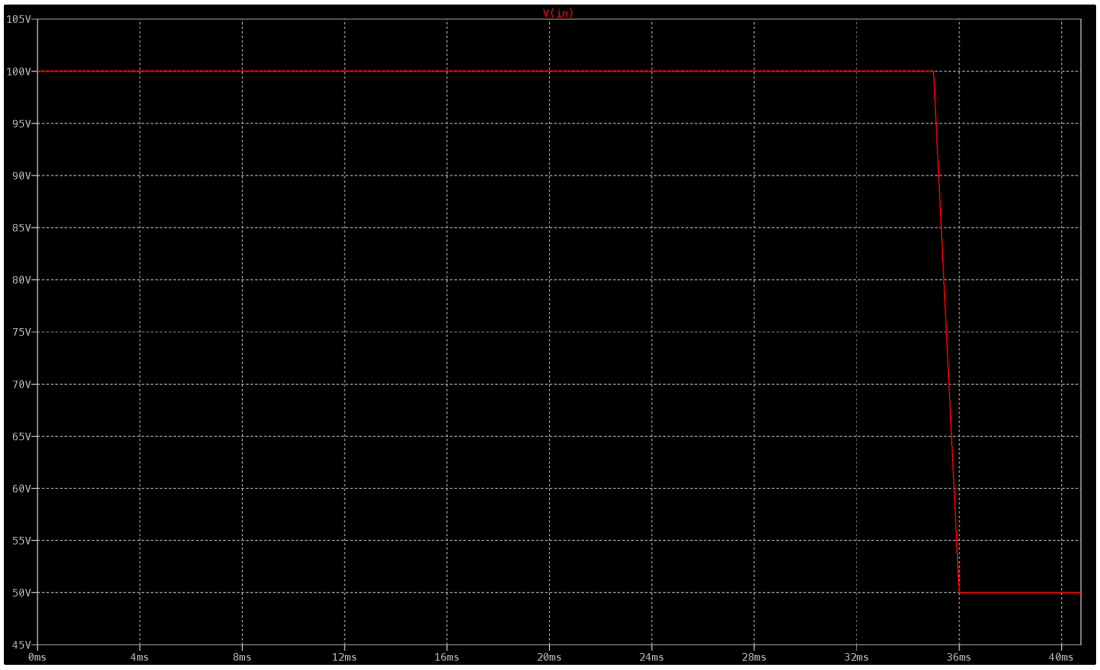


Figure F.59. Voltage as a function of time for simulation test twelve.

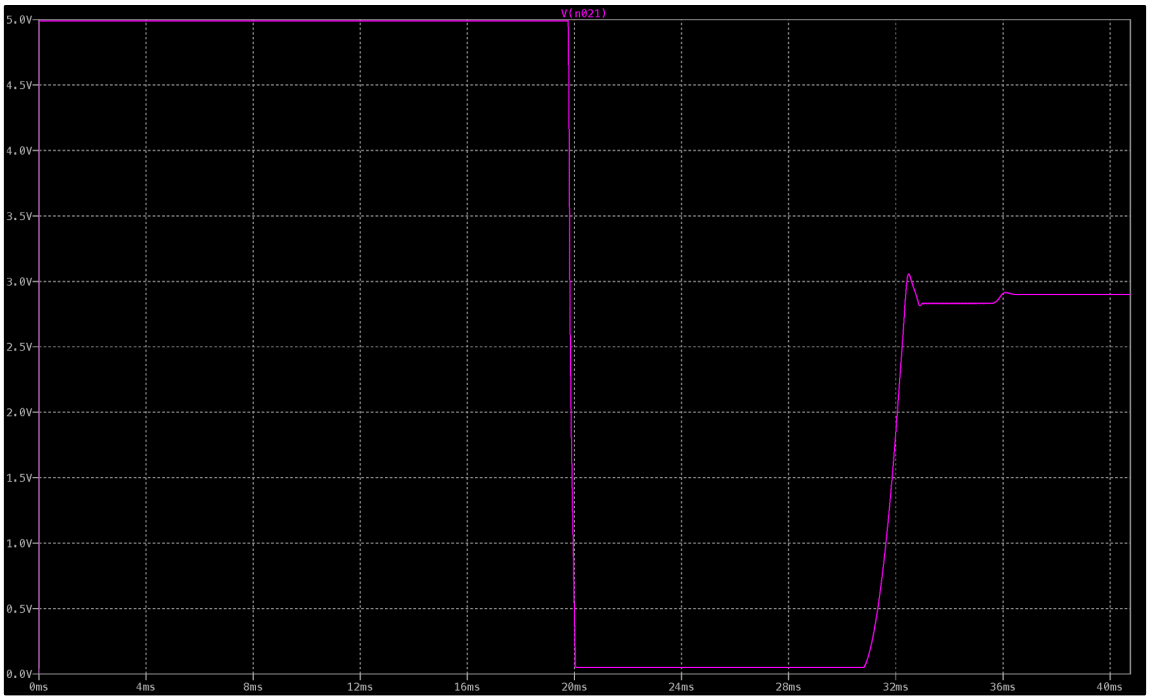

Figure F.60. Voltage waveform on the COMP pin with respect to ground for simulation test twelve. Compare this figure with Figure F.58 to discern what each non-zero voltage interval corresponds to.

## F.13 Simulation Test Thirteen

Test Description:

To properly perform this test, apply an input voltage of 50V to the converter and allow the output to settle to 280V before applying any load. After the output voltage settles, apply a resistance of 25.45Ω to the output. Once the voltage settles again, vary the input voltage from 50V to 100V in 1ms.

Test Setup:

The input of the three-phase push pull converter in simulation test thirteen is the same as shown in Figure F.43. On the contrary, the output setup is different.

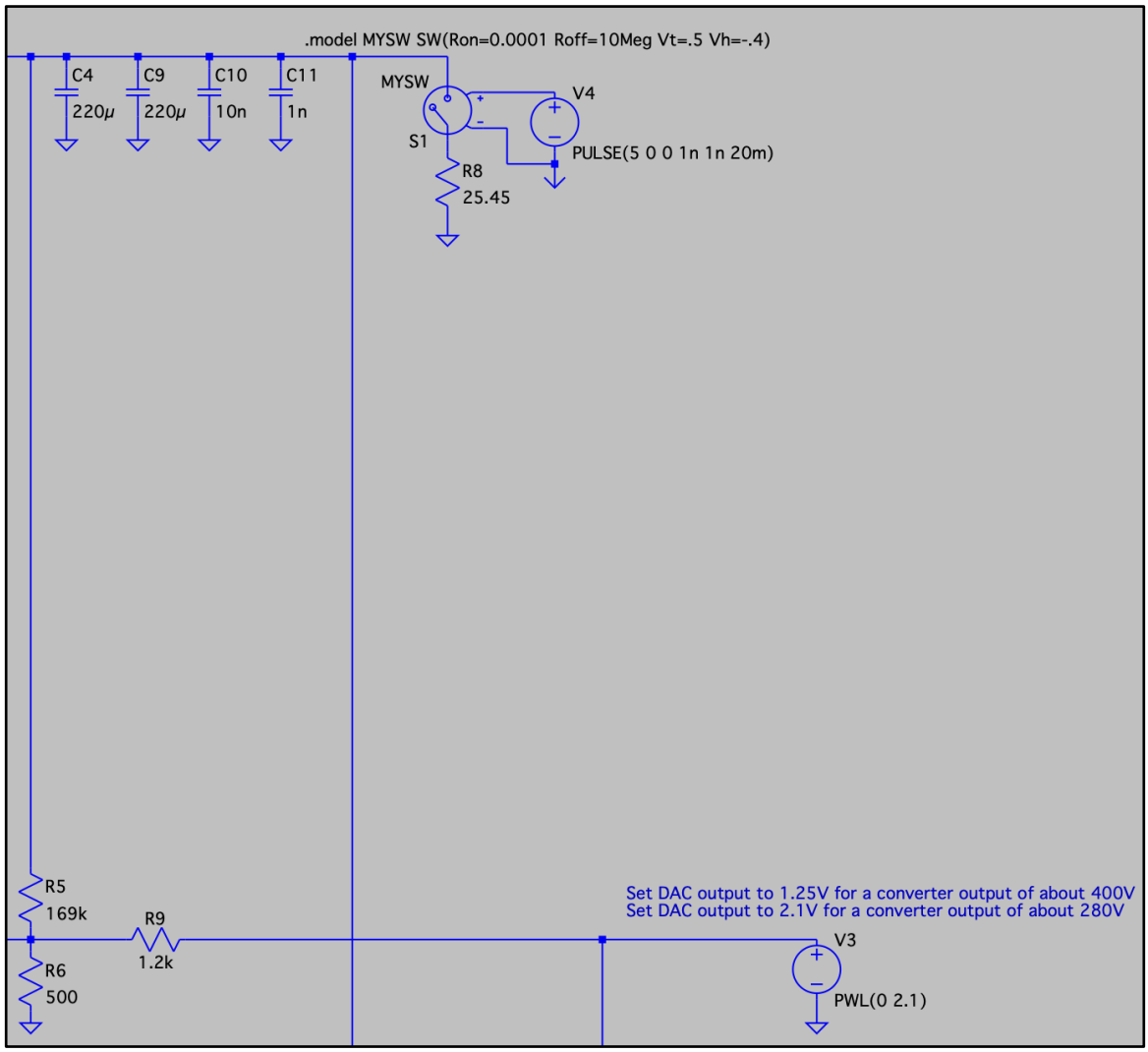


Figure F.61. Output and DAC of the three-phase push-pull converter for simulation test thirteen. A resistor in series with an ideal switch was utilized to perform this test.

Test Results:

The input voltage waveform is the same as in Figure F.46.

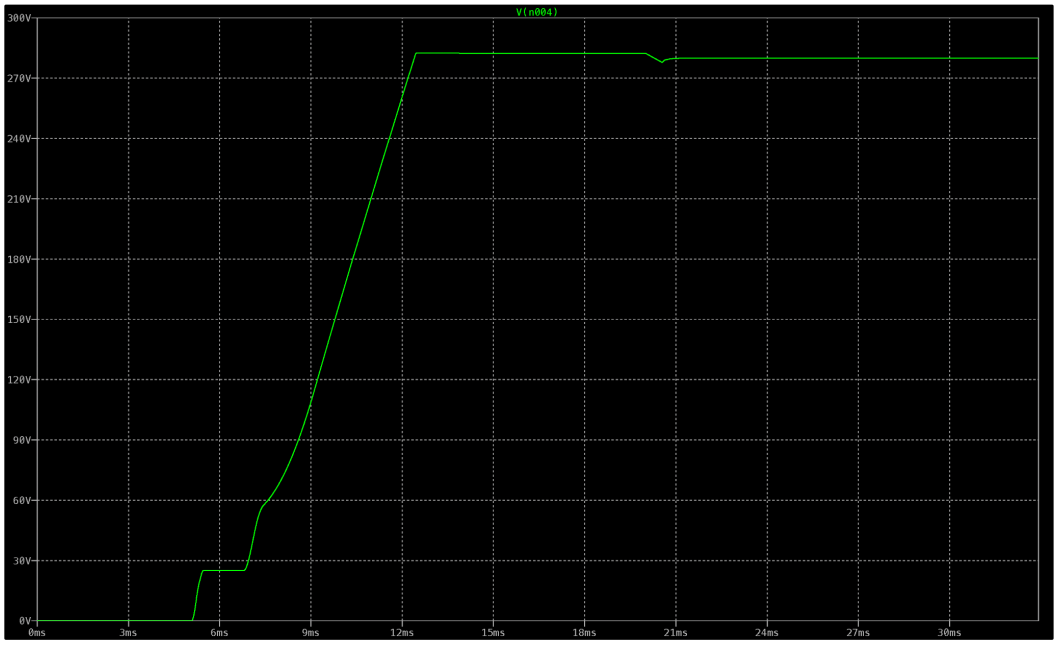


Figure F.62. Output voltage as a function of time for simulation test thirteen. At 12.5ms, the output voltage settled to 280V. Afterwards, at 20ms a resistor of 25.45Ω was applied to the output. From 30ms to 31ms, the input voltage transitioned from 50V to 100V.

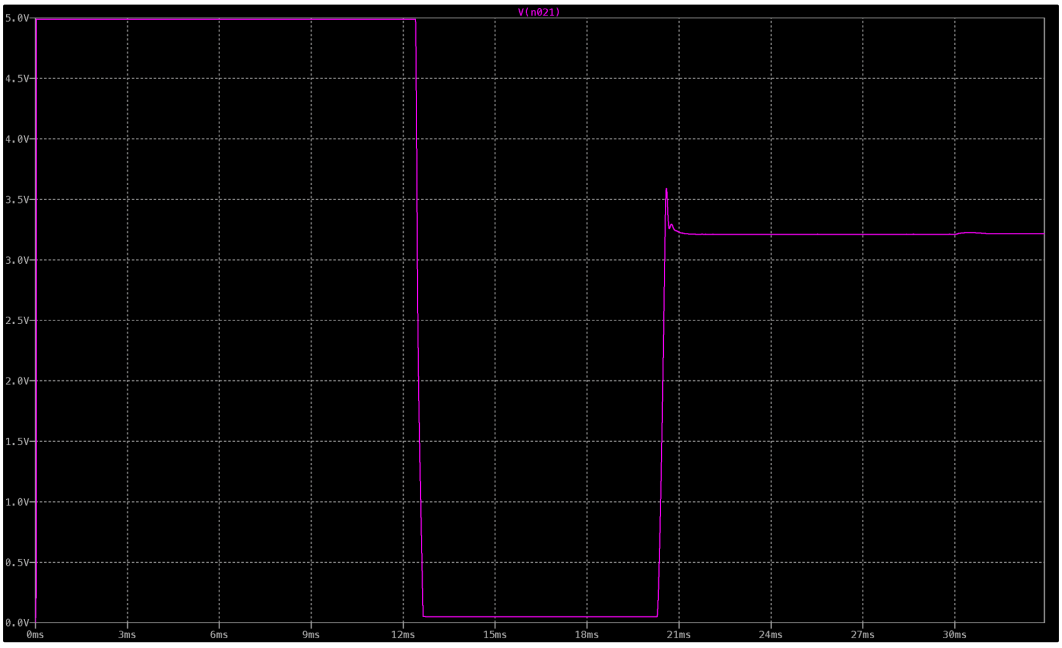


Figure F.63. Voltage waveform on the COMP pin with respect to ground for simulation test thirteen. Compare this figure with Figure F.62 to discern what each non-zero voltage interval corresponds to.

## F.14 Simulation Test Fourteen

Test Description:

To properly perform this test, apply an input voltage of 50V to the converter and allow the output to settle to 280V before applying any load. After the output voltage settles, apply a resistance of 560Ω to the output. Once the voltage settles again, vary the input voltage from 50V to 100V in 1ms.

Test Setup:

The input of the three-phase push pull converter in simulation test fourteen is the same as shown in Figure F.43. On the contrary, the output setup is different.

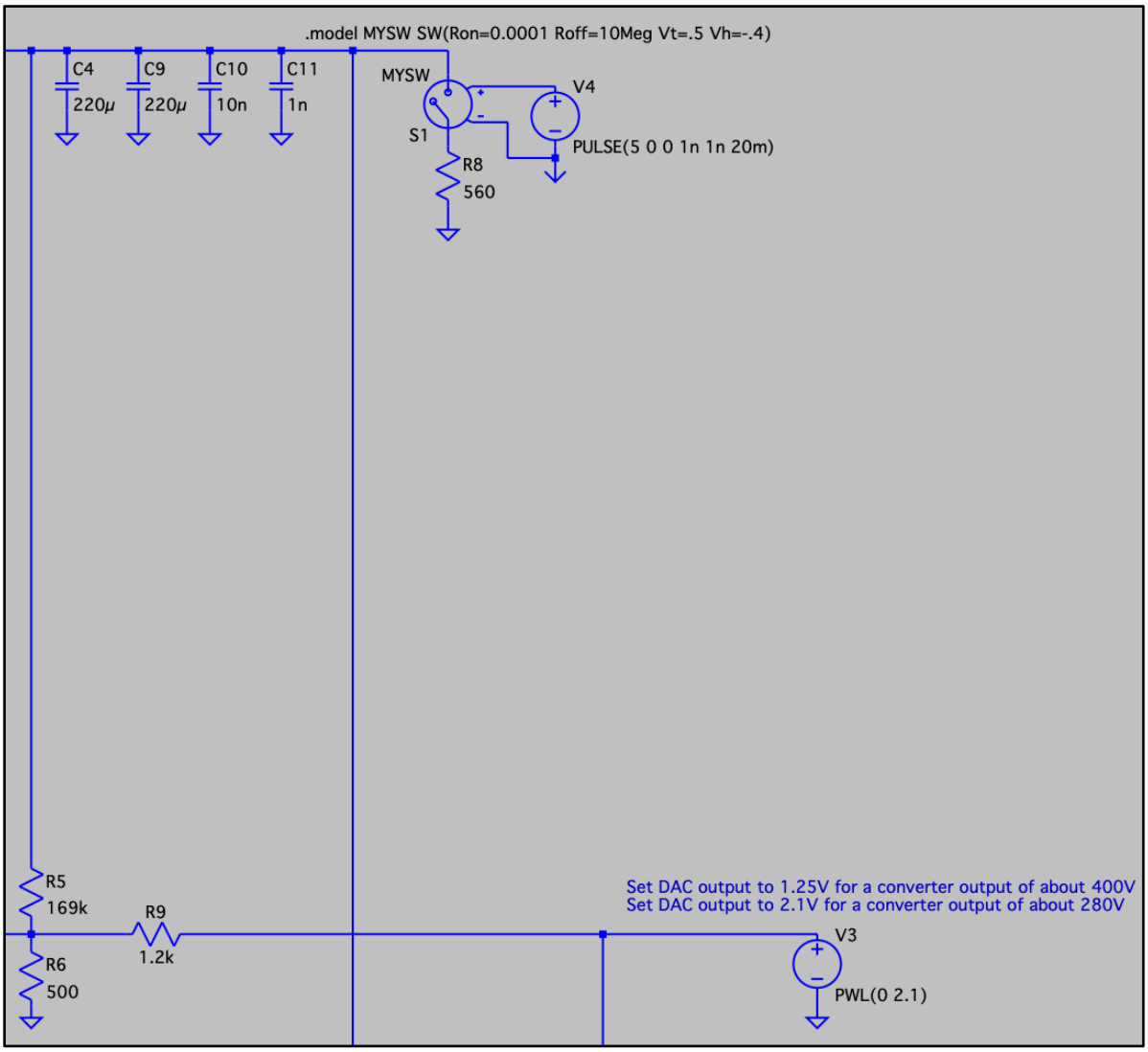


Figure F.64. Output and DAC of the three-phase push-pull converter for simulation test fourteen. A resistor in series with an ideal switch was utilized to perform this test.

Test Results:

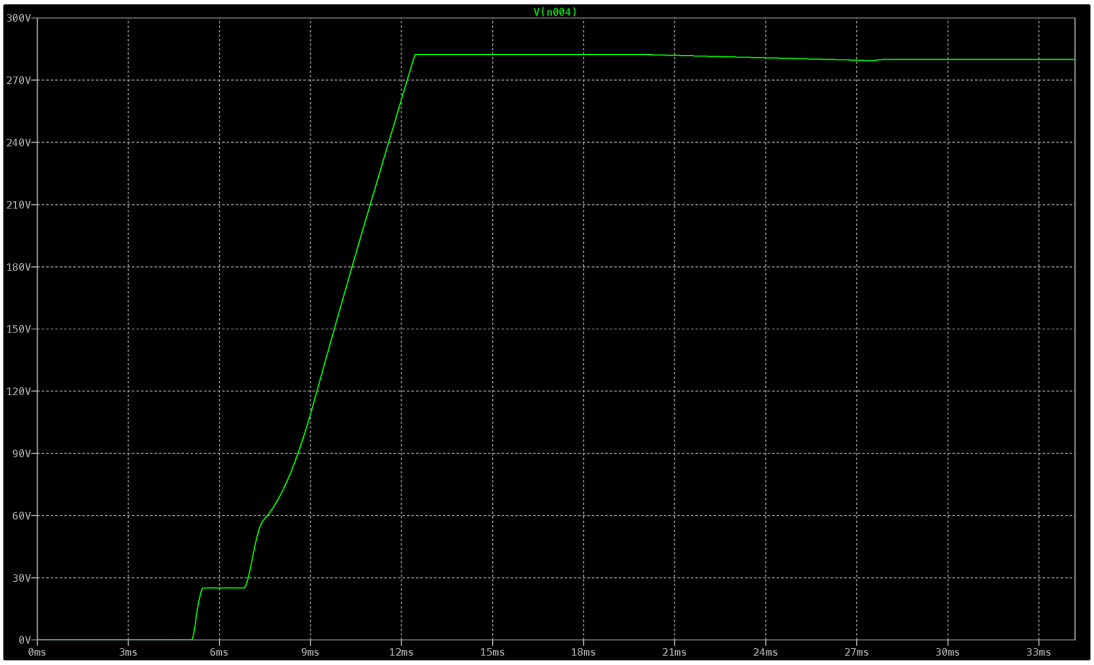


Figure F.65. Output voltage as a function of time for simulation test fourteen. At 12.5ms, the output voltage settled to 280V. Afterwards, at 20ms a resistor of 560Ω was applied to the output. From 30ms to 31ms, the input voltage transitioned from 50V to 100V.

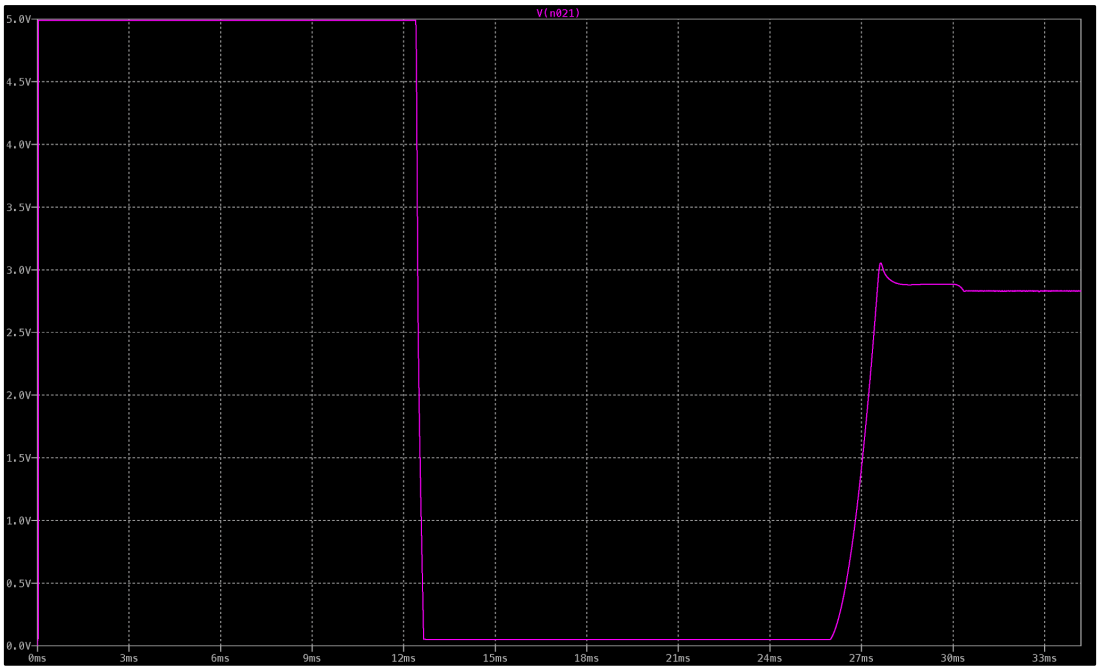


Figure F.66. Voltage waveform on the COMP pin with respect to ground for simulation test fourteen. Compare this figure with Figure F.65 to discern what each non-zero voltage interval corresponds to.

## F.15 Simulation Test Fifteen

Test Description:

To properly perform this test, apply an input voltage of 100V to the converter and allow the output to settle to 280V before applying any load. After the output voltage settles, apply a resistance of 25.45Ω to the output. Once the voltage settles again, vary the input voltage from 100V to 50V in 1ms.

Test Setup:

The input of the three-phase push pull converter in simulation test fifteen is the same as shown in Figure F.56. The output is the same as in Figure F.61.

Test Results:

The input voltage waveform is the same as in Figure F.59.

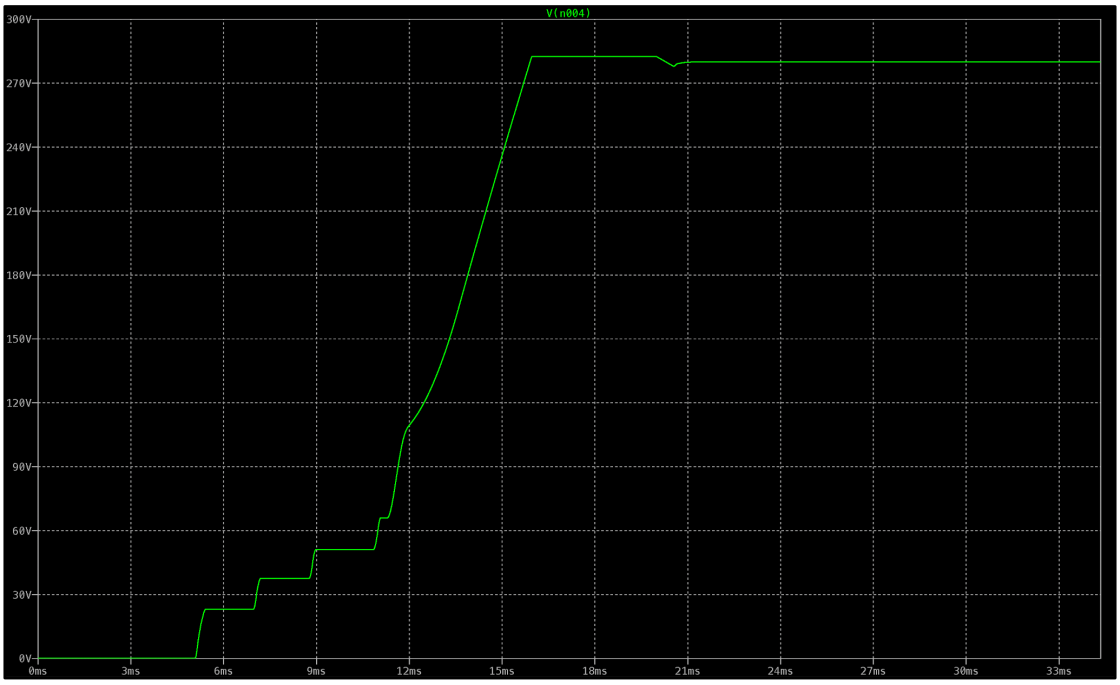


Figure F.67. Output voltage as a function of time for simulation test fifteen. At approximately 16ms, the output voltage settled to 280V. Afterwards, at 20ms a resistor of 25.45Ω was applied to the output. From 30ms to 31ms, the input voltage transitioned from 100V to 50V.

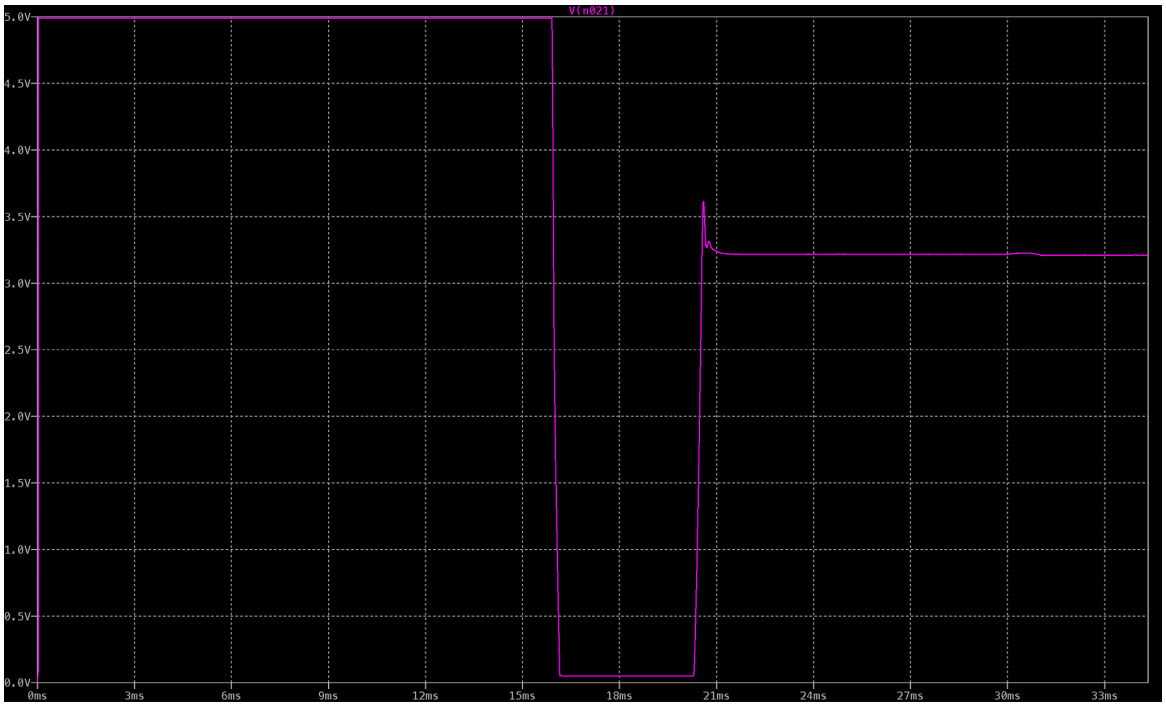

Figure F.68. Voltage waveform on the COMP pin with respect to ground for simulation test fifteen. Compare this figure with Figure F.67 to discern what each non-zero voltage interval corresponds to.

## F.16 Simulation Test Sixteen

Test Description:

To properly perform this test, apply an input voltage of 100V to the converter and allow the output to settle to 280V before applying any load. After the output voltage settles, apply a resistance of 560Ω to the output. Once the voltage settles again, vary the input voltage from 100V to 50V in 1ms.

Test Setup:

The input of the three-phase push pull converter in simulation test sixteen is the same as shown in Figure F.56. The output is the same as in Figure F.64.

Test Results:

The input voltage waveform is the same as in Figure F.59.

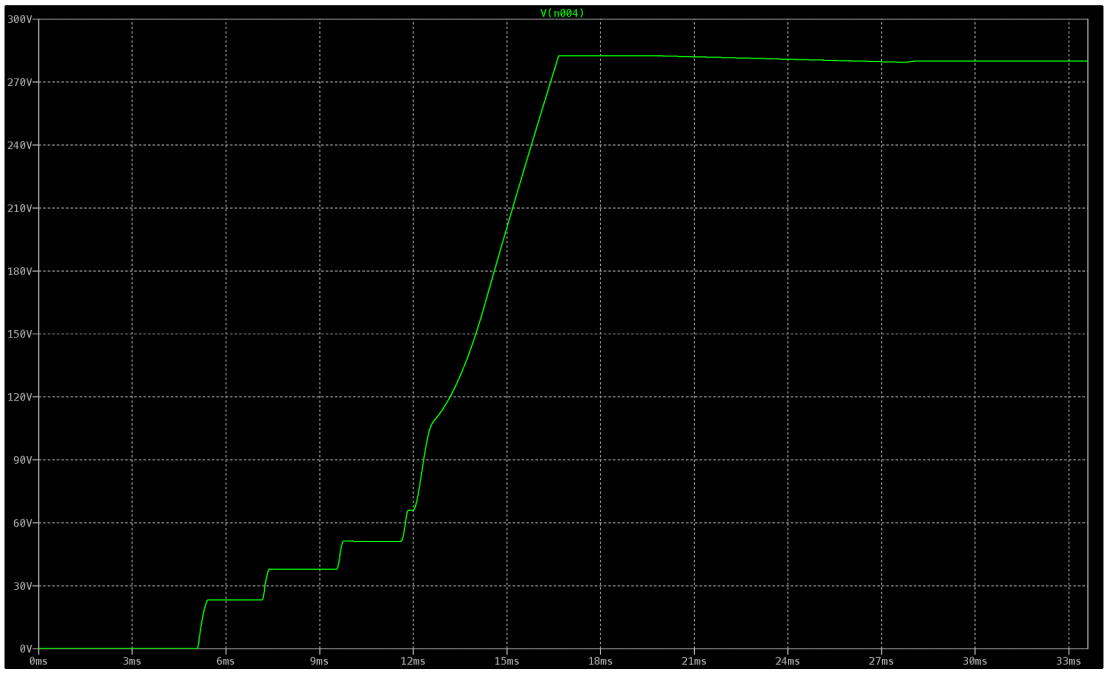


Figure F.69. Output voltage as a function of time for simulation test sixteen. At approximately 16ms, the output voltage settled to 280V. Afterwards, at 20ms a resistor of 560Ω was applied to the output. From 30ms to 31ms, the input voltage transitioned from 50V to 100V.

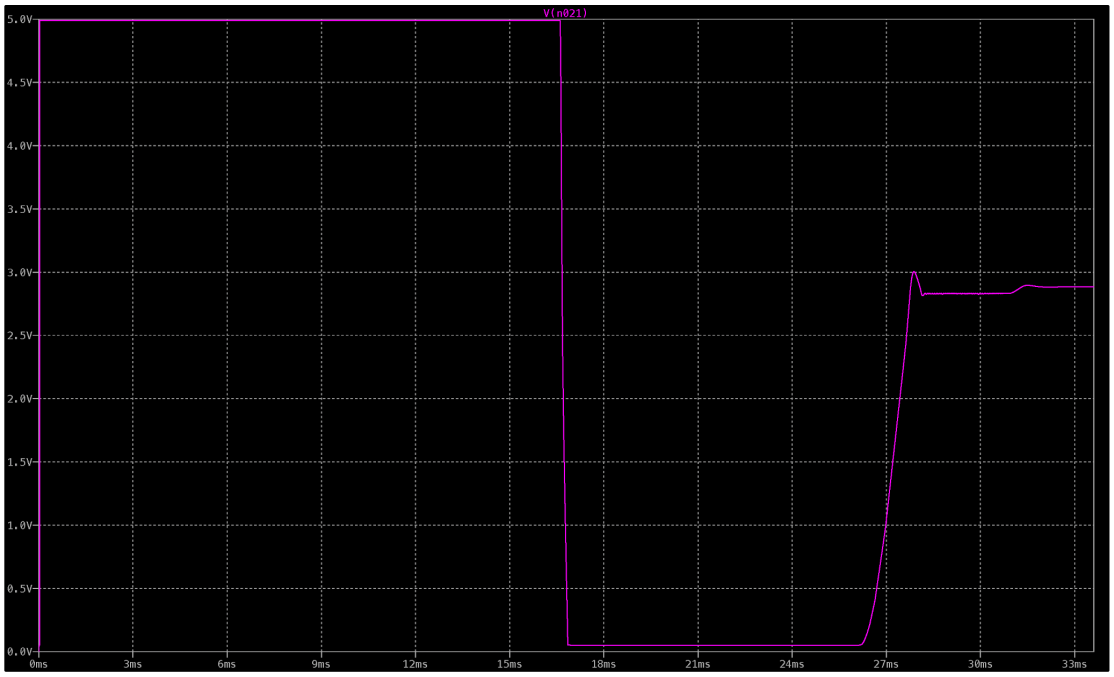

Figure F.70. Voltage waveform on the COMP pin with respect to ground for simulation test sixteen. Compare this figure with Figure F.69 to discern what each non-zero voltage interval corresponds to.

# Appendix G: SPICE Netlist for Non-Isolated Design

To quickly simulate the non-isolated design on your computer, the following SPICE netlist can be utilized:

```
V1 IN 0 50 Rser=0
D3 N036 N050 RF04UA2D
C12 0 N037 10µ
C13 N043 0 30µ
R10 N062 0 12.1K
R13 N009 N062 900k
R14 N063 0 3.3m
C14 N050 N054 0.22µ
C15 N051 N055 0.22µ
C16 N058 0 0.005µ
C17 N060 0 10n
R15 N061 N060 10K
L3 N054 N055 450µ
R16 N043 N009 3.3m
R17 N059 0 150k
C18 N009 0 56µ
R18 N009 N044 100
R19 N043 N047 100
C19 N044 N047 4.7µ
R20 IN N048 10K
R21 N046 0 1.6k
R22 IN N046 133K
C20 N036 0 10µ
C21 N061 0 100p
D4 N036 N051 RF04UA2D
XU2 N062 N058 N063 0 N061 0 NC_01 N059 N048 IN N042 N037 N047 N044 N046 N055 N053 N051 N057 0 N037 IN N056
0 N050 N052 N054 N049 N036 IN NC_02 MP_03 MP_04 IN N038 N040 MP_05 MP_06 MP_07 MP_08 MP_09 0 LTC3777
L4 N038 BOUT 220µ Rpar=1K
C30 BOUT 0 44µ
R24 BOUT N040 309k
R27 N040 0 97.6k
R29 N049 N037 100k
V2 NC_10 NC_11 PULSE(0 10 0.9u 0.1n 0.1n 0.9u 1.8u)
V3 NC_12 NC_13 PULSE(0 10 0 0.1n 0.1n 0.9u 1.8u)
C31 N021 N016 6µ Rser=1m
D11 N021 N025 VS-E5PX7506
C32 N017 N016 6µ Rser=1m
C34 N018 N022 50µ Rser=1m
C35 N022 N025 50µ Rser=1m
R26 N018 0 77
C36 N025 0 50µ Rser=1m
D1 N001 N014 RF04UA2D
C1 0 N002 10µ
M§Q2 N007 N020 N024 N024 AOTL66518
C2 N007 0 30µ
R1 N033 0 12.1K
R2 N009 N033 900k
R3 N034 0 3.3m
```

C3 N014 N023 0.22µ
C4 N015 N024 0.22µ
C5 N029 0 0.005µ
C6 N031 0 10n
R4 N032 N031 10K
L1 N023 N024 450µ
R5 N007 N009 3.3m
R6 N030 0 150k
C7 N009 0 56µ
R7 N009 N008 100
R8 N007 N011 100
C8 N008 N011 4.7µ
R9 IN N012 10K
R11 N010 0 1.6k
R12 IN N010 133K
C9 N001 0 10µ
C10 N032 0 100p
D2 N001 N015 RF04UA2D
XU1 N033 N029 N034 0 N032 0 NC_14 N030 N012 IN N006 N002 N011 N008 N010 N024 N020 N015 N027 0 N002 IN N026 0 N014 N019 N023 N013 N001 IN NC_15 MP_16 MP_17 IN N003 N005 MP_18 MP_19 MP_20 MP_21 MP_22 0 LTC3777
L5 N003 N004 220µ Rpar=1K
C22 N004 0 20µ
R32 N004 N005 715k
R33 N005 0 51.1k
R35 N013 N002 100k
XU3 N004 0 N041 0 N035 N009 LTC4440-5
C23 N009 0 0.1µ
C24 N004 0 0.1µ
XU4 0 N039 NC_23 N028 NC_24 N004 ADP3654
M2 N024 N027 N034 N034 AOTL66518
M3 IN N019 N023 N023 AOTL66518
M4 N023 N026 N034 N034 AOTL66518
M5 IN N052 N054 N054 AOTL66518
M6 N054 N056 N063 N063 AOTL66518
M§Q1 N043 N053 N055 N055 AOTL66518
M7 N055 N057 N063 N063 AOTL66518
C25 IN 0 0.1µ
C26 IN 0 0.1µ
D6 N025 N016 VS-E5PX7506
D7 N016 N022 VS-E5PX7506
D8 N022 N017 VS-E5PX7506
D9 N017 N018 VS-E5PX7506
XU7 BOUT 0 0 N041 N039 NC_25 NC_26 0 0 N045 LTC6902
R31 BOUT N045 357k
M§Q3 N009 N035 N021 N021 AOTL66518
M§Q4 N021 N028 0 0 AOTL66518
C11 BOUT 0 0.1µ
C27 N004 0 5µ
R23 N007 N006 1k
R25 N043 N042 1k
.model D D
.model NMOS NMOS
.model PMOS PMOS
.tran 20m startup

```
* When R_L = 77 ohm and Vin = 50VDC, Vout is about 400VDC and efficiency is 64%\nWhen R_L = 43 ohm and Vin = 50VDC, Vout is about 280VDC and efficiency is 56.4%
* Voltage on Ith pin \ncontrols inductor current
.lib ADP3654.sub
.lib LTC3777.sub
.lib LTC4440-5.sub
.lib LTC6902.sub
.backanno
.end
```

# Appendix H: SPICE Netlist for Isolated Design

To quickly simulate the isolated design on your computer, the following SPICE netlist can be utilized:

```
XU1 N022 N017 N019 0 0 N030 MP_01 N021 N023 N025 N024 N028 N027 N018 N020 LTC3721-1
R1 N015 0 1m
R2 N015 N023 100
C1 N030 0 330p
R3 N020 N021 100K
R4 N024 0 100K
C2 N027 0 .1µ
V1 IN 0 50 Rser=0
L1 IN N002 9.25µ Rser=0.15m
L2 N011 IN 9.25µ Rser=0.15m
L3 N003 N008 1332µ Rser=25m
L4 N005 N006 110µ
R5 N006 N028 169k
R6 N028 0 500
C3 N028 N026 .001µ
R7 N026 N025 200k
C4 N006 0 220µ
C6 N018 0 .001µ
M§Q3 N002 N019 N015 N015 IPP200N25N3
M§Q1 N011 N022 N015 N015 IPP200N25N3
C5 IN 0 220µ
C7 IN 0 220µ
R8 N010 0 50
R9 N028 N029 1.2k
D5 N004 N005 VS-E5PX6012
D3 N009 N005 VS-E5PX6012
D1 N014 N008 VS-E5PX6012
D2 N001 N003 VS-E5PX6012
M§Q2 N011 N022 N015 N015 IPP200N25N3
M§Q4 N002 N019 N015 N015 IPP200N25N3
S1 N010 N006 N007 COM MYSW
V4 N007 COM PULSE(5 0 0 1n 1n 40m) Rser=0
C9 N006 0 220µ
C10 N006 0 10n
C11 N006 0 1n
C8 IN 0 1n
C12 IN 0 10n
M§Q5 N011 N022 N015 N015 IPP200N25N3
M§Q6 N002 N019 N015 N015 IPP200N25N3
C13 N020 0 1µ
R10 IN N018 15k
R11 N018 0 1.74k
C14 N017 0 47µ
C15 N017 0 0.1µ
V2 N017 0 10.5
V5 VR 0 PWL(0 100Meg 20m 100Meg 20.01m 560 30m 560 30.01m 25.45)
R32 VR 0 R=V(VR)
C16 N030 0 7p
```

XU2 N049 N044 N046 0 0 N056 MP_02 N048 N050 N052 N051 N055 N054 N045 N047 LTC3721-1
R15 N042 0 1m
R16 N042 N050 100
C17 N056 0 330p
R17 N047 N048 100K
R18 N051 0 100K
C18 N054 0 .1µ
L5 IN N032 9.25µ Rser=0.15m
L6 N038 IN 9.25µ Rser=0.15m
L7 N033 N036 1332µ Rser=25m
L8 N035 N006 110µ
R19 N006 N055 169k
R20 N055 0 500
C19 N055 N053 .001µ
R21 N053 N052 200k
C20 N006 0 220µ
C21 N045 0 .001µ
M§Q7 N032 N046 N042 N042 IPP200N25N3
M§Q8 N038 N049 N042 N042 IPP200N25N3
C22 IN 0 220µ
C23 IN 0 220µ
R23 N055 N029 1.2k
D9 N034 N035 VS-E5PX6012
D10 N037 N035 VS-E5PX6012
D11 N041 N036 VS-E5PX6012
D12 N031 N033 VS-E5PX6012
M§Q9 N038 N049 N042 N042 IPP200N25N3
M§Q10 N032 N046 N042 N042 IPP200N25N3
C24 N006 0 220µ
C25 N006 0 10n
C26 N006 0 1n
C27 IN 0 1n
C28 IN 0 10n
M§Q11 N038 N049 N042 N042 IPP200N25N3
M§Q12 N032 N046 N042 N042 IPP200N25N3
C29 N047 0 1µ
R24 IN N045 15k
R25 N045 0 1.74k
C30 N044 0 47µ
C31 N044 0 0.1µ
V7 N044 0 10.5
C32 N056 0 7p
XU3 N075 N070 N072 0 0 N082 MP_03 N074 N076 N078 N077 N081 N080 N071 N073 LTC3721-1
R29 N068 0 1m
R30 N068 N076 100
C33 N082 0 330p
R31 N073 N074 100K
R33 N077 0 100K
C34 N080 0 .1µ
L9 IN N058 9.25µ Rser=0.15m
L10 N064 IN 9.25µ Rser=0.15m
L11 N059 N062 1332µ Rser=25m
L12 N061 N006 110µ
R34 N006 N081 169k

```
R35 N081 0 500
C35 N081 N079 .001µ
R36 N079 N078 200k
C36 N006 0 220µ
C37 N071 0 .001µ
M§Q13 N058 N072 N068 N068 IPP200N25N3
M§Q14 N064 N075 N068 N068 IPP200N25N3
C38 IN 0 220µ
C39 IN 0 220µ
R38 N081 N029 1.2k
D17 N060 N061 VS-E5PX6012
D18 N063 N061 VS-E5PX6012
D19 N067 N062 VS-E5PX6012
D20 N057 N059 VS-E5PX6012
M§Q15 N064 N075 N068 N068 IPP200N25N3
M§Q16 N058 N072 N068 N068 IPP200N25N3
C40 N006 0 220µ
C41 N006 0 10n
C42 N006 0 1n
C43 IN 0 1n
C44 IN 0 10n
M§Q17 N064 N075 N068 N068 IPP200N25N3
M§Q18 N058 N072 N068 N068 IPP200N25N3
C45 N073 0 1µ
R39 IN N071 15k
R40 N071 0 1.74k
C46 N070 0 47µ
C47 N070 0 0.1µ
V12 N070 0 10.5
C48 N082 0 7p
V3 N029 0 PWL(0 1.25)
D4 N008 N009 VS-E5PX6012
D6 N003 N004 VS-E5PX6012
D7 0 N014 VS-E5PX6012
D8 0 N001 VS-E5PX6012
D13 N033 N034 VS-E5PX6012
D14 N036 N037 VS-E5PX6012
D15 0 N031 VS-E5PX6012
D16 0 N041 VS-E5PX6012
D21 N059 N060 VS-E5PX6012
D22 N062 N063 VS-E5PX6012
D23 0 N057 VS-E5PX6012
D24 0 N067 VS-E5PX6012
.model D D
.model NMOS NMOS
.model PMOS PMOS
K1 L1 L2 L3 1
.model MYSW SW(Ron=0.0001 Roff=10Meg Vt=.5 Vh=-.4)
* DCDC2400-001 Transformer from Premo
* CPEX3635L-111MC Inductor
.tran 2 startup
* Set DAC output to 1.25V for a converter output of about 400V
* Set DAC output to 2.1V for a converter output of about 280V
* R10: RNCP1206FTD15K0
```

```
* R11: ERJ-1GNF1741C
* R3, R4: RC0402FR-07100KL
* R2: RC0402FR-07100RL
* R7: ERA-3AEB204V
* R5: CRCW2512169KFKEG
* R6: PNM0402E5000BST1
* R9: RC0402JR-071K2L
* C14: CGA9N3X7R1C476M230KB (ceramic)
* C15: KGM05AR71C104KH (ceramic)
* C6: GRM1555C1H102JA01D (ceramic)
* C13: CC0603KRX7R7BB105 (ceramic)
* C2: CL05B104KP5NNNC (ceramic)
* C1: GRM1555C1H331JA01D (ceramic)
* C16: CL10C070CB8NNNC (ceramic)
* C3: GRM1555C1H102JA01D (ceramic)
* C8: KGM15BR72D102KT (ceramic)
* C12: C0603X103K2RECAUTO (ceramic)
* C5, C7: UCS2C221MHD1TN (aluminum electrolytic)
* C10: C1206C103KCRAC7800 (ceramic)
* C11: VPCT501W102K1GV001T (ceramic)
* C4, C9: 450VXH220MEFCSN25X35 (aluminum electrolytic)
* R1: SSA2512LR001JWR
K2 L5 L6 L7 1
K3 L9 L10 L11 1
.lib LTC3721-1.sub
.backanno
.end
```

# Appendix I: Bill of Materials (BOM) for Isolated Design

The BOM associated with the Altium schematic in Figure 9.1. Please note, R13 in Tables I.1 and I.2 should instead be implemented with the SSA2512LR001JWR, which was in-stock as of April 2024 but not present in Altium.

Table I.1. Overview of the BOM.

**LTC3721-1_Single_Phase_Final.PrjPcb**

LTC3721-1_Single_Phase.BomDoc
None
4/9/2024 5:46 PM

| Designator | Qty | Supplier | Manufacturer | Manufacturer Part Number | Supplier Unit Price | Supplier Total Price |
|---|---|---|---|---|---|---|
| C1 | 1 | Digikey | KEMET | C1206C103KCRACTU | 0.1800 | 0.18 |
| C2, C3 | 2 | Digikey | Rubycon | 450VXH220MEFCSN25X35 | 6.5700 | 13.14 |
| C4 | 1 | Digikey | Johanson | VPCT501W102K1GV001T | 0.2300 | 0.23 |
| C5, C6 | 2 | Digikey | Nichicon | UCS2C221MHD1TN | 1.8500 | 3.7 |
| C7 | 1 | Digikey | Kyocera AVX | KGM15BR72D102KT | 0.1000 | 0.1 |
| C8 | 1 | Digikey | KEMET | C0603X103K2RECAUTO | 0.2400 | 0.24 |
| C9 | 1 | Digikey | TDK | CGA9N3X7R1C476M230KB | 1.8600 | 1.86 |
| C10 | 1 | Digikey | Kyocera AVX | KGM05AR71C104KH | 0.1000 | 0.1 |
| C11, C12 | 2 | Digikey | Murata | GRM1555C1H102JA01D | 0.1000 | 0.2 |
| C13 | 1 | Digikey | Yageo | CC0603KRX7R7BB105 | 0.1000 | 0.1 |
| C14 | 1 | Digikey | Samsung | CL05B104KP5NNNC | 0.1000 | 0.1 |
| C15 | 1 | Digikey | Samsung | CL10C070CB8NNNC | 0.1000 | 0.1 |
| C16 | 1 | Digikey | Murata | GRM1555C1H331JA01D | 0.1000 | 0.1 |
| D1, D2, D3, D4, D5, D6, D7, D8 | 8 | Digikey | Vishay | VS-E5PX6012L-N3 | 4.7700 | 38.16 |
| J1, J2, J3, J4, J5, J6 | 6 | | | | | 0 |
| L1 | 1 | Digikey | Codaca | CPEX3635L-111MC | 25.4500 | 25.45 |
| Q1, Q2, Q3, Q4, Q5, Q6 | 6 | Digikey | Infineon | IPP200N25N3G | 8.2600 | 49.56 |
| R1, R2, R4 | 3 | Digikey | Panasonic | ERJ-2GE0R00X | 0.0240 | 0.072 |
| R3 | 1 | Digikey | Stackpole Electronics | RNCP1206FTD15K0 | 0.1000 | 0.1 |
| R5, R10 | 2 | Digikey | Yageo | RC0402FR-07100KL | 0.0150 | 0.03 |
| R6 | 1 | Digikey | Vishay Dale | CRCW2512169KFKEG | 0.3400 | 0.34 |
| R7 | 1 | Digikey | Yageo | RC0402FR-07100RL | 0.1000 | 0.1 |
| R8 | 1 | Digikey | Vishay Dale | WSLF25121L000FEB | 0.8000 | 0.8 |
| R9 | 1 | Digikey | Panasonic | ERJ-1GNF1741C | 0.1000 | 0.1 |
| R11 | 1 | Digikey | Panasonic | ERA-3AEB204V | 0.1300 | 0.13 |
| R12 | 1 | Digikey | Yageo | RC0402JR-071K2L | 0.1000 | 0.1 |
| R13 | 1 | Digikey | Vishay Dale | PNM0402E5000BST1 | 1.2100 | 1.21 |
| TF1 | 1 | Premo S.L. | Premo S.L. | DCDC2400-001 | 54.0300 | 54.03 |
| U1 | 1 | Digikey | Analog Devices | LTC3721EUF-1#PBF | 12.7900 | 12.79 |
| | | | | | Total BOM Price | 203.122 |

Table I.2. Detailed description of the BOM.

**Bill of Materials for** LTC3721-1_Single_Phase_Final.PrjPcb

Source Data From: LTC3721-1_Single_Phase.BomDoc
Variant: None
Report Date: 4/9/2024 5:46 PM

| Altium Vault P/N | Designator | Description | Qty | Supplier | Supplier Part Number | Manufacturer | Manufacturer Part Number | Supplier Unit Price | Supplier Total Price |
|---|---|---|---|---|---|---|---|---|---|
| C1206C103KCRACTU | C1 | Ceramic Capacitor, Multilayer, Ceramic, 500V, 10% +Tol, 10% -Tol, X7R, 15% TC, 0.01uF, Surface Mount, 1206 | 1 | Digikey | 399-C1206C103KCRAC7800CT-ND | KEMET | C1206C103KCRACTU | 0.1800 | 0.18 |
| 450VXH220MEFCSN25X35 | C2, C3 | Aluminum Electrolytic Capacitor, Polarized, Aluminum (wet), 450V, 20% +Tol, 20% -Tol, 220uF, Through Hole Mount | 2 | Digikey | 1189-2033-ND | Rubycon | 450VXH220MEFCSN25X35 | 6.5700 | 13.14 |
| VPCT501W102K1GV001T | C4 | Ceramic Capacitor, 1000PF 500V X7R 0805 | 1 | Digikey | 709-VPCT501W102K1GV001TCT-ND | Johanson | VPCT501W102K1GV001T | 0.2300 | 0.23 |
| UCS2C221MHD1TN | C5, C6 | Aluminum Electrolytic Capacitor- 160volts, 220uF Sm Package, High Ripple, Hi Re | 2 | Digikey | 493-13277-1-ND | Nichicon | UCS2C221MHD1TN | 1.8500 | 3.7 |
| KGM15BR72D102KT | C7 | Ceramic Capacitor, 1000PF 200V X7R 0603 | 1 | Digikey | 478-KGM15BR72D102KTCT-ND | Kyocera AVX | KGM15BR72D102KT | 0.1000 | 0.1 |
| C0603X103K2RECAUTO | C8 | Ceramic Capacitor, Multilayer, Ceramic, 200V, 10% +Tol, 10% -Tol, X7R, 15% TC, 0.01uF, Surface Mount, 0603 | 1 | Digikey | 399-14200-1-ND | KEMET | C0603X103K2RECAUTO | 0.2400 | 0.24 |
| CGA9N3X7R1C476M230KB | C9 | Ceramic Capacitor, Multilayer, Ceramic, 16V, 20% +Tol, 20% -Tol, X7R, 15% TC, 47uF, Surface Mount, 2220 | 1 | Digikey | 445-7935-1-ND | TDK | CGA9N3X7R1C476M230KB | 1.8600 | 1.86 |
| KGM05AR71C104KH | C10 | Ceramic Capacitor, 0.1UF 16V X7R 0402 | 1 | Digikey | 478-KGM05AR71C104KHCT-ND | Kyocera AVX | KGM05AR71C104KH | 0.1000 | 0.1 |
| GRM1555C1H102JA01D | C11, C12 | Ceramic Capacitor, Multilayer, Ceramic, 50V, 5% +Tol, 5% -Tol, C0G, 30ppm/Cel TC, 0.001nF, Surface Mount, 0402 | 2 | Digikey | 490-3244-1-ND | Murata | GRM1555C1H102JA01D | 0.1000 | 0.2 |
| CC0603KRX7R7BB105 | C13 | Ceramic Capacitor, Multilayer, Ceramic, 16V, 10% +Tol, 10% -Tol, X7R, 15% TC, 1uF, Surface Mount, 0603 | 1 | Digikey | 311-1446-6-ND | Yageo | CC0603KRX7R7BB105 | 0.1000 | 0.1 |
| CL05B104KP5NNNC | C14 | Ceramic Capacitor, Multilayer, Ceramic, 10V, 10% +Tol, 10% -Tol, X7R, 15% TC, 0.1uF, Surface Mount, 0402 | 1 | Digikey | 1276-1002-1-ND | Samsung | CL05B104KP5NNNC | 0.1000 | 0.1 |
| CL10C070CB8NNNC | C15 | Ceramic Capacitor, Multilayer, Ceramic, 50V, 3.57% +Tol, 3.57% -Tol, C0G, -/+30ppm/Cel TC, 0.000007uF, Surface Mount, 0603 | 1 | Digikey | 1276-2137-1-ND | Samsung | CL10C070CB8NNNC | 0.1000 | 0.1 |
| GRM1555C1H331JA01D | C16 | Ceramic Capacitor, Multilayer, Ceramic, 50V, 5% +Tol, 5% -Tol, C0G, 30ppm/Cel TC, 0.00033uF, Surface Mount, 0402 | 1 | Digikey | 490-1295-1-ND | Murata | GRM1555C1H331JA01D | 0.1000 | 0.1 |
| VS-E5PX6012L-N3 | D1, D2, D3, D4, D5, D6, D7, D8 | Rectifier Diode, 1 Phase, 1 Element, 1200V V(RRM), Silicon, TO-247AD | 8 | Digikey | VS-E5PX6012L-N3-ND | Vishay | VS-E5PX6012L-N3 | 4.7700 | 38.16 |
| PAD_WITH_HOLE_4MMx1MM5 | J1, J2, J3, J4, J5, J6 | Pad with a hole 4mm x 1.5mm | 6 | | | | | | 0 |
| CPEX3635L-111MC | L1 | Power Inductor, 110 µH Shielded Wirewound Inductor 30 A 7.41mOhm Max Nonstandard Flat Wire, High Current, Soft Saturation | 1 | Digikey | 4044-CPEX3635L-111MC-ND | Codaca | CPEX3635L-111MC | 25.4500 | 25.45 |
| IPP200N25N3G | Q1, Q2, Q3, Q4, Q5, Q6 | Power Field-Effect Transistor, 64A I(D), 250V, 0.02ohm, 1-Element, N-Channel, Silicon, Metal-oxide Semiconductor FET, TO-220AB | 6 | Digikey | IPP200N25N3GXKSA1-ND | Infineon | IPP200N25N3G | 8.2600 | 49.56 |
| ERJ-2GE0R00X | R1, R2, R4 | Fixed Resistor, Metal Glaze/thick Film, 0.1W, 0ohm, Surface Mount, 0402 | 3 | Digikey | P0.0JCT-ND | Panasonic | ERJ-2GE0R00X | 0.0240 | 0.072 |
| RNCP1206FTD15K0 | R3 | Fixed Resistor, Thin Film, 0.5W, 15000ohm, 200V, 1% +/-Tol, 100ppm/Cel, Surface Mount, 1206 | 1 | Digikey | RNCP1206FTD15K0CT-ND | Stackpole Electronics | RNCP1206FTD15K0 | 0.1000 | 0.1 |
| RC0402FR-07100KL | R5, R10 | Fixed Resistor, Metal Glaze/thick Film, 0.0625W, 100000ohm, 50V, 1% +/-Tol, 100ppm/Cel, Surface Mount, 0402 | 2 | Digikey | 311-100KLRCT-ND | Yageo | RC0402FR-07100KL | 0.0150 | 0.03 |
| CRCW2512169KFKEG | R6 | Fixed Resistor, Metal Glaze/thick Film, 1W, 169000ohm, 500V, 1% +/-Tol, 100ppm/Cel, Surface Mount, 2512 | 1 | Digikey | 541-169KAFCT-ND | Vishay Dale | CRCW2512169KFKEG | 0.3400 | 0.34 |
| RC0402FR-07100RL | R7 | Fixed Resistor, Metal Glaze/thick Film, 0.0625W, 100ohm, 50V, 1% +/-Tol, 100ppm/Cel, Surface Mount, 0402 | 1 | Digikey | 311-100LRCT-ND | Yageo | RC0402FR-07100RL | 0.1000 | 0.1 |
| WSLF25121L000FEB | R8 | Fixed Resistor, Metal Strip, 8W, 0.007ohm, 0.0774W, 1% +/-Tol, 170ppm/Cel, Surface Mount, 2512 | 1 | Digikey | 541-3130-1-ND | Vishay Dale | WSLF25121L000FEB | 0.8000 | 0.8 |
| ERJ-1GNF1741C | R9 | Fixed Resistor, Thick Film 0201 1.74K Ohm 1% 0.05W ±200ppm/°C Molded SMD TR | 1 | Digikey | P122778CT-ND | Panasonic | ERJ-1GNF1741C | 0.1000 | 0.1 |
| ERA-3AEB204V | R11 | Fixed Resistor, Thin Film, 0.1W, 200000ohm, 75V, 0.1% +/-Tol, 25ppm/Cel, Surface Mount, 0603 | 1 | Digikey | P200KDBCT-ND | Panasonic | ERA-3AEB204V | 0.1300 | 0.13 |
| RC0402JR-071K2L | R12 | Fixed Resistor, Metal Glaze/thick Film, 0.0625W, 1200ohm, 50V, 5% +/-Tol, 100ppm/Cel, Surface Mount, 0402 | 1 | Digikey | 311-1.2KJRCT-ND | Yageo | RC0402JR-071K2L | 0.1000 | 0.1 |
| PNM0402E5000BST1 | R13 | Fixed Resistor, Thin Film, 0.05W, 500ohm, 75V, 0.1% +/-Tol, 25ppm/Cel, Surface Mount, 0402 | 1 | Digikey | 541-1905-1-ND | Vishay Dale | PNM0402E5000BST1 | 1.2100 | 1.21 |
| DCDC2400-001 | TF1 | Push-Pull Transformer 2kW 100kHz 1+1:12 | 1 | Premo S.L. | DCDC2400-001 | Premo S.L. | DCDC2400-001 | 54.0300 | 54.03 |
| LTC3721EUF-1#PBF | U1 | Switching Controller, Current-mode, 1000kHz Switching Freq-Max, PDSO16 | 1 | Digikey | LTC3721EUF-1#PBF-ND | Analog Devices | LTC3721EUF-1#PBF | 12.7900 | 12.79 |
| | | | | | | | | Total BOM Price | 203.122 |

# Appendix J: Datasheet Links

Table J.1. Datasheets for each component in Figure 9.1.

| Designator | Manufacturer Part Number Datasheet Links |
|---|---|
| C1 | C1206C103KCRACTU |
| C2, C3 | 450VXH220MEFCSN25X35 |
| C4 | VPCT501W102K1GV001T |
| C5, C6 | UCS2C221MHD1TN |
| C7 | KGM15BR72D102KT |
| C8 | C0603X103K2RECAUTO |
| C9 | CGA9N3X7R1C476M230KB |
| C10 | KGM05AR71C104KH |
| C11, C12 | GRM1555C1H102JA01D |
| C13 | CC0603KRX7R7BB105 |
| C14 | CL05B104KP5NNNC |
| C15 | CL10C070CB8NNNC |
| C16 | GRM1555C1H331JA01D |
| D1, D2, D3, D4, D5, D6, D7, D8 | VS-E5PX6012L-N3 |
| L1 | CPEX3635L-111MC |
| Q1, Q2, Q3, Q4, Q5, Q6 | IPP200N25N3G |
| R1, R2, R4 | ERJ-2GE0R00X |
| R3 | RNCP1206FTD15K0 |
| R5, R10 | RC0402FR-07100KL |
| R6 | CRCW2512169KFKEG |
| R7 | RC0402FR-07100RL |
| R8 | WSLF25121L000FEB |
| R9 | ERJ-1GNF1741C |
| R11 | ERA-3AEB204V |
| R12 | RC0402JR-071K2L |
| R13 | PNM0402E5000BST1 |
| TF1 | DCDC2400-001 |
| U1 | LTC3721EUF-1#PBF |

# Appendix K: Poster

The poster below was designed for the undergraduate research projects showcase–formerly coined as project presentation day–at WPI.

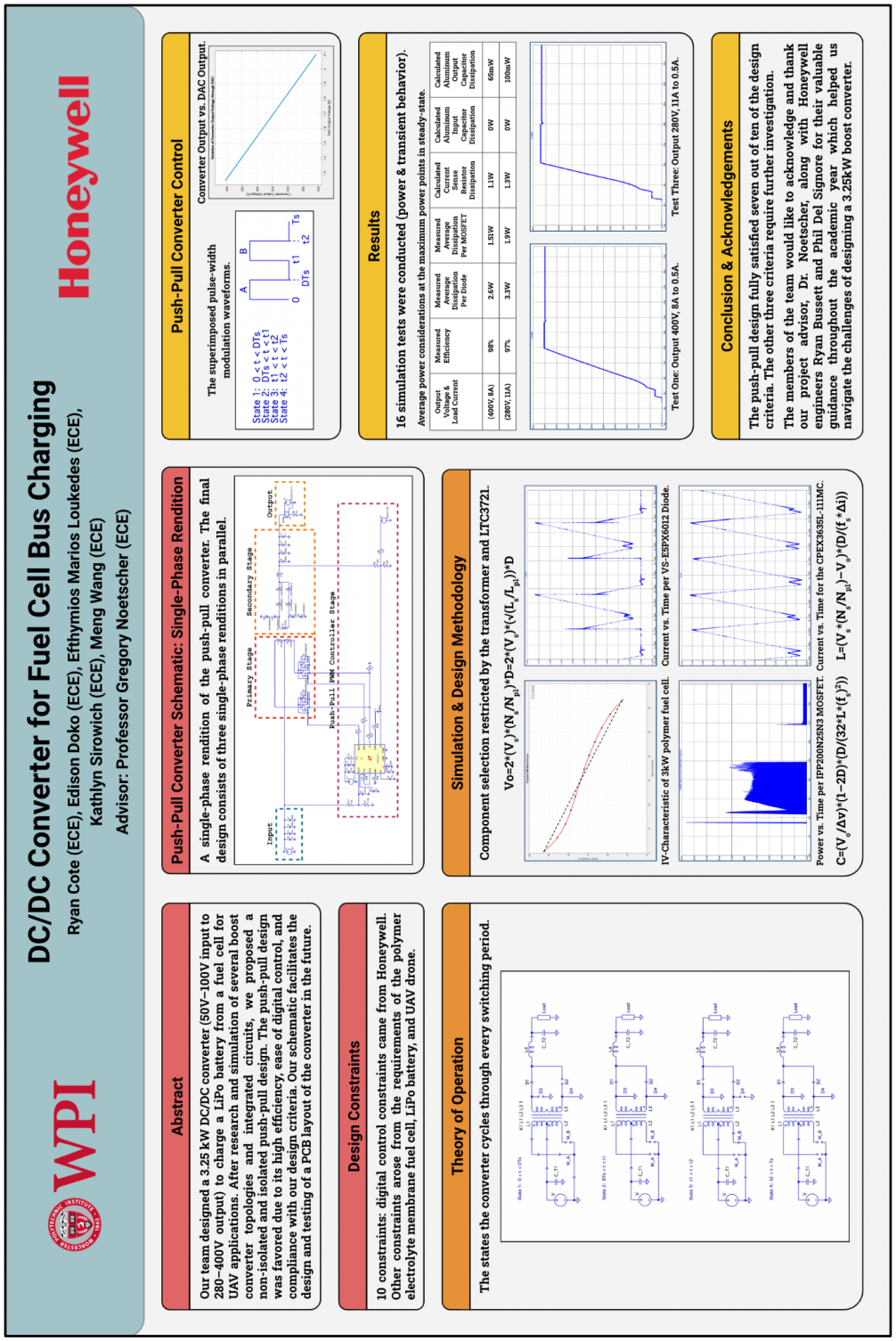


Figure K.1. MQP poster.