Integrated Circuit Building Blocks for a Cyclic Analog-to-Digital Converter in 0.18um CMOS

Shant Orchanian | Gentian Rrudho | Alvaro Soares Jr.

NECAMSID
The New England Center for Analog & Mixed-Signal Design at WPI

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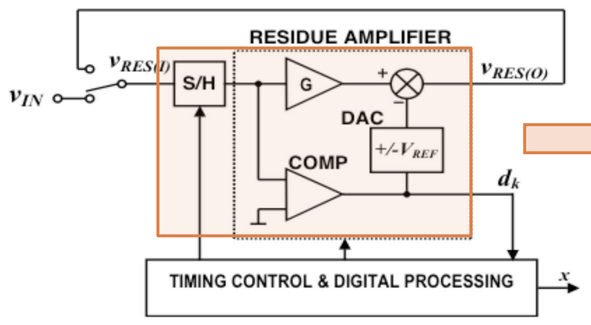
Advisor: Prof. McNeill

WPI

Cyclic ADC

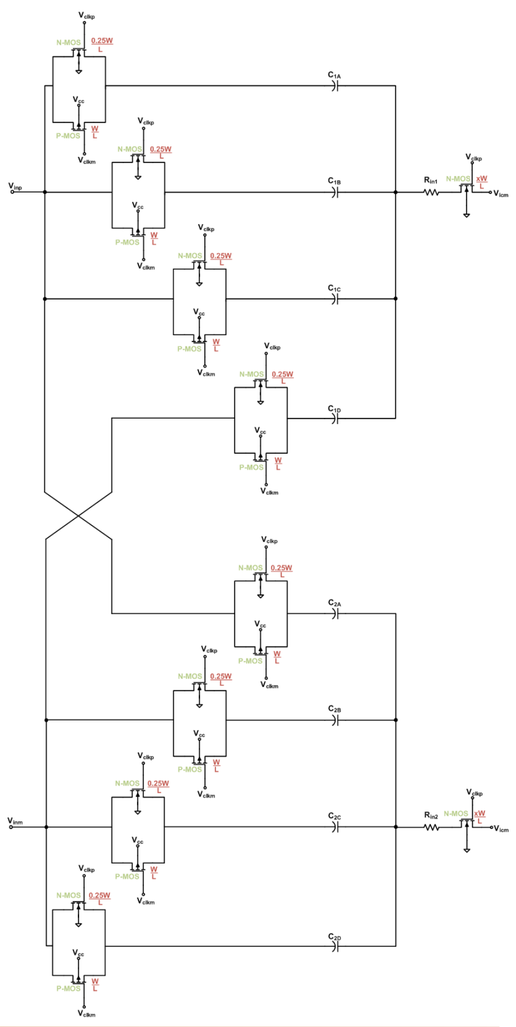


Specifications

SIZE	1 mm^2
PROCESS	0.18 MICRON CMOS
RESOLUTION	12-14 BITS
THROUGHPUT	1 Msps
TEST TIME	LESS THAN 1 sec

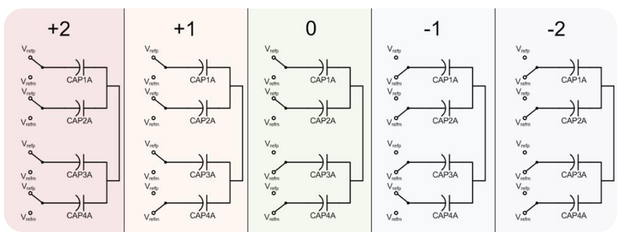
1 Input Block

• TO KEEP SYMMETRY IN OUR CIRCUIT, WE HAVE THE INPUT ALSO GO THROUGH THE RESIDUE AMPLIFIER. THEREFORE, WE DIVIDED THE INPUT BY 2 BY CONNECTING 3 CAP TO Vin_p AND 1 CAP TO Vin_m.



Making the Decisions

• WE IMPLEMENTED OUR DECISIONS FOR THE SUBTRACTION FUNCTION AS A COMBINATION OF 4 CAPACITORS BY SWITCHING THE CAPS TO DIFFERENT REFERENCE VALUES.



Gain and Voltage Ranges

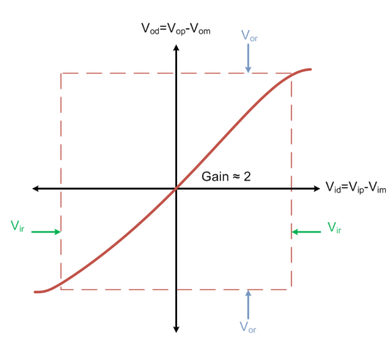
• PRIOR RESEARCH HAS INDICATES THAT WE MUST MAINTAIN A DIFFERENTIAL **GAIN OF 2** OR LESS.

$V_{ir} = 0.34V$

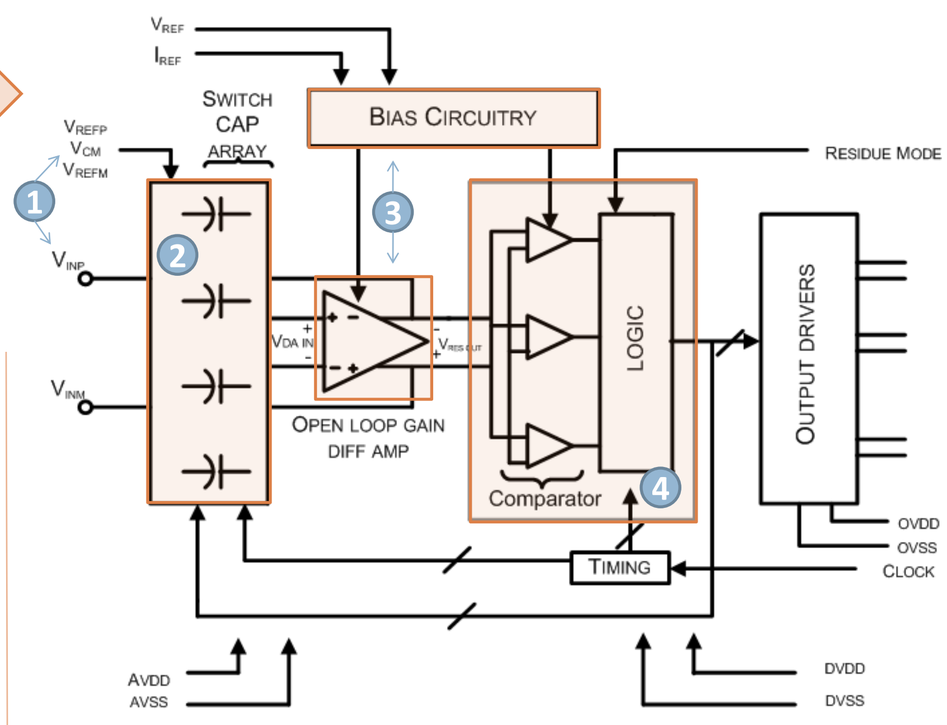
$V_{ICM} = 1.09V$

$V_{or} = 0.68V$

$V_{OCM} = 1.3V$

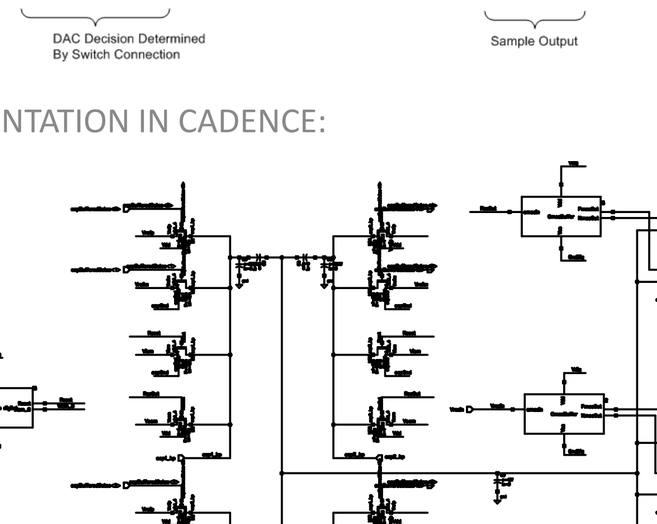


IC Block Diagram



2 Switched Capacitor Array

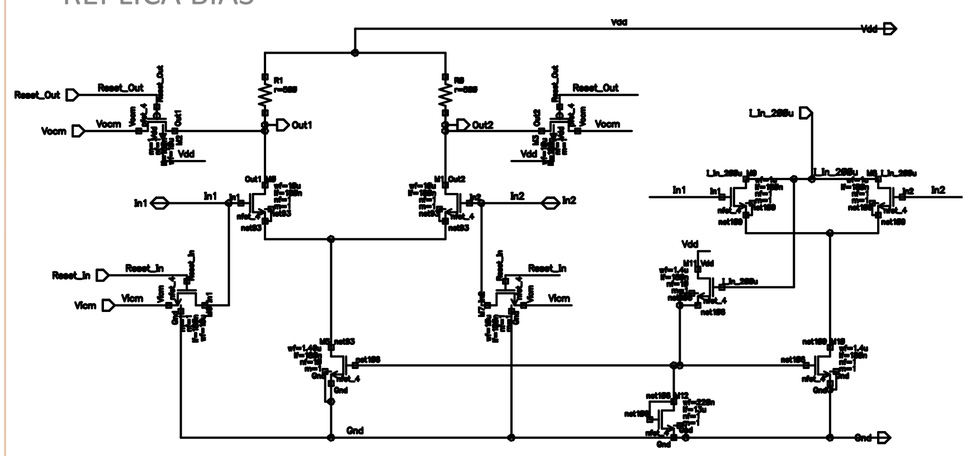
• IN ORDER TO BE ABLE TO USE THE RESIDUE SIGNAL FROM OUR CONVERSIONS, WE NEED TO IMPLEMENT A **SWITCHED CAPACITOR NETWORK**.



• IMPLEMENTATION IN CADENCE:

3 Open Loop Differential Amplifier

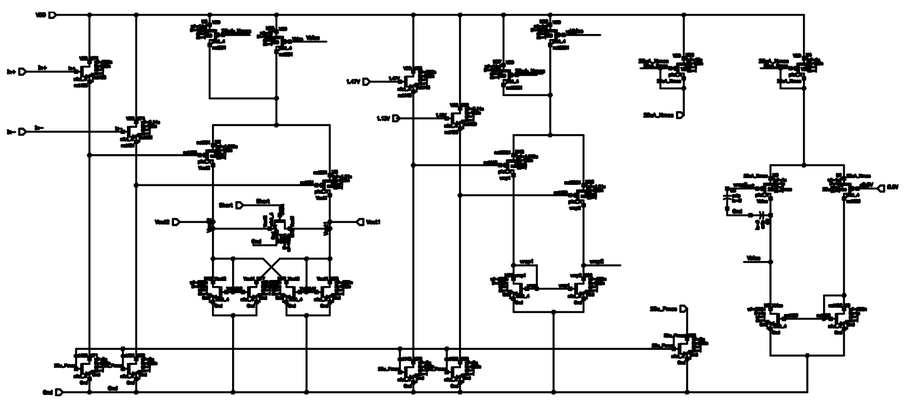
• OPEN LOOP GAIN ≈ 2
• RESISTIVE LOAD
• REPLICA BIAS



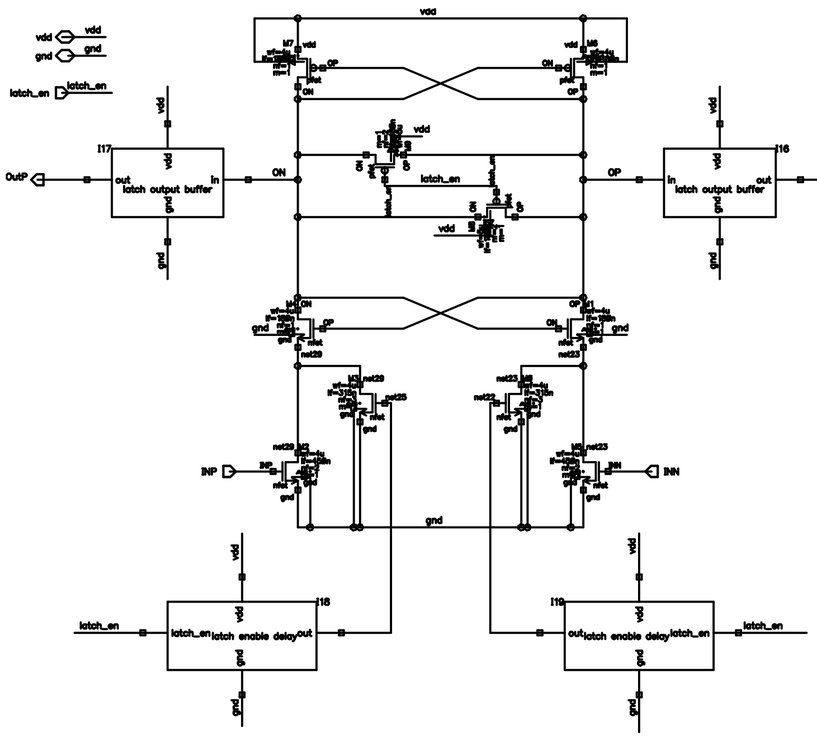
4 Logic and Comparators

• THE **COMPARATORS** CREATE THE THERMOMETER CODE FOR THE OUTPUT, SHOWN BELOW:

(PRE-AMP IS BALANCED WITH 0.34V DIFFERENTIAL INPUT)



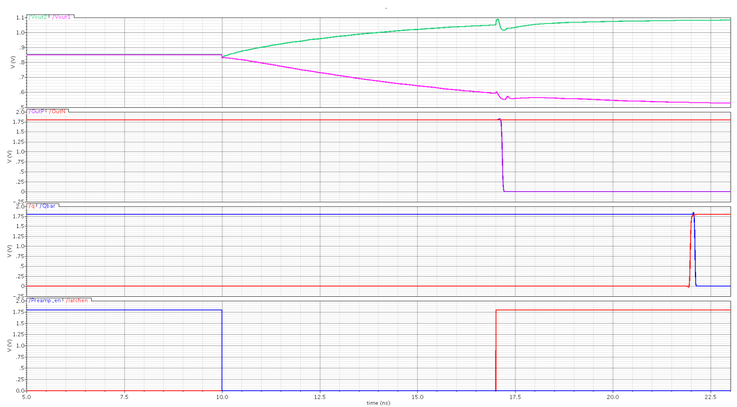
• THIS ANALOG LATCH WAS USED FOR THIS BLOCK, AS WELL:



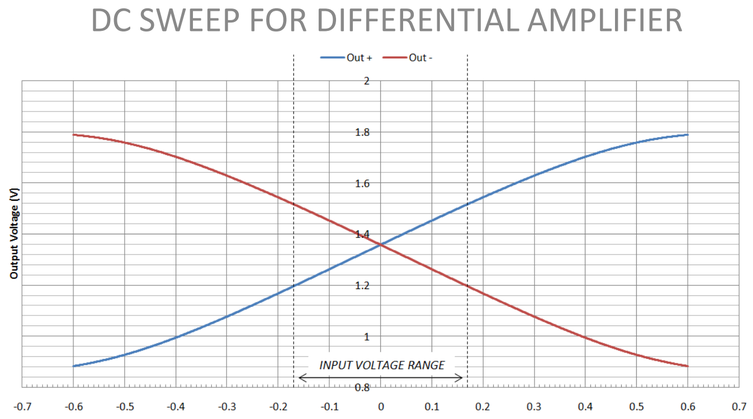
SIMULATED RESULTS

SIMULATED IMPLEMENTATION OF COMPARATORS

(TESTING CONDITION: 0.28 V DIFFERENTIAL VOLTAGE TRIGGERS LATCH)

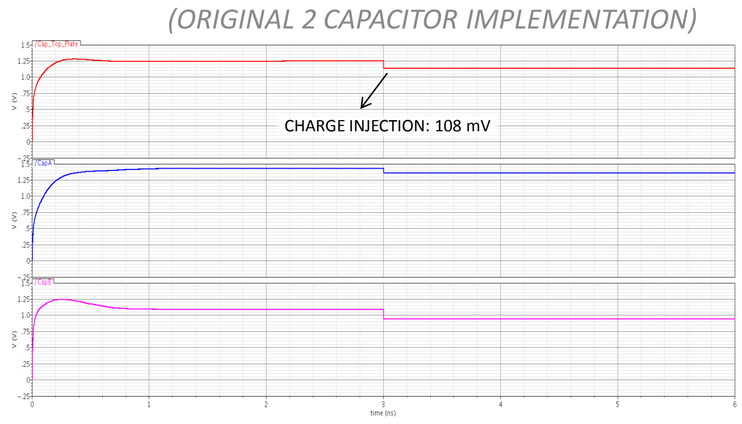


DC SWEEP FOR DIFFERENTIAL AMPLIFIER



CHARGE INJECTION IN SWITCHED CAP CIRCUIT

(ORIGINAL 2 CAPACITOR IMPLEMENTATION)



CHARGE INJECTION IN SWITCHED CAP CIRCUIT

(NEW 4 CAPACITOR IMPLEMENTATION)