Worcester Polytechnic Institute

Major Qualifying Project

Low Power Skin Impedance Spectrometer

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1 Introduction

Skin impedance is the opposition that skin presents to current as a function of applied voltage. Its value depends on the structure of cell membranes, amount of intra and extracellular fluid and compactness of tissue. [1] The value of skin impedance can be used as an indicator in many applications because there is a relation between impedance and cell structure. Some of these applications are: diabetes diagnosis [2], Body Mass Index (BMI) calculation, [3] pain and exertion level measurement [4] and cancer diagnosis [5]. Additionally, recent studies [4] [2] [5] show skin impedance measurement can be considered as an alternative to other more invasive and complex diagnostic methods.

The goal of our project is to develop a low power biomedical device that measures skin impedance across a wide frequency range. This frequency range was chosen to be 5 kHz to 100 kHz. Additionally, our device will provide the user with a visual representation of the measurements in Matlab. Unlike many available meters, this skin impedance meter will be designed to be low power, portable, and versatile for multiple applications.

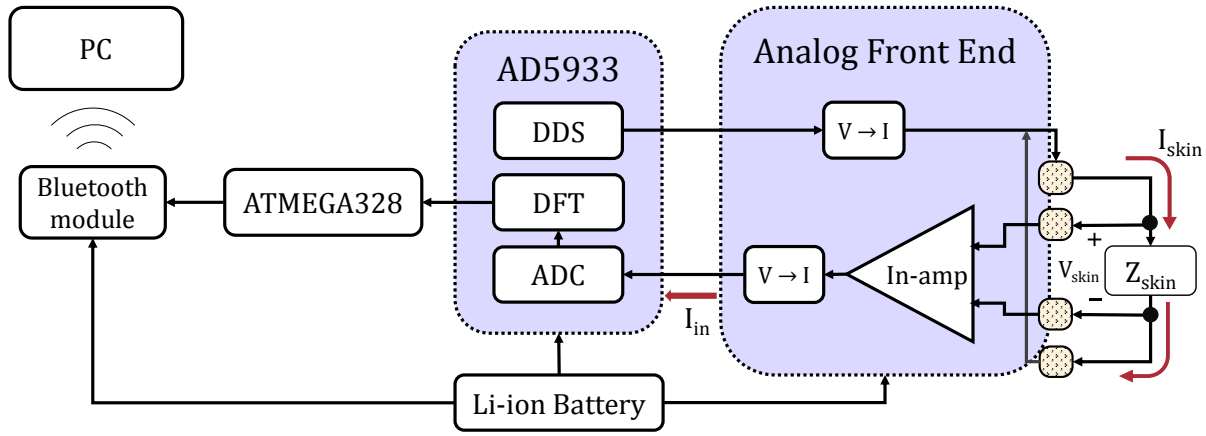

Figure 1.1: Simple Block Diagram

As shown in Figure 1.1, our project involves a measurement system that interfaces with the subjects body with four electrodes. Two of these electrodes inject current into the body, and the other two measure the voltage drop across the body. Knowing both the injected current and voltage drop, the system can compute the skin impedance of the subject. The computed data is then transmitted through Bluetooth to a laptop running Matlab where the data is presented in two plots. One plot that shows impedance vs. frequency, and the other that shows impedance vs. time.

As described in Section 2.2 Measuring impedance is a more complex task than measuring Electrocardiogram (EKG). This is because it requires an active system to both inject a signal into the body and measure the body's response to this signal. Another challenge is that this measurement can be affected by many factors. These factors include: body temperature, skin moisture level, stress or anxiety levels, age and sex. These challenges need to be considered during development of design requirements.

It is important to validate the results obtained from the system. In order to do so, we will compare our results with results obtained from other impedance measurement techniques. Additionally, to ensure our system is capable of measuring skin impedance, we will build an electrical model that represents a persons skin. As another validation method, we will use Bioelectrical Impedance Analysis (BIA) to calculate BMI and then compare the value to BMI values obtained using skin folding.

2 Background

In this chapter, we discuss about topics related to our project. We first examine what is electrical and skin impedance. Then, we present different applications of skin impedance measurement in order to highlight its importance. We also studied about safety considerations and standards since our project is related to human subject. Finally, we will discuss about the techniques commonly used for calculating real and imaginary part of an unknown impedance.

2.1 Electrical Impedance

Impedance is defined as the frequency domain ratio of the voltage to the current. In other words, it is the voltage-current at a particular frequency ω. [6] Impedance is a complex number with a real and an imaginary part. The real part of the impedance is known as resistance, R [Ohms, Ω], and the imaginary part of the impedance is known as reactance, X [Ohms, Ω]. Impedance can be expressed in polar or rectangular form.

$$Z = |Z|\, e^{j \cdot arg(Z)} \tag{2.1}$$

$$Z = R + jX \tag{2.2}$$

Where:

- |Z| is the magnitude of the complex impedance, or the ratio of the voltage amplitude to the current amplitude.
- arg(Z) is the phase of the complex impedance, or the phase shift by which the current lags the voltage.

It is important to note that the polar form of the impedance in (2.1) relates the amplitude and phase Eq. (2.2) of a sinusoidal current and voltage signal.

2.2 Skin Impedance

The human body impedance can be modeled as being composed of resistive and capacitive elements. More specifically, cell membranes act like capacitors and body fluids act like resistors. [1] Cell membranes behave as capacitors when AC current passes through them because they consist of a layer of non-conductive lipids sandwiched between conductive protein molecules, as shown in Figure 2.1. Therefore, at low frequencies, current can primarily pass through extracellular fluids and, at high frequencies, current can primarily pass through cell membranes.

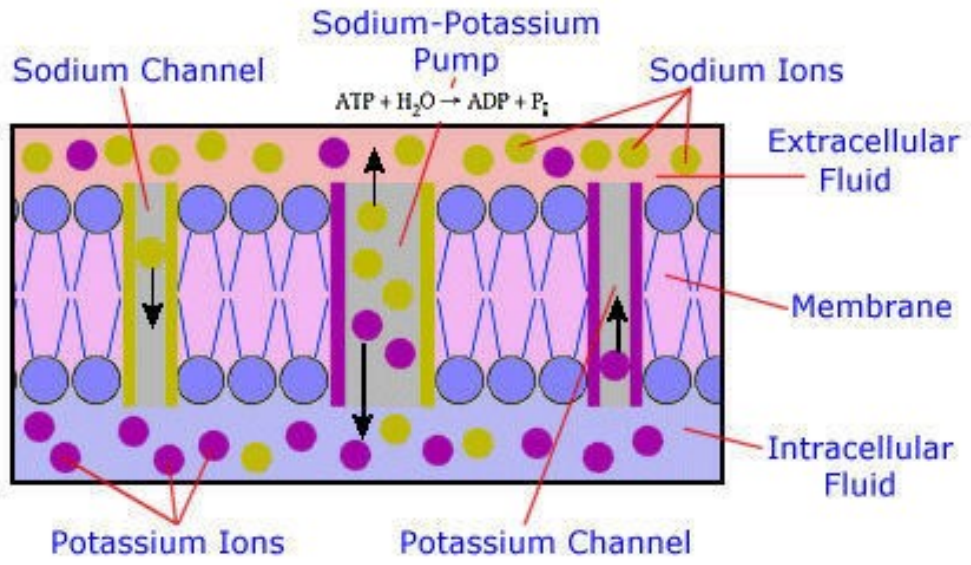

Figure 2.1: Cell Membrane and Extracellular Fluid [7]

In more detail, the skin impedance can be modeled according to Figure 2.2:

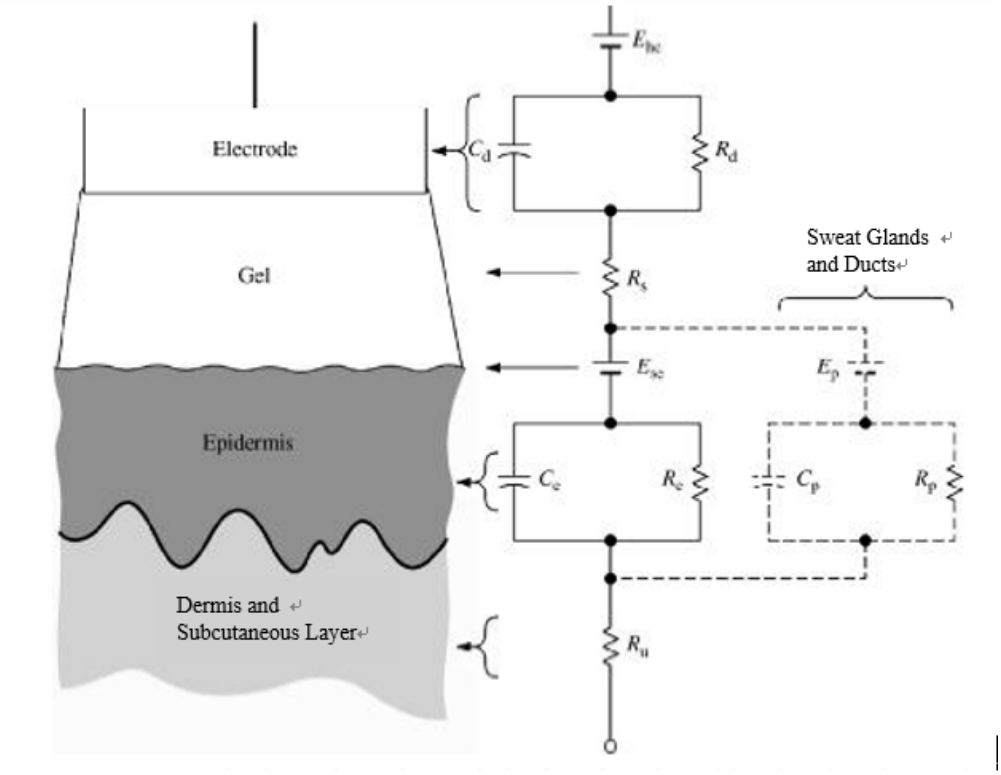

Figure 2.2: Equivalent model of skin and electrode configuration [8]

There are three frequency dependent regions of impedance in the skin known as α, β and γ-dispersions. [9] In each of these regions, there is a sharp decrease in impedance as frequency increases. This decrease is known as a dielectric dispersion. The three regions can be observed in Figure 2-3.

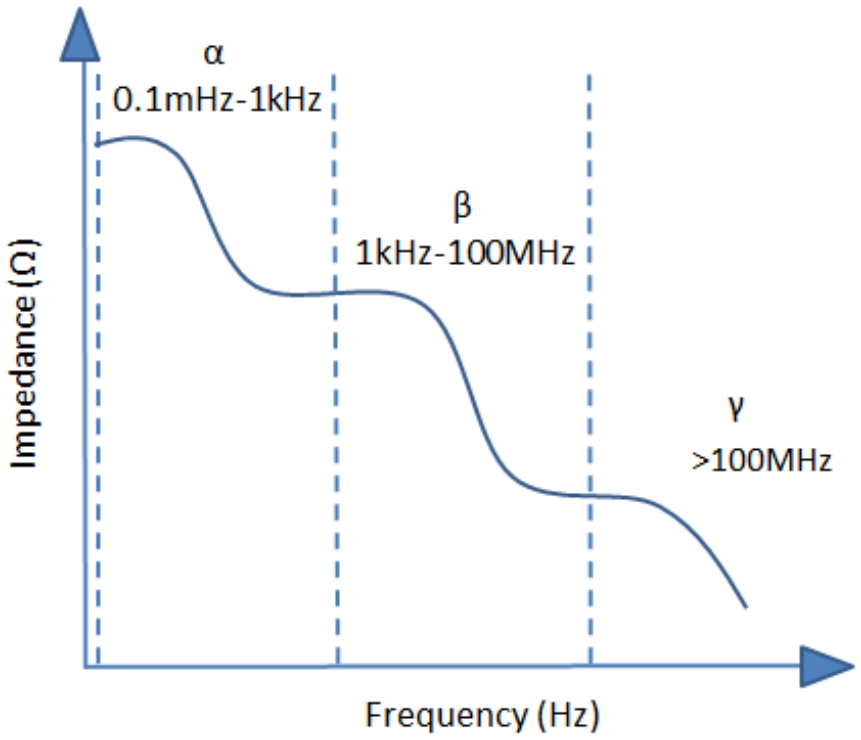

Figure 2.3: Skin Dispersion Regions

The α-dispersion occurs typically from DC to 1 kHz, and it is caused by surface conductance and interfacial polarization at the membrane boundaries. [10] The β-dispersion occurs from 1 kHz to 100 MHz, and it happens because the cell membrane capacitances are shorted over this frequency range. Above 100 MHz, the γ-dispersion occurs because of the relaxation of the water dipoles in the cells. [10] It is important to mention that α- and β-dispersion windows are the most relevant for medical applications because most changes in electrical properties of skin occur within these regions. Skin impedance varies depending on frequency, electrode type, and the age and sex of the subject. It is important to understand what the typical skin impedance ranges in human subjects are. A research study [11] that measures skin impedance of 10 healthy males can help us better understand what this typical range is. In [11], the skin impedance values at different frequencies were measured in 10 different locations.

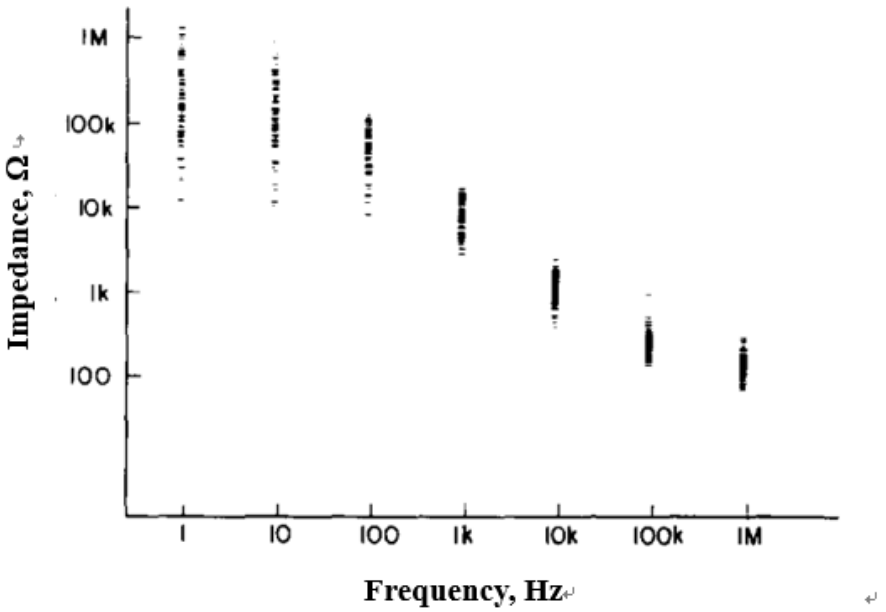

Figure 2.4: Impedance Values over Different Frequency [11]

Additionally, skin impedance measurements also depend on the test setup and type and surface area of the electrodes used to record them. In [12], the skin impedance of 367 human subjects was measured. This study used two different types of electrodes to understand how these affect the measurements. First, researchers use cylindrical brass rod (diameter = 1.5 cm, length = 14 cm) for grasping contact with the hand. Afterwards, they repeated the study using a square copper plate electrode of area 144 or 25 mm^2 for contact with the index finger. The magnitude and phase angle of the skin impedance was measured across different frequencies and the results for these two types of electrodes are presented in Figures 2.5, 2.6, 2.7 and 2.8.

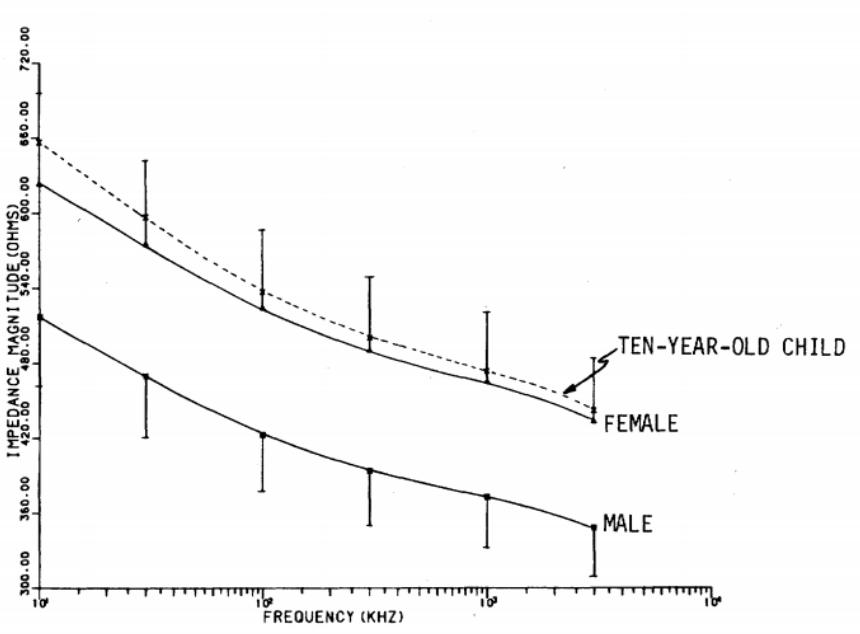

Figure 2.5: Impedance Magnitude vs. Frequency for Grasping Contact [12]

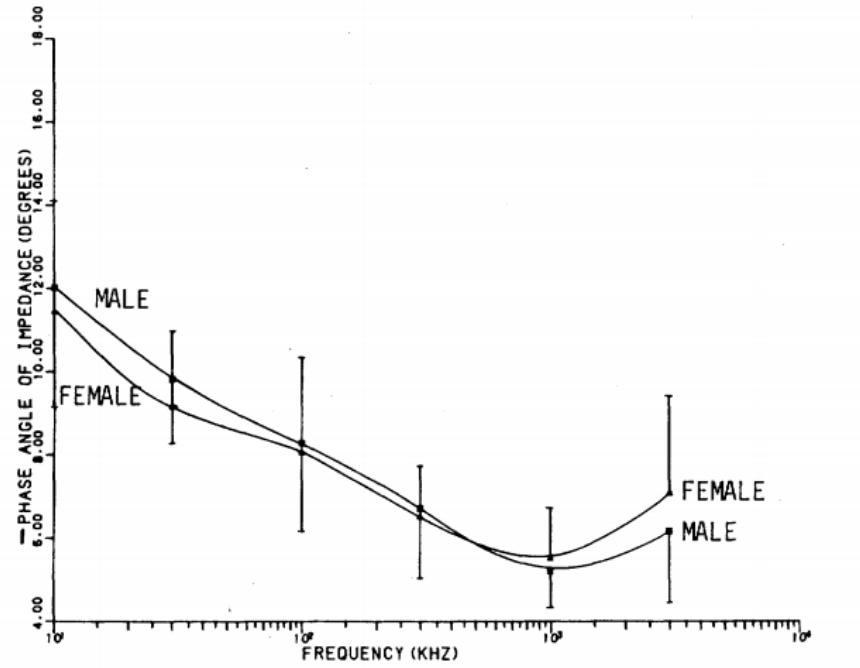

Figure 2.6: Avg. Impedance Phase Angle vs. Frequency for Grasping Contact [12]

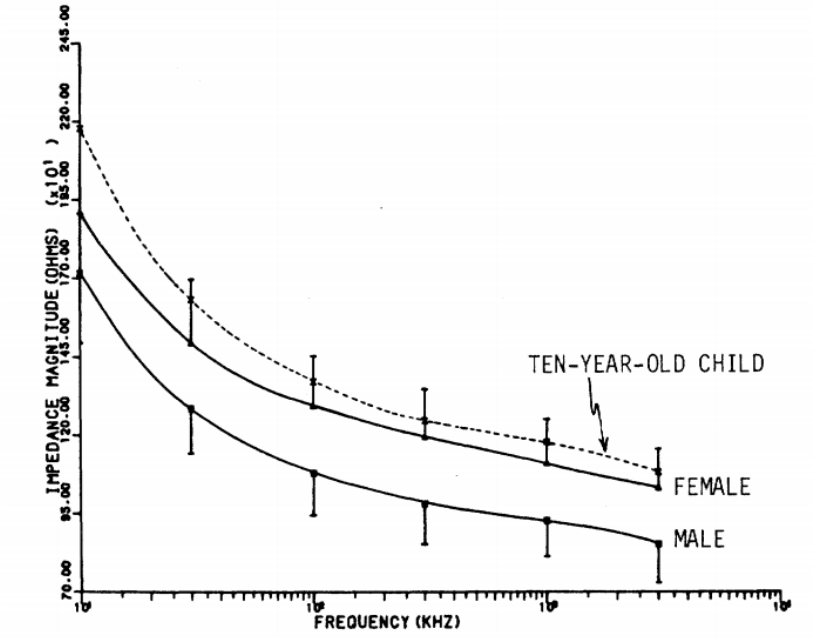

Figure 2.7: Avg. Impedance Magnitude vs. Frequency for Finger Electrode [12]

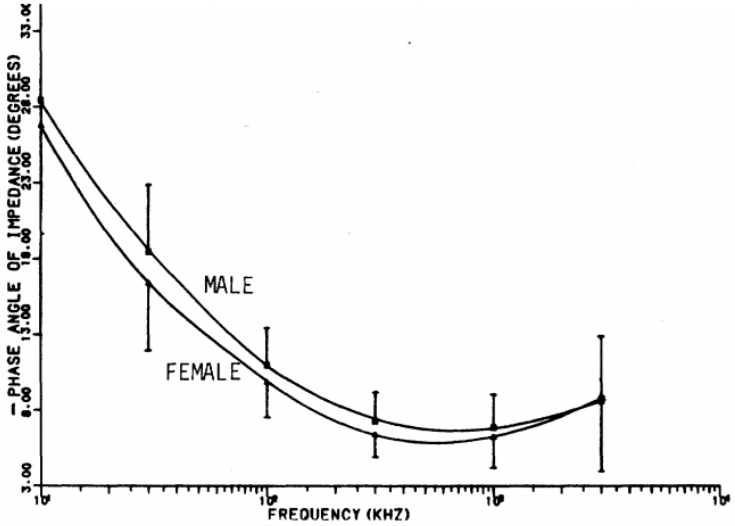

Figure 2.8: Avg. Impedance Phase Angle vs. Frequency for Finger Electrode [12]

In addition to showing the dependency of skin impedance measurements to frequency and electrode surface area, these figures also show how impedance varies according to the age and sex of the individuals.

2.2.1 Applications

Bioelectrical Impedance Analysis

The first application of skin impedance that we researched was Bioelectrical Impedance Analysis (BIA), which is a common method to measure body composition.[3] BIA uses the impedance, height, and weight of subjects to calculate their Fat Free Mass (FFM), Total Body Water (TBW), and Skeletal Muscle Mass (SMM).

The research we studied involves a setup with two or three electrodes attached to the subjects body. In a two electrode setup, the electrodes can be attached either on both wrists or one wrist and an ankle on the same side of the body. Then, a current of 800 μA is sent through the body in order to find the impedance. The impedance, height, and weight of the individual can be used in Eq. (4.25) to obtain the FFM. [3]

$$FFM = 6.37 + 0.64 \cdot Weight + \frac{0.64 \cdot Height^2}{Z} - 0.16 \cdot Age - 2.71 \cdot Sex \tag{2.3}$$

(Sex: Man = 1, Woman = 2)

There are limitations when using skin impedance to determine body composition. One of the main limitations is that certain activities, such as eating, drinking and exercising, prior to testing will skew the results.[13] For example, eating less than 4 hours before BIA testing will cause impedance result to decreases by up to 2.5%, and exercising changes the impedance value by 3% and the reactance by around 8%. Another issue is that the equations used in these calculations are dependent on race, age-range, and body type.

Diabetes

Another important application of skin impedance is diabetes diagnosis. [2] There are several ways to diagnose diabetes or high glucose content in the blood. Table 2.1 summarizes the detection principle and drawbacks of some methods.

Detection Method	**Drawback**
Finger Pricking	Invasive and prone to infection
Radio wave transmission	Requires high frequency (5 GHz 12 GHz) to penetrate skin
Infrared radiation absorption	Sensor impedance depends on frequency so it is not convenient to use this parameter for blood glucose level estimation.

Table 2.1: Methods of Diabetes Testing [2]

Considering all these drawbacks, there is a need for a more accurate and cheaper system which measures blood glucose level. Impedance decreases when blood glucose level increases and impedance increases when blood glucose level decreases. By measuring the skin impedance, a good indication of blood glucose levels can be obtained. This non-invasive

method reduces finger pricking for blood glucose detection and hence reduces chances of infection.

Pain / Exertion Measurement

Skin impedance can also be used as an objective indicator for pain or exertion. [14] This is because the skin impedance changes with the increase in sweating or cardiovascular activity. When an individual experiences pain, his or her sympathetic nervous system increases the activity of the sweat glands. Additionally, other studies [12][4] have shown high correlation between the objective pain measurement obtained from skin impedance measurement and the subjective pain measurement indicated by the patients.

To measure pain, a variety of bio-impedance meters can be used. The device used in the cited researches was the EIM 105-TI impedance meter from General Devices. To objectively assess pain, the skin impedance of the patient is initially measured before the patients muscle/joint is strained. This establishes a baseline level for the pain level of the individual. After that, pain is induced by standing up, squatting, walking up and down the stairs or by knee and spine loading. Different impedance meters inject different signals in the body to measure its impedance. For example, the EIM 105-TI measures impedances between 0.1 and 199.999K Ohms using 10A at 10 or 100 kHz through three electrodes. [15]

Skin Cancer

Typical skin cancer diagnosis involves visual inspection of a suspicious skin lesion and examination of a biopsy. This process is invasive and dependent on the skill of the inspector. However, using the difference between skin impedance of normal tissue and that of melanoma tissue, skin cancer can be diagnosed non-invasively.

For skin cancer detection, a probe consisted of circular electrodes is commonly used to inject current signals and measure voltages. A single frequency or multi-frequency screening can be used, but higher accuracy is achieved by using multi-frequency [5]. In order to compare the impedances, it is required to measure the impedance of a benign skin lesion. Skin tissues with melanoma or other types of skin cancer have lower skin impedance, or higher conductivity, than normal tissues. The differences in measurements are more noticeable at lower frequencies. The accuracy of this method is significant enough, generally around 90% specificity with nearly 100% sensitivity for multi-frequency scanning, to be considered as a diagnostic tool.

Summary

Table 2.2 shows the requirements of Skin Impedance measurements for the applications included in the background. The table includes the following requirements: number of the electrodes and their location, the range of operation and the current signal used in each of the operations. Figures 2.9 and 2.10 show the specialized electrode used in the skin cancer applications, and the electrode mesh for the tomography application.

Application	**Number of Electrode(s)**	**Impedance Range**	**Range of Frequencies**	**Current**	**Error in |Z|**	**Error in ∠Z**
Unit		Ω	Hz	μA	%	∘
Single	2	200 - 1.2k	50k	800	≤ 8	0.8 - 1.6
Frequency	4	175 - 1.1k	50k	800	≤ 1.2	0.2 - 0.8
BIA	4+	150 - 1.05k	50k	800	≤ 0.5	0.8 - 1.2
Multi	2	175 - 110k	0 - 500k	800	≤ 8	0.8 - 1.2
Frequency	4	140 - 101k	0 - 500k	800	≤ 1.2	0.8 - 1.2
BIA	4+	120 - 100k	0 - 500k	800	≤ 0.5	0.8 - 1.2
ImpediMed SBF7 BIA	4	50 - 1100	4k - 1000k	N/A	≤ 1	N/A
Diabetes	2	1.2k - 3k	10k - 100k	1	≤ 5	0.8 - 1.2
Pain	3	200 - 1000	10k - 100k	10	≤ 3	0.6 - 1
Cancer	1	80 - 150k	1k - 3M	75	≤ 0.5	0.2 - 0.8
Tomography	Mesh	100 - 100k	1k - 1M	≤ 5000	≤ 0.1	0.1 - 0.2

Table 2.2: Skin Impedance Applications Summary [13][2][14][15][16][17][18]

Figure 2.9: Skin Cancer Electrode [19]

Figure 2.10: Electrode Mesh for Tomography[20]

2.3 Safety Considerations

2.3.1 Electrical Safety Standards for Medical Devices

Since this project involves passing AC current through a human body, it is important to know the current safety standards. A person can feel AC currents above 1 mA (RMS) at 60 Hz or DC currents above 5 mA. [21] At around 10 mA, AC current passing through the arm of a 68-kilogram (150 lb.) human can cause powerful muscle contractions. This means the subject is unable to voluntarily control muscles and cannot release an electrified object. These current levels can be used to establish the maximum limit of current that our device can pass through the body to avoid injuring the subject.

The IEC 60601 is the safety standard for medical electrical devices. [22] This standard warns about the dangers of micro and macroshock. Microshock occurs when the current flows through the heart and macroshock occurs when the safety ground in the device breaks causing a dangerous current ($>$ 10mA) to pass through the body, resulting in breathing problems or ventricular fibrillation. The standard states that isolating the power supply and limiting the current injected into the body are the best ways to avoid both micro and macroshock. Limiting the current can be done by making a current source circuit and isolating the power supply can be done by the use of an isolation transformer, as shown in Figure 2.11.

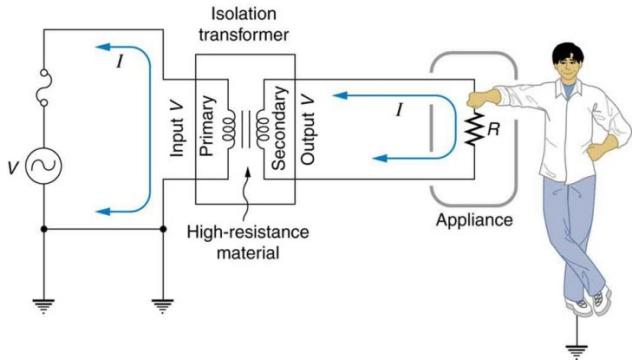

Figure 2.11: Isolation Transformer [23]

2.3.2 WPI Institutional Review Board Approval

Since the project will involve system testing on human subjects, it is required to receive an approval from WPI's Institutional Review Board for conducting in vivo testing. In general, an Institutional Review Board (IRB) is a committee that is in charge of reviewing, approving and monitoring biomedical and behavioral research involving humans. [3] The IRB at WPI has detailed criteria for projects that are exempted from IRB. These criteria can be found in appendix C. The general procedures for WPIs IRB application is listed below.

1. Set up detailed specifications or test conditions that will affect human subjects.
2. Complete the IRB application form and apply for the review of the project.
3. If the Chair needs more information, a representative of the project, in this case, the advisor, will be summoned to the IRB board meeting.
4. After reviewing the details, some modification or suggestion of the project may be presented to ensure the safety of subjects.
5. Accept or negotiate suggestions.
6. Project approved.

Some facts to take into consideration are:

- Approval is given for a full year
- Changes can be made after the review is done and the approval is given
- The team can test themselves with self-consents.

The team was able to acquire the approval from WPI IRB office. The IRB application and the letter of approval is included in Appendix C.

2.4 Data Processing

Skin impedance is a complex number and can be calculated by injecting current through and then measuring voltage across skin. After measuring voltage drop, it is necessary to compute both real and imaginary parts of impedance using the current signal and voltage drop. This section details the two most common methods used to find the real and imaginary parts of an unknown impedance.

2.4.1 Quadrature Demodulation

The first method Quadrature Demodulation [24], also known as I/Q Demodulation or Sine Correction method, is a method for finding the phase and magnitude of a signal by multiplying the signal by both an in-phase signal and a quadrature signal. These two signals are separated by a 90 degree phase shift. Figure 2.12 is a block diagram of Quadrature Demodulation.

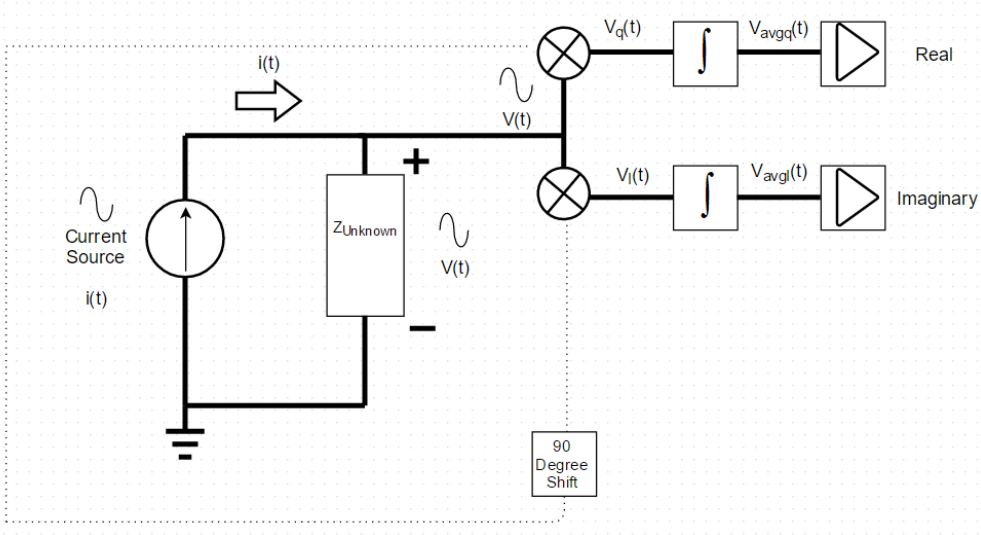

Figure 2.12: Quadrature Demodulation Block Diagram

When used in measuring an unknown impedance, this method makes use of the known current signal $i(t)$ flowing through the unknown impedance Z, and the resulting voltage across the impedance $V(t)$. $V(t)$ is the magnitude of the impedance multiplied by $i(t)$ where its frequency dependent part is shifted by the phase of the impedance.

$$Z = |Z(\omega)| \cdot e^{j\theta_Z \omega} \tag{2.4}$$

$$i(t) = I_{\mathrm{O}} \cdot \sin \omega t \tag{2.5}$$

$$V(t) = |Z(\omega)| \cdot I_{\mathrm{O}} \cdot \sin \omega t + \theta_Z \omega \tag{2.6}$$

Next this $V(t)$ is multiplied by the in-phase, $\sin(t)$, and quadrature signals, $\cos(t)$, in order to make $V_{\mathrm{q}}(t)$ and $V_{\mathrm{I}}(t)$.

$$V_q(t) = V(t) \cdot \sin \omega t = \frac{|Z(\omega)| \cdot I_O}{2} \cdot [\cos \theta_Z \omega - \sin \theta_Z \omega + 2\omega t] \tag{2.7}$$

$$V_I(t) = V(t) \cdot \cos \omega t = \frac{|Z(\omega)| \cdot I_O}{2} \cdot [\sin \theta_Z \omega - \sin \theta_Z \omega + 2\omega t] \tag{2.8}$$

When the new in-phase and quadrature signals are averaged over a time $t = n/f = 2\pi$ n/ω such that t is equal to n periods of the frequency. As a result, the cosine and sine terms varying with time, t will cancel out leaving the following equations: Eq. (2.9) & Eq. (2.10).

$$V_{avgq}(t) = \frac{|Z(\omega)| \cdot I_O}{2} \cdot \cos \theta_Z \omega = \frac{I_O}{2} \cdot Re(Z(\omega)) \tag{2.9}$$

$$V_{avgI}(t) = \frac{|Z(\omega)| \cdot I_O}{2} \cdot \sin\theta_Z\omega = \frac{I_O}{2} \cdot Im(Z(\omega)) \tag{2.10}$$

The last step to calculate the real and imaginary part of an unknown impedance would be to multiply these two signals by a factor of $a = 2/\mathrm{I}_0$ in order to get rid of the scaling left in them.

$$\frac{I_O}{2} \cdot Im(Z(\omega)) \cdot a = Im(Z(\omega)) \tag{2.11}$$

$$\frac{I_O}{2} \cdot Re(Z(\omega)) \cdot a = Re(Z(\omega)) \tag{2.12}$$

The drawback of this method is that, if the signals are not averaged over an integral number of periods, then an error will occur in both real and imaginary parts.

2.4.2 DFT and FFT Implementation

Another method of obtaining the real and imaginary parts of an unknown impedance is the Discrete Fourier Transforms. DFT is the discrete version of the Fourier Transform which states that any function can be represented by a series of sinusoids. [25] Since this transform does not deal with continuous time, the Nyquist rate applies: in order to correctly analyze a signal with a frequency of f Hz, the signal must be sampled at minimum frequency of $2f$ Hz.

The definition of a DFT is shown below, where x(n), the unknown impedance in terms of the voltage across the impedance and the current into the impedance, is a real discrete periodic signal with a period length of N and X(k) is a complex discrete periodic signal with period length N. [25]

$$X(k) = \frac{1}{N} \sum_{n=0}^{N-1} x(n) \cdot e^{\frac{-i(2\pi)nk}{N}} \tag{2.13}$$

Using Eulers Identity, this definition can be re-written as following.

$$Re\{X(k)\} = \frac{2}{N} \sum_{n=0}^{N-1} x(n) \cdot \cos\frac{(2\pi)nk}{N} \tag{2.14}$$

$$Im\{X(k)\} = -\frac{2}{N} \sum_{n=0}^{N-1} x(n) \cdot \sin\frac{(2\pi)nk}{N} \tag{2.15}$$

$$X(k) = Re\{X(k)\} + j \cdot Im\{X(k)\} \tag{2.16}$$

A possible problem of using the DFT method is that the number of calculations to compute the DFT grows exponentially as N increases. A way to alleviate the number of computations is to use Fast Fourier Transform (FFT). [25] A FFT reduces the number of calculations required. For example, using a 4,096 point DFT requires 16,777,216 calculations to work while a FFT computation uses only 24,575 calculations.

3 System Specifications and Requirements

This chapter includes design requirements derived from the research, the preliminary block diagram of our system, and the selection of the needed components.

Based on the research about skin impedance applications, we were able to list the design requirements for our design. As mentioned in the introduction, our goal is to design a skin impedance meter that is versatile and low power.

1. Frequency sweeping
2. Able to measure impedance of a sufficiently wide range
3. Data collection & Storage
4. Wireless communication: Bluetooth
5. Low power
6. Rechargeable
7. Safe
8. Real-time

The table below, Table 3.1, shows the technical specifications that we are aiming to achieve in our design. These specifications are based on the specifications of AD5933 and the requirements of skin impedance applications. We are setting the most of our specifications similar to those of AD5933, as found in its data sheet. However, our maximum frequency will be 100 kHz in order to graph part of the dispersion region. Also, as shown in Figure 3.1, the impedance and frequency range of our design is comprehensive; these ranges will allow our design to be a versatile device.

Parameter	**Value**	
	Min.	Max.
Frequency	5kHz	100kHZ
Peak Injecting Current	< 1 mA	
Impedance	200Ω	2kΩ
% Error of Impedance	$< 1\%$	
Phase Error	$< 1^\circ$	
FFT	1024 points	

Table 3.1: Technical Specifications

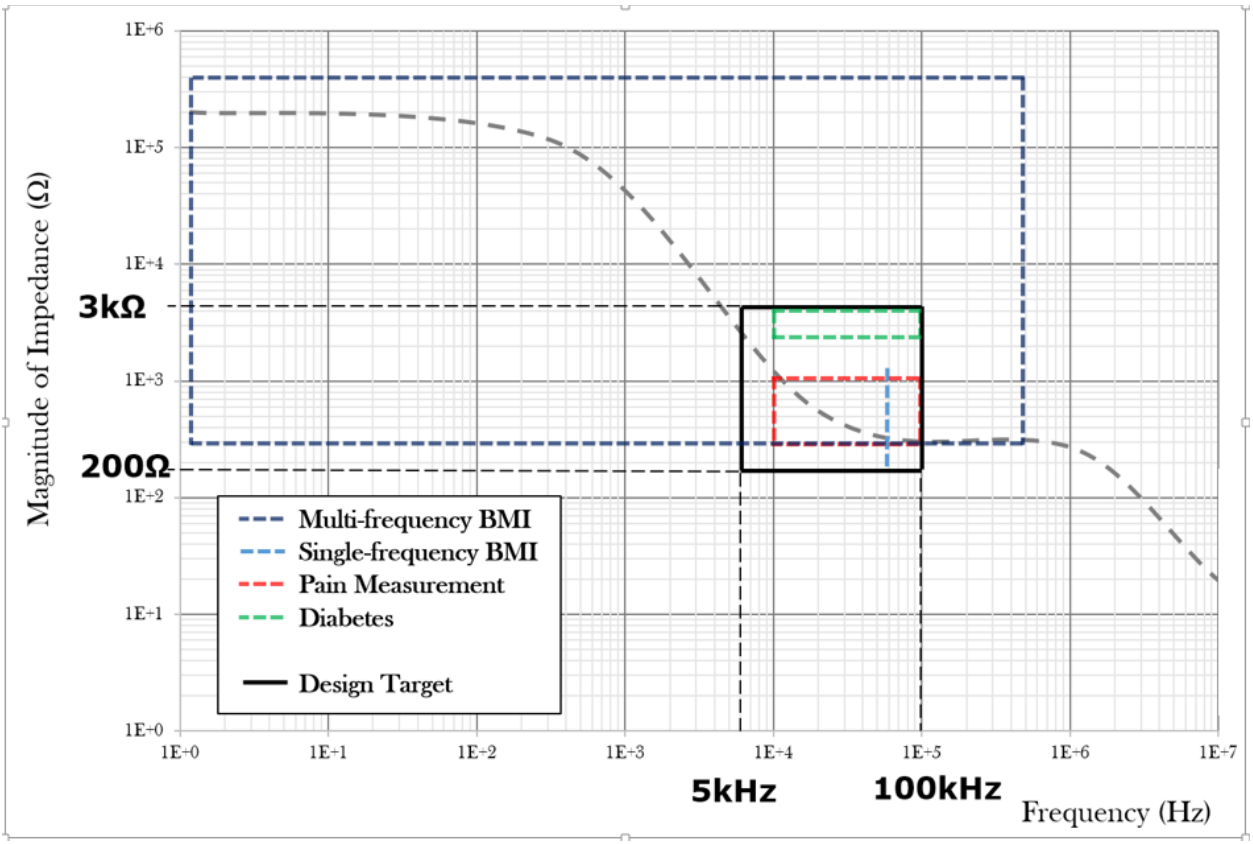

Figure 3.1: Range of Frequency and Impedance for Different Applications

4 Design Options

In this chapter, we will discuss about design options for important parts of our system, as shown in Figure 4.1. We will examine and compare advantages and disadvantages of each option to find out which is the best for our project regarding time resource and intellectual capabilities we have. We first analyze different options for stimulus generation. Then, discussions about power management, V-I converter, microcontroller, wireless communication module, and mobile application will follow.

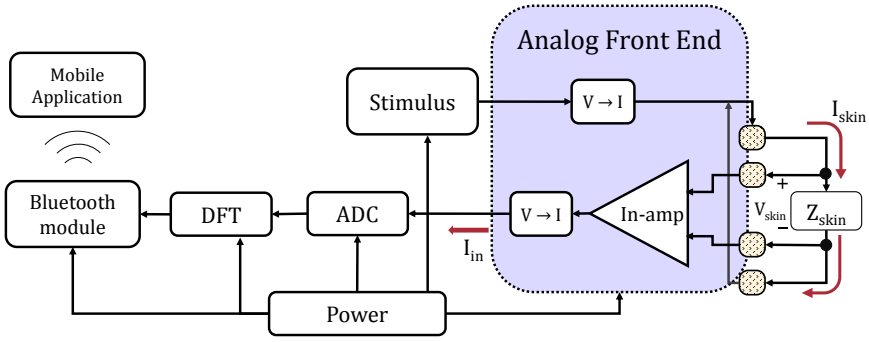

Figure 4.1: Top Level Block Diagram

4.1 Stimulus Generation

4.1.1 Micro-Controller

The project was initially designed in a way that the Atmega328p micro-controller would generate sine waves of a known frequency. However, coding the micro-controller to generate frequency waves within the range of 5kHz - 100kHz was time consuming. As the primary goal of the team was to design a reliable generator within the specified time of the project, the idea of using a micro-controller for frequency generation was abandoned. The team decided to use Analog Devices' chip - AD5933 as a frequency generator.

4.1.2 AD5933 Impedance Analyzer

Even with AD5933, a micro-controller has to be used in the circuit, however the AD5933 chip brings some advantages to the design. The chip has built-in capabilities for Direct Digital Synthesis and Discrete Fourier Transforms, which means known values of frequency generation and a reliable return of real and imaginary impedance values. AD5933 has an accuracy of 0.5%, and this accuracy of its digital synthesis makes it a very good addition to the design.

4.2 Power Management

For this project, the team considered two main power source options: Batteries and Outlet connection. Because one of the project specifications is low power consumption, the team decided to use batteries as the main power source option. Two battery options were considered: 3V coin cell battery and 9V battery. The 3V coin cell battery would require a voltage booster, but after preliminiary testing, the team estabilished that the switching regulator would not be suitable. This is because of the voltage ripple produced on the voltage supply. Since the signal generation and signal biasing are highly sensitive, the team decided not use the coin cell battery. The next option was to use the 9V battery. A voltage regulator was used when necessary to regulate the voltage to the required 5 volts. Section 5.2 further details the power management for this project.

4.3 Analog Front End (AFE)

4.3.1 V-I Converter

The AD5933 chip is designed to inject a voltage waveform into the body. For the safety of the subject under test, it is better to control the current injected into the body. Because of this, the AFE includes a voltage to current converted that converts the voltage V_{ADI} into current(I_{BODY}). The team studied many voltage to current configurations which are presented below:

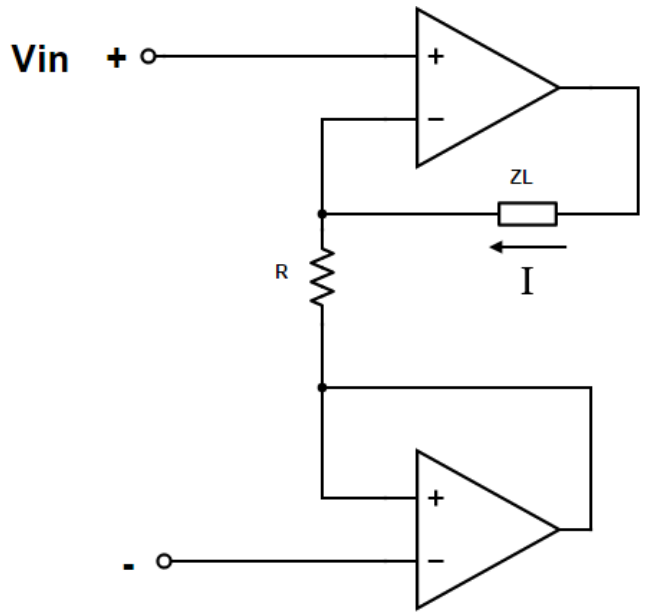

Figure 4.2: Voltage to current converter configuration 1

Figure 4.1 (a) shows the fist voltage to current converter studied by the team. In this circuit configuration the load under test is represented by Z_L. The current to voltage relationship can be calculated using equation 2.17.

$$I = \frac{V_I}{R} \tag{4.17}$$

This configuration does not need precise resistor matching, but it does use two operational amplifiers.

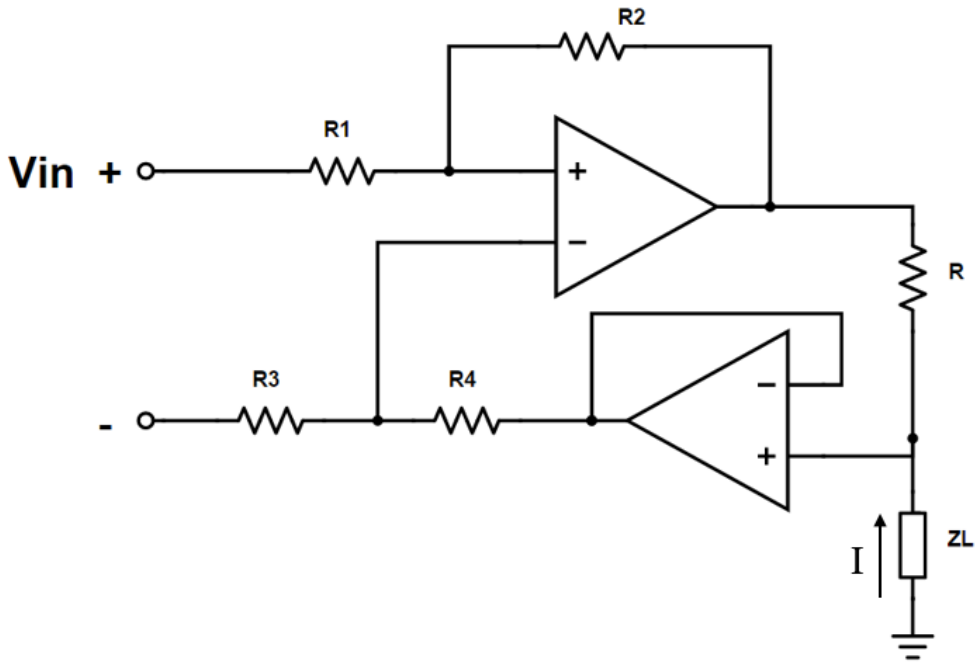

Figure 4.3: Voltage to current converter configuration 2

Figure 4.2 shows the second voltage to current converter studied by the team. In this circuit configuration the load under test is represented by Z_L. The voltage to current relationsh can be calculated using equation 4.18.

$$I = -\frac{V_I}{R} \tag{4.18}$$

This configuration requires two Operational amplifiers and also requires precise matching of the ratio of the resistors as equation 4.19 shows

$$\frac{R_1}{R_2} = \frac{R_3}{R_4} \tag{4.19}$$

If the ratio of the resistors is not matched, the voltage to current relation equation chages to equation 4.20.

$$I = -\frac{V_I}{R} - \frac{\frac{percentange}{100} * I * Z_L}{R} \tag{4.20}$$

or equivalently

$$I = -\frac{V_I}{R} - \frac{\frac{percentange}{100} * (V_I - R_1 - R_2 - R)}{R} \tag{4.21}$$

It is important to note that a consequence of the resistor ratios not being matched, is that the current now depends on other circuit components such as the load or resistors other than R.

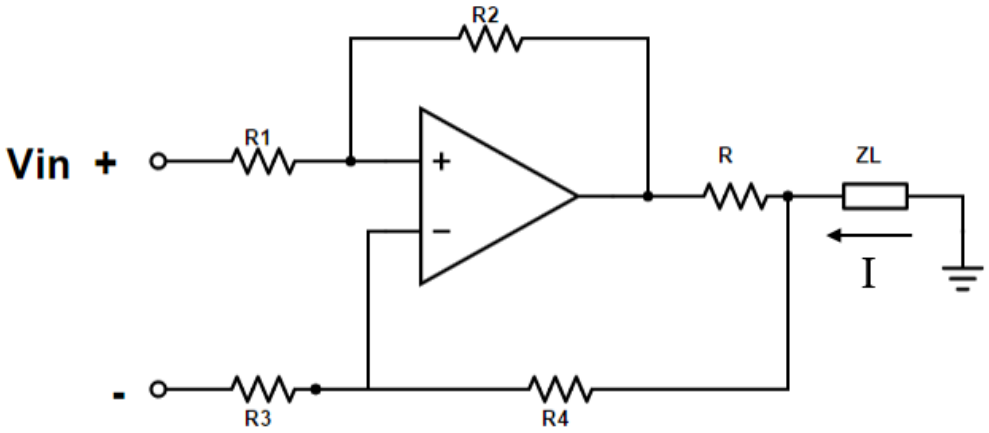

Figure 4.4: Voltage to current converter configuration 3

The third voltage to current configuration studied by the team is very similar to the second configuration. The main difference is that this configuration lacks of a second operational amplifier to act as a buffer when setting the voltage reference in the negative input terminal of the op amp. This causes some of the current I to go through the resistor divider network of R3 and R4.

$$I = -\frac{V_I}{R} - \frac{V_{ZL}}{R_3 + R_4} \tag{4.22}$$

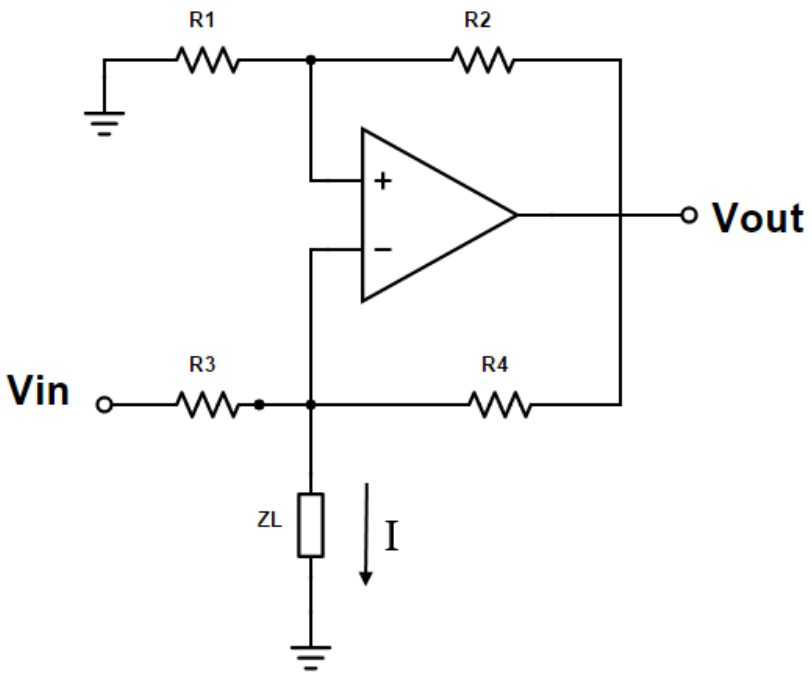

Figure 4.5: Voltage to current converter configuration 4

The fourth voltage to current circuit configuration studied by the team requires one operational amplifier and precise match of resistor ratios as well. If the resistor ratios are exactly matches matched the voltage to current relation is given by equation 4.23.

$$I = \frac{V_I}{R} * \frac{R_3}{R_3 + R_4} \tag{4.23}$$

The ratio of resistors R1, R2 and R3,R4 should be matched such that:

$$\frac{R_1}{R_2} = \frac{R_3}{R_4} \tag{4.24}$$

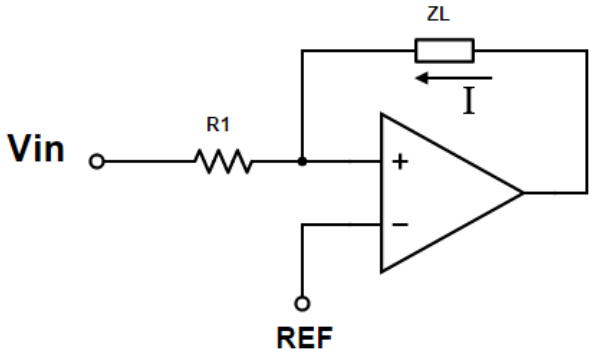

Figure 4.6: Voltage to current converter configuration 5

The circuit configuration con Figure 4.6 is simply an operation amplifier in an inverting configuration. The voltage to current configuration is given by equation 4.24.

$$I = -\frac{V_{in}}{Z_L} \tag{4.25}$$

The configuration on Figure 4.6 was chosen because of multiple reasons. First, compared to the options that require two operational amplifiers, this configuration uses less power because it only uses one. Unlike some of the other options, this one does not require precise matching of some of the resistors. Also, the simple design means less parts, lower cost and less area in the PCB. Section 5.31 further details the chosen voltage to current converter configuration.

4.4 Micro-controller Options

Even though the team decided to choose AD5933 in the design, there is still a need for a micro-controller in order to control the AD5933 via I2C. The other reason for having a micro-controller is to send the results of the AD5933 off to a Bluetooth module through universal asynchronous receiver/transmitter (UART). Considering the feasibility factor and the scope of the project into account, the team only considered familiar group of micro-controllers, namely Texas Instruments MSP430F248 and Atmels Atmega328p.

The function of the micro-controller in this project is limited to the following tasks; program the AD5933, receive the real and imaginary parts of skin impedance, transmit the real and imaginary parts to the Bluetooth, and have the clock frequency and memory to achieve this for the project. From the datasheets of the MSP430F248 and the Atmega328p, both meet the requirements needed to implement our design. However, the only real difference is that the Atmega328p uses the Arduino language while the MSP430F248 uses C.

The group decided to use the Atmega328p chip. The reason behind this decision was that the Atmega328p uses Arduino, which is a simpler language to implement the functionality required for this project. This is due to the Arduino being made with serial communication in mind.

Section 5.4 further details the function of the Atmega328p in the project and 5.8 shows a flow diagram of this function.

4.5 Wireless Communication

Our device needs wireless connectivity to be able to transfer data to the computer to display relevant information to the user. There are many technologies that enable wireless connectivity on a portable device.

Under IEEE 802.15 standardization, Wireless Personal Area Networks (WPAN) technologies are developed for short range intercommunication between devices.[26] The two most popular WPAN technologies are Bluetooth and ZigBee. This section will cover the basics of Bluetooth and ZigBee and end with the comparison between the two.

4.5.1 Bluetooth

Bluetooth is a wireless technology with the purpose of short range communication between devices. The information is transferred over 2.4-2.485 GHz unlicensed-band frequency range using IEEE 802.15.1 standards. Bluetooth has a transmission range of up to 10 meters. [26]

A typical interconnection of Bluetooth devices is known as a piconet. A piconet consists of up to 8 devices connected via Bluetooth. At any single point of time in a piconet, only one master device chooses a slave device and communicates using its address. Once a slave device is chosen, data transmission can begin. [27] The power usage of Bluetooth depends on the time transferring data which causes the device to be in active mode. Table 4.1 shows the characteristics of HC-06 Bluetooth module.

Criteria	Data Specifications
Frequency range	2.4 —2.485 GHz
Transmitting Current	20 —35 mA
Voltage Supply Range	3.3 —6.4 V
Active Current	25 mA
Standby Current	N/A
Data Rate	1000 kbps
Flash Memory	N/A
RAM Memory	N/A

Table 4.1: Characteristics of HC-06 JY-MCU Bluetooth Smart Device[28]

4.5.2 ZigBee

ZigBee is an alternative to Bluetooth for short range communication between multiple devices. It can connect up to 65,000 devices together. ZigBee is commonly used in sensor networking. Like Bluetooth, it operates at 2.4 GHz frequency and its transmission range between two devices is around 10 to 20 meters with a WPAN setting. The standard used for ZigBee is IEEE 802.15.4. [26]

ZigBee transmits in short data bursts and consumes more power while transmitting data as shown in Table 4.2 This characteristic is not suitable for applications that require continuous communication between the devices. However, ZigBee is more commonly used for sporadic data transmission. A few of most common types are temperature, pressure value or other metrics.

Criteria	Data Specifications
Frequency range	2.4 GHz
Transmitting Current	35 mA
Voltage Supply Range	2.1 —3.6 V
Active Current	38mA
Standby Current	$<10\mu$A
Data Rate	250 kbps
Flash Memory	32 KB
RAM Memory	2 KB

Table 4.2: Characteristics of ZigBee Module[29]

4.5.3 Comparison

While Bluetooth and ZigBee are both used in similar applications in Wireless Personal Area Networking,[26] there are clear differences between the technologies. Bluetooth modules have higher data rate and some modules have larger memory sizes than those of ZigBee modules. Also, Bluetooth requires higher current for different modes. However, ZigBee has a longer coverage range than Bluetooth. The characteristics of HC-06 Bluetooth and a ZigBee module are presented side by side in Table 4.3.

Criteria	Bluetooth	ZigBee
Frequency range	2.4 —2.485 GHz	2.4GHz
Transmitting Current	20 —35 mA	35 mA
Voltage Supply Range	3.3 —6.4 V	2.1 —3.6V
Active Current	25 mA	38 mA
Standby Current	N/A	$<10\mu$A
Data Rate	1000 kbps	250kbps
Flash Memory	N/A	32 KB
RAM Memory	N/A	2 KB

Table 4.3: Characteristics of Bluetooth and ZigBee Module[28][29]

The key difference for a low power device is power consumption. There are two factors involved in comparing power consumption of the two technologies. The first factor is the current requirements for Standby and Active mode. [25] The second is the amount of time to switch between Active and Standby modes. The relationship between these factors and power consumption is visually shown in Figure 4.7.

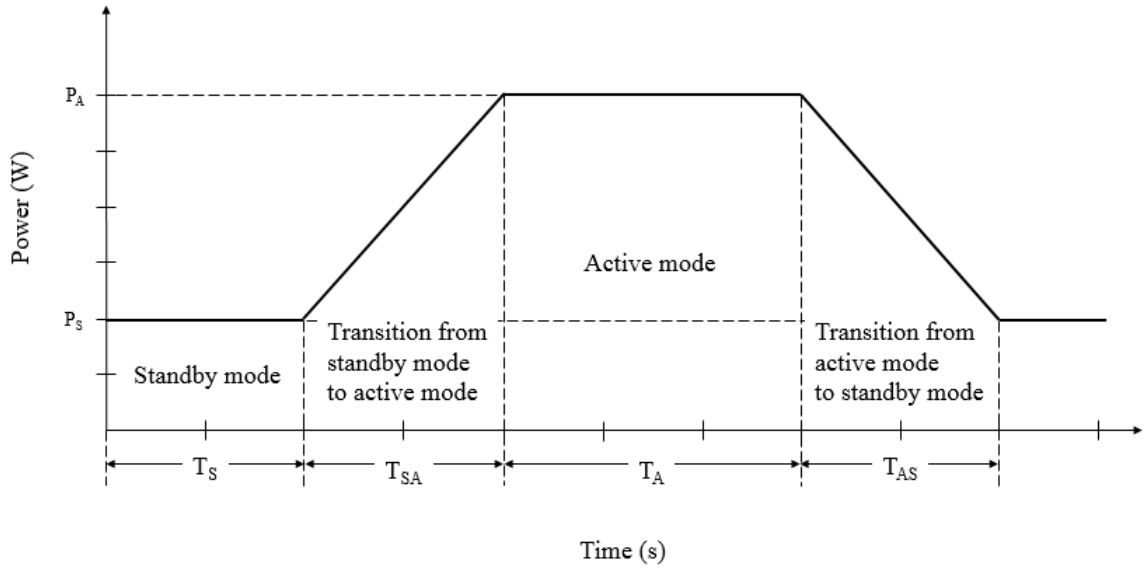

Figure 4.7: Power Consumption vs. Time

The total energy consumption for a data transmission is equal to the sum of consumption during Standby mode, Active mode, and transitions between the modes. In other words, the total energy consumption for a transmission depends on not only the current requirements for different modes but also the frequency and duration of data transmissions. For example, if devices communicate continuously, or transmission time is infinite, then the power consumption only depends on the Active mode power consumption. On the other hand, if devices communicate at a certain interval, then power consumption during mode transitions contributes more in total consumption.

$$TotalEnergy(J) = \sum P_i \cdot T_i \tag{4.26}$$

$$E_{Total} = P_S T_S + \{P_S T_{SA} + \frac{1}{2}(P_A - P_S)T_{SA}\} + P_A T_A + \{P_S T_{AS} + \frac{1}{2}(P_A - P_S)T_{AS}\} \tag{4.27}$$

If $T_{SA} = T_{AS}$

$$E_{Total} = P_S T_S + T_{SA}(P_S + P_A) + P_A T_A \tag{4.28}$$

The equations Eq. 4.26, Eq. 4.27, and Eq. 4.28 can be used to calculate the energy consumption for a transmission. For example, if the P_A is equal to 30W, P_S is 5W, T_S is 2s, T_{SA} and T_{AS} are 15s, and T_A is 3s, then, using Eq.4.28, the total energy consumed is 625J. In this scenario, the switching between Active and Standby mode consumes the most energy. It is important to consider the transmission characteristics of specific application when comparing power consumption of these options.

Research by Microsoft [30] states that Bluetooth used less power than ZigBee when transmitting for the same amount of time because Bluetooth switches faster between two modes.

As shown in Eq. (4.28) Bluetooth can send more data and use less power than ZigBee. Thus, Bluetooth is the more efficient choice when low power consumption is required, while ZigBee is the more suitable when a long distance communication is required. Thus the team will go with the HC-06 JY-MCU Bluetooth module in this project.

4.6 Matlab Code

Another part of the project is to develop a Matlab code. The goal of this code is to calculate the impedance and phase of the skin from the real and imaginary parts calculated by the AD5933 and to graph it on the screen of a cell phone.

This would allow an offload of these computations from the micro-controller in the circuit to a cell phone, making use of its higher computational power.Additionally, it will also save power in the micro-controller which is the biggest reason for doing this. Moreover, this also eliminates any memory limitations associated with the micro-controller.

5 Final Design

After exploring different design options, we have made decisions on each part and performed simulations for each part in order to verify that each design decision would work as desired. In this chapter, we will cover all of the final design decisions and simulation results for all of specifics parts. Finally, we will also briefly talk about the PCB board layout.

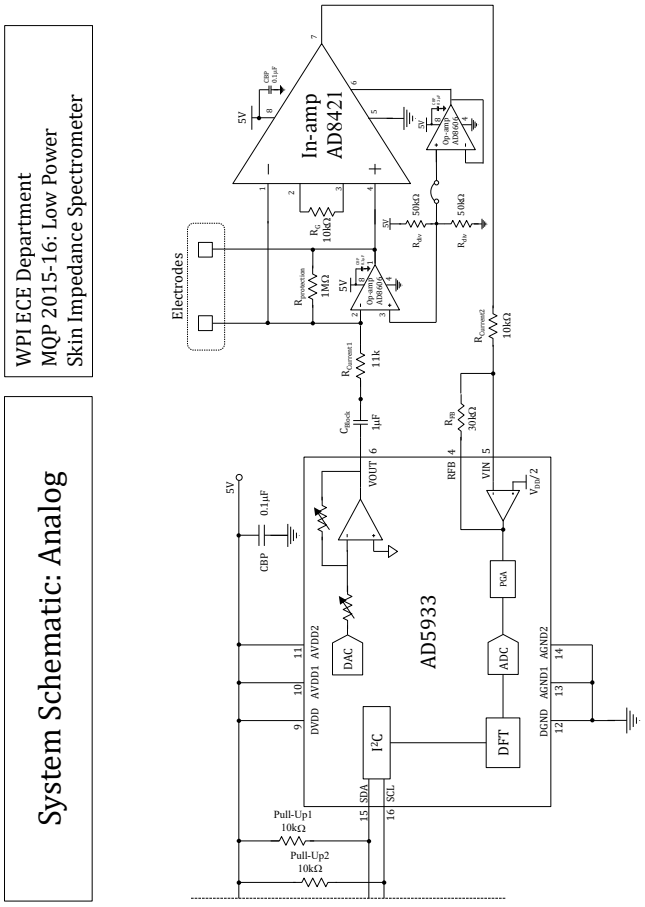

Figure 5.1: Analog Schematic

5.1 Stimulus Generation

This project uses AD5933 which is a high impedance converter system. The chip combines an onboard frequency generator with a 12 bit analog to digital converter. With the help of AD5933, an external complex impedance can be excited with a known frequency. The DFT algorithm, processed by an onboard DSP engine, returns a real and imaginary data point at each output frequency. Between a voltage input of 2.7V - 5.5V, the chip can accurately measure within 0.5 % of the correct impedance value.

5.2 Power Management

A positive voltage regulator MC78L05AB from ON Semiconductor is used to regulate power to the system. The connection between the regulator and the battery is shown in Figure 5.2. As shown in the figure, the input of the regulator is directly connected to the positive end of the battery with a bypassing capacitor. The output of the regulator is fixed and constant at 5V.

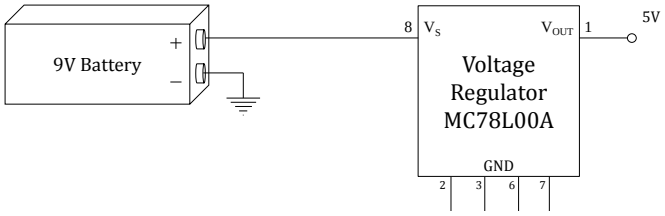

Figure 5.2: Regulator Connection for 5V Supply

The estimated power consumption of few selected parts are shown in Table 5.1. These parts were particularly considered in context of power, since the estimated consumption of these parts were most significant. Once the capacity of battery is found out, battery life of the system can be estimated just taking ratio of capacity to the total power consumption.

Part	**Current (mA)**		**Supply Voltage (V)**	**Power Consumption (mW)**	
	Min.	Max.		Min.	Max.
AD5933	11	16	5	55	80
ATMEGA328P	0.39	6.6		1.95	33
HC-06	20	35		100	175
			Total Power	156.95	288

Table 5.1: Estimated Power Consumption of Main Units

5.3 Analog Front End

5.3.1 V-I Converter

Figure 5.3 shows the chosen voltage to current converter configuration. This circuit converts the output signal of the AD5933 chip (V_{ADI}) to current waveform (I_{BODY}) that is injected into the body. The $R_{current}$ is the voltage to current factor following Ohms Law. Equation (5.3.1) shows the mathematical relation between (V_{ADI}) and (I_{BODY}) The resistor (R_{BODY}) and the capacitor (C_{BODY}) are models for the typical skin impedance.

$$I_{BODY} = \frac{V_{ADI}}{R_{CURRENT}} \tag{5.29}$$

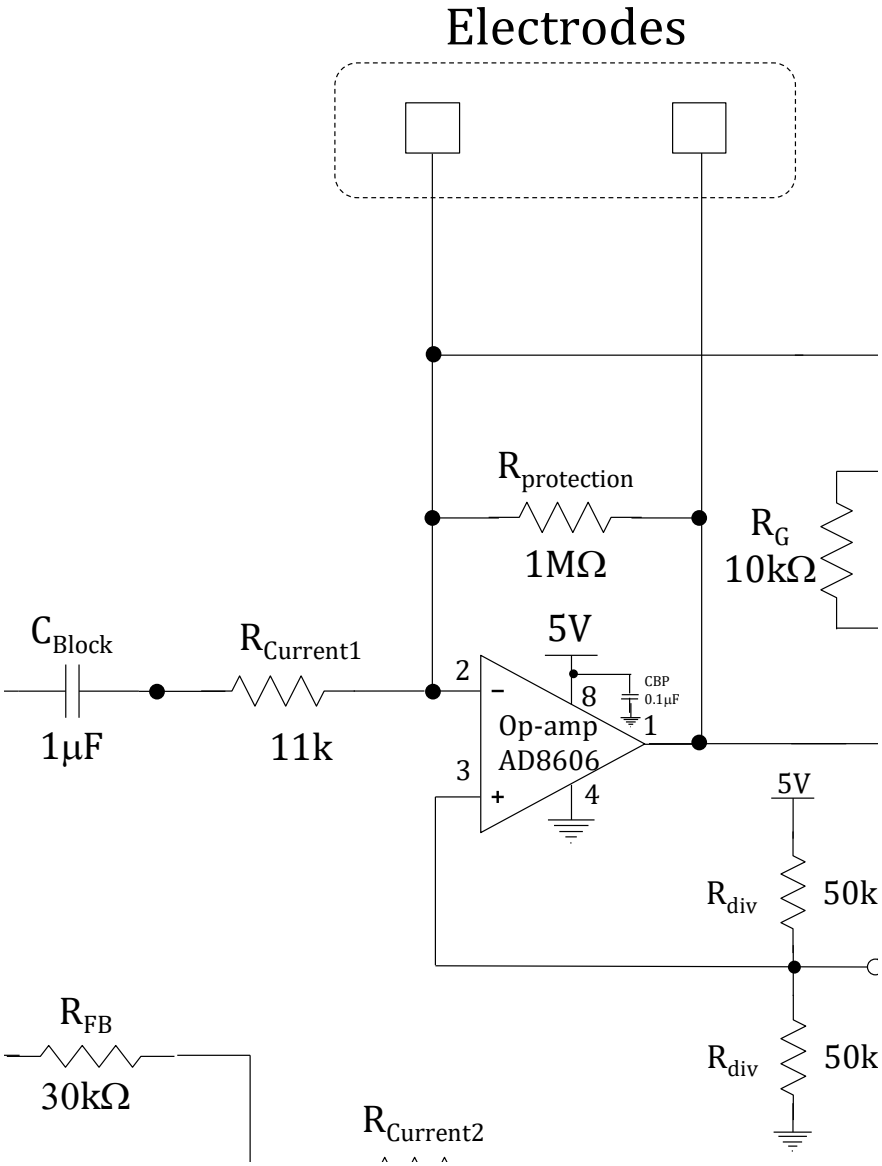

Figure 5.3: Voltage to Current Converter

The transfer function of this circuit block can be observed in Equation (5.30).

$$V_{OUT} = V_{IN} \times \left(\frac{R_{BODY} \,||\, \frac{1}{sC_{BODY}} \,||\, R_{PROTEC}}{R_{CURRENT}}\right) + V_{REF} \times \left(\frac{R_{BODY} \,||\, \frac{1}{sC_{BODY}} \,||\, R_{PROTEC}}{R_{CURRENT}} + 1\right) \tag{5.30}$$

V_{ADI} is generated with a 2.24V offset. However, for safety reasons, it is not desired to have DC voltage across the body when measuring skin impedance. To eliminate this DC bias, the circuit includes a blocking capacitor connected to the negative input terminal of the AD8606 operational amplifier.

The RC model for skin impedance consists of a resistor R_{BODY} in parallel with a capacitor C_{BODY}. Based on our background research, the values of R_{BODY} and C_{BODY} are set to 2KΩ and 10nF respectively. Once you include the skin impedance RC model in the voltage to current converter. This circuit configuration turns into an active band pass filter. This circuit configuration can be observed on figure 5.4.

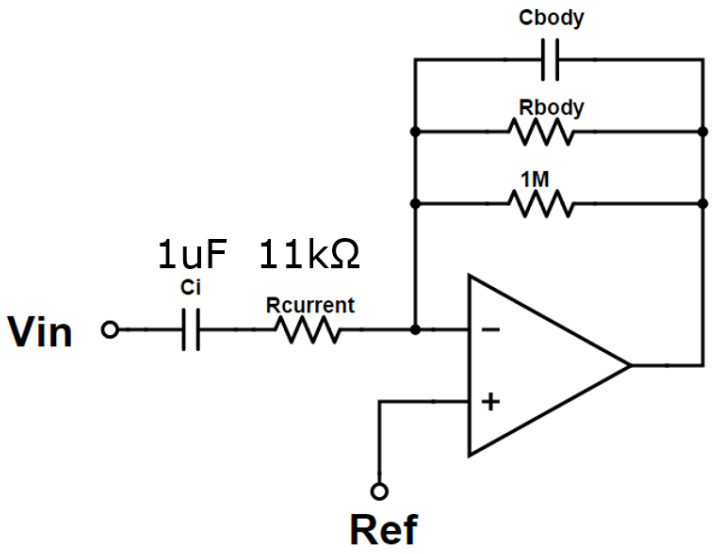

Figure 5.4: Active Bandpass Configuration

This band-pass filter configuration has two poles at frequencies determined by equations 5.31 and 5.32.

$$f_{3db} = \frac{1}{2\pi R_{current} C_i} = \frac{1}{(2\pi)(11k)(1uF)} = 14.4Hz \tag{5.31}$$

$$f_{3db} = \frac{1}{2\pi R_{body} C_{body}} = \frac{1}{(2\pi)(1.985k)(10nF)} = 8035Hz \tag{5.32}$$

Figure 5.5 shows the AC response of this active bandpass filter. The cursors show the two cut off frequencies of the system. It can be observed that the gain of this circuit

changes dramatically through our frequency range of interest (5kHz 100KHz). This is due to the change of impedance of the feedback network of the operational amplifier. At higher frequencies, the feedback impedance is lower which causes greater attenuation of the input signal.

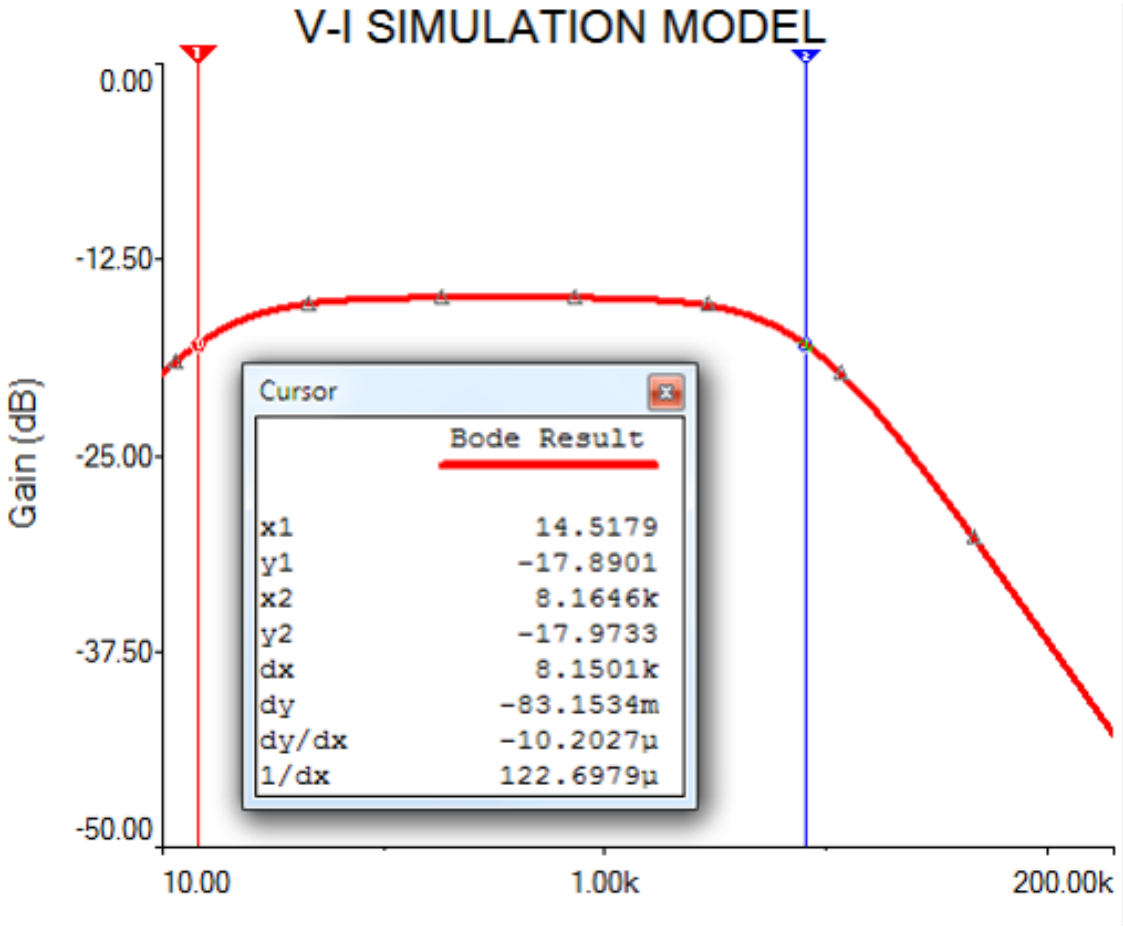

Figure 5.5: V-I Simulation

The cutoff frequency values shown by the cursors on figure 5.4. It can be observed that the both f_{3db} (x1 and x2) frequencies match the values with equations 5.31 and 5.32.

5.3.2 Instrumentation Amplifier

After differential current signals are passed through the body, an adequate amplification is needed to ensure the signal flowing back to AD5933 is sitting at the right DC bias and swinging within the right range. As shown in Figure 5.6, the voltage difference across the both ends of electrodes is fed into an instrumentation amplifier, AD8421 from Analog Devices.

The transfer function of this block can be written as shown in Eq. (5.33). The in-amp output V_{OUT} at pin 7 is equal to the difference of two differential input at pin 1 and 4, scaled by gain factor, G and biased with V_{ref} at pin 6. The gain factor G is determined by the gain

resistor R_G shown across pin 2 and 3. The gain factor equation is also shown below in Eq. (5.34).

$$V_{OUT} = G \cdot (V_{in+} - V_{in-}) + V_{ref} \tag{5.33}$$

$$G = 1 + \frac{9.9k\Omega}{R_G} \tag{5.34}$$

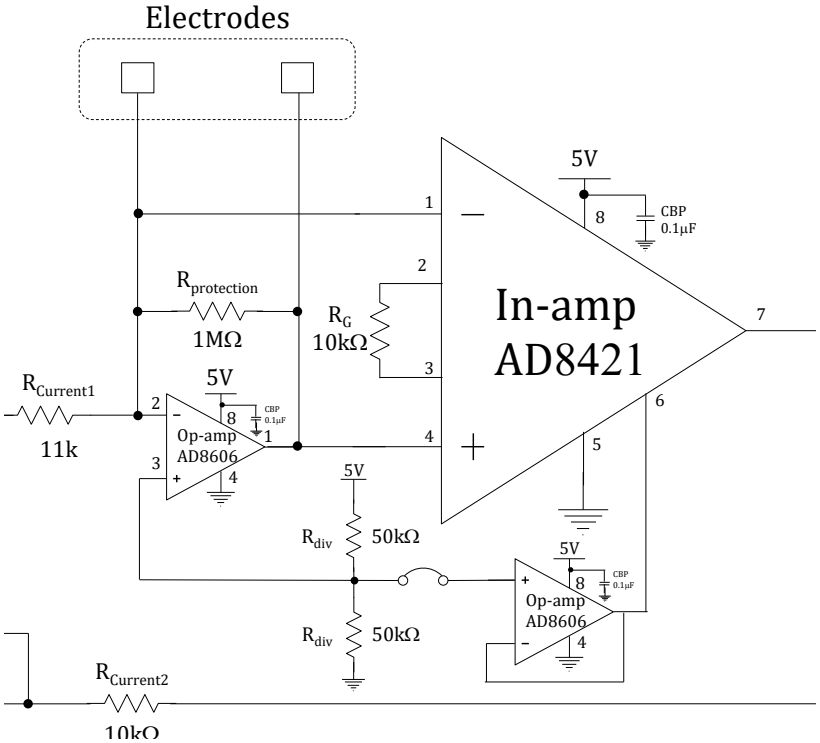

Figure 5.6: Instrumentation Amplifier Configuration

As shown in Figure 5.7, the REF pin is internally connected to the one end of a 10kΩ resistor of an difference amplification stage. This means that R_{ref} any impedance seen from the REF pin will affect the amplification factor since it will add to the 10kΩ resistor. Its impact on gain factor can be described as in Eq. (5.35). Therefore, it is recommended to keep the source impedance to the REF pin very low, or below 1Ω . Therefore, it is necessary to use a voltage follower, as shown at the right bottom of Figure 5.6, to provide 2.5V at REF pin of the in-amp. Another half of AD8606 is configured as a voltage follower to provide low impedance at REF.

$$G = \frac{2(10k\Omega + R_{ref})}{(20k\Omega + R_{ref})} = 2 \tag{5.35}$$

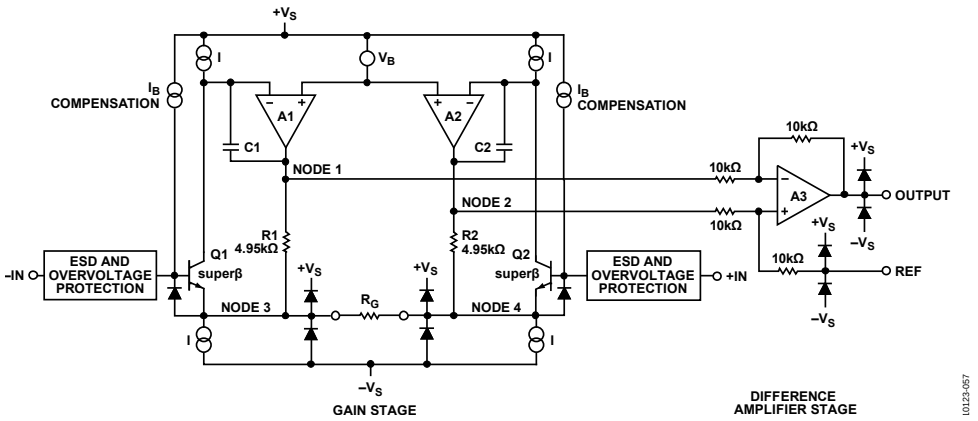

Figure 5.7: Simple Schematic of AD8421 [31]

5.3.3 Voltage To Current Converter

The amplified voltage V_{INA} needs to be converted back into current. This is achieved by the resistor $R_{current2}$. Because V_{INA} is biased at $V_{DD}/2$, the current created by this voltage to current converter is equal to:

$$I_{TIA} = \frac{V_{INA}}{R_{CURRENT2}} \tag{5.36}$$

The $R_{current2}$ was set to 30K to minimize the I_{TIA} thus minimizing the power consumption.

5.3.4 Transimpedance Amplifier

The transimpedance amplifier included in the AD5933 chip converts I_{TIA} into V_{ADC} according to the following equation:

$$R_{FB} = \frac{(V_{PK} + \frac{V_{DD}}{2} - V_{DCOFFSET})}{I_{TIAMAX}} \cdot GAIN \tag{5.37}$$

which simplifies to:

$$R_{FB} = \frac{(1.5V)}{I_{TIAMAX}} \tag{5.38}$$

The team chose a gain of 3 for the voltage to current converter to utilize the ADC's maximum range. To achieve this gain the team set the $R_{current2}$ to 10K and the R_{FB} to 30K. Large resistor values were chosen to minimize the power consumption of the instrumentation amplifier.

5.4 Micro-controller: ATMEGA328P

The Atmega328p microcontroller goes through three main steps: initialization of the AD533 chip configuration of the AD5933 chip, and running impedance sweep. These steps can be visualized in the flow diagram in Figure 5.8.

During the Initialization, the Atmega 328 uses a list of define statements to hard code the addresses of the registers of the AD5933 chip. This is required for the AD5933 to be able to perform an impedance sweep and output the skin impedance data. The register addresses correlate to area where the the following parameters are stored: the PGA gain in the AD5933, the AD5933 output range, the number of cycles in the sweep, the starting frequency, the frequency increment amount, the number of increments, and the real and imaginary parts of skin impedance measurements.

The configuration stage of the code writes to the AD5933 registers to set up the sweep process. First, the output is set to Range 1, which is a 3Vpk-pk sine-wave biased at 2.24V, and the PGA gain is set to 1V/V. Next, it sets the sweep frequency range from 5kHz to 100kHz in increments of 1kHz.

The last stage involves reading the imaginary and real data from the AD5933 and sending that data to the Bluetooth module. Since both the real and imaginary data are stored in two separate bit addresses, Bit wise operation is needed to read the 16 bit real and imaginary values. This is done by reading the highest 8 bits of the real value into a variable (r_e) and right shifting the bit 8 times so the highest 8 bits are in the correct location. The next step involves reading the lowest 8 bits of the real data and bit-wise OR'ing it with the variable holding the highest 8 bits. This finally results in the variable holding the complete real value. The process is then repeated for the imaginary data.

The data containing the real, imaginary, and frequency values is sent through the transmission pin in the ATmega328p to the Bluetooth module. Finally the frequency data is incremented so it matches the data being read in. This is done by incrementing the frequency variable by the frequency step.

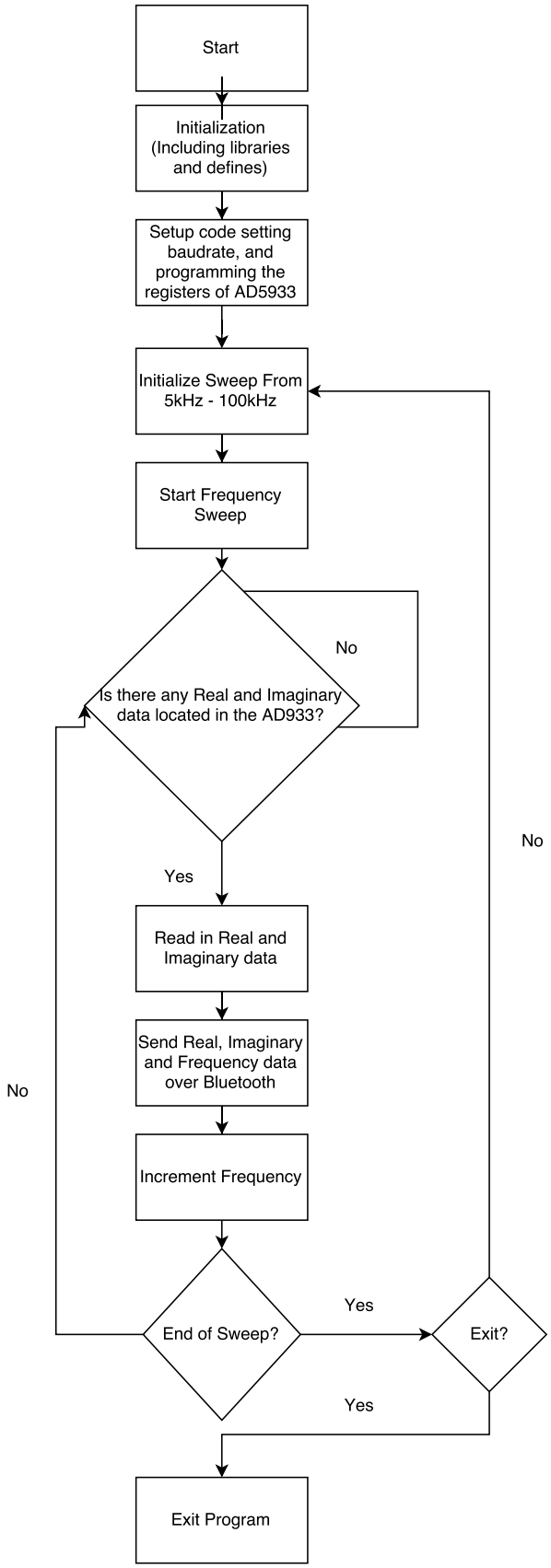

Figure 5.8: ATMEGA328P Flow Diagram

5.5 Wireless Communication: HC-06

Figure 5.9 shows how the Bluetooth device is connected in the circuit. The transmission pin of the Hc-06 is connected to the receiving pin of the Atmega328p, which is connected to the transmission pin of the Atmega328p. Next the VCC and GND pins are connected to 5V and ground respectively. This set up transmits anything it receives in the RX pin over Bluetooth and writes whatever it receives over Bluetooth to the Atmega328p.

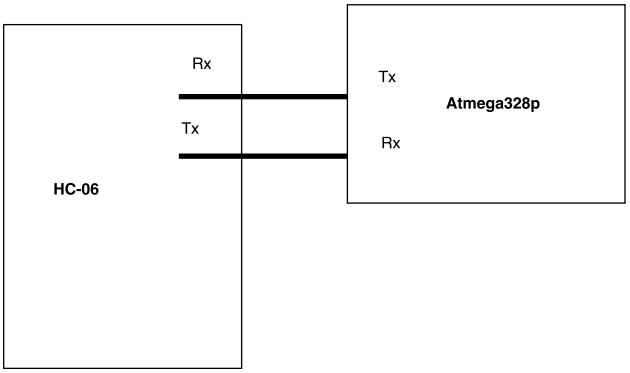

Figure 5.9: Connection between HC-06 and ATMEGA328P

5.6 Matlab Code

The Matlab code in this project calculates the magnitude and phase of the impedance and displays the data graphically. This was made since a computer has more computational power and more memory space than the Atmega328p chosen for this project. The code stores all the gain factors needed to convert the real and imaginary values into magnitude and phase of the impedance. The functionality of the code is shown in the flow diagram in Figure 5.10.

When the code receives a single data transfer containing a real, an imaginary, and a frequency values, it calculates magnitude and phase from the real and imaginary data using the equations below which are modified from the ones used by the AD5933 normally to affect the changes made by the Analog Front end:

Table 5.2: Calculating Unknown Phase

Calculating Unknown Phase			
Real	Imaginary	Quadrant	Unknown Phase Angle [°]
Positive	Positive	First	$\arctan(\frac{R}{I})(\frac{180}{\pi})$
Negative	Positive	Second	$178 + \arctan(\frac{R}{I})(\frac{180}{\pi})$
Negative	Negative	Third	$-2 + \arctan(\frac{R}{I})(\frac{180}{\pi})$
Positive	Negative	Fourth	$-180 + \arctan(\frac{R}{I})(\frac{180}{\pi})$

$$Magnitude = \sqrt{R^2 + I^2} \tag{5.39}$$

After that, it relates them to an actual value using the two equations below:

$$ActualPhase = UnknownPhase - SystemPhase[^\circ] \tag{5.40}$$

$$Impedance = GainFactor \cdot Magnitude[\Omega] \tag{5.41}$$

The code is also able to calculate the correct gain factors and phase values. The code calculates gain and phase, when a known resistor and capacitor is used for calibration. The equations shown in the Table 5.2 can be used to calculate the phase and Eq. 5.42 can be used to calculate the gain factor.

$$GainFactor = \frac{1}{Magnitude \cdot \frac{1}{Impedance}}[\Omega] \tag{5.42}$$

Once all the impedance and phase values from 5kHz to 100kHz are stored, the app then plots both impedance vs. frequency and phase vs. frequency.

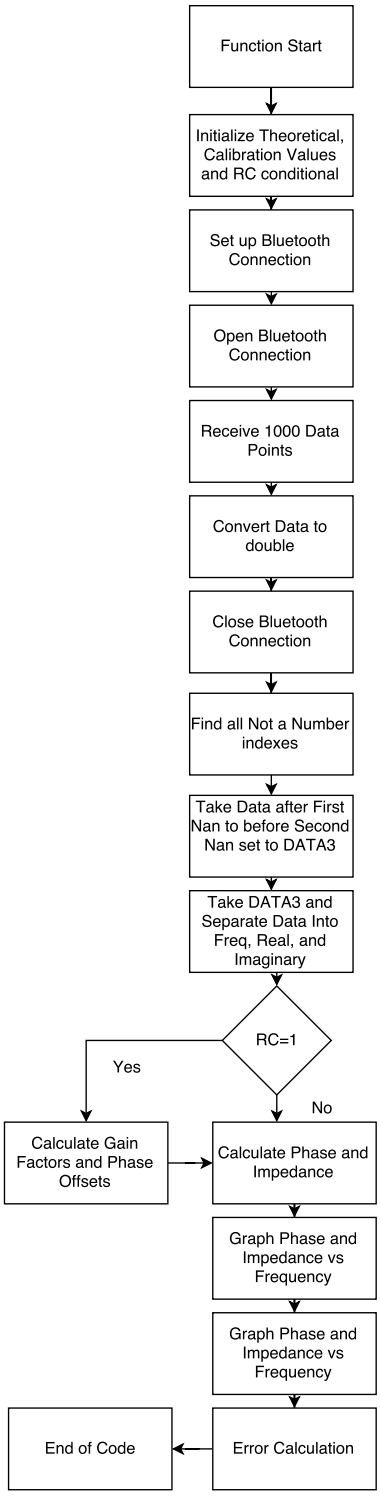

Figure 5.10: Flow Chart of Matlab Code

5.7 PCB Layout

After each part of the project is designed thoroughly, the team decided to build the system on a printed circuit board. Initially, the circuit was built on a breadboard to verify and compare its functionality with the simulations. The results from the breadboard version, along with the results from PCB test version, are described in Chapter 6. In this section, stages of the PCB design will be discussed.

The team chose Multisim and Ultiboard from National Instrument to draw the schematic and design the circuit board. Multisim can transfer a schematic drawn with it to Ulitboard, a PCB design tool. Since most of the team members were familiar with the schematic designs in Multisim, they just needed to learn the designing of the PCB in Ultiboard. Also, both tools were easily accessible since they were already installed on the computers in the AtWater Kent Laboratory.

For this project, a 4-layer board was selected: the top and bottom layers for the signals and two inner layers for the power and ground. Once the schematic was transferred to Ultiboard, all the components were classified according to the type of signals they carry: analog, digital, and power. With AD5933 chip, which pertains to both analog and digital signals, at the center, the team placed the devices and traces so that the traces were as short as possible, but the devices were spaced out enough for easier soldering. When needed, vias were used to connect the top and bottom layer and traces on the bottom layer, in order to avoid unnecessarily long and complicated traces. Whenever a connection to either power or ground plane was necessary, a via was placed to make the connection. Some extra vias on traces and ground vias were added for testing purposes. Figure 5.11 shows the top and bottom layer of the PCB design. In this figure, the green traces are on the top layer and the red ones are on the bottom. Figure 5.12 and 5.13 show the power and ground plane, respectively.

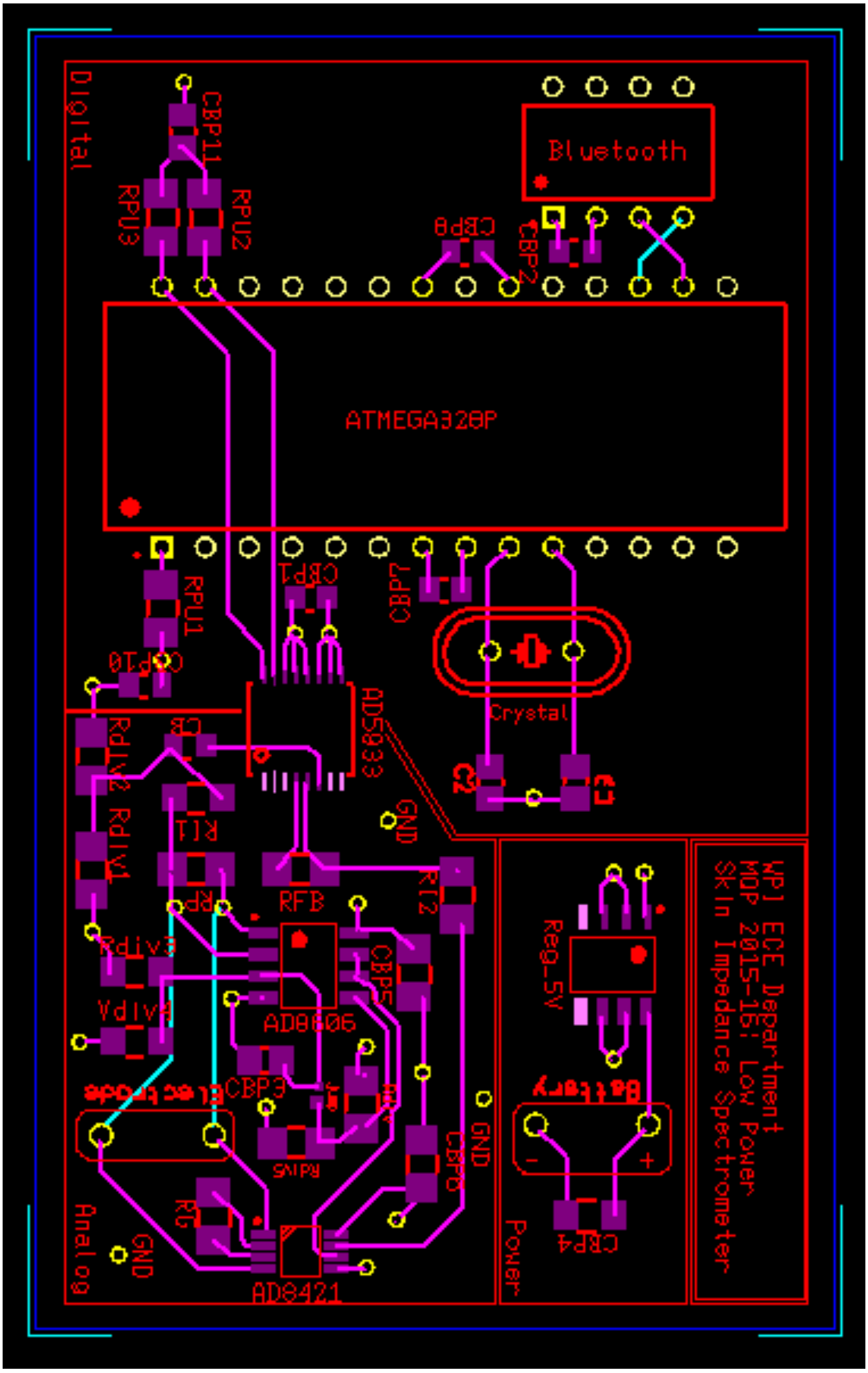

Figure 5.11: Top and Bottom Layer of PCB Design

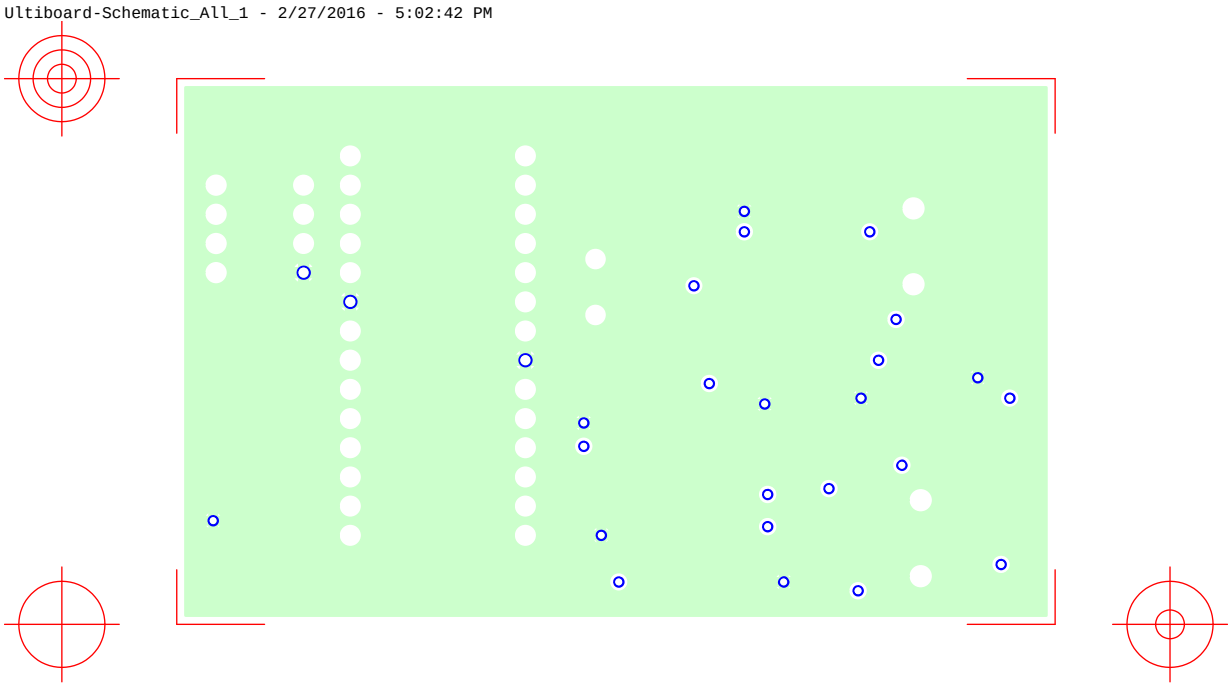

Figure 5.12: Power plane of PCB Design

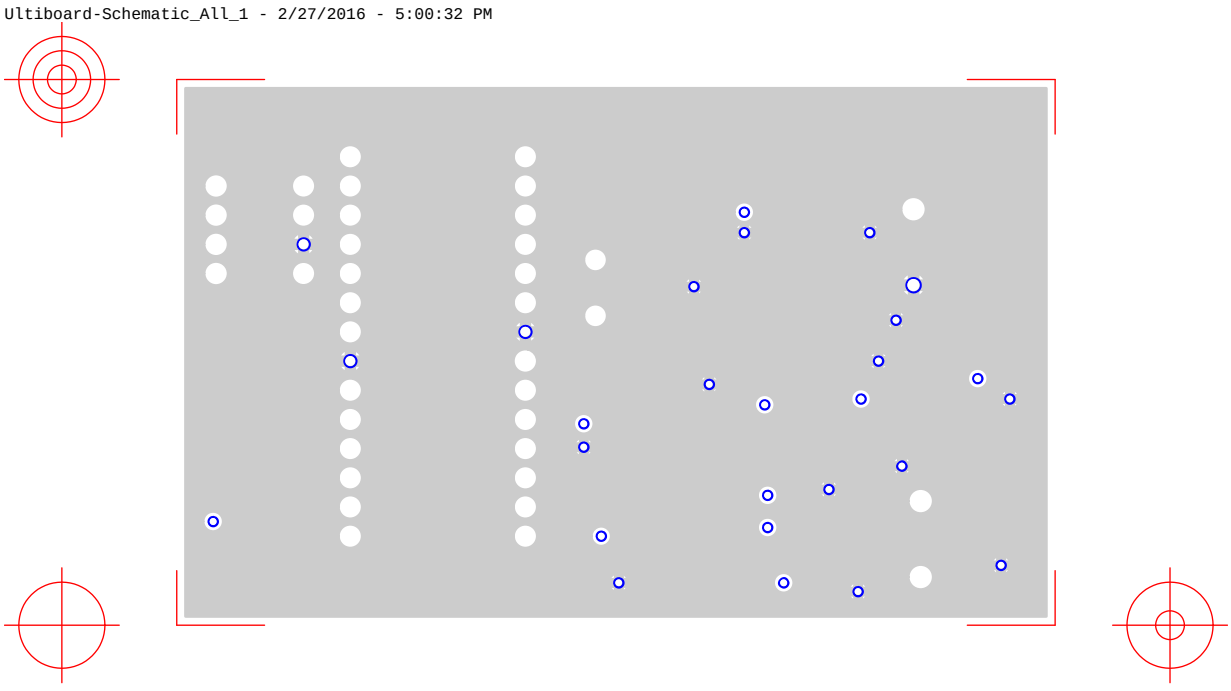

Figure 5.13: Ground plane of PCB Design

6 Test & Results

After the system design process and simulation, the built the circuit on breadboard to verify the design. When all the parts of the system was verified to be functional as expected, the team designed and assembled the printed circuit board. The again performed functionality test on the PCB in order to make sure it worked as intended. In this section, the test results of the prototype and final testing are presented. Then they are compared with simulation and this comparison is analyzed.

6.1 V-I converter

The testing of the voltage to current converter was performed in two stages. First, it was tested on a breadboard using through hole components. After this, the circuit was tested on the PCB. It is important to note that the passive components used on the breadboard were of higher tolerance, which can cause larger variations in results as described in sections 6.1.1 and 6.1.2.

6.1.1 Breadboard Results

For the preliminary experimental results, the team built and tested the circuit on a breadboard. For the V-I converter, R_{BODY} was set to 1.98kΩ and the C_{BODY} was set to 10.61nF. With these values, when frequency is swept in from 10 to 200kHz, its impedance ranges from 74.458Ω to 1,980Ω. The results were included in Table **??** containing the values of input voltage, output voltage, delay, period and phase shift. These tables are shown with frequency values in the frequency range of our project (10 to 200kHz).

Frequency (Hz)	V_{in} (V_{pp})	V_{out} (V_{pp})	Delay (s)	Magnitude (dB)	Phase (°)
10	3.08	0.317	0.032	-19.74982909	-115.2
20	3.04	0.529	0.0184	-15.18835823	-132.48
50	3.04	0.733	0.0086	-12.35539218	-154.8
80	3.04	0.773	0.0057	-11.89388179	-164.16
100	3	0.784	0.0047	-11.65610384	-169.2
200	3.04	0.801	0.0024	-11.58482135	-172.8
500	3.04	0.801	0.001	-11.58482135	-180
1000	3.04	0.789	0.00051	-11.71593161	-183.6
2000	3.1	0.789	0.000272	-11.88569381	-195.84
5000	3.09	0.678	0.000118	-13.17457571	-212.4
10000	3.1	0.494	6.50E-05	-15.9526949	-234
20000	3.09	0.287	3.44E-05	-20.64153165	-247.68
50000	4.99	0.204	1.44E-05	-27.76940756	-259.2
100000	4.97	0.113	7.50E-06	-32.8655589	-270
200000	4.94	0.072	3.90E-06	-36.72788905	-280.8

Table 6.1: Breadboard V to I Results

The team also plotted the AC response of this circuit in two plots: Gain and Bode Plot

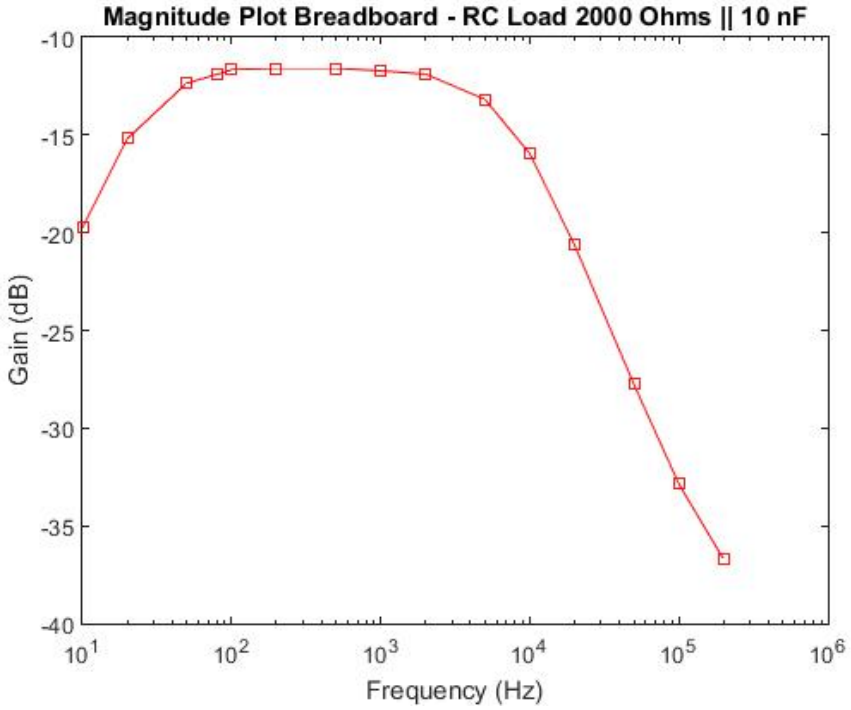

Figure 6.1: Magnitude Plot - Breadboard

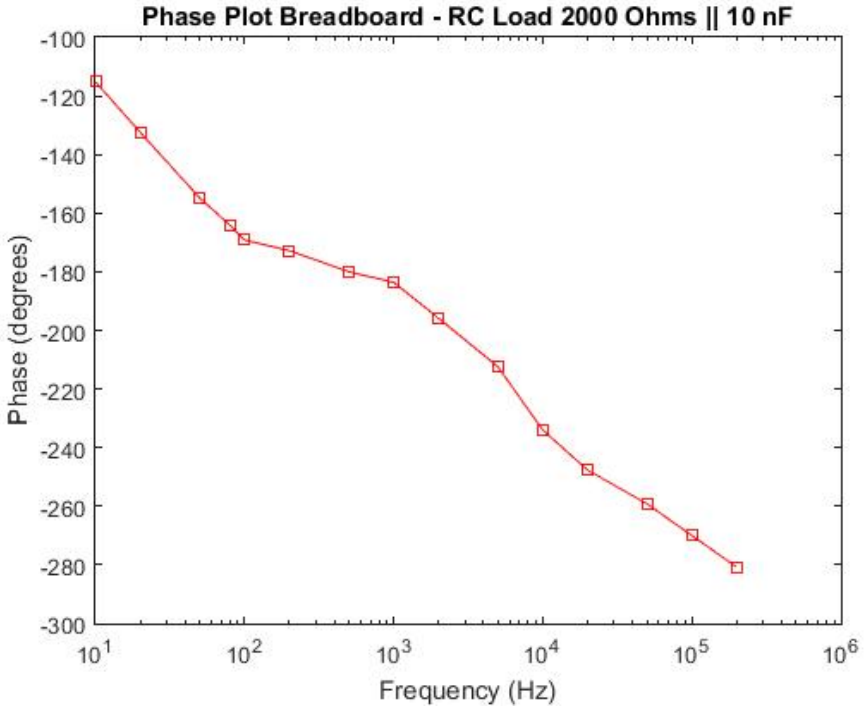

Figure 6.2: Phase Plot - Breadboard

6.1.2 PCB Results

For the final testing, the team tested the PCB circuit. The components were soldered on the printed circuit board and the function generator was used to provide the input.

Frequency (Hz)	V_{in} (V_{pp})	V_{out} (V_{pp})	Delay (s)	Magnitude (dB)	Phase (°)
10	3.12	0.36	0.032	-18.75704187	-115.2
20	3.07	0.564	0.019	-14.71718543	-136.8
50	3.06	0.741	0.0088	-12.31806437	-158.4
80	3.07	0.78	0.00596	-11.90087546	-171.648
100	3.06	0.792	0.00468	-11.7399249	-168.48
200	3.04	0.803	0.00248	-11.56316077	-178.56
500	3.06	0.811	0.00101	-11.53401145	-181.8
1000	3.06	0.807	0.00052	-11.57695784	-187.2
2000	3.12	0.803	0.000272	-11.78878097	-195.84
5000	3.12	0.695	0.000118	-13.04339579	-212.4
10000	3.12	0.51	6.48E-05	-15.73168836	-233.28
20000	3.12	0.296	3.48E-05	-20.45725766	-250.56
50000	4.16	0.171	1.46E-05	-27.7219444	-262.8
100000	4.97	0.109	7.48E-06	-33.17859782	-269.28
200000	4.94	0.056	3.74E-06	-38.91077844	-269.28

Table 6.2: PCB V to I Results

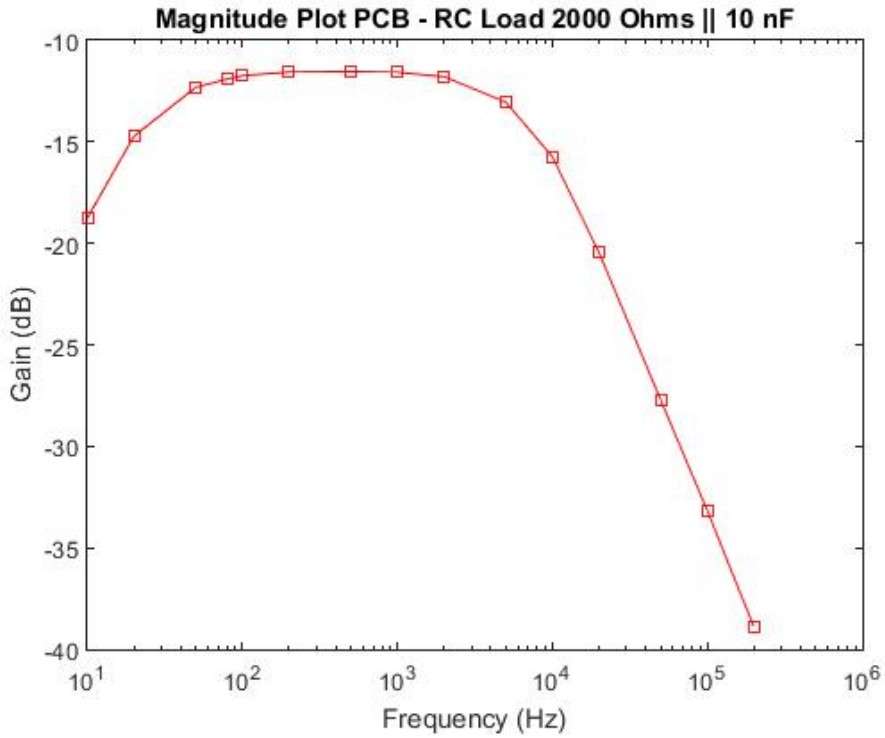

Figure 6.3: Magnitude Plot - PCB

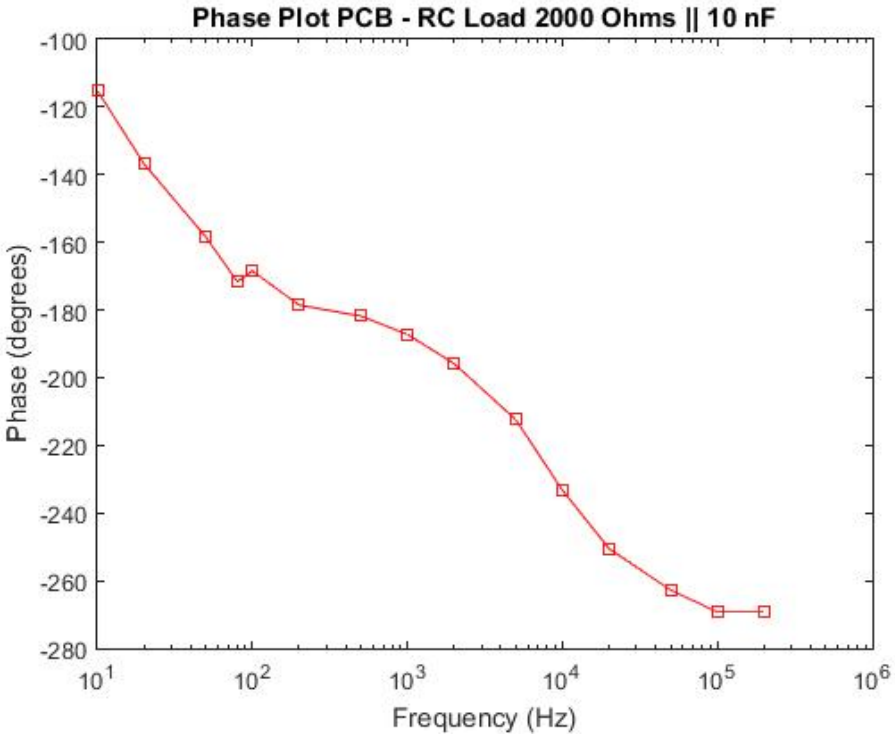

Figure 6.4: Phase Plot - PCB

6.2 Instrumentation Amplifier

The instrumentation amplifier circuit was configured on the PCB with a gain resistor of 10.002kΩ, which following equation 5.34 creates a gain of -1.9898 V/V. Figures 6.5 and 6.6 show the input and output waveforms of the instrumentation amplifier at 5kHz. Figures 6.7 and 6.8 show the input and output waveforms of the instrumentation amplifier at 100kHz.

At 5kHz, figures 6.5 and 6.6 show that the amplitude of the output waveform, shown in blue, is approximately two times, the input waveform, shown in yellow. According to the gain of the system, the output amplitude should be 1.9898 times the input amplitude. Therefore there is a 0.37% deviation from the expected output amplitude.

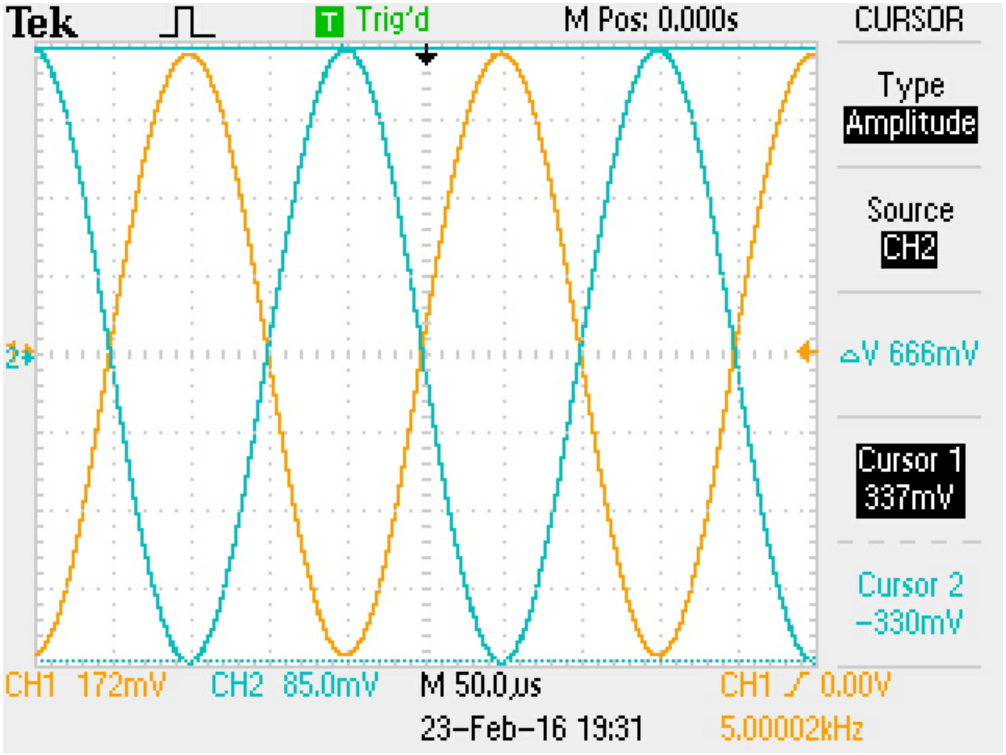

Figure 6.5: Vin INA at 5kHz

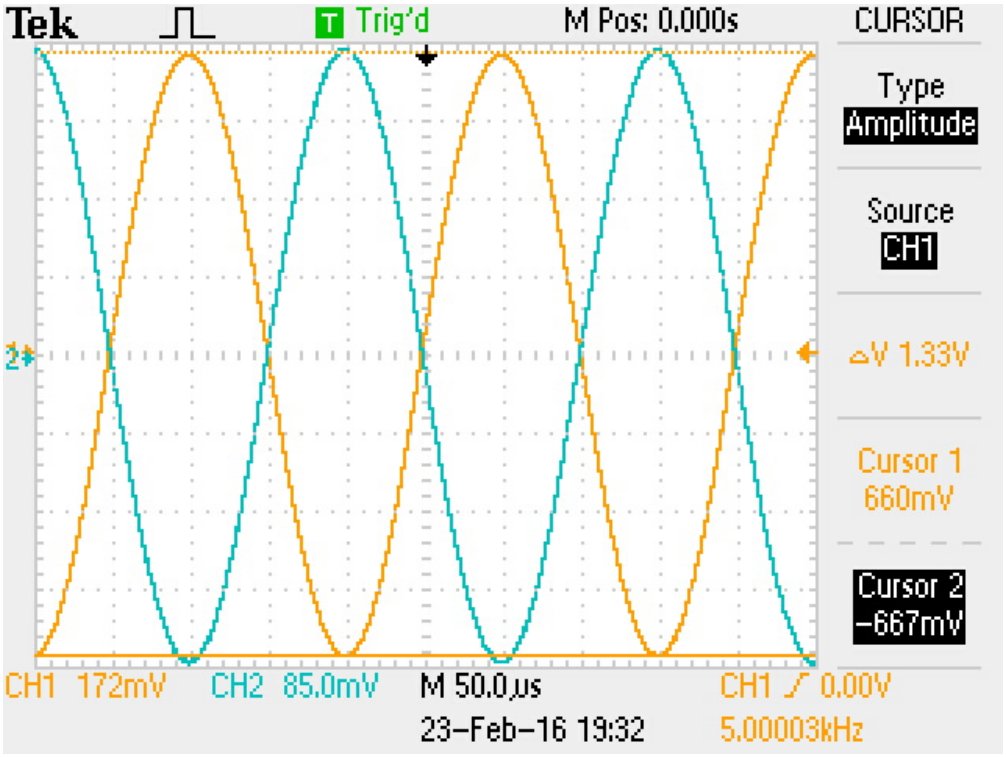

Figure 6.6: Vout INA at 5kHz

At 100kHz, figures 6.7 and 6.8 show that the amplitude of the output waveform, shown in blue, is approximately two times, the input waveform, shown in yellow. According to the gain of the system, the output amplitude should be -1.9898 times the input amplitude. Therefore, there is a 0.47% deviation from the expected output amplitude.

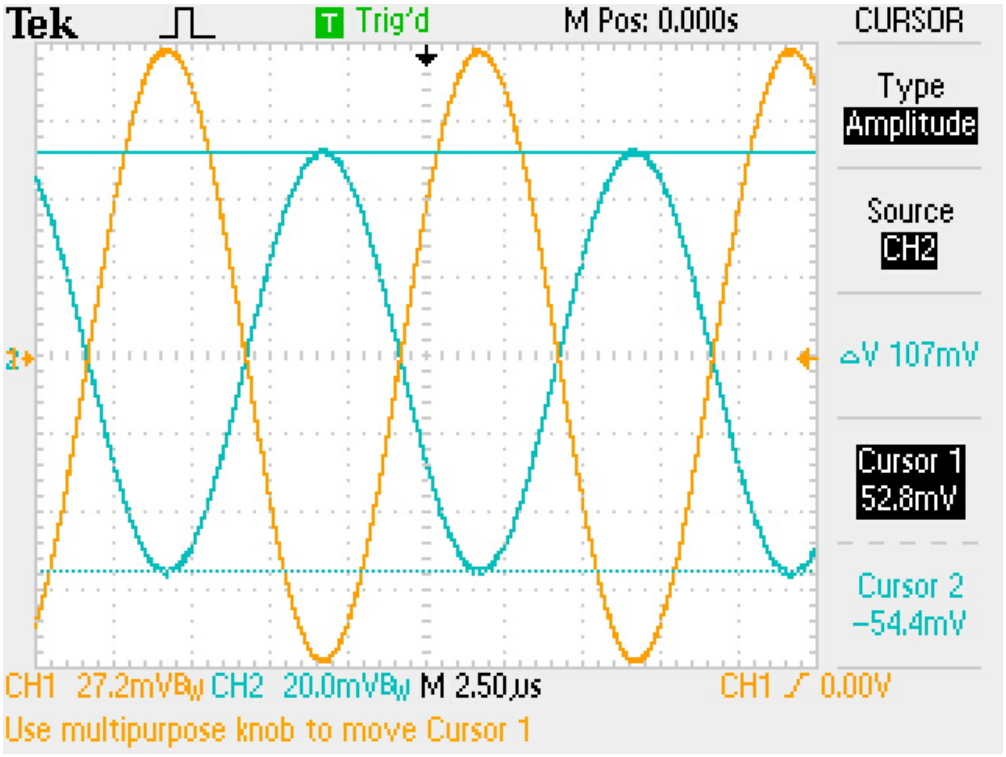

Figure 6.7: Vin INA at 100kHz

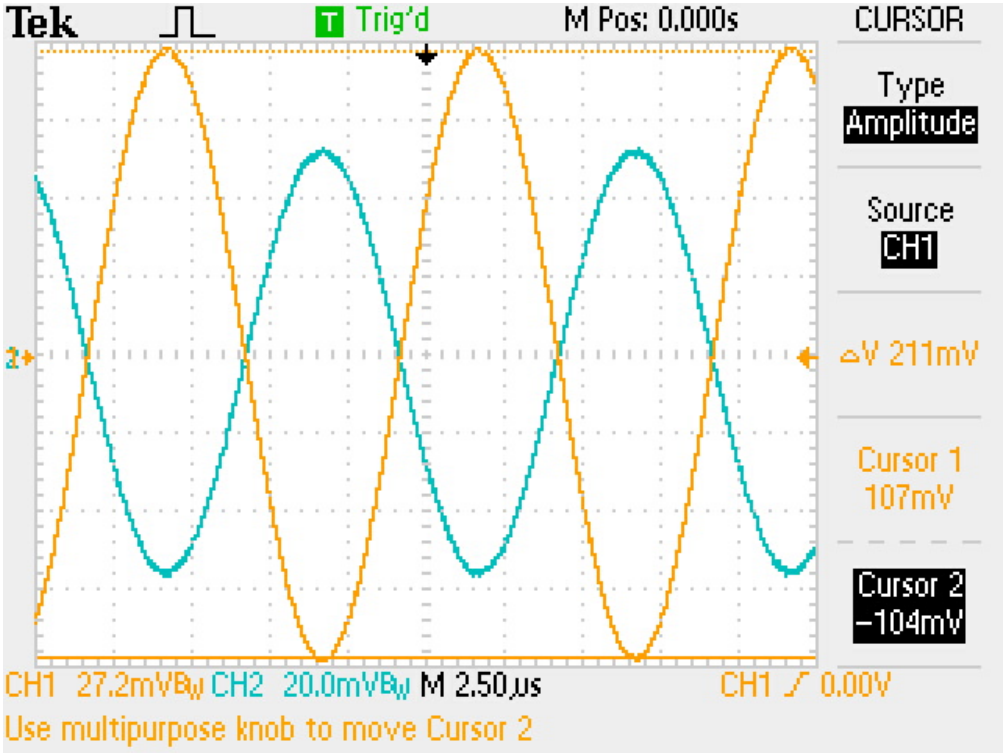

Figure 6.8: Vout INA at 100kHz

These deviations can be attributed to the experimental error and the low DC errors of the AD8421 instrumentation amplifier. Refer to appendix **??** for more information on the error margins of the AD8421 chip.

6.3 Transimpedance Amplifier

The AD5933 chip expects a current waveform into the output pin. Because of this, the AFE requires another voltage converter. For this V-I converter, the team chose a current setting resistor $R_{current2}$ which combined with an op amp internal to the AD5933 chip, and a feedback resistor $R_{current2}$ creates a trans-impedance amplifier. In simpler terms, the output of the instrumentation amplifier is amplified once again by an inverting amplifier with a gain of -3.002V/V

At 5kHz, figures 6.9 and 6.10 show the amplitude of the input voltage waveform and output voltage waveform respectively. According to the gain of the system, the output amplitude should be -3.002 times the input amplitude. Therefore, there is a 0.256% deviation from the expected output amplitude of 3.90V.

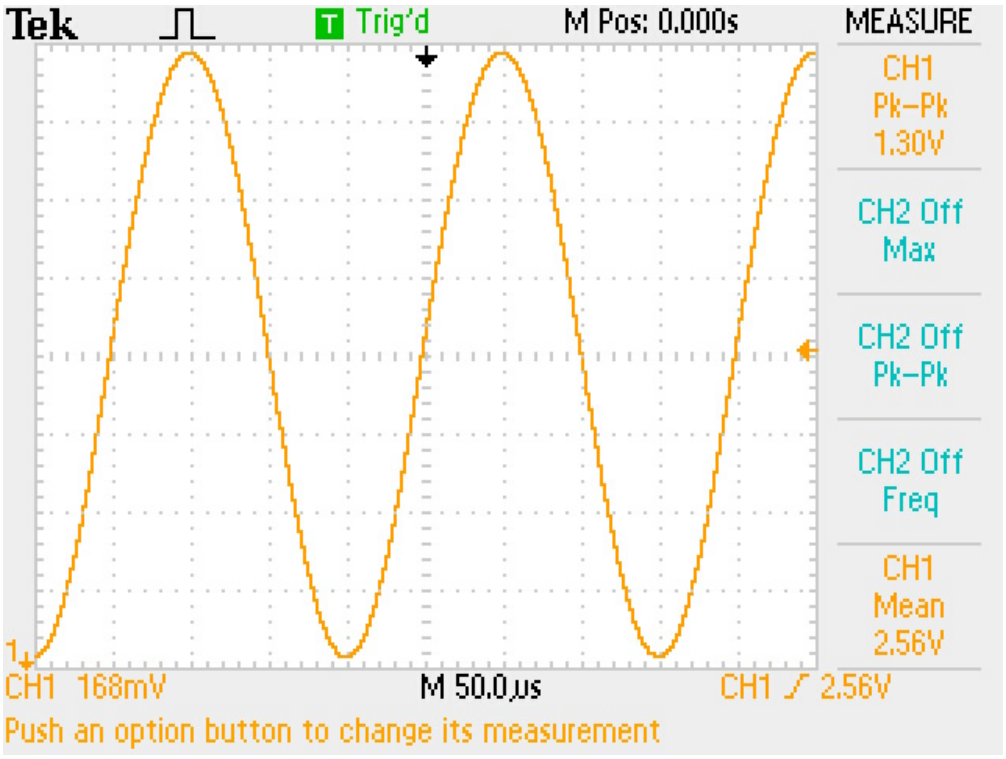

Figure 6.9: Trans-Impedance Amp input at 5kHz

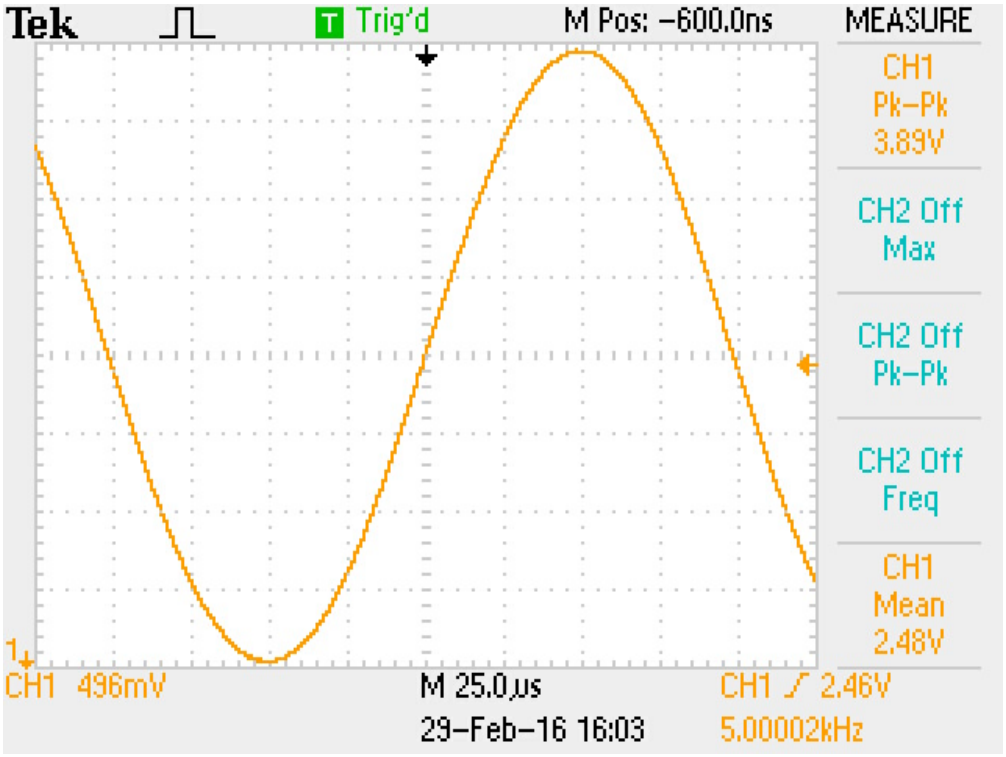

Figure 6.10: Trans-Impedance Amp output at 5kHz

At 100kHz, Figure 6.11 and 6.12 show the amplitude of the input voltage waveform and output voltage waveform respectively. According to the gain of the system, the output amplitude should be -3.002 times the input amplitude. Therefore, there is a 0.52% deviation from the expected output amplitude of 381mV.

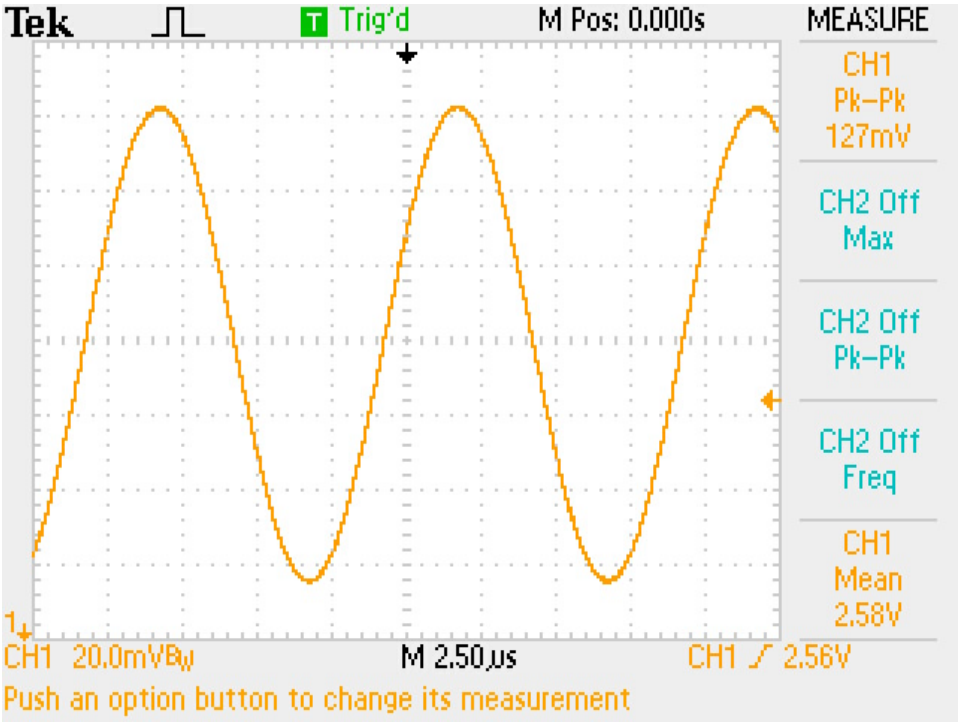

Figure 6.11: Trans-Impedance Amp input at 100kHz

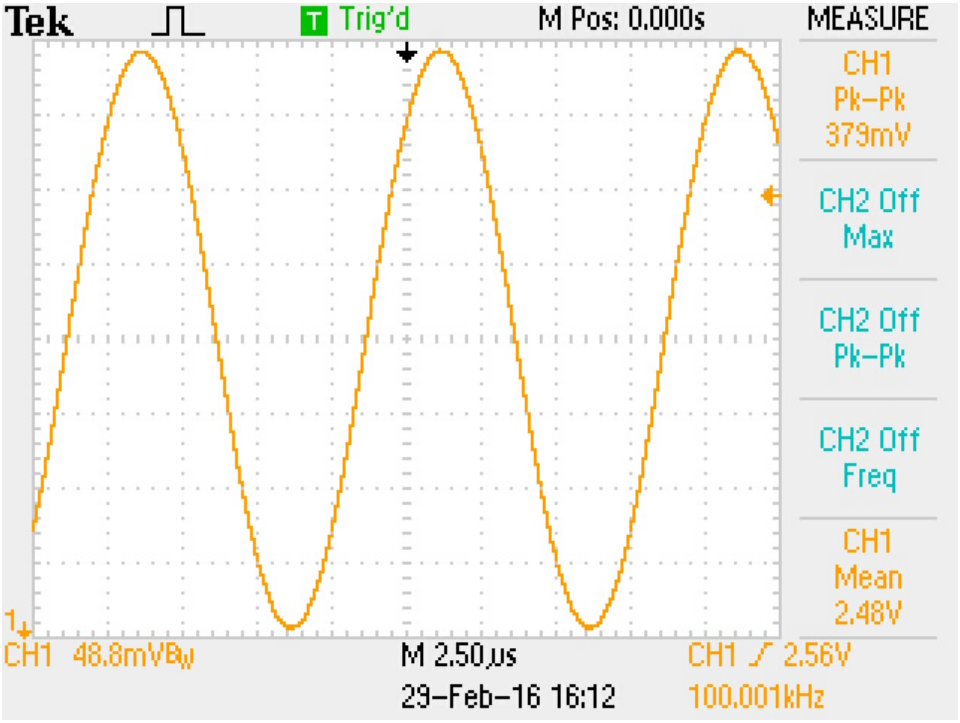

Figure 6.12: Trans-Impedance Amp output at 100kHz

These deviations can be attributed to experimental error and the low DC errors of the operational amplifier.

6.4 Atmega328p/Bluetooth/AD5933 Testing

This section will cover the testing and results of the Atmega328p, HC-06 Bluetooth Module and the AD5933. The testing being done is to validate the correct functionality of all the parts.

6.4.1 Atmega328p

The test on the Atmega328p was conducted to ensure its communication with the HC-06, and also to make sure that the AD5933 was working as intended.

When the Atmega328p was tested for correct functionality with the Bluetooth module, a simplified Bluetooth code was loaded onto the Atmega328p. This code simply made the Bluetooth module send message that incremented by one each time . The message was successfully received and displayed in Matlab, which verified that the connections between the Bluetooth module and the Atmega328p work as intended. Figure 6.13 shows the Bluetooth transmission between the Tx pin of the Atmega328p and the Rx pin of the HC-06 Bluetooth module when sending this message.

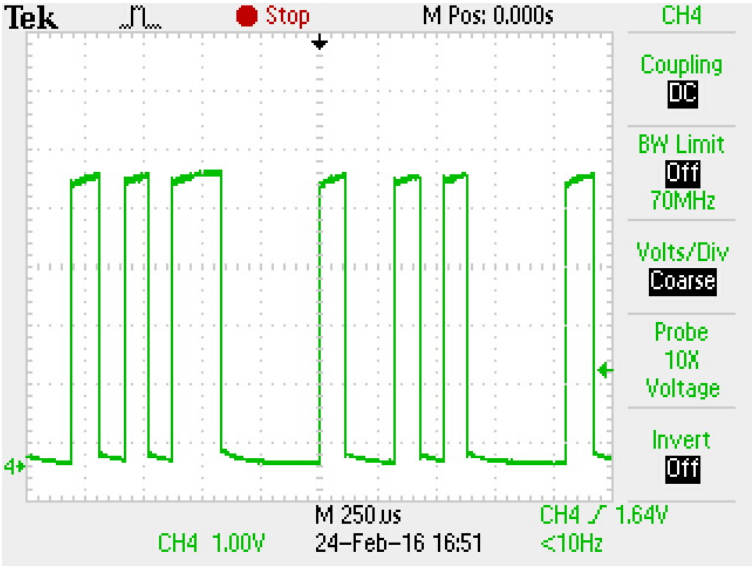

Figure 6.13: Bluetooth Transmission

The next test involved checking the communication between the ATmega328p and the AD5933 chip. This was done by probing the I2C pins that connect the Atmega328p to the AD5933. Figure 6.14 shows the communication between these chips as sudden spikes down to zero volts, because I2C is open-drain method of transmitting data.

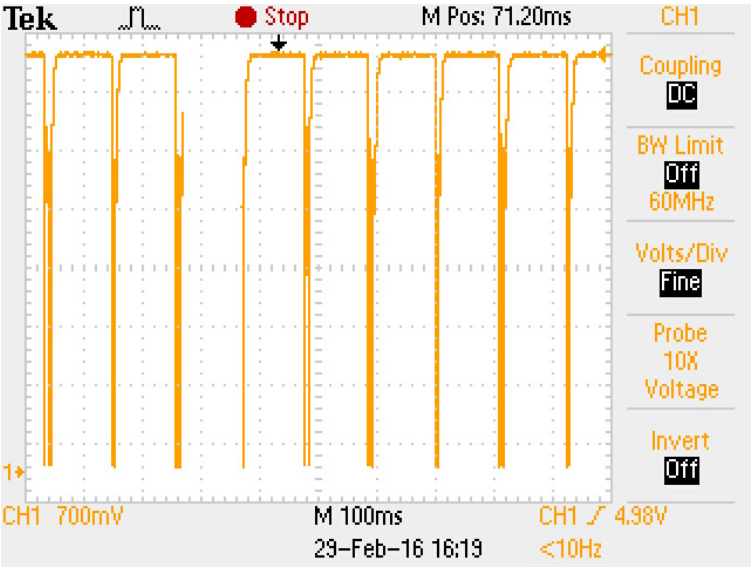

Figure 6.14: I2C Transmission

6.4.2 Bluetooth Module (HC-06)

The Bluetooth Module was tested to ensure it was sending the correct data to the computer.This was done by testing the HC-06. Another test was performed to check the effect of transmission on the power supply. The following figure shows the result of Bluetooth transmission from the computer. This shows the start of one transmission Nan followed by the frequency value, real number, and imaginary number sent consecutively.

	151	152	153	154	155	156	157	158	159	160	161	162
1	NaN	5	-7327	10287	6	-7784	8980	7	-8000	7772	8	-8054

Figure 6.15: HC-06 Bluetooth Transmission

There was no noticeable change in the power supply voltage while the bluetooth transmitted continuously for five minutes. This could mean that the HC-06 and its transmission take longer than five minutes in order to show a visible change in the battery's voltage.

6.4.3 AD5933

The AD5933 chip's output was tested by checking the Vout pin of the AD5933. This was to ensure that the chip produced the expected signal of a 1.5V-pk signal biased at 2.24 V, and that it sweeps from 5kHz to 100kHz. Figure6.17 and 6.16 show the output of the AD5933 after a DC blocking capacitor at both 8 kHz and 100 kHz. This shows that the AD5933 is working correctly even though the team could not stop the oscilloscope when the waveform was at 5 kHz to save a picture.

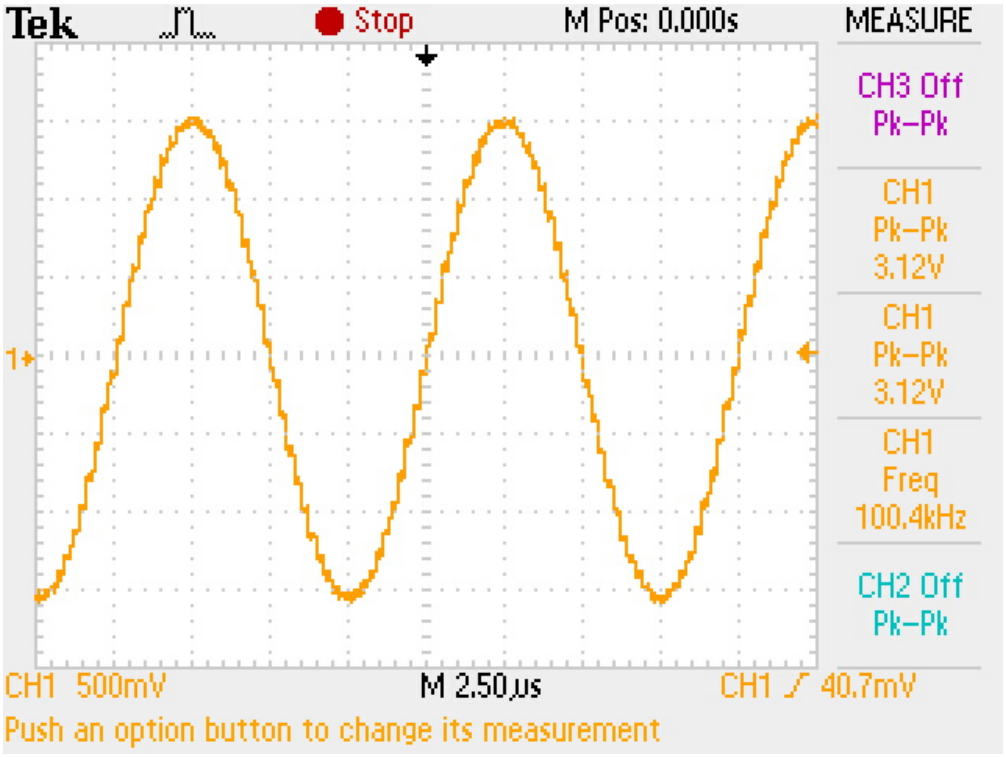

Figure 6.16: Output of AD5933 - 100kHz

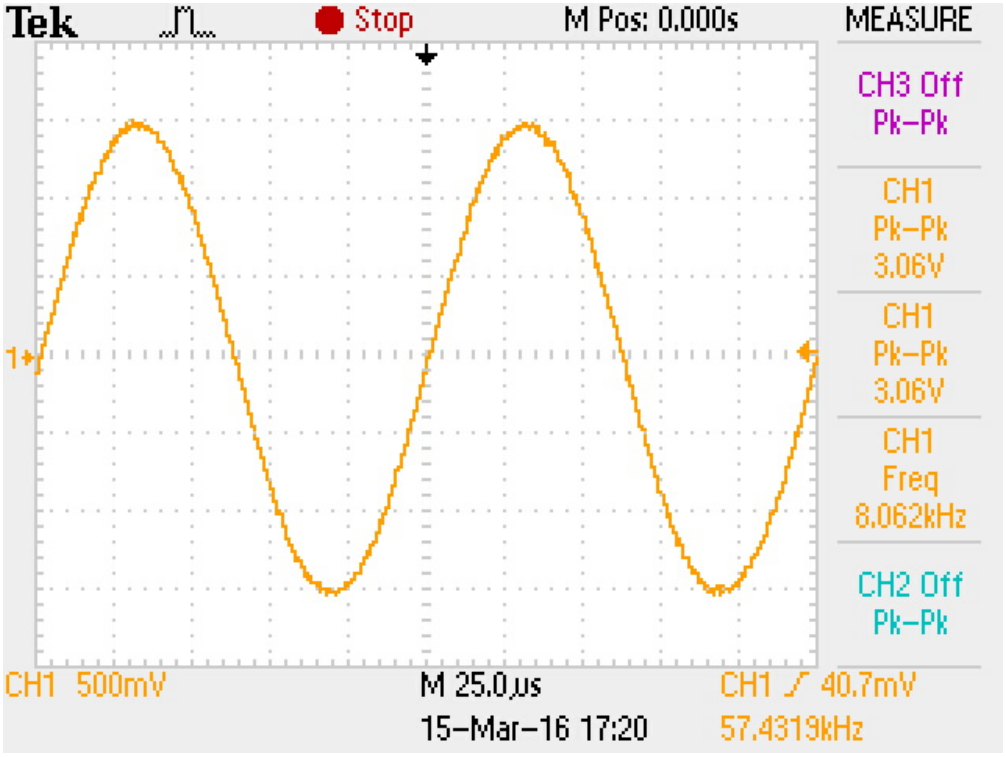

Figure 6.17: Output of AD5933 - 8kHz

6.5 System Validation

The complete system was tested on RC circuits and on human subjects. In-depth analysis was performed on eight RC loads to study the performance of our device.The following resistor-capacitor parallel loads were used in testing:

- R = 905 Ω C = 5.34 nF (283.09 Ω $\leq |Z| \leq$ 894.75Ω)
- R = 905 Ω C = 10.6 nF (147.99 Ω $\leq |Z| \leq$ 866.44Ω)
- R = 1797 Ω C = 5.34 nF (294.06 Ω $\leq |Z| \leq$ 1,720.51Ω)
- R = 1797 Ω C = 10.6 nF (149.62 Ω $\leq |Z| \leq$ 1,541.99Ω)
- R = 1980 Ω C = 5.34 nF (294.72 Ω $\leq |Z| \leq$ 1,879.04Ω)
- R = 1980 Ω C = 10.6 nF (149.71 Ω $\leq |Z| \leq$ 1,653.01Ω)
- R = 2209 Ω C = 5.34 nF (295.36 Ω $\leq |Z| \leq$ 2,071.34Ω)
- R = 2209 Ω C = 10.6 nF (149.80 Ω $\leq |Z| \leq$ 1,779.40Ω)
- R = 2947 Ω C = 5.34 nF (296.53 Ω $\leq |Z| \leq$ 2,641.78Ω)
- R = 2947 Ω C = 10.6 nF (149.80 Ω $\leq |Z| \leq$ 2102.36Ω)
- R = 3024 Ω ($|Z| = 3024$ Ω)

These RC loads were chosen to reflect multiple impedance spans in the desired impedance range of approximately 200 Ω to 3k Ω. The graph in Figure 6.18 shows the RC pairs in the yellow surface that make impedance values between 200Ω and 3kΩ at 5-100kHz. All the test points listed above are also marked on the graph.

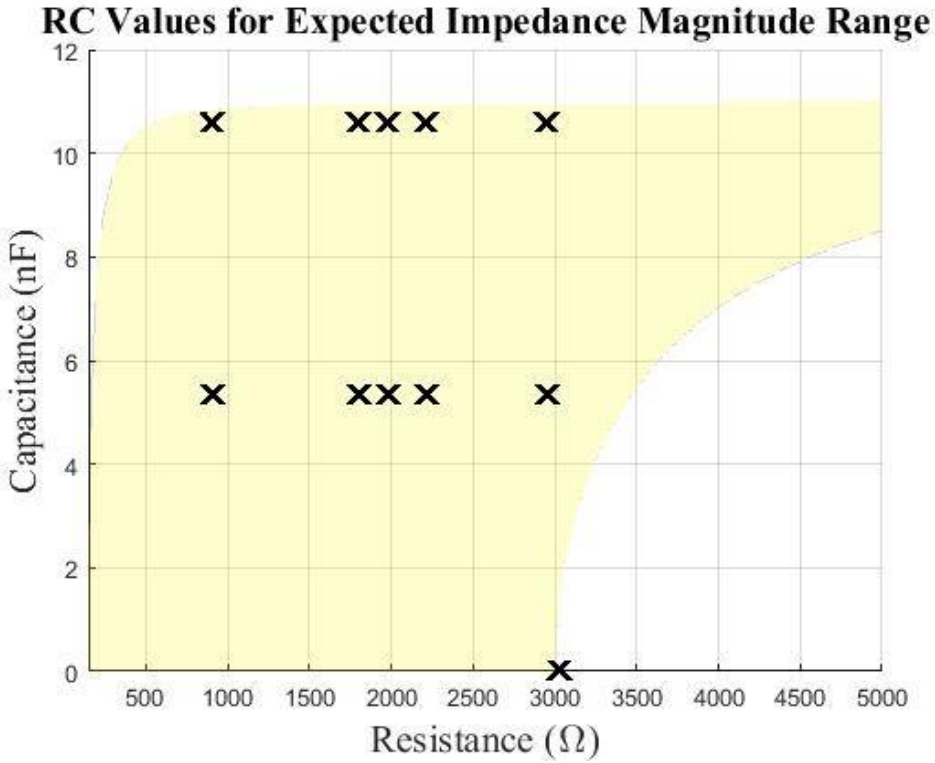

Figure 6.18: RC Ranges for Impedance Magnitude between 200Ω and 2kΩ

Figures 6.19 and 6.20 show the impedance magnitude and phase results versus frequency of the tested data points. The magnitude of all the tested RC values reside within the

expected range of 145Ω to 3kΩ. As expected, it can be observed that the loads with the same capacitance reach the same minimum impedance.

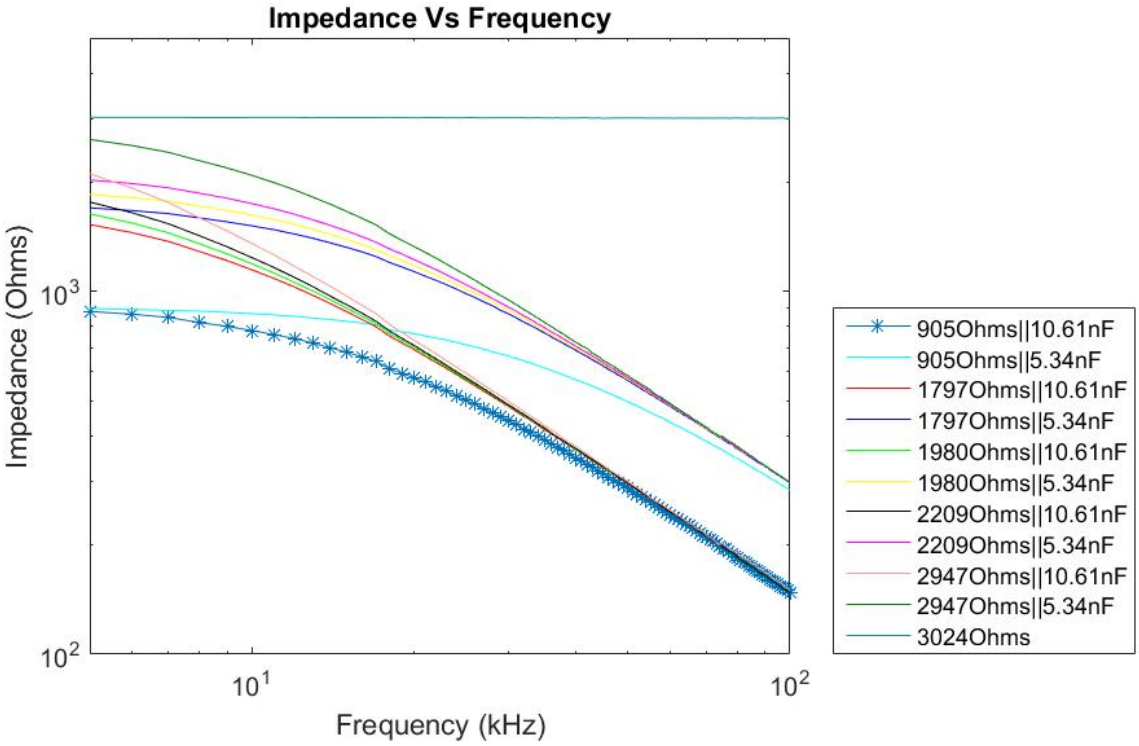

Figure 6.19: Resistance vs Frequency of Test Loads

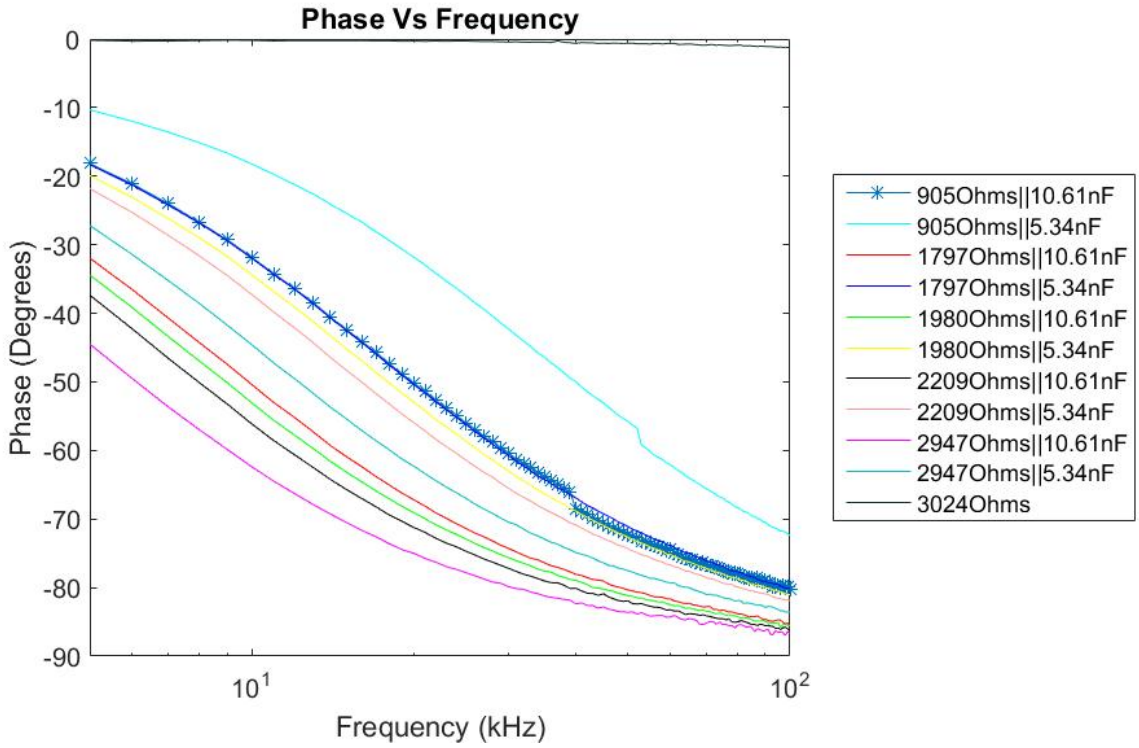

Figure 6.20: Phase vs Frequency of Test Loads

Table 6.3 and Figures 6.21 to 6.24 show the test results for the RC load of 905 Ω resistor and 5.34nF capacitor.

Table 6.3 shows the mean and the standard deviation of the error for the data collected using this RC load.

Table 6.3: RC Parallel Load Resistor = 905 Ω Capacitor = 5.34nF

Type	**Impedance**	**Phase**
Unit	%	Degrees
Mean	0.1483	0.4858
Standard Deviation	0.5040	0.6329

Figures 6.21 and 6.22 show the magnitude in the frequency range sweep. The blue line represents the theoretical values and the red squares are acquired data points. It can be observed that the data points for both magnitude and phase are very close with the theoretical values.

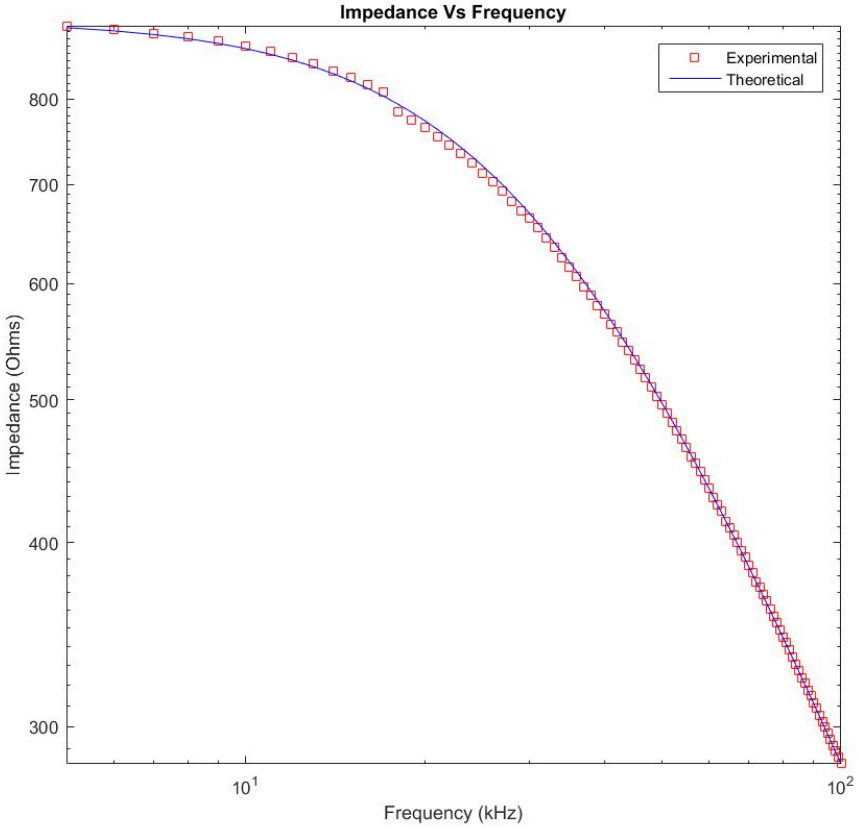

Figure 6.21: Impedance vs Frequency RC Parallel Load Resistor = 905 Ω Capacitor = 5.34nF

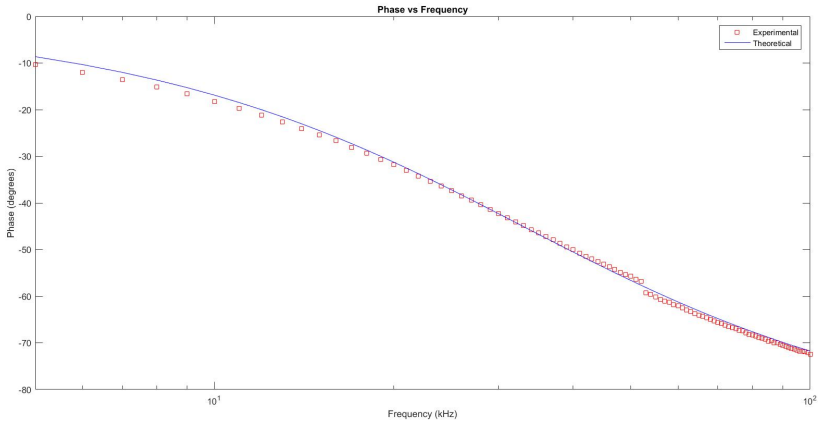

Figure 6.22: Phase vs Frequency RC Parallel Load Resistor = 905 Ω Capacitor = 5.34nF

Figures 6.23 and 6.24 show the magnitude percent error and phase degree error respec-

tively.

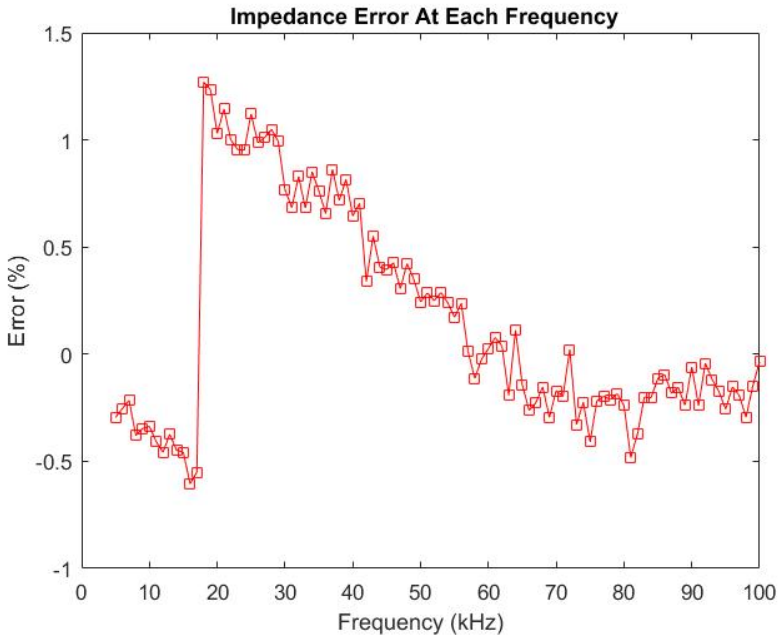

Figure 6.23: Impedance Error vs Frequency RC Parallel Load Resistor = 905 Ω Capacitor = 5.34nF

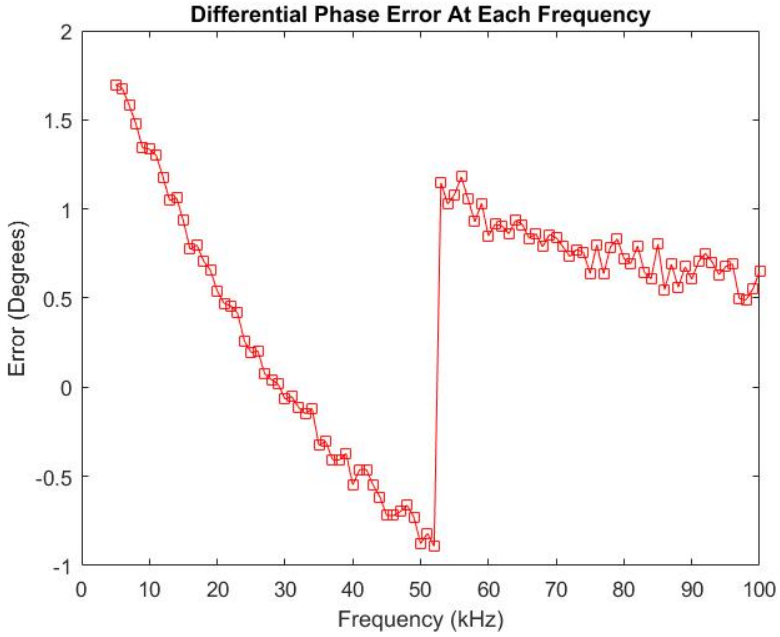

Figure 6.24: Phase Error vs Frequency RC Parallel Load Resistor = 905 Ω Capacitor = 5.34nF

Table 6.4 and Figures 6.25 to 6.28 show the test results for the RC load of 905 Ω resistor

and 10.61nF capacitor.

Table 6.4 shows the mean and the standard deviation of the error for the data collected using this RC load.

Table 6.4: RC Parallel Load Resistor = 905 Ω Capacitor = 10.61nF

Type	Impedance	Phase
Unit	%	Degrees
Mean	-0.5830	-1.073e-04
Standard Deviation	0.3785	0.5513

Figures 6.25 and 6.26 show the theoretical expectation and the measured data points. More specifically, the blue line represents the theoretical values and the red squares are acquired data points. It can be observed that the data points for both magnitude and phase are very close with the theoretical values.

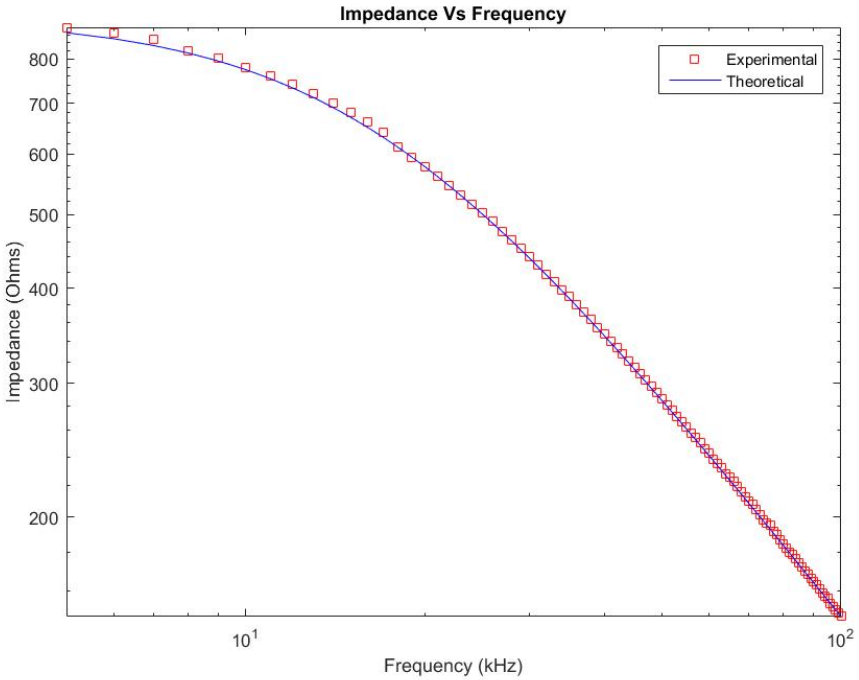

Figure 6.25: Impedance vs Frequency RC Parallel Load Resistor = 905 Ω Capacitor = 10.61nF

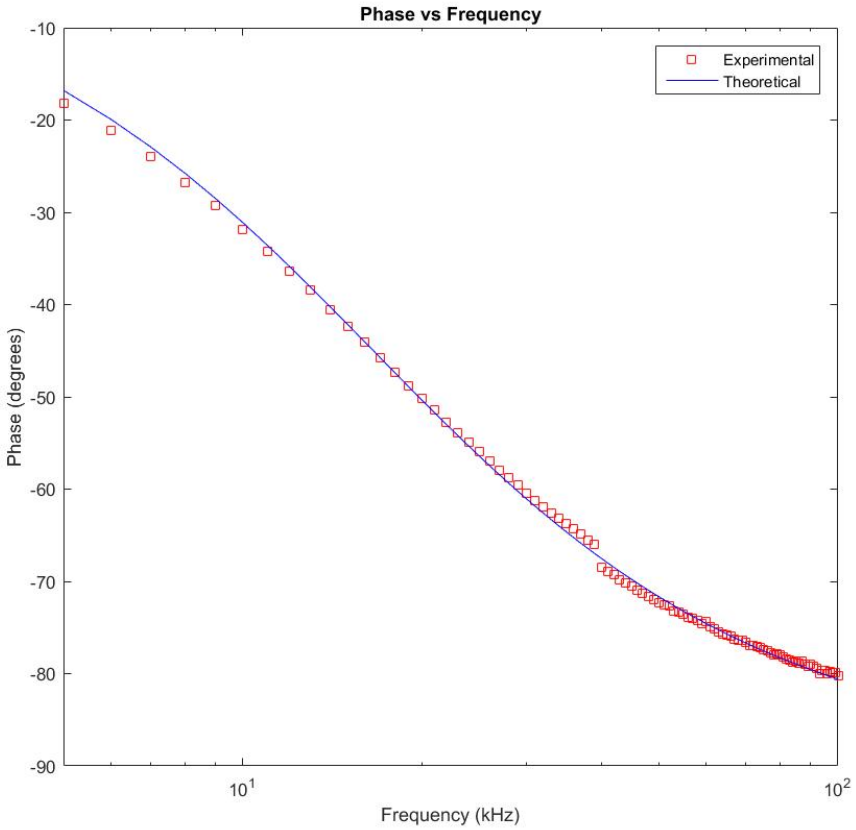

Figure 6.26: Phase vs Frequency RC Parallel Load Resistor = 905 Ω Capacitor = 10.61nF

Figures 6.27 and 6.28 show the magnitude percent error and phase degree error respectively.

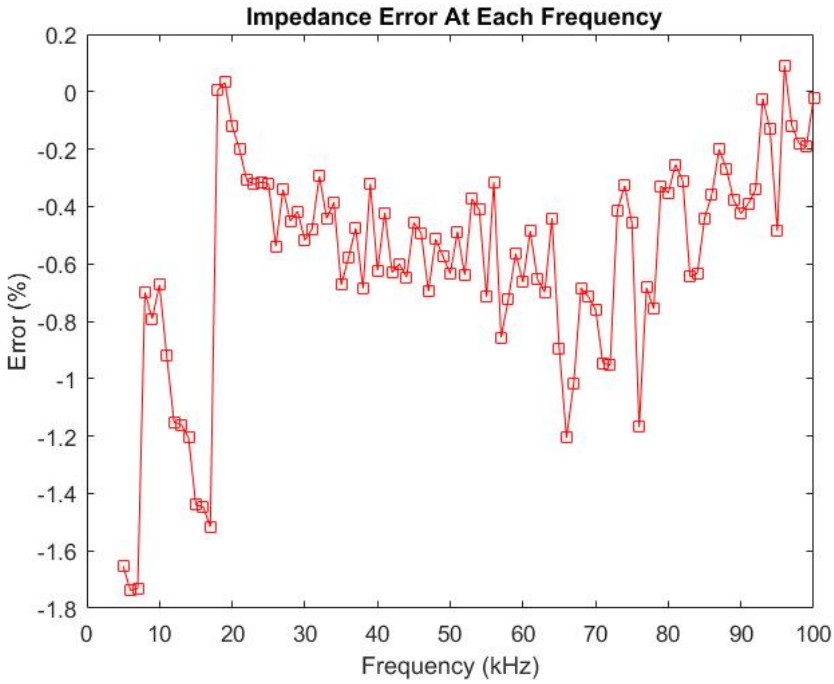

Figure 6.27: Impedance Error vs Frequency RC Parallel Load Resistor = 905 Ω Capacitor = 10.61nF

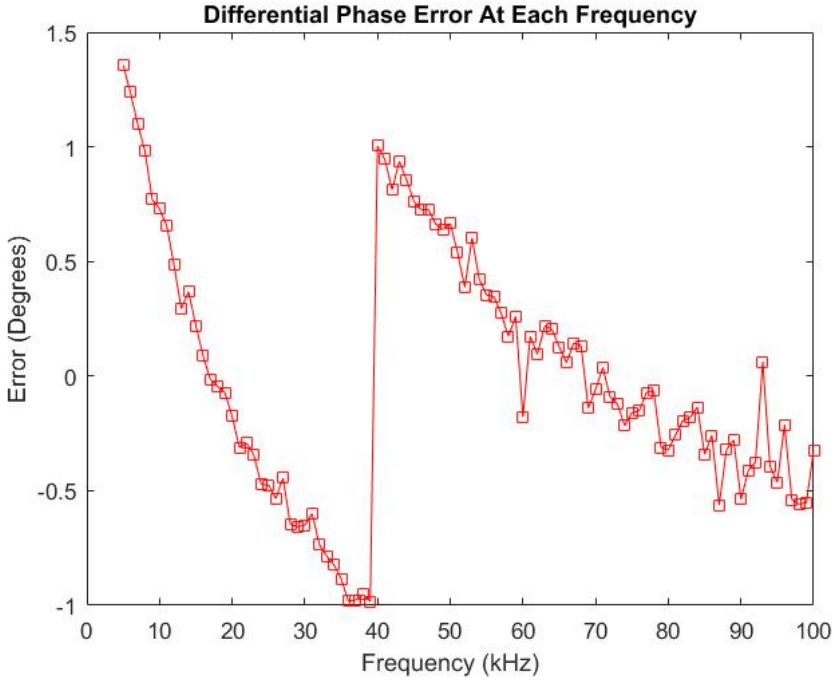

Figure 6.28: Phase Error vs Frequency RC Parallel Load Resistor = 905 Ω Capacitor = 10.61nF

Table 6.5 and Figures 6.29 to 6.32 show the test results for the RC load of 1797 Ω resistor and 5.34nF capacitor. Table 6.5 shows the mean error and the standard deviation of the error for the data collected using this RC load.

Table 6.5: RC Parallel Load Resistor = 1797 Ω Capacitor = 5.34nF

Type	**Impedance**	**Phase**
Unit	%	Degrees
Mean	-0.1500	-0.2779
Standard Deviation	0.7238	0.4948

Figures 6.29 and 6.30 show the magnitude in the frequency range sweep. The blue line represents the theoretical values and the red squares are acquired data points. It can be observed that the data points for both magnitude and phase are very close with the theoretical values.

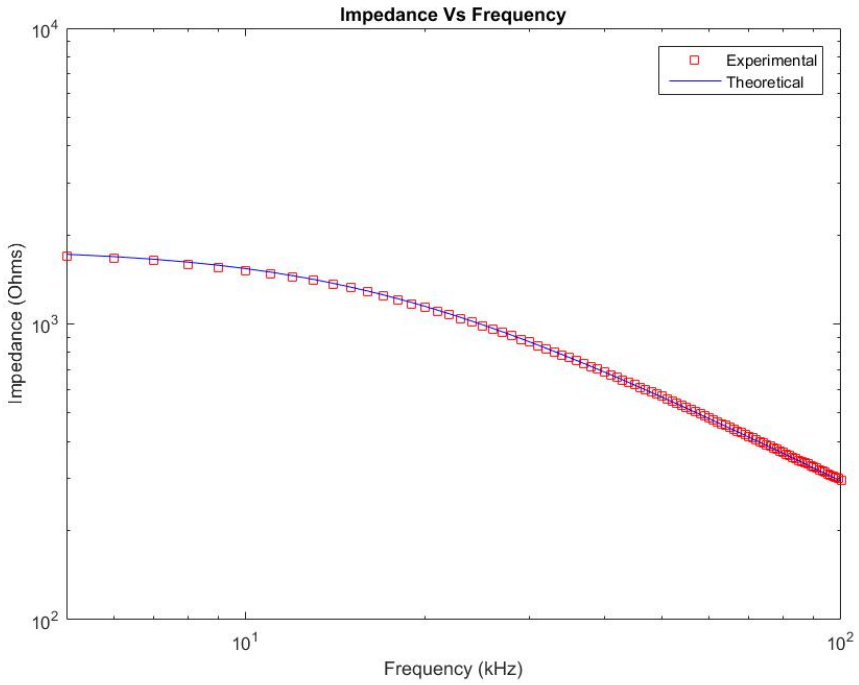

Figure 6.29: Impedance vs Frequency RC Parallel Load Resistor = 1797 Ω Capacitor = 5.34nF

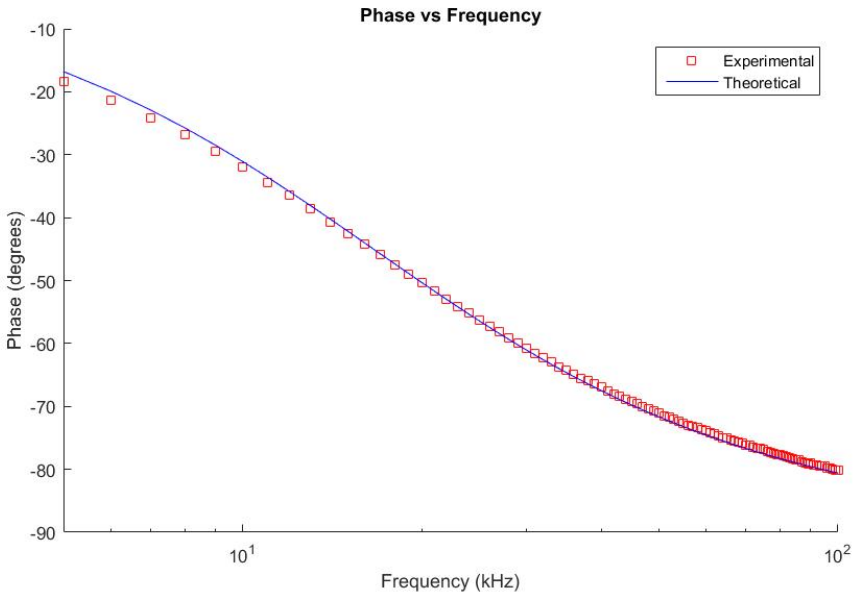

Figure 6.30: Phase vs Frequency RC Parallel Load Resistor = 1797 Ω Capacitor = 5.34nF

Figures 6.31 and 6.32 show the magnitude percent error and phase degree error respectively.

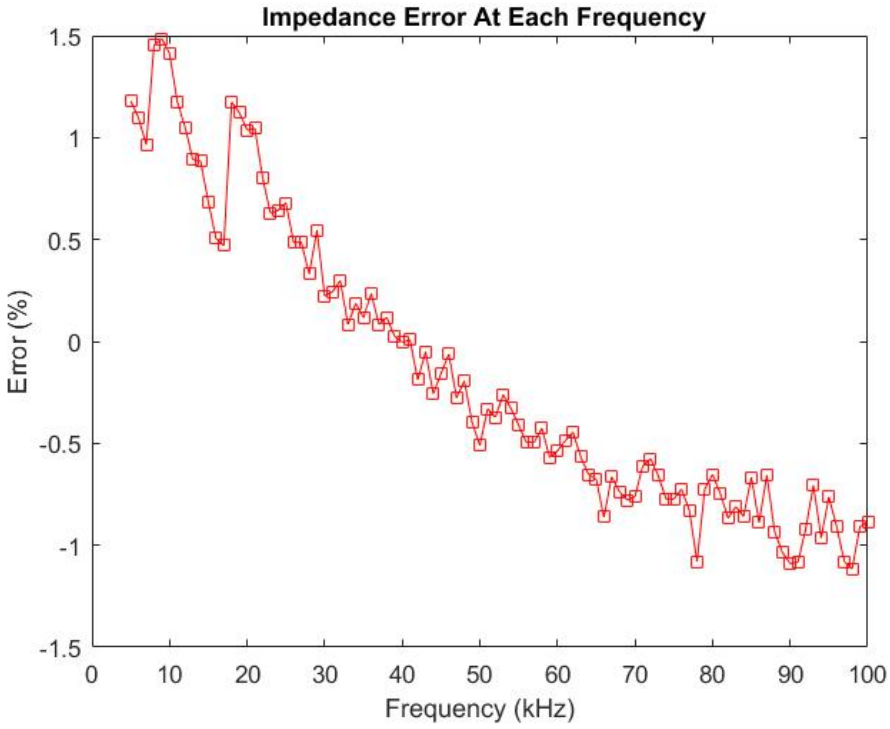

Figure 6.31: Impedance Error vs Frequency RC Parallel Load Resistor = 1797 Ω Capacitor = 5.34nF

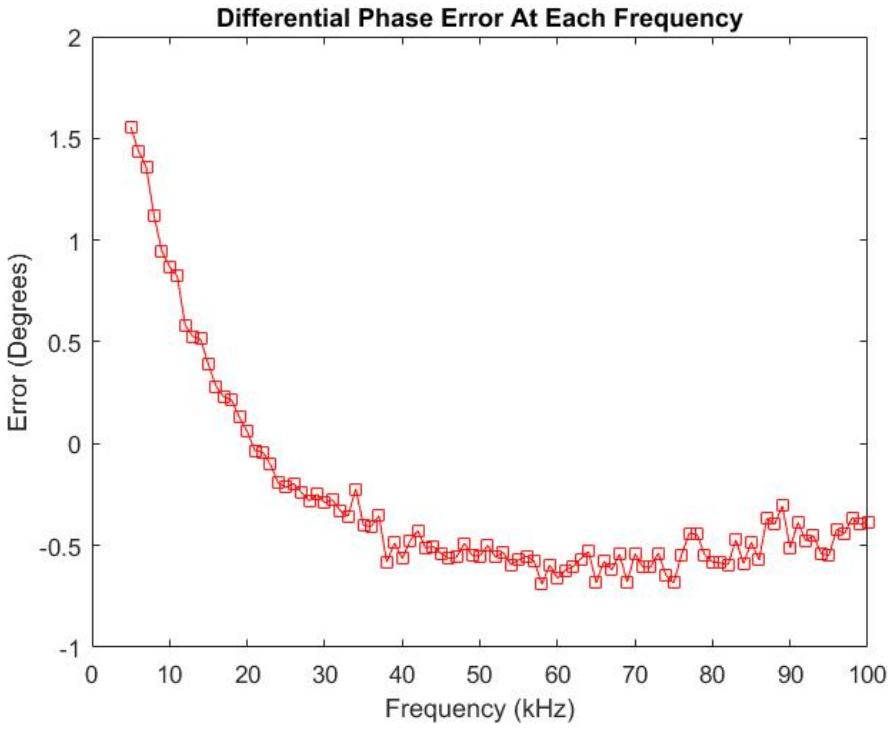

Figure 6.32: Phase Error vs Frequency RC Parallel Load Resistor = 1797 Ω Capacitor = 5.34nF

Table 6.6 and Figures 6.33 to 6.36 show the test results for the RC load of 1797 Ω resistor and 10.61nF capacitor.

Table 6.6 shows the mean error and the standard deviation of the error for the data collected using this RC load.

Table 6.6: RC Parallel Load Resistor = 1797 Ω Capacitor = 10.61nF

Type	Impedance	Phase
Unit	%	Degrees
Mean	0.4463	-0.1310
Standard Deviation	0.4715	0.2520

Figures 6.33 and 6.34 show the theoretical expectation and the measured data points. More specifically, the blue line represents the theoretical values and the red squares are acquired data points. It can be observed that the data points for both magnitude and phase are very close with the theoretical values.

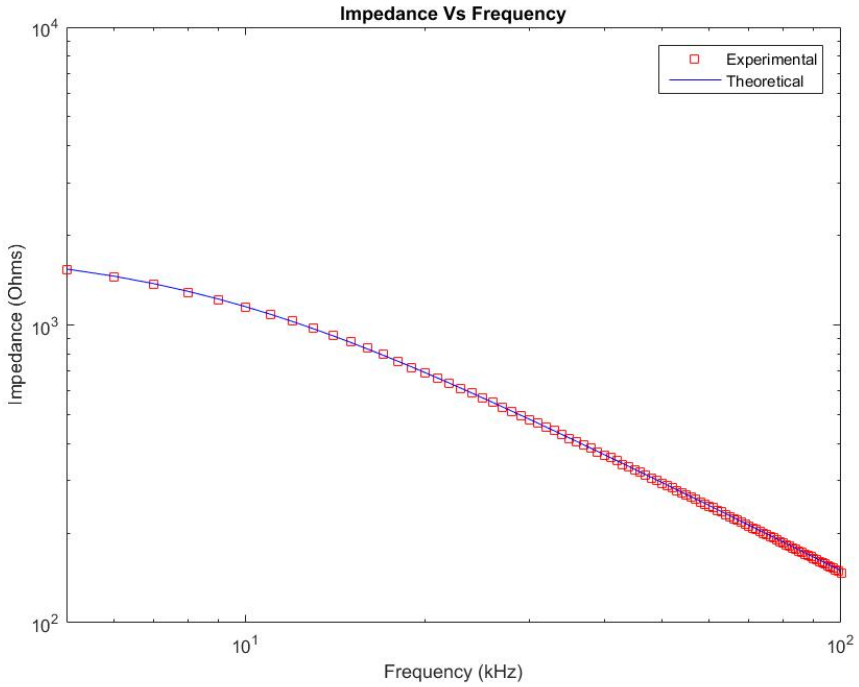

Figure 6.33: Impedance vs Frequency RC Parallel Load Resistor = 1797 Ω Capacitor = 10.61nF

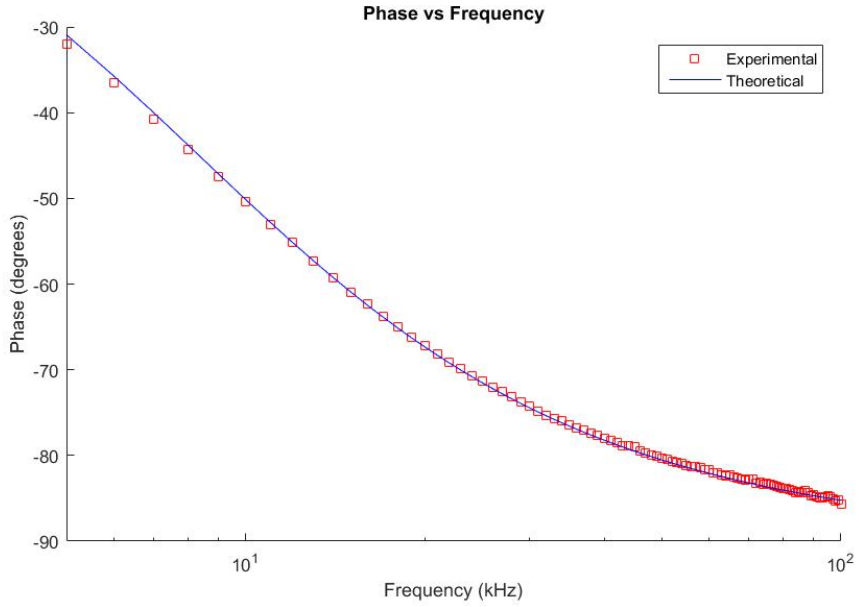

Figure 6.34: Phase vs Frequency RC Parallel Load Resistor = 1797 Ω Capacitor = 10.61nF

Figures 6.35 and 6.36 show the magnitude percent error and phase degree error respectively.

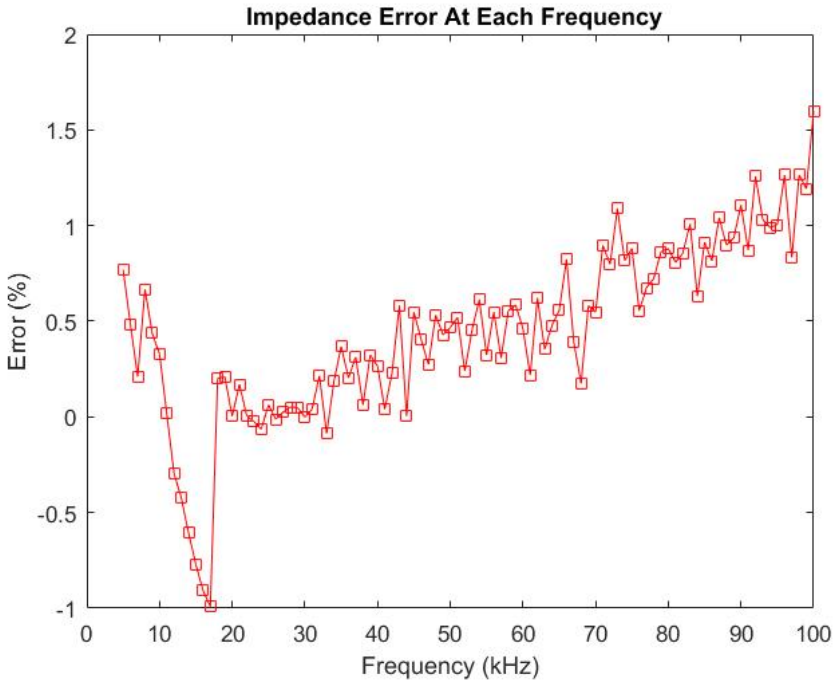

Figure 6.35: Impedance Error vs Frequency RC Parallel Load Resistor = 1797 Ω Capacitor = 10.61nF

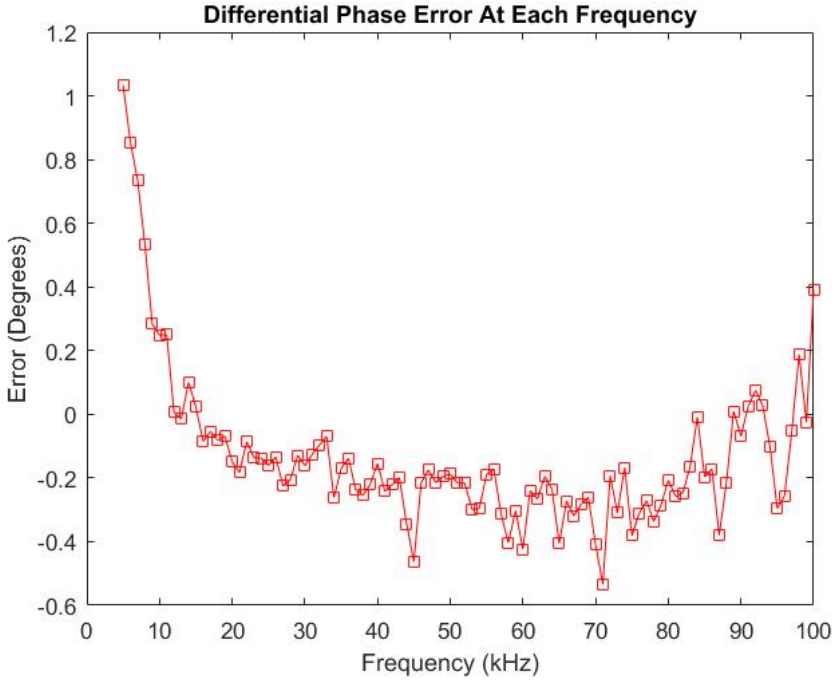

Figure 6.36: Phase Error vs Frequency RC Parallel Load Resistor = 1797 Ω Capacitor = 10.61nF

Table 6.7 and Figures 6.37 to 6.40 show the test results for the RC load of 1980.1 Ω resistor and 5.34nF capacitor.

Table 6.7 shows the mean error and the standard deviation of the error for the data collected using this RC load.

Type	Impedance	Phase
Unit	%	Degrees
Mean	-0.1991	-0.3264
Standard Deviation	0.7565	0.4747

Table 6.7: RC Parallel Load Resistor = 1980 Ω Capacitor = 5.34nF

Figures 6.37 and 6.38 show the theoretical expectation and the measured data points. More specifically, the blue line represents the theoretical values and the red squares are acquired data points. It can be observed that the data points for both magnitude and phase are very close with the theoretical values.

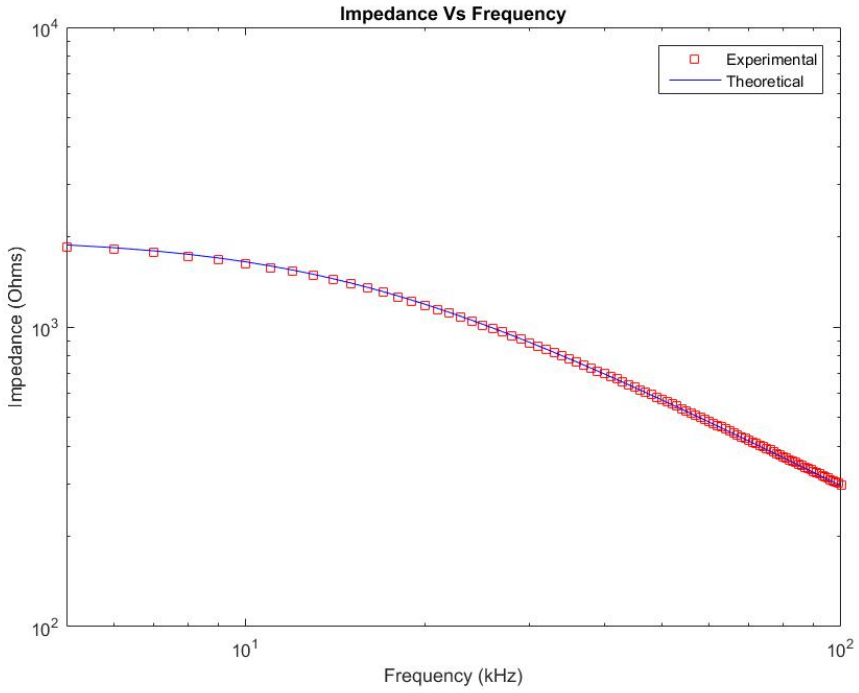

Figure 6.37: Impedance vs Frequency RC Parallel Load Resistor = 1980 Ω Capacitor = 5.34nF

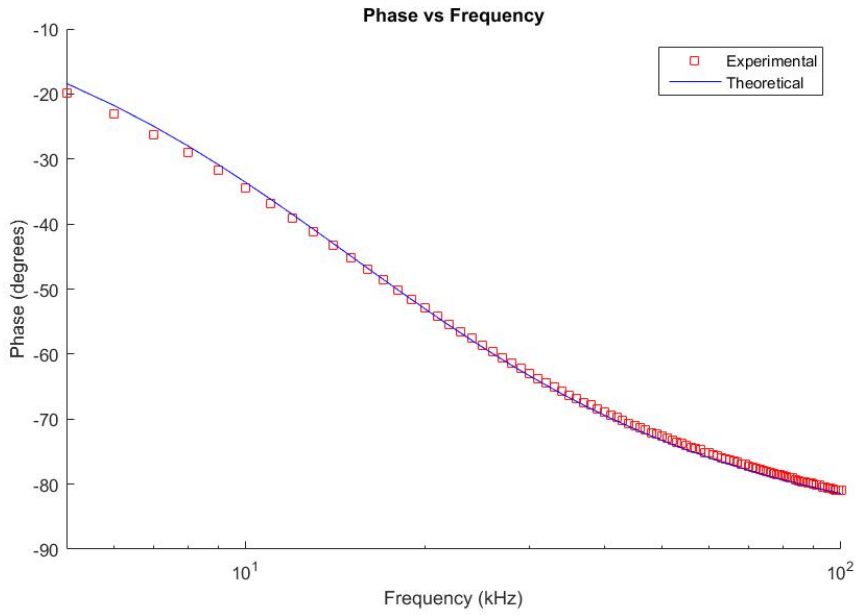

Figure 6.38: Phase vs Frequency RC Parallel Load Resistor = 1980 Ω Capacitor = 5.34nF

Figures 6.39 and 6.40 show the magnitude percent error and phase degree error respectively.

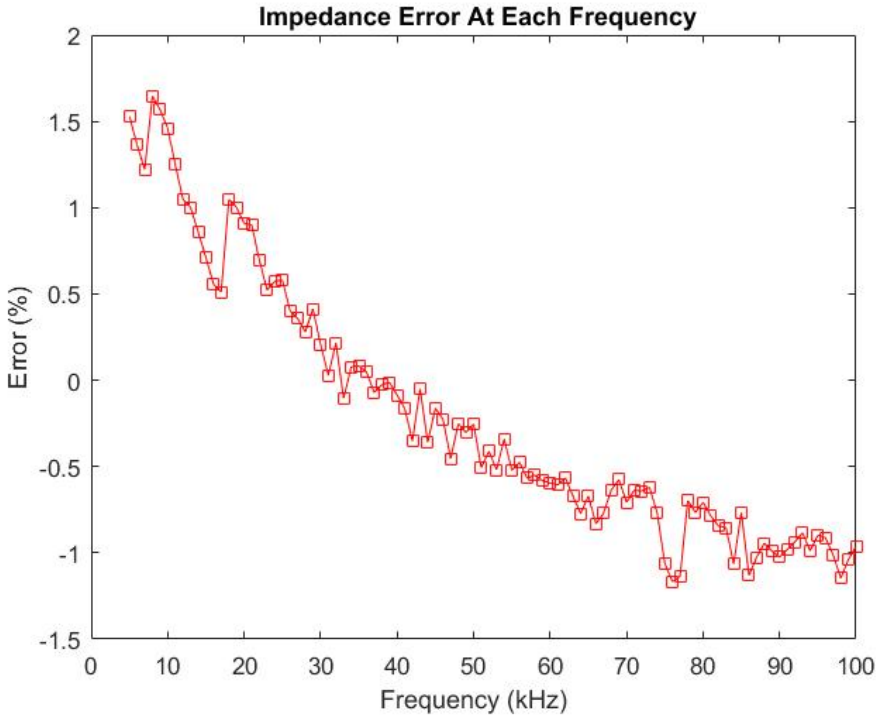

Figure 6.39: Impedance Error vs Frequency RC Parallel Load Resistor = 1980 Ω Capacitor = 5.34nF

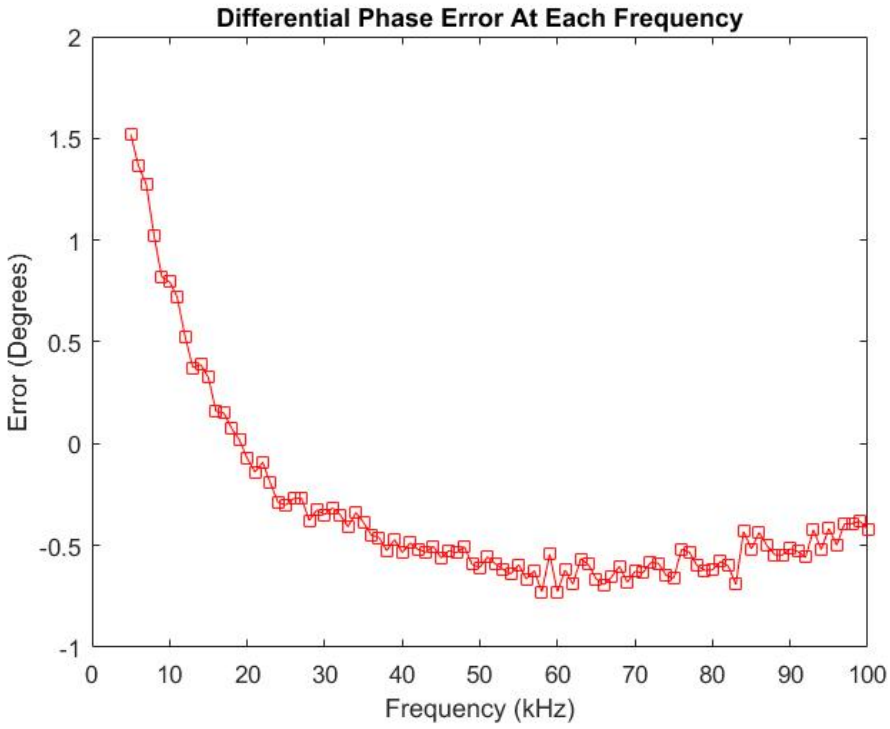

Figure 6.40: Phase Error vs Frequency RC Parallel Load Resistor =1980 Ω Capacitor = 5.34nF

Table 6.8 and Figures 6.41 to 6.44 show the test results for the RC load of 1980 Ω resistor and 10.61nF capacitor. Table 6.8 shows the mean error and the standard deviation of the error for the data collected using this RC load.

Table 6.8: RC Parallel Load Resistor = 1980 Ω Capacitor = 10.61nF

Type	Impedance	Phase
Unit	%	Degrees
Mean	0.4643	-0.1757
Standard Deviation	0.5130	0.2417

Figures 6.41 and 6.42 show the theoretical expectation and the measured data points. More specifically, the blue line represents the theoretical values and the red squares are acquired data points. It can be observed that the data points for both magnitude and phase are very close with the theoretical values.

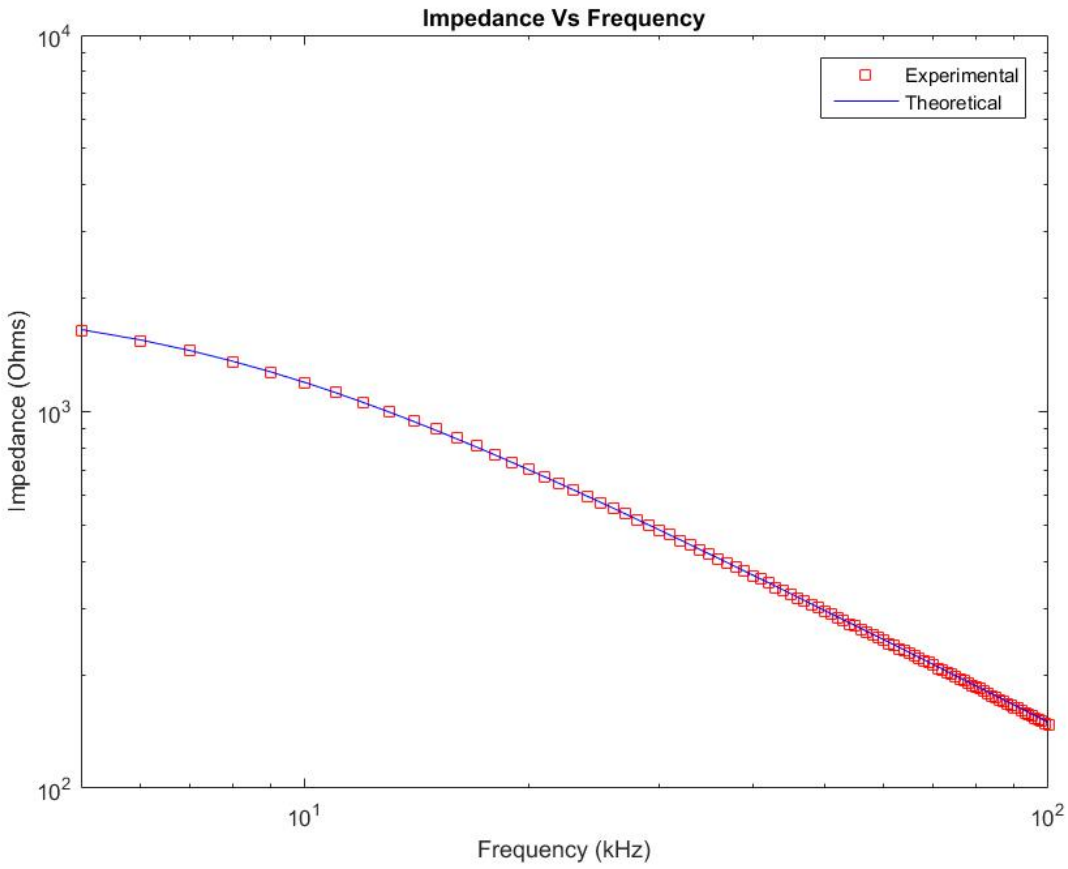

Figure 6.41: Impedance vs Frequency RC Parallel Load Resistor = 1980 Ω Capacitor = 10.61nF

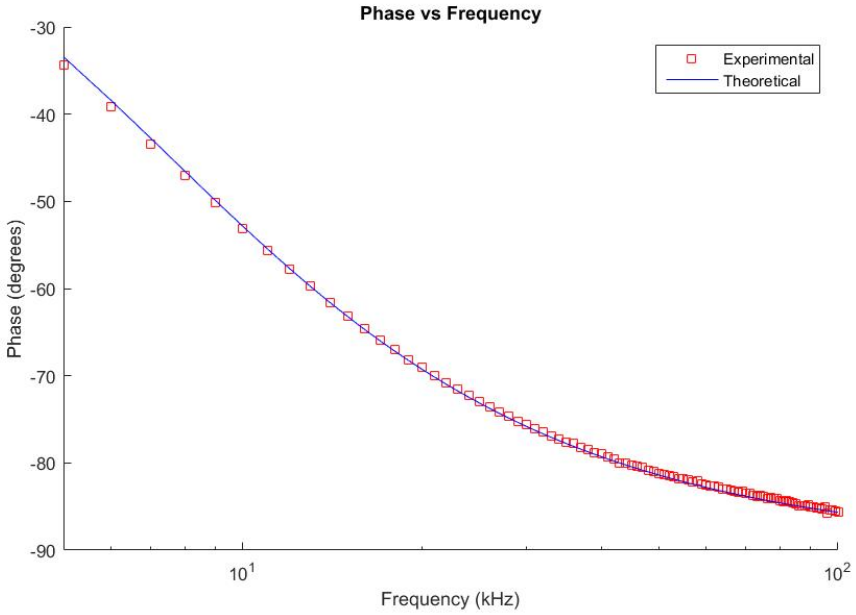

Figure 6.42: Phase vs Frequency RC Parallel Load Resistor = 1980 Ω Capacitor = 10.61nF

Figures 6.43 and 6.44 show the magnitude percent error and phase degree error respectively.

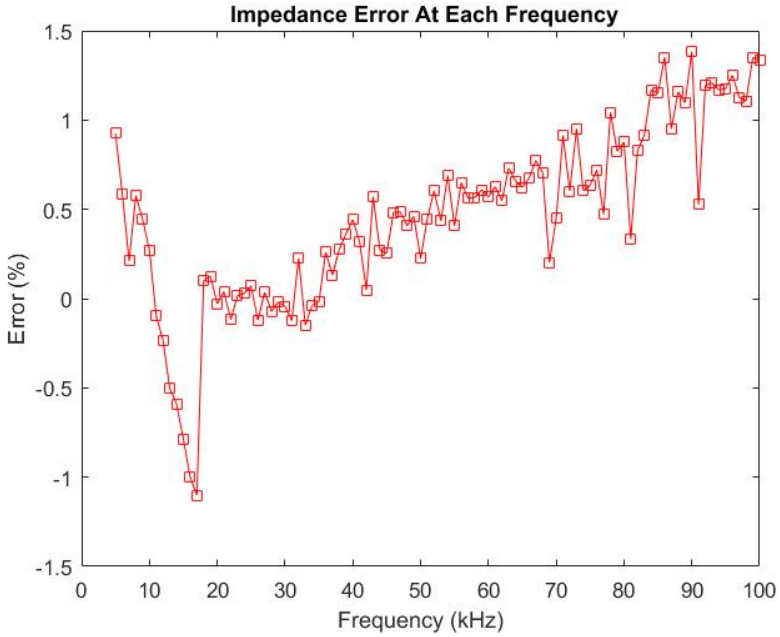

Figure 6.43: Impedance Error vs Frequency RC Parallel Load Resistor = 1980 Ω Capacitor = 10.61nF

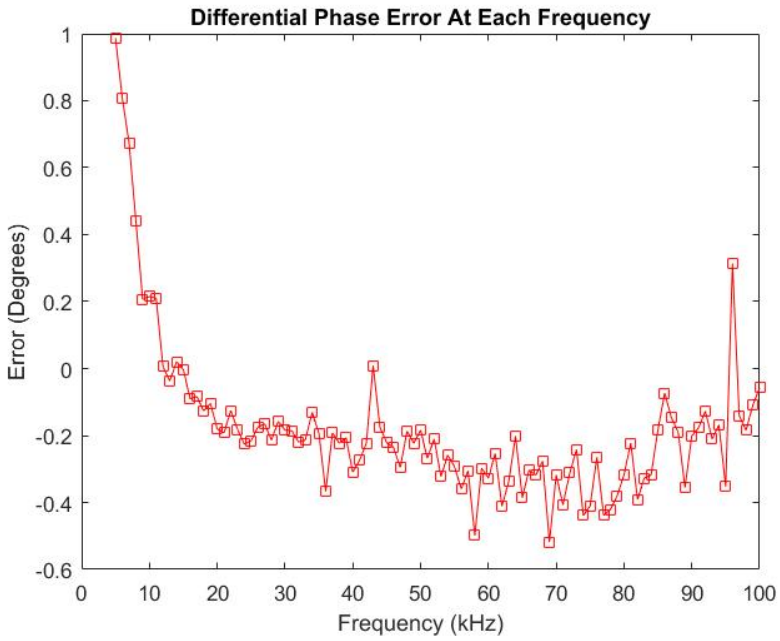

Figure 6.44: Phase Error vs Frequency RC Parallel Load Resistor = 1980 Ω Capacitor = 10.61nF

Table 6.9 and Figures 6.45 to 6.48 show the test results for the RC load of 2209 Ω resistor and 5.34nF capacitor. Table 6.9 shows the mean error and the standard deviation of the error for the data collected using this RC load.

Table 6.9: RC Parallel Load Resistor = 2209 Ω Capacitor = 5.34nF

Type	Impedance	Phase
Unit	%	Degrees
Mean	-0.1595	-0.2869
Standard Deviation	0.7306	0.4448

Figures 6.45 and 6.46 show the theoretical expectation and the measured data points. More specifically, the blue line represents the theoretical values and the red squares are acquired data points. It can be observed that the data points for both magnitude and phase are very close with the theoretical values.

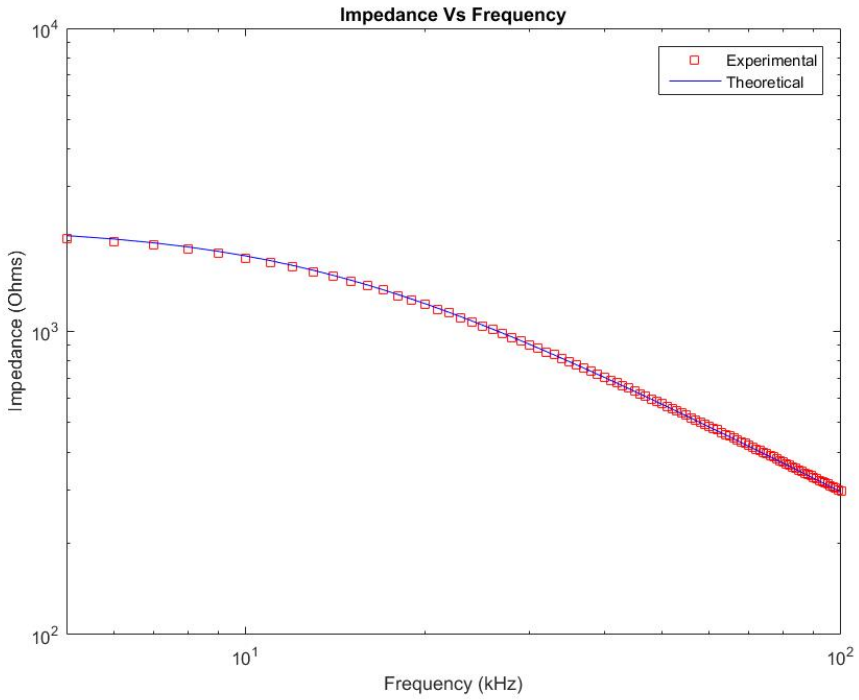

Figure 6.45: Impedance vs Frequency RC Parallel Load Resistor = 2209 Ω Capacitor = 5.34nF

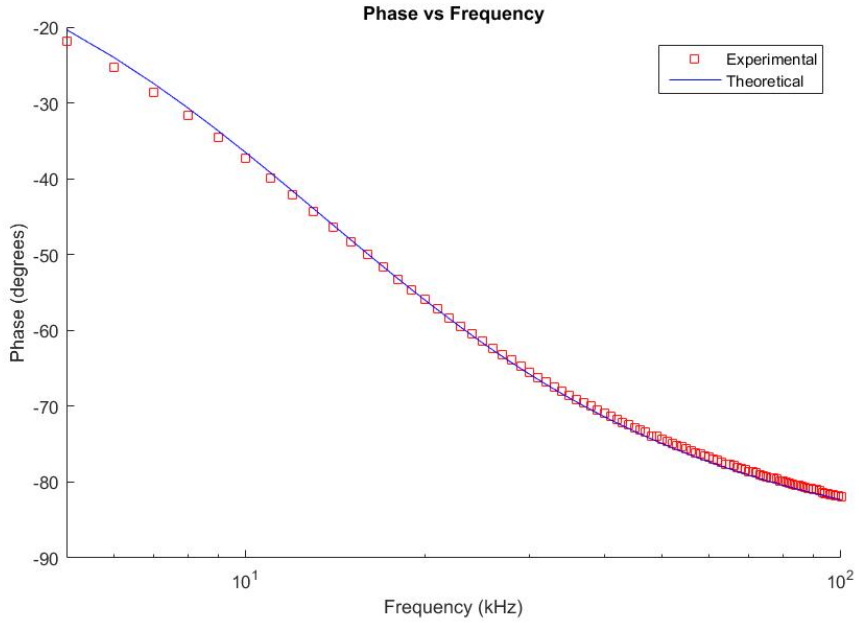

Figure 6.46: Phase vs Frequency RC Parallel Load Resistor = 2209 Ω Capacitor = 5.34nF

Figures 6.47 and 6.48 show the magnitude percent error and phase degree error respectively.

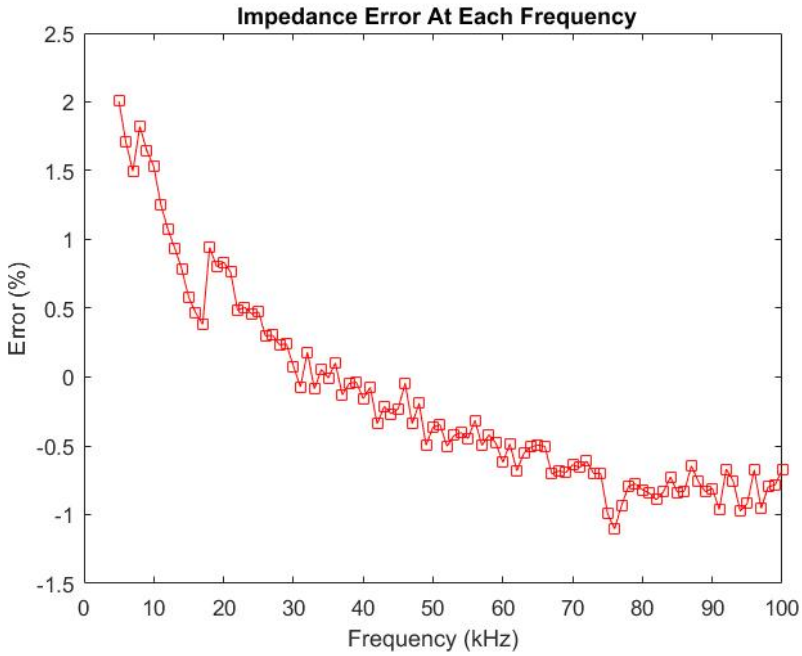

Figure 6.47: Impedance Error vs Frequency RC Parallel Load Resistor = 2209 Ω Capacitor = 5.34nF

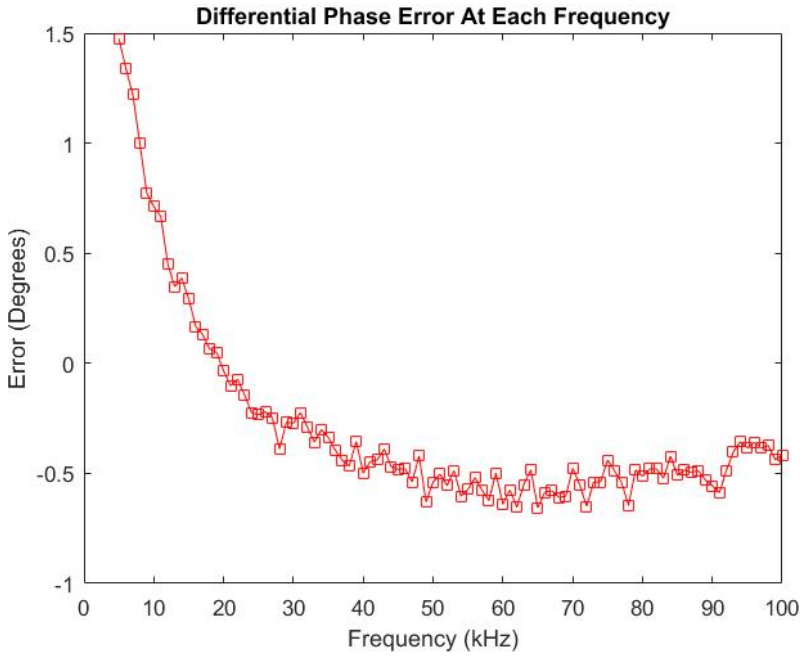

Figure 6.48: Phase Error vs Frequency RC Parallel Load Resistor =2209 Ohms Capacitor = 5.34nF

Table 6.10 and Figures 6.49 to 6.52 show the test results for the RC load of 2209 Ω resistor and 10.61nF capacitor. Table 6.10 shows the mean error and the standard deviation of the error for the data collected using this RC load.

Table 6.10: RC Parallel Load Resistor = 2209 Ω Capacitor = 10.61nF

Type	Impedance	Phase
Unit	%	Degrees
Mean	0.5042	-0.0879
Standard Deviation	0.5608	0.2398

Figures 6.49 and 6.50 show the theoretical expectation and the measured data points. More specifically, the blue line represents the theoretical values and the red squares are acquired data points. It can be observed that the data points for both magnitude and phase are very close with the theoretical values.

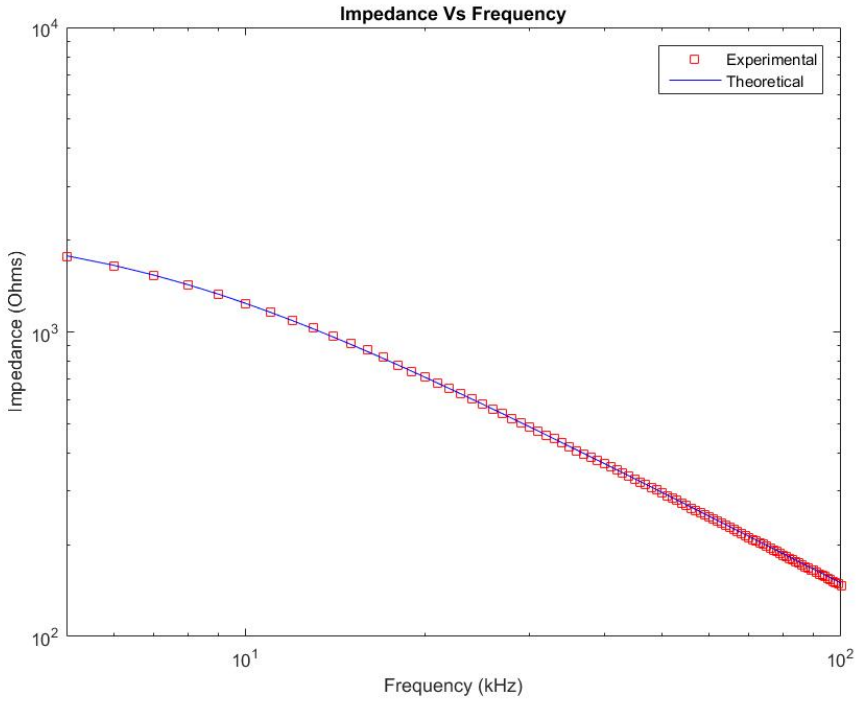

Figure 6.49: Impedance vs Frequency RC Parallel Load Resistor = 2209 Ω Capacitor = 10.61nF

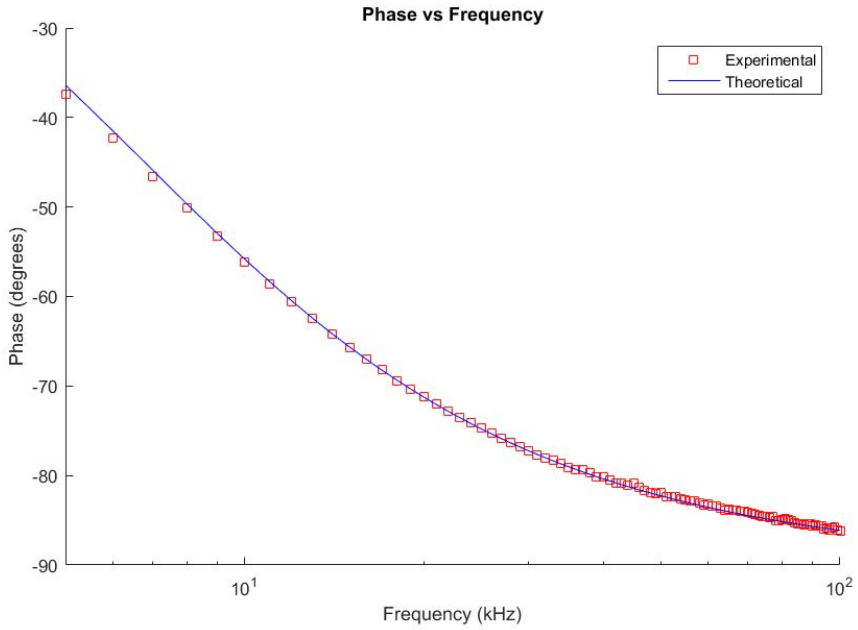

Figure 6.50: Phase vs Frequency RC Parallel Load Resistor = 2209 Ω Capacitor = 10.61nF

Figures 6.51 and 6.52 show the magnitude percent error and phase degree error respectively.

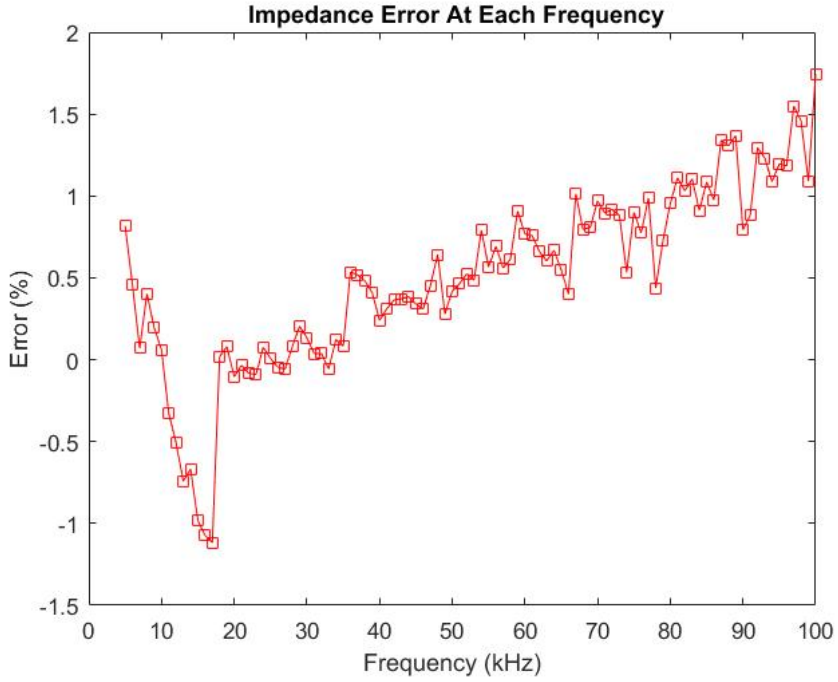

Figure 6.51: Impedance Error vs Frequency RC Parallel Load Resistor = 2209 Ω Capacitor = 10.61nF

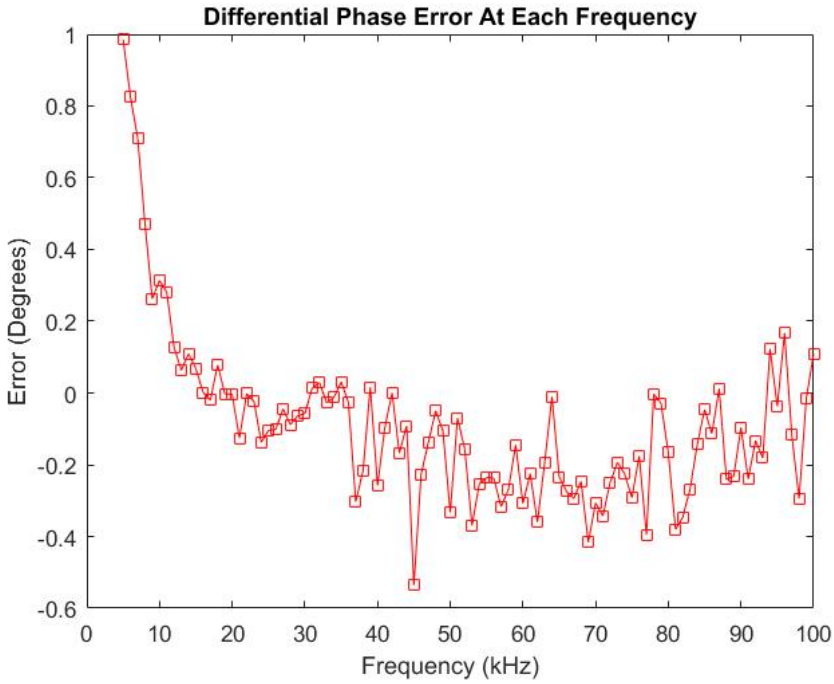

Figure 6.52: Phase Error vs Frequency RC Parallel Load Resistor =2209 Ω Capacitor = 10.61nF

Table 6.11 and Figures 6.53 to 6.56 show the test results for the RC load of 2947 Ω resistor and 5.34nF capacitor.

Table 6.11 shows the mean and the standard deviation of the error for the data collected using this RC load.

Table 6.11: RC Parallel Load Resistor = 2947 Ω Capacitor = 5.34nF

Type	**Impedance**	**Phase**
Unit	%	Degrees
Mean	-0.3202	-0.8005
Standard Deviation	0.3927	0.3699

Figures 6.53 and 6.54 show the magnitude in the frequency range sweep. The blue line represents the theoretical values and the red squares are acquired data points. It can be observed that the data points for both magnitude and phase are very close with the theoretical values.

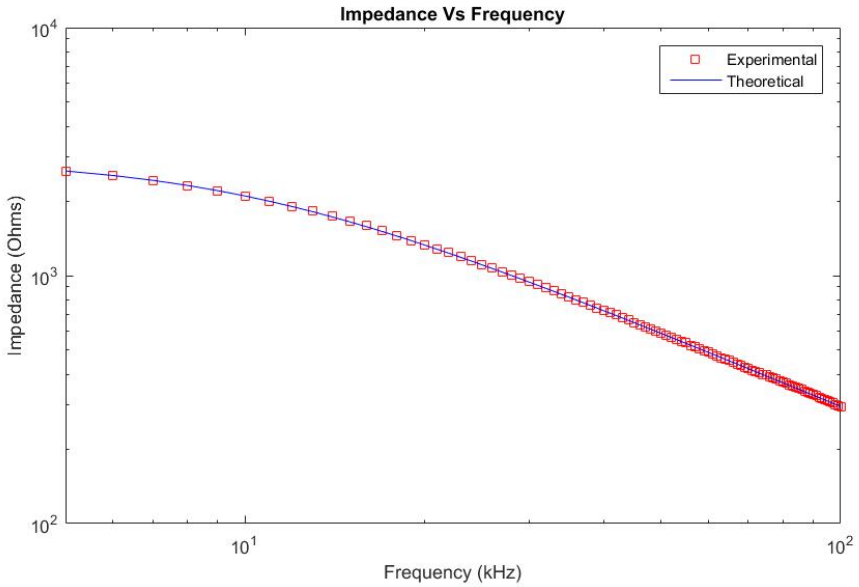

Figure 6.53: Impedance vs Frequency RC Parallel Load Resistor = 2947 Ω Capacitor = 5.34nF

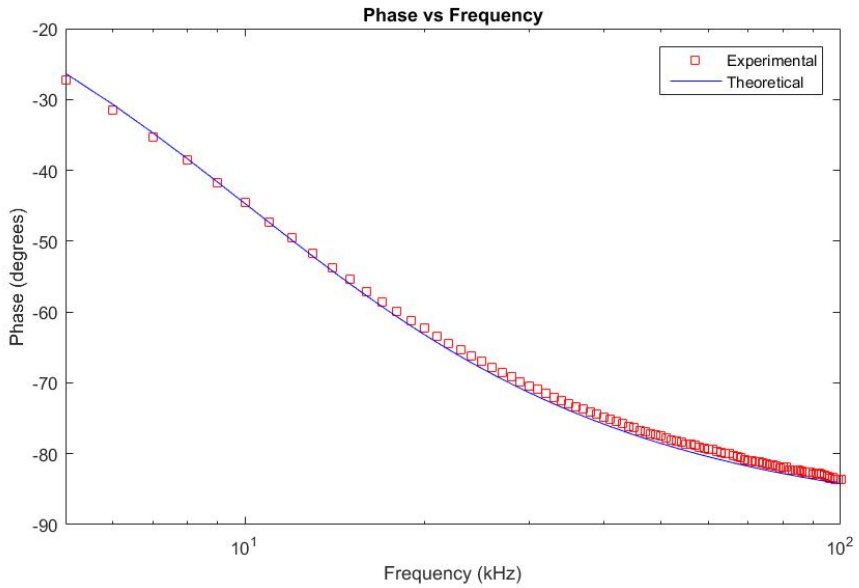

Figure 6.54: Phase vs Frequency RC Parallel Load Resistor = 2947 Ω Capacitor = 5.34nF

Figures 6.55 and 6.56 show the magnitude percent error and phase degree error respectively.

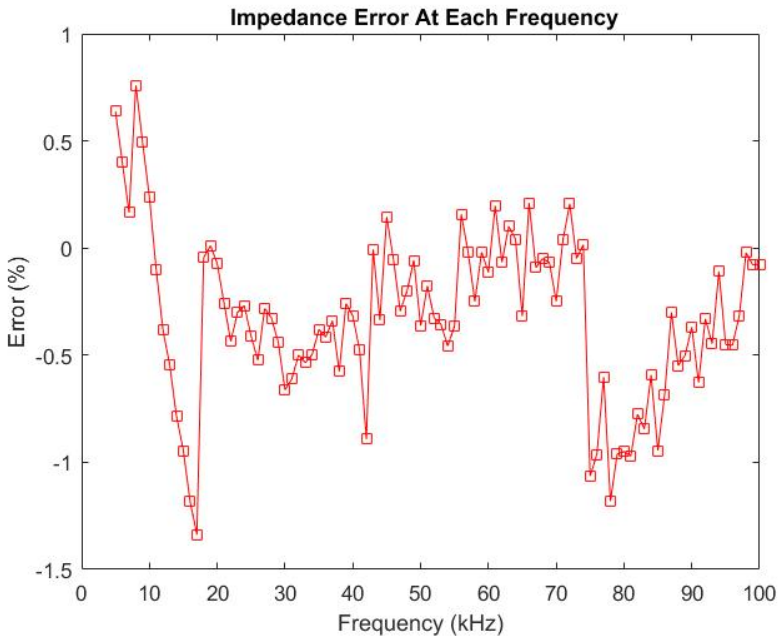

Figure 6.55: Impedance Error vs Frequency RC Parallel Load Resistor = 2947 Ω Capacitor = 5.34nF

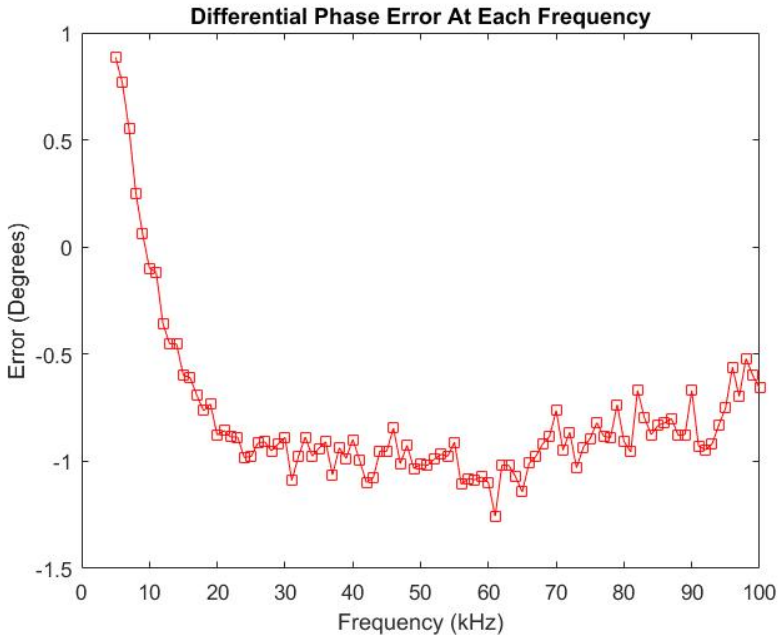

Figure 6.56: Phase Error vs Frequency RC Parallel Load Resistor = 2947 Ω Capacitor = 5.34nF

Table 6.12 and Figures 6.57 to 6.60 show the test results for the RC load of 2947 Ω resistor and 10.61nF capacitor.

Table 6.12 shows the mean and the standard deviation of the error for the data collected using this RC load.

Table 6.12: RC Parallel Load Resistor = 2947 Ω Capacitor = 10.61nF

Type	**Impedance**	**Phase**
Unit	%	Degrees
Mean	-0.7155	-0.6250
Standard Deviation	0.8178	0.2243

Figures 6.57 and 6.58 show the magnitude in the frequency range sweep. The blue line represents the theoretical values and the red squares are acquired data points. It can be observed that the data points for both magnitude and phase are very close with the theoretical values.

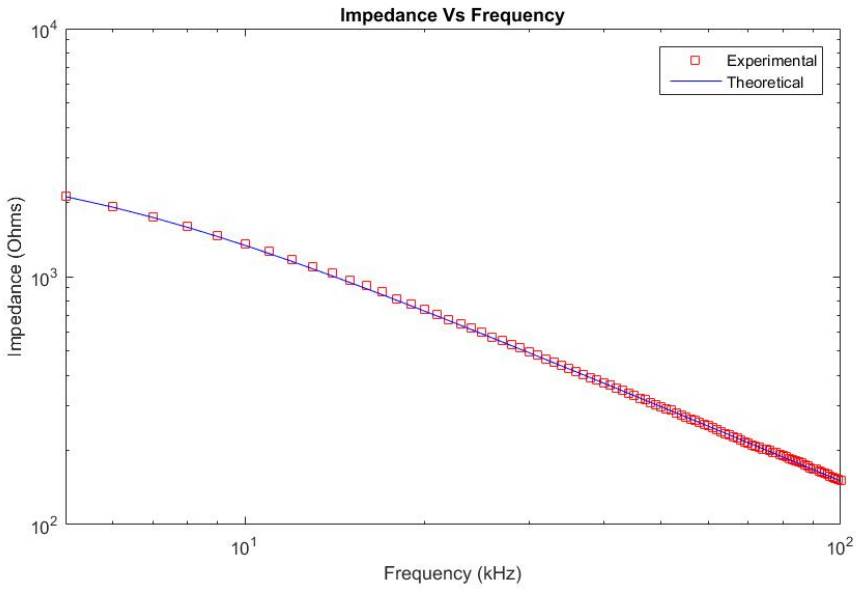

Figure 6.57: Impedance vs Frequency RC Parallel Load Resistor = 2947 Ω Capacitor = 10.61nF

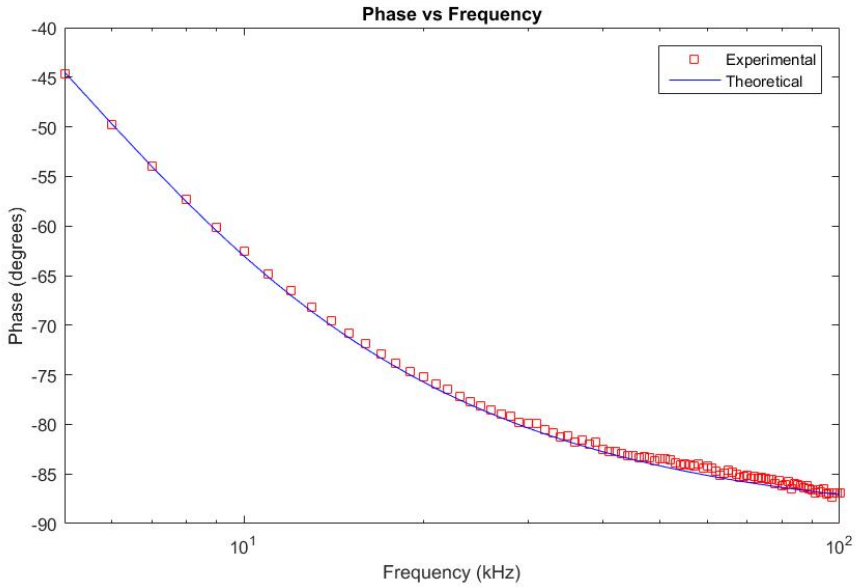

Figure 6.58: Phase vs Frequency RC Parallel Load Resistor = 2947 Ω Capacitor = 10.61nF

Figures 6.59 and 6.60 show the magnitude percent error and phase degree error respectively.

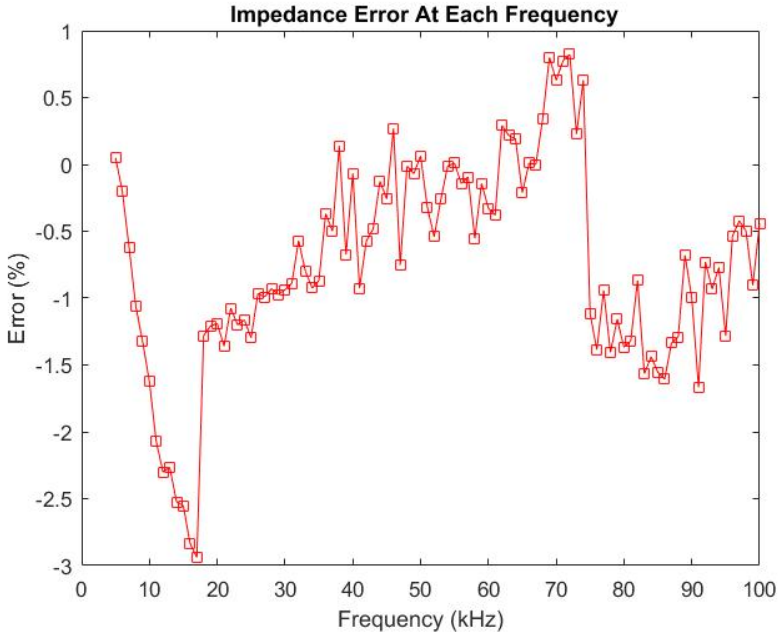

Figure 6.59: Impedance Error vs Frequency RC Parallel Load Resistor = 2947 Ω Capacitor = 10.61nF

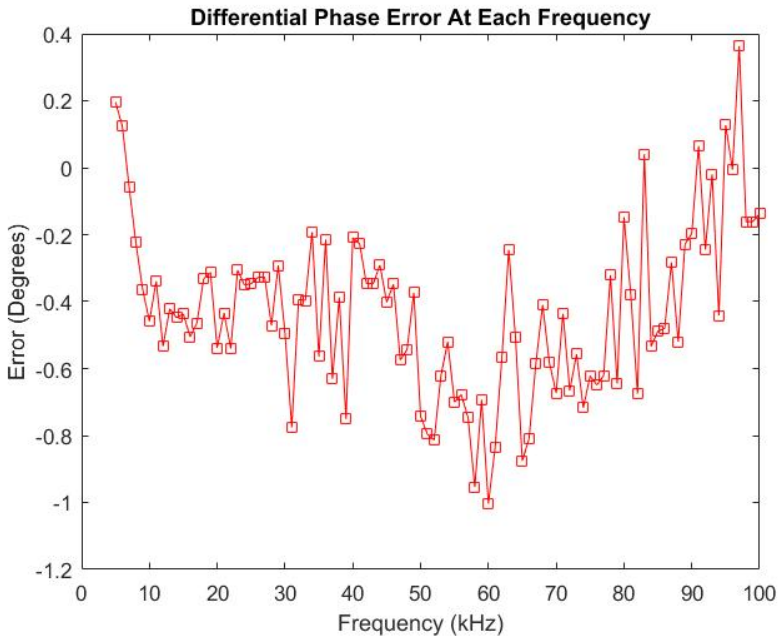

Figure 6.60: Phase Error vs Frequency RC Parallel Load Resistor = 2947 Ω Capacitor = 10.61nF

Table 6.13 and Figures 6.61 to 6.64 show the test results for the Resistor load of 2947 Ω resistor .

Table 6.13 shows the mean and the standard deviation of the error for the data collected using this Resistor load.

Table 6.13: Resistor Load Resistor = 3024 Ω

Type	**Impedance**	**Phase**
Unit	%	Degrees
Mean	-0.1455	-0.6580
Standard Deviation	0.0494	0.3089

Figures 6.61 and 6.62 show the magnitude in the frequency range sweep. The blue line represents the theoretical values and the red squares are acquired data points. It can be observed that the data points for both magnitude and phase are very close with the theoretical values.

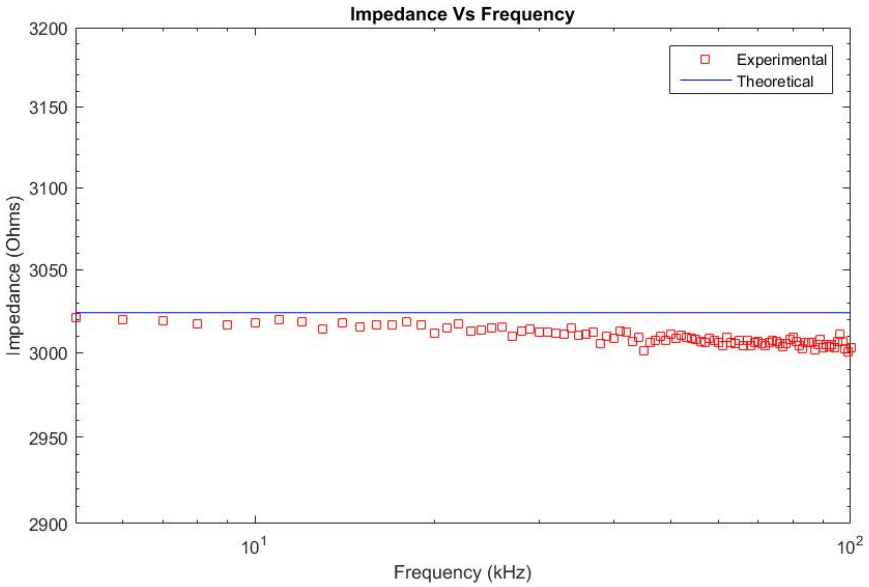

Figure 6.61: Impedance vs Frequency Resistor Parallel Load Resistor = 3024 Ω

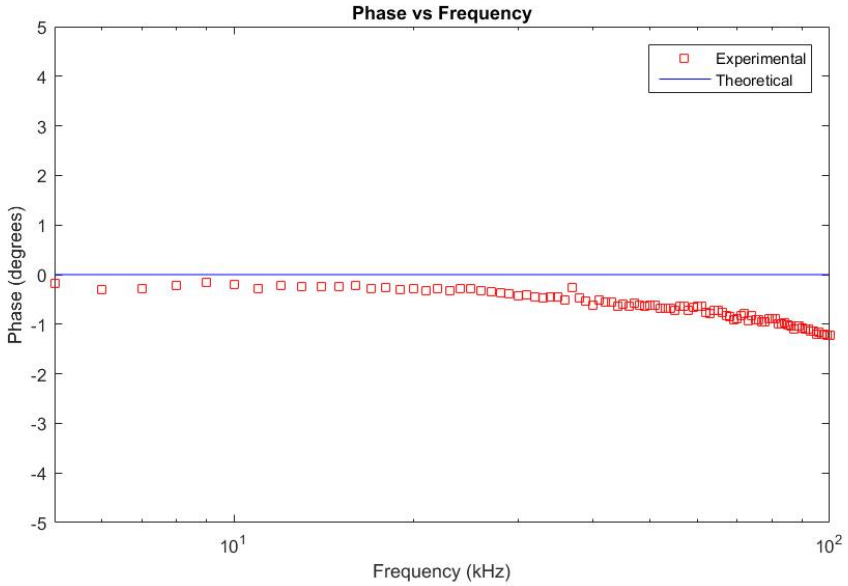

Figure 6.62: Phase vs Frequency Resistor Load Resistor = 3024 Ω

Figures 6.63 and 6.64 show the magnitude percent error and phase degree error respectively.

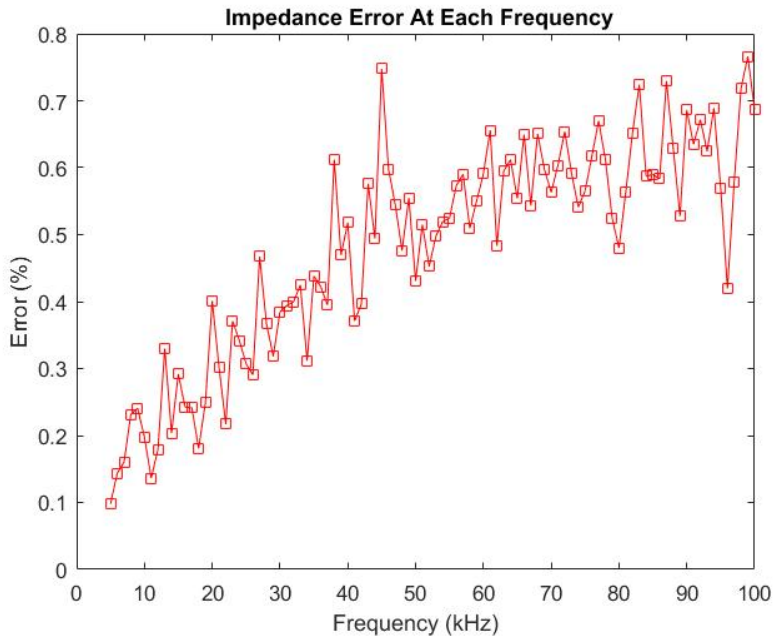

Figure 6.63: Impedance Error vs Frequency Resistor Load Resistor = 3024 Ω

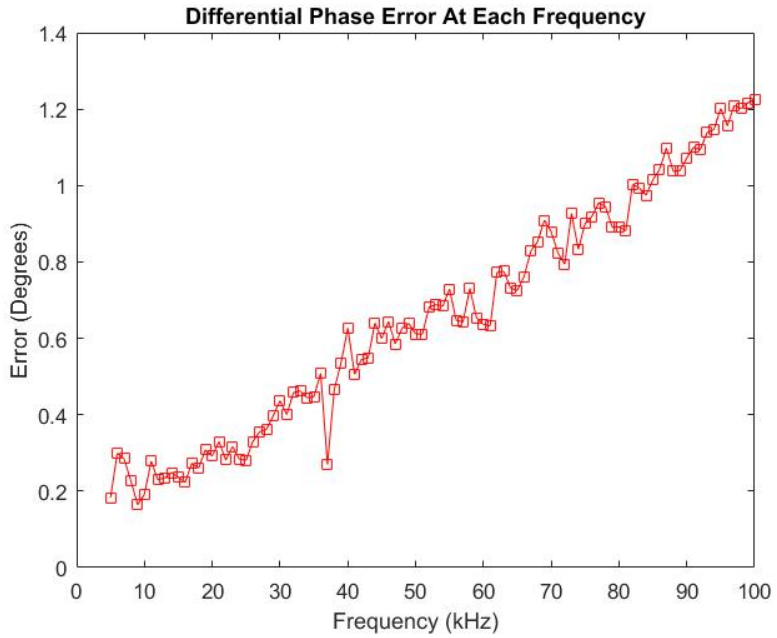

Figure 6.64: Phase Error vs Frequency Resistor Load Resistor = 3024 Ω

All of the mean and standard deviation of the error values for both magnitude and phase for each parallel load are shown in Table 6.14. In the last row, the average of mean and standard deviation errors of both the magnitude and phase are shown as well. Overall, the device meets the design targets determined in Section 3.

Table 6.14: Device Accuracy with Different Parallel Loads

Known Load	Magnitude (%)		Phase (°)	
	Mean	Std. Dev.	Mean	Std. Dev.
1797 Ω || 5.34 nF	-0.1500	0.7283	-0.2779	0.4948
1797 Ω || 10.6 nF	0.4463	0.4715	-0.1310	0.2520
1980 Ω || 5.34 nF	-0.1991	0.7565	-0.3264	0.4747
1980 Ω || 10.6 nF	0.4643	0.5130	-0.1757	0.2417
2209 Ω || 5.34 nF	-0.1595	0.7306	-0.2869	0.4448
2209 Ω || 10.6 nF	0.5042	0.5608	-0.0879	0.2398
905 Ω || 5.34 nF	0.1483	0.5040	0.4858	0.6329
905 Ω || 10.6 nF	-0.5830	0.3785	-1.703e-04	0.5513
2947 Ω || 5.34 nF	-0.3202	0.3927	-0.8005	0.3699
2947 Ω || 10.6 nF	-0.7155	0.8178	-0.6250	0.2243
3024 Ω	-0.1455	0.0494	-0.6580	0.3089
Average	0.06557	0.5366	-0.2621	0.3850

6.6 Human Testing

In order to ensure that the device is also applicable to human skin, the team measured skin impedance of four test subjects. Since the team was not able to acquire another skin impedance meter to compare, the team developed an electrical skin model to get a calculated data to compare with the measurements. In Section 6.5, only 1R1C circuit was used to test the functionality of the device, but for more accurate modeling, the team used a 2R1C circuit, as shown in Figure 6.65. Human testing results and impedance calculations with electrical skin model are shown in Figure 6.66 through Figure 6.69.

As expected, the magnitude of the human testing falls within the specified range targeted in Section 3. However, the phases were increasing as the frequency increased. First, the RC values were found to be 200-Ω resistor in series with a parallel RC with 15-nF capacitor and 1200-Ω resistor, as indicated in Figure 6.65. However, the electrical model these values is only successful at accurately modeling magnitude of skin impedance, but not at modeling phase. When tried with R1 of 200Ω, R2 of 3000Ω, and C1 of 50nF, the electrical model better fits with the actual phase. As a trade-off, the accuracy in modeling magnitude decreased. Moreover, concavities of graphs of actual skin impedance was not precisely modeled. It can be concluded that the electrical model can be modified in order to more accurately model the actual magnitude and phase skin impedance and also that there exist other factors that influence the behavior of phase.

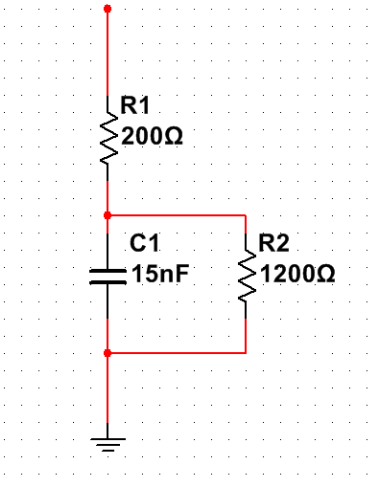

Figure 6.65: Electrical Model of Human Skin

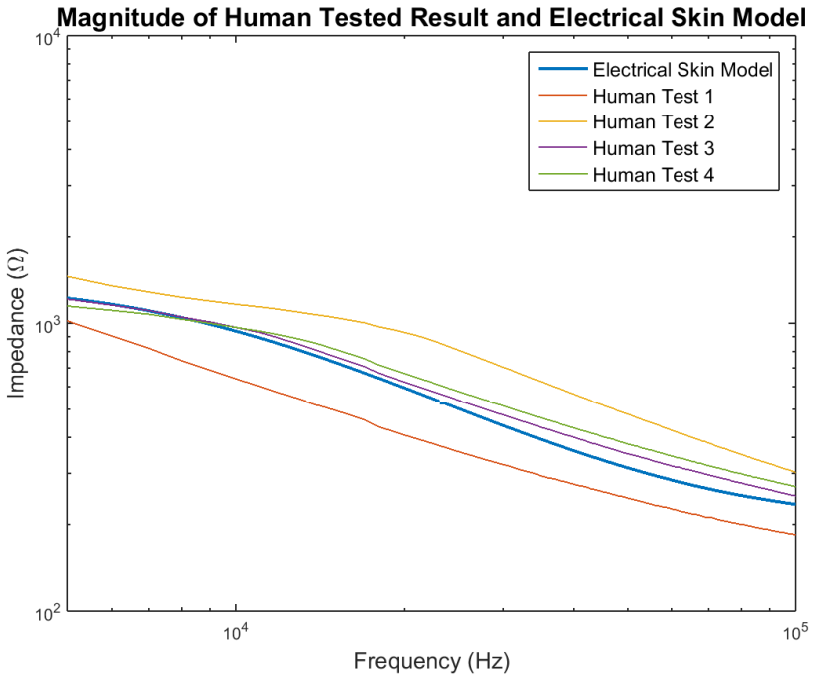

Figure 6.66: Magnitudes of Human Testing Result and Electrical Skin Model

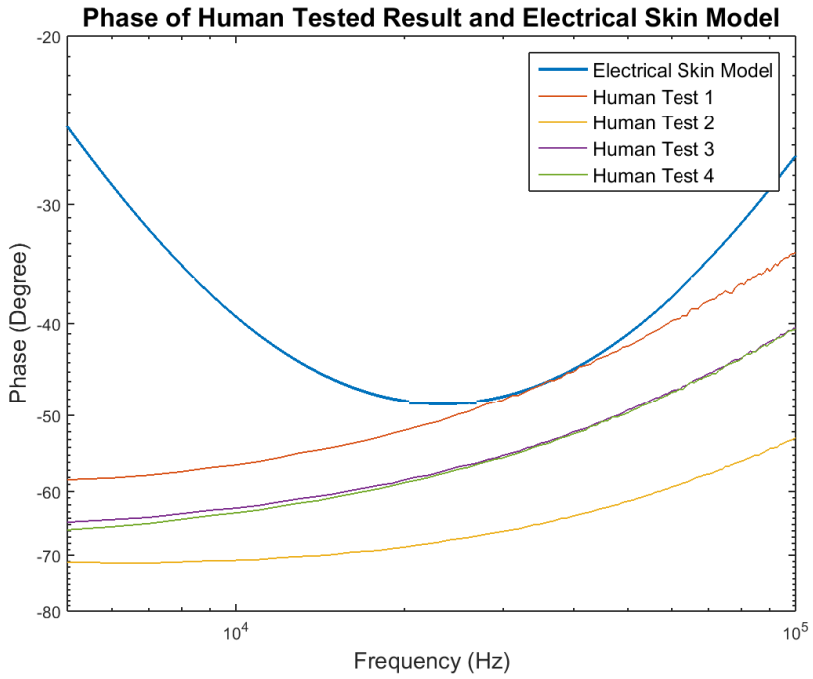

Figure 6.67: Phase of Human Testing Result and Electrical Skin Model

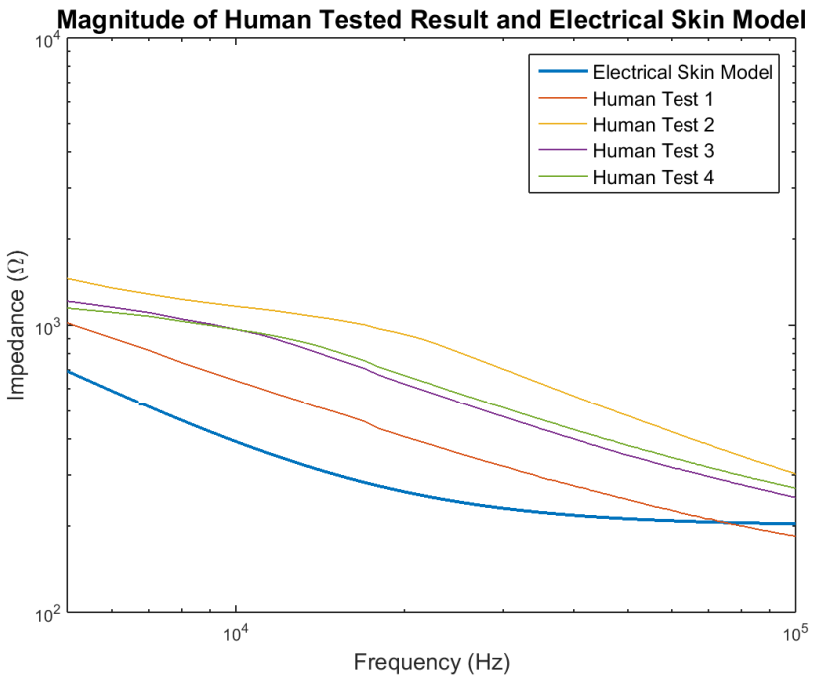

Figure 6.68: Magnitudes of Human Testing Result and Electrical Skin Model (R1 = 200Ω, R2 = 3000Ω, C1 = 50nF)

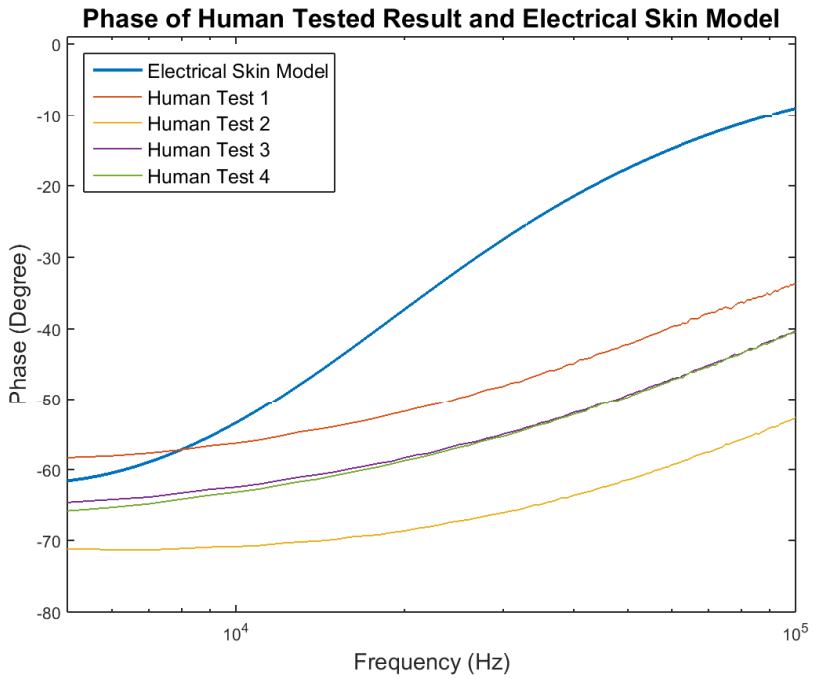

Figure 6.69: Phase of Human Testing Result and Electrical Skin Model (R1 = 200Ω, R2 = 3000Ω, C1 = 50nF)

7 Conclusion

In this project, we have designed and built a skin impedance spectrometer. The system was cored with an impedance analyzer IC, AD5933 and custom designed analog front end. IC control and data communication was done by ATMEGA328P. Collected data was sent through Bluetooth and processed in a PC using MATLAB. We also tested the system with pure electrical components that model skin impedance and actual human subject.

We were able to collect data from electrical skin model and human subject. For the system functionality test, 1R1C circuit was used to model human skin. The device was very successful at measuring impedance over all frequencies. The magnitude measurement was accurate with an average percentage error of 0.06557% and standard deviation of 0.5366, and the average phase error was -0.2621 degree with standard deviation of 0.3850. Overall, the design targets were successfully met.

When tested with human subject, a quite different trend in phase was observed. With 1R1C circuit, the phase decreased as frequency increased; however, for actual human skin, the phase increased with frequency. Therefore, the team found out an electrical skin model that fits into actual skin impedance data. The 2R1C circuit sufficiently modeled actual skin impedance but not most accurately. The electrical model can be modified to produce better model of human skin impedance.

Overall, the project was successful at accurately determining the impedance and phase of an unknown load to within the design specifications. Section 8 highlights future recommendations to further improve the skin impedance device.

8 Future Recommendations

In this section, the team reviews further work that can be done to improve our project.

8.1 AD5933

The AD5933 is a capable chip to measure skin impedance but it has its limitations. Because the chip is configured to output a voltage signal (with an DC offset) and receive a current signal, it required the team to design an Analog Front End that is compatible with it. Due to this, extra and somewhat redundant components are needed to convert the V_{ADI} to current then to voltage then to current again. Additionally, the AD5933 uses I2C to communicate. This protocol is open drain, which means it is always high (at 5V) until it is transmitting data. This is not the most power efficient communication protocol for a battery operated, low power project. A possible improvement would be to implement the AD5933 functionality in a microcontroller or a FPGA board. This would allow for a different, more power efficient, communication protocol to be used, and it would eliminate the need of both the AD5933 and a microcontroller.

8.2 AD8421

Another improvement to the team's design would be to upgrade the AD8421 chip for a rail-to-rail instrumentation amplifier with programmable gain. Therefore, all the necessary gain could be implemented in this stage. This would translate in better noise performance and lower error. Additionally, it would be beneficial to choose an instrumentation amplifier that does not require low input impedance in its voltage reference input pin for more simplicity of the design.

8.3 Patient Detection

One more improvement in the design can be automatic detection of a patient. A mechanism can be included in the design which detects whenever the electrodes are attached to the patient. The device can then measure skin impedance once it detects a body and shut off once the measurement is done.

8.4 Battery size

The circuit currently uses a 9V battery. Improvement can be made in this regard and a less bulky battery can be used. Further research needs to be done to make sure the battery delivers enough current and the boost regulator is suitable for the application. Ideas include using a appropriate battery and stabilizing the output voltage of the switching regulator.

8.5 Mobile Application

Further research can be done in the field of communication. Currently the device uses MATLAB and a computer to plot and display results. A mobile application which plots and

displays the data, maybe in real time, on the mobile screen can be developed to improve the project interface.

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Appendix

Appendix

A Data Sheets

A.1 AD5933

1 MSPS, 12-Bit Impedance Converter, Network Analyzer

Data Sheet **AD5933**

FEATURES

- Programmable output peak-to-peak excitation voltage to a maximum frequency of 100 kHz
- Programmable frequency sweep capability with serial I²C interface
- Frequency resolution of 27 bits (<0.1 Hz)
- Impedance measurement range from 1 kΩ to 10 MΩ
- Capable of measuring of 100 Ω to 1 kΩ with additional circuitry
- Internal temperature sensor (±2°C)
- Internal system clock option
- Phase measurement capability
- System accuracy of 0.5%
- 2.7 V to 5.5 V power supply operation
- Temperature range: −40°C to +125°C
- 16-lead SSOP package
- Qualified for automotive applications

APPLICATIONS

- Electrochemical analysis
- Bioelectrical impedance analysis
- Impedance spectroscopy
- Complex impedance measurement
- Corrosion monitoring and protection equipment
- Biomedical and automotive sensors
- Proximity sensing
- Nondestructive testing
- Material property analysis
- Fuel/battery cell condition monitoring

GENERAL DESCRIPTION

The AD5933 is a high precision impedance converter system solution that combines an on-board frequency generator with a 12-bit, 1 MSPS, analog-to-digital converter (ADC). The frequency generator allows an external complex impedance to be excited with a known frequency. The response signal from the impedance is sampled by the on-board ADC and a discrete Fourier transform (DFT) is processed by an on-board DSP engine. The DFT algorithm returns a real (R) and imaginary (I) data-word at each output frequency.

Once calibrated, the magnitude of the impedance and relative phase of the impedance at each frequency point along the sweep is easily calculated. This is done off chip using the real and imaginary register contents, which can be read from the serial I²C interface.

A similar device, also available from Analog Devices, Inc., is the AD5934, a 2.7 V to 5.5 V, 250 kSPS, 12-bit impedance converter, with an internal temperature sensor and is packaged in a 16-lead SSOP.

FUNCTIONAL BLOCK DIAGRAM

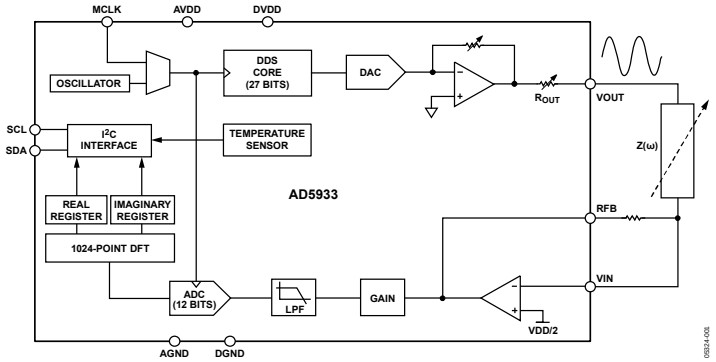

Figure 1.

Rev. E
Document Feedback

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9/05—Revision 0: Initial Version

SPECIFICATIONS

VDD = 3.3 V, MCLK = 16.776 MHz, 2 V p-p output excitation voltage @ 30 kHz, 200 kΩ connected between Pin 5 and Pin 6; feedback resistor = 200 kΩ connected between Pin 4 and Pin 5; PGA gain = ×1, unless otherwise noted.

Table 1.

		Y Version[1]			
Parameter	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
SYSTEM					
Impedance Range	1 K		10 M	Ω	100 Ω to 1 kΩ requires extra buffer circuitry, see the Measuring Small Impedances section
Total System Accuracy		0.5		%	2 V p-p output excitation voltage at 30 kHz, 200 kΩ connected between Pin 5 and Pin 6
System Impedance Error Drift		30		ppm/°C	
TRANSMIT STAGE					
Output Frequency Range[2]	1		100	kHz	
Output Frequency Resolution		0.1		Hz	<0.1 Hz resolution achievable using DDS techniques
MCLK Frequency			16.776	MHz	Maximum system clock frequency
Internal Oscillator Frequency[3]		16.776		MHz	Frequency of internal clock
Internal Oscillator Temperature Coefficient		30		ppm/°C	
TRANSMIT OUTPUT VOLTAGE					
Range 1					
AC Output Excitation Voltage[4]		1.98		V p-p	See Figure 4 for output voltage distribution
DC Bias[5]		1.48		V	DC bias of the ac excitation signal; see Figure 5
DC Output Impedance		200		Ω	T_A = 25°C
Short-Circuit Current to Ground at VOUT		±5.8		mA	T_A = 25°C
Range 2					
AC Output Excitation Voltage[4]		0.97		V p-p	See Figure 6
DC Bias[5]		0.76		V	DC bias of output excitation signal; see Figure 7
DC Output Impedance		2.4		kΩ	
Short-Circuit Current to Ground at VOUT		±0.25		mA	
Range 3					
AC Output Excitation Voltage[4]		0.383		V p-p	See Figure 8
DC Bias[5]		0.31		V	DC bias of output excitation signal; see Figure 9
DC Output Impedance		1		kΩ	
Short-Circuit Current to Ground at VOUT		±0.20		mA	
Range 4					
AC Output Excitation Voltage[4]		0.198		V p-p	See Figure 10
DC Bias[5]		0.173		V	DC bias of output excitation signal. See Figure 11
DC Output Impedance		600		Ω	
Short-Circuit Current to Ground at VOUT		±0.15		mA	
SYSTEM AC CHARACTERISTICS					
Signal-to-Noise Ratio		60		dB	
Total Harmonic Distortion		−52		dB	
Spurious-Free Dynamic Range					
Wide Band (0 MHz to 1 MHz)		−56		dB	
Narrow Band (±5 kHz)		−85		dB	

Parameter	Y Version[1] Min	Typ	Max	Unit	Test Conditions/Comments
RECEIVE STAGE					
Input Leakage Current		1		nA	To VIN pin
Input Capacitance[6]		0.01		pF	Pin capacitance between VIN and GND
Feedback Capacitance (C_{FB})		3		pF	Feedback capacitance around current-to-voltage amplifier; appears in parallel with feedback resistor
ANALOG-TO-DIGITAL CONVERTER[6]					
Resolution		12		Bits	
Sampling Rate		1		MSPS	ADC throughput rate
TEMPERATURE SENSOR					
Accuracy		±2.0		°C	−40°C to +125°C temperature range
Resolution		0.03		°C	
Temperature Conversion Time		800		µs	Conversion time of single temperature measurement
LOGIC INPUTS					
Input High Voltage (V_{IH})	0.7 × VDD				
Input Low Voltage (V_{IL})			0.3 × VDD		
Input Current[7]			1	µA	T_A = 25°C
Input Capacitance			7	pF	T_A = 25°C
POWER REQUIREMENTS					
VDD	2.7		5.5	V	
IDD (Normal Mode)		10	15	mA	VDD = 3.3 V
		17	25	mA	VDD = 5.5 V
IDD (Standby Mode)		11		mA	VDD = 3.3 V; see the Control Register (Register Address 0X80, Register Address 0X81) section
		16		mA	VDD = 5.5 V
IDD (Power-Down Mode)		0.7	5	µA	VDD = 3.3 V
		1	8	µA	VDD = 5.5 V

[1] Temperature range for Y version = −40°C to +125°C, typical at 25°C.
[2] The lower limit of the output excitation frequency can be lowered by scaling the clock supplied to the AD5933.
[3] Refer to Figure 14, Figure 15, and Figure 16 for the internal oscillator frequency distribution with temperature.
[4] The peak-to-peak value of the ac output excitation voltage scales with supply voltage according to the following formula:
Output Excitation Voltage (V p-p) = [2/3.3] × *VDD*
where *VDD* is the supply voltage.
[5] The dc bias value of the output excitation voltage scales with supply voltage according to the following formula:
Output Excitation Bias Voltage (V) = [2/3.3] × *VDD*
where *VDD* is the supply voltage.
[6] Guaranteed by design or characterization, not production tested. Input capacitance at the VOUT pin is equal to pin capacitance divided by open-loop gain of current-to-voltage amplifier.
[7] The accumulation of the currents into Pin 8, Pin 15, and Pin 16.

I²C SERIAL INTERFACE TIMING CHARACTERISTICS

VDD = 2.7 V to 5.5 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.[1]

Table 2.

Parameter[2]	Limit at T_{MIN}, T_{MAX}	Unit	Description
f_{SCL}	400	kHz max	SCL clock frequency
t_1	2.5	µs min	SCL cycle time
t_2	0.6	µs min	t_{HIGH}, SCL high time
t_3	1.3	µs min	t_{LOW}, SCL low time
t_4	0.6	µs min	$t_{HD, STA}$, start/repeated start condition hold time
t_5	100	ns min	$t_{SU, DAT}$, data setup time
t_6[3]	0.9	µs max	$t_{HD, DAT}$, data hold time
	0	µs min	$t_{HD, DAT}$, data hold time
t_7	0.6	µs min	$t_{SU, STA}$, setup time for repeated start
t_8	0.6	µs min	$t_{SU, STO}$, stop condition setup time
t_9	1.3	µs min	t_{BUF}, bus free time between a stop and a start condition
t_{10}	300	ns max	t_F, rise time of SDA when transmitting
	0	ns min	t_R, rise time of SCL and SDA when receiving (CMOS compatible)
t_{11}	300	ns max	t_F, fall time of SCL and SDA when transmitting
	0	ns min	t_F, fall time of SDA when receiving (CMOS compatible)
	250	ns max	t_F, fall time of SDA when receiving
	20 + 0.1 C_b[4]	ns min	t_F, fall time of SCL and SDA when transmitting
C_b	400	pF max	Capacitive load for each bus line

[1] See Figure 2.
[2] Guaranteed by design and characterization, not production tested.
[3] A master device must provide a hold time of at least 300 ns for the SDA signal (referred to $V_{IH\ MIN}$ of the SCL signal) to bridge the undefined falling edge of SCL.
[4] C_b is the total capacitance of one bus line in picofarads. Note that t_R and t_F are measured between 0.3 VDD and 0.7 VDD.

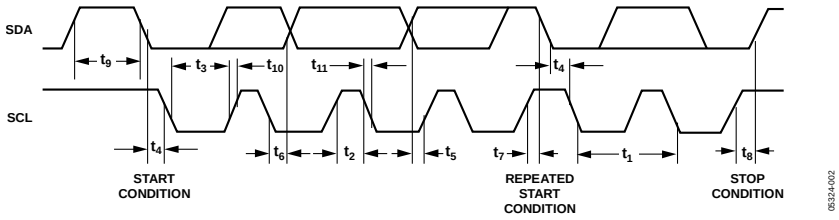

Figure 2. I²C Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
DVDD to GND	−0.3 V to +7.0 V
AVDD1 to GND	−0.3 V to +7.0 V
AVDD2 to GND	−0.3 V to +7.0 V
SDA/SCL to GND	−0.3 V to VDD + 0.3 V
VOUT to GND	−0.3 V to VDD + 0.3 V
VIN to GND	−0.3 V to VDD + 0.3 V
MCLK to GND	−0.3 V to VDD + 0.3 V
Operating Temperature Range	
Extended Industrial (Y Grade)	−40°C to +125°C
Storage Temperature Range	−65°C to +160°C
Maximum Junction Temperature	150°C
SSOP Package, Thermal Impedance	
θ_{JA}	139°C/W
θ_{JC}	136°C/W
Reflow Soldering (Pb-Free)	
Peak Temperature	260°C
Time at Peak Temperature	10 sec to 40 sec

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND DESCRIPTIONS

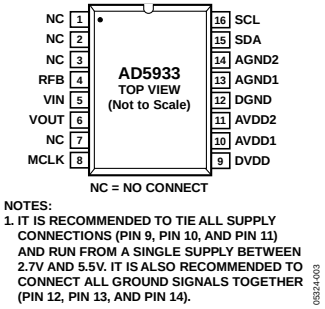

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 3, 7	NC	No Connect.
4	RFB	External Feedback Resistor. Connected from Pin 4 to Pin 5 and used to set the gain of the current-to-voltage amplifier on the receive side.
5	VIN	Input to Receive Transimpedance Amplifier. Presents a virtual earth voltage of VDD/2.
6	VOUT	Excitation Voltage Signal Output.
8	MCLK	The master clock for the system is supplied by the user.
9	DVDD	Digital Supply Voltage.
10	AVDD1	Analog Supply Voltage 1.
11	AVDD2	Analog Supply Voltage 2.
12	DGND	Digital Ground.
13	AGND1	Analog Ground 1.
14	AGND2	Analog Ground 2.
15	SDA	I^2C Data Input. Open-drain pins requiring 10 kΩ pull-up resistors to VDD.
16	SCL	I^2C Clock Input. Open-drain pins requiring 10 kΩ pull-up resistors to VDD.

TYPICAL PERFORMANCE CHARACTERISTICS

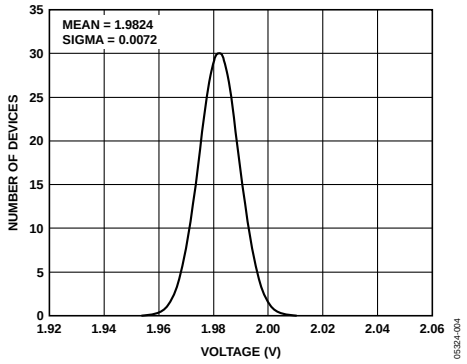

Figure 4. Range 1 Output Excitation Voltage Distribution, VDD = 3.3 V

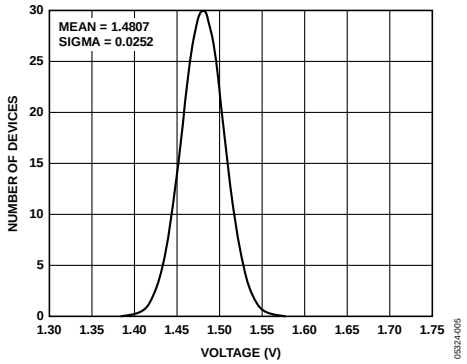

Figure 5. Range 1 DC Bias Distribution, VDD = 3.3 V

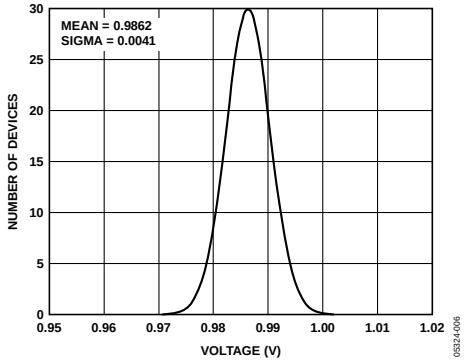

Figure 6. Range 2 Output Excitation Voltage Distribution, VDD = 3.3 V

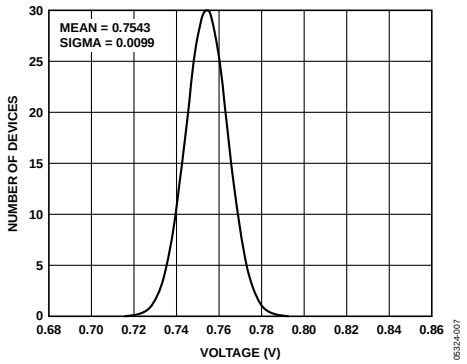

Figure 7. Range 2 DC Bias Distribution, VDD = 3.3 V

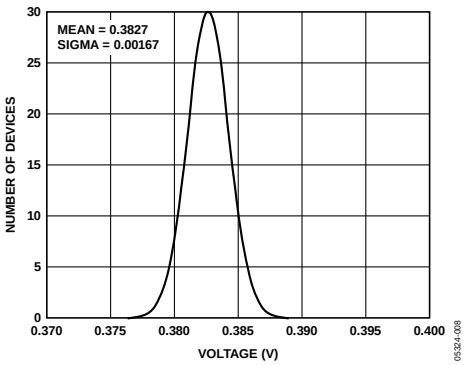

Figure 8. Range 3 Output Excitation Voltage Distribution, VDD = 3.3 V

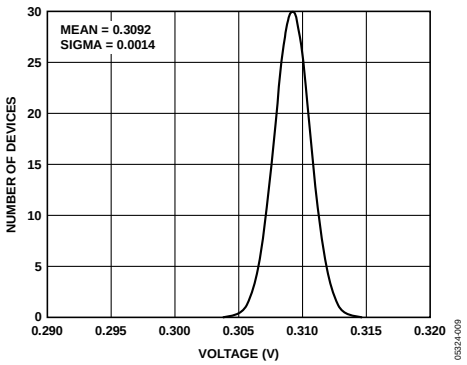

Figure 9. Range 3 DC Bias Distribution, VDD = 3.3 V

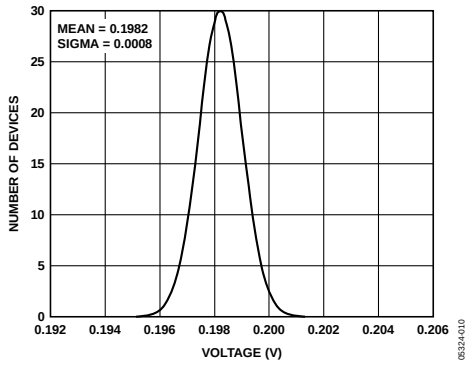

Figure 10. Range 4 Output Excitation Voltage Distribution, VDD = 3.3 V

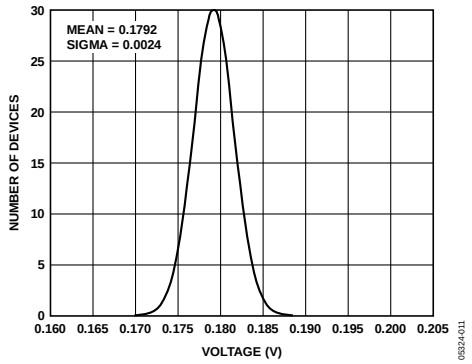

Figure 11. Range 4 DC Bias Distribution, VDD = 3.3 V

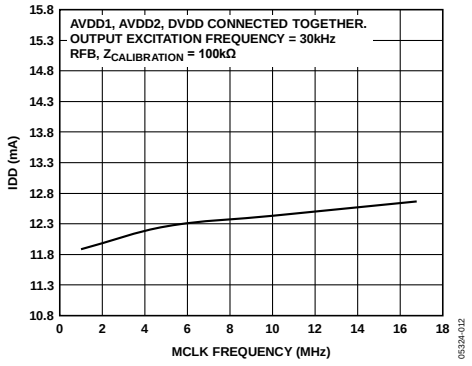

Figure 12. Typical Supply Current vs. MCLK Frequency

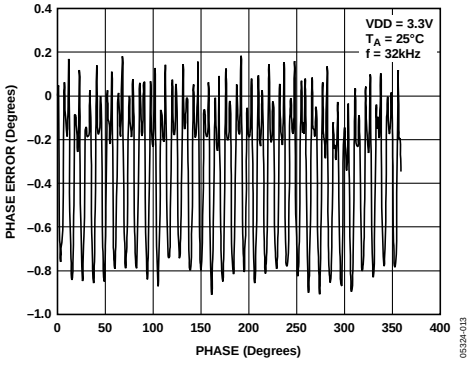

Figure 13. Typical Phase Error

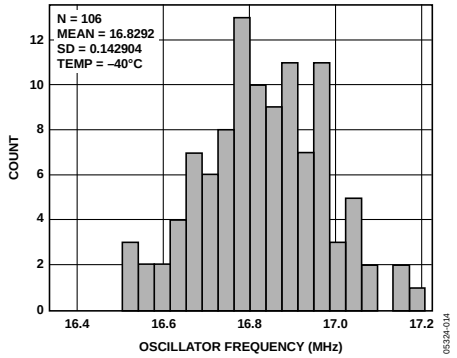

Figure 14. Frequency Distribution of Internal Oscillator at –40°C

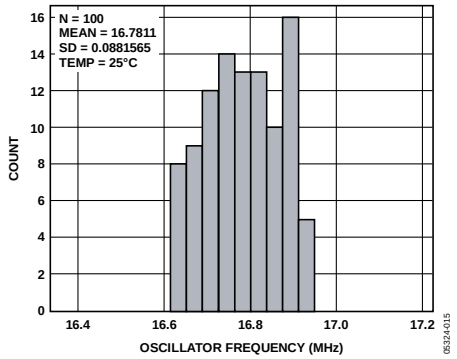

Figure 15. Frequency Distribution of Internal Oscillator at 25°C

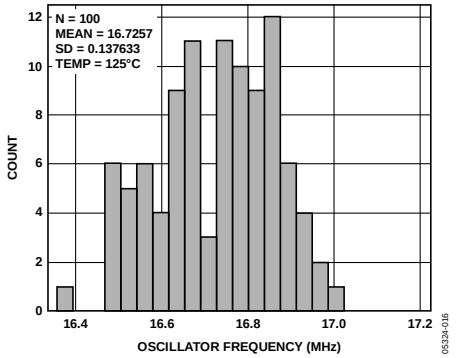

Figure 16. Frequency Distribution of Internal Oscillator at 125°C

TERMINOLOGY

Total System Accuracy
The AD5933 can accurately measure a range of impedance values to less than 0.5% of the correct impedance value for supply voltages between 2.7 V to 5.5 V.

Spurious-Free Dynamic Range (SFDR)
Along with the frequency of interest, harmonics of the fundamental frequency and images of these frequencies are present at the output of a DDS device. The spurious-free dynamic range refers to the largest spur or harmonic present in the band of interest. The wideband SFDR gives the magnitude of the largest harmonic or spur relative to the magnitude of the fundamental frequency in the 0 Hz to Nyquist bandwidth. The narrow-band SFDR gives the attenuation of the largest spur or harmonic in a bandwidth of ±200 kHz, about the fundamental frequency.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency. The value for SNR is expressed in decibels.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of harmonics to the fundamental, where V1 is the rms amplitude of the fundamental and V2, V3, V4, V5, and V6 are the rms amplitudes of the second through the sixth harmonics. For the AD5933, THD is defined as

$$THD\ (\text{dB}) = 20 \log \frac{\sqrt{V2^2 + V3^2 + V4^2 + V5^2\ V6^2}}{V1}$$

SYSTEM DESCRIPTION

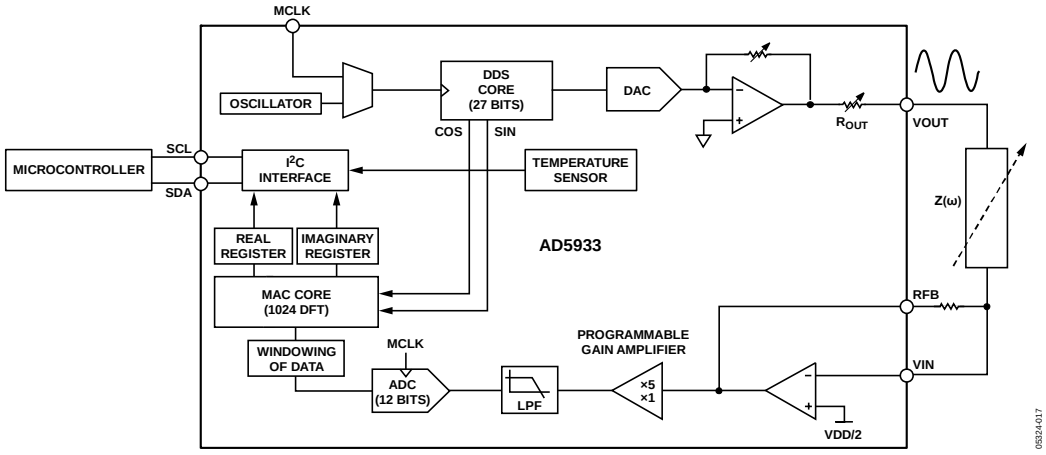

Figure 17. Block Overview

The AD5933 is a high precision impedance converter system solution that combines an on-board frequency generator with a 12-bit, 1 MSPS ADC. The frequency generator allows an external complex impedance to be excited with a known frequency. The response signal from the impedance is sampled by the on-board ADC and DFT processed by an on-board DSP engine. The DFT algorithm returns both a real (R) and imaginary (I) data-word at each frequency point along the sweep. The impedance magnitude and phase are easily calculated using the following equations:

$$Magnitude = \sqrt{R^2 + I^2}$$

$$Phase = \tan^{-1}(I/R)$$

To characterize an impedance profile Z(ω), generally a frequency sweep is required, like that shown in Figure 18.

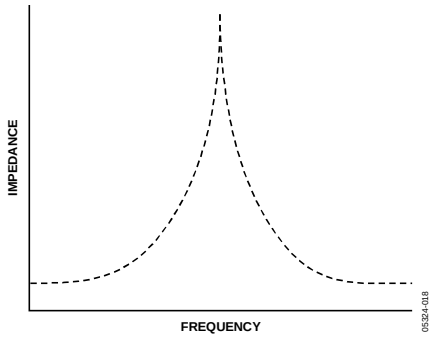

Figure 18. Impedance vs. Frequency Profile

The AD5933 permits the user to perform a frequency sweep with a user-defined start frequency, frequency resolution, and number of points in the sweep. In addition, the device allows the user to program the peak-to-peak value of the output sinusoidal signal as an excitation to the external unknown impedance connected between the VOUT and VIN pins.

Table 5 gives the four possible output peak-to-peak voltages and the corresponding dc bias levels for each range for 3.3 V. These values are ratiometric with VDD. So for a 5 V supply

$$Output\ Excitation\ Voltage\ for\ Range\ 1 = 1.98 \times \frac{5.0}{3.3} = 3\ \text{V p-p}$$

$$Output\ DC\ Bias\ Voltage\ for\ Range\ 1 = 1.48 \times \frac{5.0}{3.3} = 2.24\ \text{V p-p}$$

Table 5. Voltage Levels Respective Bias Levels for 3.3 V

Range	Output Excitation Voltage Amplitude	Output DC Bias Level
1	1.98 V p-p	1.48 V
2	0.97 V p-p	0.76 V
3	383 mV p-p	0.31 V
4	198 mV p-p	0.173 V

The excitation signal for the transmit stage is provided on-chip using DDS techniques that permit subhertz resolution. The receive stage receives the input signal current from the unknown impedance, performs signal processing, and digitizes the result. The clock for the DDS is generated from either an external reference clock, which is provided by the user at MCLK, or by the internal oscillator. The clock for the DDS is determined by the status of Bit D3 in the control register (see Register Address 0x81 in the Register Map section).

TRANSMIT STAGE

As shown in Figure 19, the transmit stage of the AD5933 is made up of a 27-bit phase accumulator DDS core that provides the output excitation signal at a particular frequency. The input to the phase accumulator is taken from the contents of the start frequency register (see Register Address 0x82, Register Address 0x83, and Register Address 0x84). Although the phase accumulator offers 27 bits of resolution, the start frequency register has the three most significant bits (MSBs) set to 0 internally; therefore, the user has the ability to program only the lower 24 bits of the start frequency register.

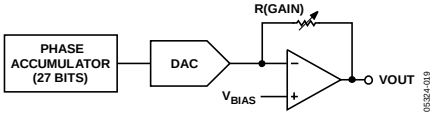

Figure 19. Transmit Stage

The AD5933 offers a frequency resolution programmable by the user down to 0.1 Hz. The frequency resolution is programmed via a 24-bit word loaded serially over the I^2C interface to the frequency increment register.

The frequency sweep is fully described by the programming of three parameters: the start frequency, the frequency increment, and the number of increments.

Start Frequency

This is a 24-bit word that is programmed to the on-board RAM at Register Address 0x82, Register Address 0x83, and Register Address 0x84 (see the Register Map section). The required code loaded to the start frequency register is the result of the formula shown in Equation 1, based on the master clock frequency and the required start frequency output from the DDS.

$$Start\ Frequency\ Code = \left(\frac{Required\ Output\ Start\ Frequency}{\left(\frac{MCLK}{4} \right)} \right) \times 2^{27} \quad (1)$$

For example, if the user requires the sweep to begin at 30 kHz and has a 16 MHz clock signal connected to MCLK, the code that needs to be programmed is given by

$$Start\ Frequency\ Code = \left(\frac{30\ \text{kHz}}{\left(\frac{16\ \text{MHz}}{4} \right)} \right) \times 2^{27} \equiv 0\text{x}0\text{F}5\text{C}28$$

The user programs the value of 0x0F to Register Address 0x82, the value of 0x5C to Register Address 0x83, and the value of 0x28 to Register Address 0x84.

Frequency Increment

This is a 24-bit word that is programmed to the on-board RAM at Register Address 0x85, Register Address 0x86, and Register Address 0x87 (see the Register Map). The required code loaded to the frequency increment register is the result of the formula shown in Equation 2, based on the master clock frequency and the required increment frequency output from the DDS.

$$Frequency\ Increment\ Code = \left(\frac{Required\ Frequency\ Increment}{\left(\frac{MCLK}{4} \right)} \right) \times 2^{27} \quad (2)$$

For example, if the user requires the sweep to have a resolution of 10 Hz and has a 16 MHz clock signal connected to MCLK, the code that needs to be programmed is given by

$$Frequency\ Increment\ Code = \left(\frac{10\ \text{Hz}}{\left(\frac{16\ \text{MHz}}{4} \right)} \right) \equiv 0\text{x}00014\text{F}$$

The user programs the value of 0x00 to Register Address 0x85, the value of 0x01 to Register Address 0x86, and the value of 0x4F to Register Address 0x87.

Number of Increments

This is a 9-bit word that represents the number of frequency points in the sweep. The number is programmed to the on-board RAM at Register Address 0x88 and Register Address 0x89 (see the Register Map section). The maximum number of points that can be programmed is 511.

For example, if the sweep needs 150 points, the user programs the value of 0x00 to Register Address 0x88 and the value of 0x96 to Register Address 0x89.

Once the three parameter values have been programmed, the sweep is initiated by issuing a start frequency sweep command to the control register at Register Address 0x80 and Register Address 0x81 (see the Register Map section). Bit D2 in the status register (Register Address 0x8F) indicates the completion of the frequency measurement for each sweep point. Incrementing to the next frequency sweep point is under the control of the user. The measured result is stored in the two register groups that follow: 0x94, 0x95 (real data) and 0x96, 0x97 (imaginary data) that should be read before issuing an increment frequency command to the control register to move to the next sweep point. There is the facility to repeat the current frequency point measurement by issuing a repeat frequency command to the control register. This has the benefit of allowing the user to average successive readings. When the frequency sweep has completed all frequency points, Bit D3 in the status register is set, indicating completion of the sweep. Once this bit is set, further increments are disabled.

FREQUENCY SWEEP COMMAND SEQUENCE

The following sequence must be followed to implement a frequency sweep:

1. Enter standby mode. Prior to issuing a start frequency sweep command, the device must be placed in a standby mode by issuing an enter standby mode command to the control register (Register Address 0x80 and Register Address 0x81). In this mode, the VOUT and VIN pins are connected internally to ground so there is no dc bias across the external impedance or between the impedance and ground.
2. Enter initialize mode. In general, high Q complex circuits require a long time to reach steady state. To facilitate the measurement of such impedances, this mode allows the user full control of the settling time requirement before entering start frequency sweep mode where the impedance measurement takes place.
   An initialize with a start frequency command to the control register enters initialize mode. In this mode the impedance is excited with the programmed start frequency, but no measurement takes place. The user times out the required settling time before issuing a start frequency sweep command to the control register to enter the start frequency sweep mode.
3. Enter start frequency sweep mode. The user enters this mode by issuing a start frequency sweep command to the control register. In this mode, the ADC starts measuring after the programmed number of settling time cycles has elapsed. The user can program an integer number of output frequency cycles (settling time cycles) to Register Address 0x8A and Register Address 0x8B before beginning the measurement at each frequency point (see Figure 28).

The DDS output signal is passed through a programmable gain stage to generate the four ranges of peak-to-peak output excitation signals listed in Table 5. The peak-to-peak output excitation voltage is selected by setting Bit D10 and Bit D9 in the control register (see the Control Register (Register Address 0X80, Register Address 0X81) section) and is made available at the VOUT pin.

RECEIVE STAGE

The receive stage comprises a current-to-voltage amplifier, followed by a programmable gain amplifier (PGA), antialiasing filter, and ADC. The receive stage schematic is shown in Figure 20. The unknown impedance is connected between the VOUT and VIN pins. The first stage current-to-voltage amplifier configuration means that a voltage present at the VIN pin is a virtual ground with a dc value set at VDD/2. The signal current that is developed across the unknown impedance flows into the VIN pin and develops a voltage signal at the output of the current-to-voltage converter. The gain of the current-to voltage amplifier is determined by a user-selectable feedback resistor connected between Pin 4 (RFB) and Pin 5 (VIN). It is important for the user to choose a feedback resistance value that, in conjunction with the selected gain of the PGA stage, maintains the signal within the linear range of the ADC (0 V to VDD).

The PGA allows the user to gain the output of the current-to-voltage amplifier by a factor of 5 or 1, depending upon the status of Bit D8 in the control register (see the Register Map section, Register Address 0x80). The signal is then low-pass filtered and presented to the input of the 12-bit, 1 MSPS ADC.

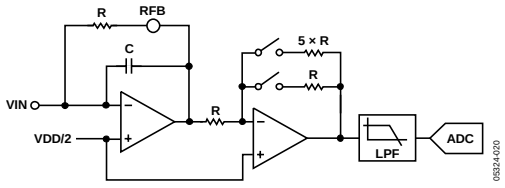

Figure 20. Receive Stage

The digital data from the ADC is passed directly to the DSP core of the AD5933, which performs a DFT on the sampled data.

DFT OPERATION

A DFT is calculated for each frequency point in the sweep. The AD5933 DFT algorithm is represented by

$$X(f) = \sum_{n=0}^{1023} (x(n)(\cos(n) - j\sin(n)))$$

where:
X(f) is the power in the signal at the Frequency Point f.
x(n) is the ADC output.
cos(*n*) and sin(*n*) are the sampled test vectors provided by the DDS core at the Frequency Point f.

The multiplication is accumulated over 1024 samples for each frequency point. The result is stored in two, 16-bit registers representing the real and imaginary components of the result. The data is stored in twos complement format.

SYSTEM CLOCK

The system clock for the AD5933 can be provided in one of two ways. The user can provide a highly accurate and stable system clock at the external clock pin (MCLK). Alternatively, the AD5933 provides an internal clock with a typical frequency of 16.776 MHz by means of an on-chip oscillator.

The user can select the preferred system clock by programming Bit D3 in the control register (Register Address 0x81, see Table 11). The default clock option on power-up is selected to be the internal oscillator.

The frequency distribution of the internal clock with temperature can be seen in Figure 14, Figure 15, and Figure 16.

TEMPERATURE SENSOR

The temperature sensor is a 13-bit digital temperature sensor with a 14th bit that acts as a sign bit. The on-chip temperature sensor allows an accurate measurement of the ambient device temperature to be made.

The measurement range of the sensor is −40°C to +125°C. At +150°C, the structural integrity of the device starts to deteriorate when operated at voltage and temperature maximum specifications. The accuracy within the measurement range is ±2°C.

TEMPERATURE CONVERSION DETAILS

The conversion clock for the part is internally generated; no external clock is required except when reading from and writing to the serial port. In normal mode, an internal clock oscillator runs an automatic conversion sequence.

The temperature sensor block defaults to a power-down state. To perform a measurement, a measure temperature command is issued by the user to the control register (Register Address 0x80 and Register Address 0x81). After the temperature operation is complete (typically 800 µs later), the block automatically powers down until the next temperature command is issued.

The user can poll the status register (Register Address 0x8F) to see if a valid temperature conversion has taken place, indicating that valid temperature data is available to read at Register Address 0x92 and Register Address 0x93 (see the Register Map section).

TEMPERATURE VALUE REGISTER

The temperature value register is a 16-bit, read-only register that stores the temperature reading from the ADC in 14-bit, twos complement format. The two MSB bits are don't cares. D13 is the sign bit. The internal temperature sensor is guaranteed to a low value limit of −40°C and a high value limit of +150°C. The digital output stored in Register Address 0x92 and Register Address 0x93 for the various temperatures is outlined in Table 6. The temperature sensor transfer characteristic is shown in Figure 21.

Table 6. Temperature Data Format

Temperature	Digital Output D13…D0
−40°C	11, 1011, 0000, 0000
−30°C	11, 1100, 0100, 0000
−25°C	11, 1100, 1110, 0000
−10°C	11, 1110, 1100, 0000
−0.03125°C	11, 1111, 1111, 1111
0°C	00, 0000, 0000, 0000
+0.03125°C	00, 0000, 0000, 0001
+10°C	00, 0001, 0100, 0000
+25°C	00, 0011, 0010, 0000
+50°C	00, 0110, 0100, 0000
+75°C	00, 1001, 0110, 0000
+100°C	00, 1100, 1000, 0000
+125°C	00, 1111, 1010, 0000
+150°C	01, 0010, 1100, 0000

TEMPERATURE CONVERSION FORMULA

Positive Temperature = *ADC Code* (*D*)/32

Negative Temperature = (*ADC Code* (*D*) − 16384)/32

where *ADC Code* uses all 14 bits of the data byte, including the sign bit.

Negative Temperature = (*ADC Code* (*D*) − 8192)/32

where *ADC Code (D)* is D13, the sign bit, and is removed from the ADC code.)

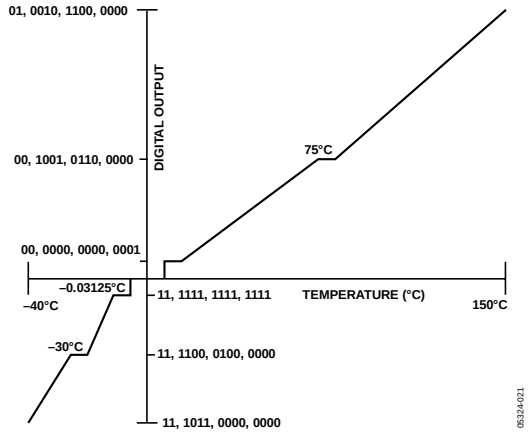

Figure 21. Temperature Sensor Transfer Function

IMPEDANCE CALCULATION

MAGNITUDE CALCULATION

The first step in impedance calculation for each frequency point is to calculate the magnitude of the DFT at that point.

The DFT magnitude is given by

$$Magnitude = \sqrt{R^2 + I^2}$$

where:
R is the real number stored at Register Address 0x94 and Register Address 0x95.
I is the imaginary number stored at Register Address 0x96 and Register Address 0x97.

For example, assume the results in the real data and imaginary data registers are as follows at a frequency point:

Real data register = 0x038B = 907 decimal

Imaginary data register = 0x0204 = 516 decimal

$$Magnitude = \sqrt{(907^2 + 516^2)} = 1043.506$$

To convert this number into impedance, it must be multiplied by
a scaling factor called the gain factor. The gain factor is calculated during the calibration of the system with a known impedance connected between the VOUT and VIN pins.

Once the gain factor has been calculated, it can be used in the calculation of any unknown impedance between the VOUT and VIN pins.

GAIN FACTOR CALCULATION

An example of a gain factor calculation follows, with the following assumptions:

Output excitation voltage = 2 V p-p

Calibration impedance value, $Z_{CALIBRATION}$ = 200 kΩ

PGA Gain = ×1

Current-to-voltage amplifier gain resistor = 200 kΩ

Calibration frequency = 30 kHz

Then typical contents of the real data and imaginary data registers after a frequency point conversion are:

Real data register = 0xF064 = −3996 decimal

Imaginary data register = 0x227E = +8830 decimal

$$Magnitude = \sqrt{(-3996)^2 + (8830)^2} = 9692.106$$

$$Gain\ Factor = \left(\frac{Admittance}{Code}\right) = \frac{\left(\frac{1}{Impedance}\right)}{Magnitude}$$

$$Gain\ Factor = \left(\frac{\frac{1}{200\ k\Omega}}{9692.106}\right) = 515.819 \times 10^{-12}$$

IMPEDANCE CALCULATION USING GAIN FACTOR

The next example illustrates how the calculated gain factor derived previously is used to measure an unknown impedance. For this example, assume that the unknown impedance = 510 kΩ.

After measuring the unknown impedance at a frequency of 30 kHz, assume that the real data and imaginary data registers contain the following data:

Real data register = 0xFA3F = −1473 decimal

Imaginary data register = 0x0DB3 = +3507 decimal

$$Magnitude = \sqrt{((-1473)^2 + (3507)^2)} = 3802.863$$

Then the measured impedance at the frequency point is given by

$$Impedance = \frac{1}{Gain\ Factor \times Magnitude}$$

$$= \frac{1}{515.819273 \times 10^{-12} \times 3802.863}\ \Omega = 509.791\ k\Omega$$

GAIN FACTOR VARIATION WITH FREQUENCY

Because the AD5933 has a finite frequency response, the gain factor also shows a variation with frequency. This variation in gain factor results in an error in the impedance calculation over a frequency range. Figure 22 shows an impedance profile based on a single-point gain factor calculation. To minimize this error, the frequency sweep should be limited to as small a frequency range as possible.

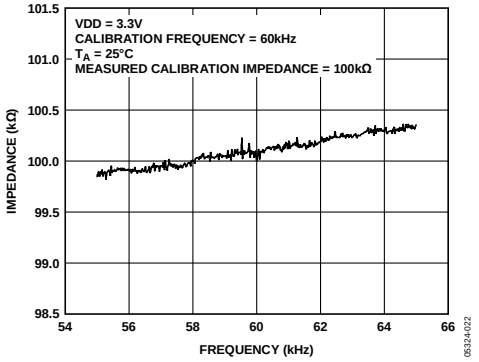

Figure 22. Impedance Profile Using a Single-Point Gain Factor Calculation

TWO-POINT CALIBRATION

Alternatively, it is possible to minimize this error by assuming that the frequency variation is linear and adjusting the gain factor with a two-point calibration. Figure 23 shows an impedance profile based on a two-point gain factor calculation.

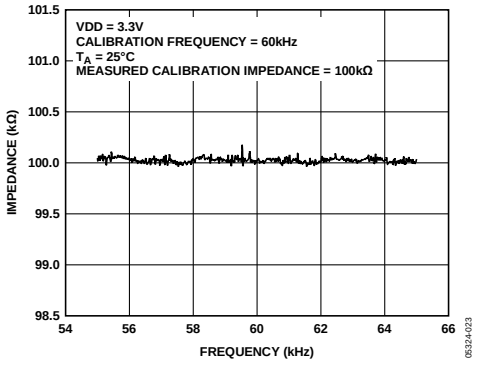

Figure 23. Impedance Profile Using a Two-Point Gain Factor Calculation

TWO-POINT GAIN FACTOR CALCULATION

This is an example of a two-point gain factor calculation assuming the following:

Output excitation voltage = 2 V (p-p)

Calibration impedance value, $Z_{UNKNOWN}$ = 100.0 kΩ

PGA gain = ×1

Supply voltage = 3.3 V

Current-to-voltage amplifier gain resistor = 100 kΩ

Calibration frequencies = 55 kHz and 65 kHz

Typical values of the gain factor calculated at the two calibration frequencies read

Gain factor calculated at 55 kHz is 1.031224E-09

Gain factor calculated at 65 kHz is 1.035682E-09

Difference in gain factor (ΔGF) is 1.035682E-09 – 1.031224E-09 = 4.458000E-12

Frequency span of sweep (ΔF) = 10 kHz

Therefore, the gain factor required at 60 kHz is given by

$$\left(\frac{4.458000\text{E-}12}{10\text{ kHz}} \times 5\text{ kHz}\right) + 1.031224 \times 10^{-9}$$

The required gain factor is 1.033453E-9.

The impedance is calculated as previously described.

GAIN FACTOR SETUP CONFIGURATION

When calculating the gain factor, it is important that the receive stage operate in its linear region. This requires careful selection of the excitation signal range, current-to-voltage gain resistor, and PGA gain.

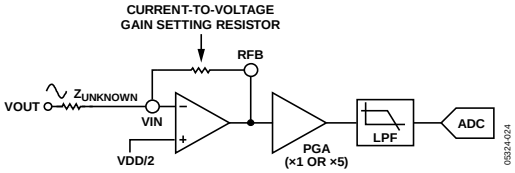

Figure 24. System Voltage Gain

The gain through the system shown in Figure 24 is given by

$$Ouput\ Excitation\ Voltage\ Range \times \frac{Gain\ Setting\ \text{Re}sistor}{Z_{UNKNOWN}} \times PGA\ Gain$$

For this example, assume the following system settings:

VDD = 3.3 V

Gain setting resistor = 200 kΩ

$Z_{UNKNOWN}$ = 200 kΩ

PGA setting = ×1

The peak-to-peak voltage presented to the ADC input is 2 V p-p. However, if a PGA gain of ×5 was chose, the voltage would saturate the ADC.

GAIN FACTOR RECALCULATION

The gain factor must be recalculated for a change in any of the following parameters:

- Current-to-voltage gain setting resistor
- Output excitation voltage
- PGA gain

GAIN FACTOR TEMPERATURE VARIATION

The typical impedance error variation with temperature is in the order of 30 ppm/°C. Figure 25 shows an impedance profile with a variation in temperature for 100 kΩ impedance using a two-point gain factor calibration.

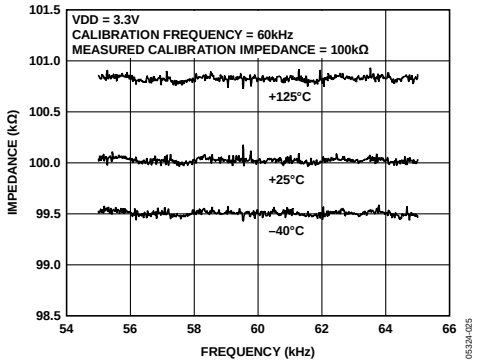

Figure 25. Impedance Profile Variation with Temperature Using a Two-Point Gain Factor Calibration

IMPEDANCE ERROR

It is important when reading the following section to note that the output impedance associated with the excitation voltages was actually measured and then calibrated out for each impedance error measurement. This was done using a Keithley current source/sink and measuring the voltage.

R_{OUT} (for example ,200 Ω specified for a 1.98 V p-p in the specification table) is only a typical specification and can vary from part to part. This method may not be achievable for large volume applications and in such cases, it is advised to use an extra low impedance output amplifier, as shown in Figure 4, to improve accuracy.

Please refer to CN-0217 for impedance accuracy examples on the AD5933 product web-page.

MEASURING THE PHASE ACROSS AN IMPEDANCE

The AD5933 returns a complex output code made up of separate real and imaginary components. The real component is stored at Register Address 0x94 and Register Address 0x95 and the imaginary component is stored at Register Address 0x96 and Register Address 0x97 after each sweep measurement. These correspond to the real and imaginary components of the DFT and not the resistive and reactive components of the impedance under test.

For example, it is a very common misconception to assume that if a user is analyzing a series RC circuit, the real value stored in Register Address 0x94 and Register Address 0x95 and the imaginary value stored at Register Address 0x96 and Register Address 0x97 correspond to the resistance and capacitive reactance, respectfully. However, this is incorrect because the magnitude of the impedance (|Z|) can be calculated by calculating the magnitude of the real and imaginary components of the DFT given by the following formula:

$$Magnitude = \sqrt{R^2 + I^2}$$

After each measurement, multiply it by the calibration term and invert the product. The magnitude of the impedance is, therefore, given by the following formula:

$$Impedance = \frac{1}{Gain\ Factor \times Magnitude}$$

Where gain factor is given by

$$Gain\ Factor = \left(\frac{Admittance}{Code}\right) = \frac{\left(\frac{1}{Impedance}\right)}{Magnitude}$$

The user must calibrate the AD5933 system for a known impedance range to determine the gain factor before any valid measurement can take place. Therefore, the user must know the impedance limits of the complex impedance ($Z_{UNKNOWN}$) for the sweep frequency range of interest. The gain factor is determined by placing a known impedance between the input/output of the AD5933 and measuring the resulting magnitude of the code. The AD5933 system gain settings need to be chosen to place the excitation signal in the linear region of the on-board ADC.

Because the AD5933 returns a complex output code made up of real and imaginary components, the user can also calculate the phase of the response signal through the AD5933 signal path. The phase is given by the following formula:

$$Phase(\text{rads}) = \tan^{-1}(I/R) \quad (3)$$

The phase measured by Equation 3 accounts for the phase shift introduced to the DDS output signal as it passes through the internal amplifiers on the transmit and receive side of the AD5933 along with the low-pass filter and also the impedance connected between the VOUT and VIN pins of the AD5933.

The parameters of interest for many users are the magnitude of the impedance ($|Z_{UNKNOWN}|$) and the impedance phase (ZØ). The measurement of the impedance phase (ZØ) is a two step process.

The first step involves calculating the AD5933 system phase. The AD5933 system phase can be calculated by placing a resistor across the VOUT and VIN pins of the AD5933 and calculating the phase (using Equation 3) after each measurement point in the sweep. By placing a resistor across the VOUT and VIN pins, there is no additional phase lead or lag introduced to the AD5933 signal path and the resulting phase is due entirely to the internal poles of the AD5933, that is, the system phase.

Once the system phase has been calibrated using a resistor, the second step involves calculating the phase of any unknown impedance by inserting the unknown impedance between the VIN and VOUT terminals of the AD5933 and recalculating the

new phase (including the phase due to the impedance) using the same formula. The phase of the unknown impedance (ZØ) is given by the following formula:

$$Z\text{Ø} = (\Phi unknown - \nabla system)$$

where:
$\nabla system$ is the phase of the system with a calibration resistor connected between VIN and VOUT.
$\Phi unknown$ is the phase of the system with the unknown impedance connected between VIN and VOUT.
ZØ is the phase due to the impedance, that is, the impedance phase.

Note that it is possible to calculate the gain factor and to calibrate the system phase using the same real and imaginary component values when a resistor is connected between the VOUT and VIN pins of the AD5933, for example, measuring the impedance phase (ZØ) of a capacitor.

The excitation signal current leads the excitation signal voltage across a capacitor by −90 degrees. Therefore, an approximate −90 degree phase difference exists between the system phase responses measured with a resistor and that of the system phase responses measured with a capacitive impedance.

As previously outlined, if the user would like to determine the phase angle of capacitive impedance (ZØ), the user first has to determine the system phase response (∇system) and subtract this from the phase calculated with the capacitor connected between VOUT and VIN (Φunknown).

A plot showing the AD5933 system phase response calculated using a 220 kΩ calibration resistor (R_{FB} = 220 kΩ, PGA = ×1) and the repeated phase measurement with a 10 pF capacitive impedance is shown in Figure 26.

One important point to note about the phase formula used to plot Figure 26 is that it uses the arctangent function that returns a phase angle in radians and, therefore, it is necessary to convert from radians to degrees.

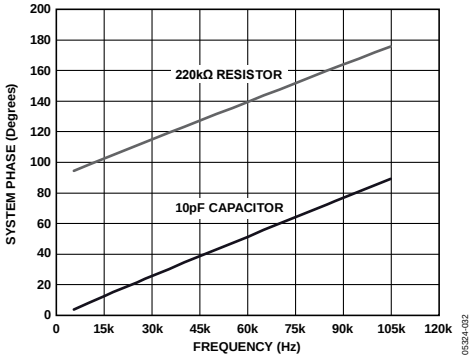

Figure 26. System Phase Response vs. Capacitive Phase

The phase difference (that is, ZØ) between the phase response of a capacitor and the system phase response using a resistor is the impedance phase of the capacitor, ZØ (see Figure 27).

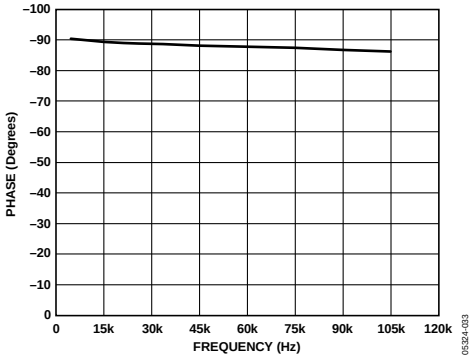

Figure 27. Phase Response of a Capacitor

Also when using the real and imaginary values to interpret the phase at each measurement point, take care when using the arctangent formula. The arctangent function returns the correct standard phase angle only when the sign of the real and imaginary values are positive, that is, when the coordinates lie in the first quadrant. The standard angle is the angle taken counterclockwise from the positive real x-axis. If the sign of the real component is positive and the sign of the imaginary component is negative, that is, the data lies in the second quadrant, then the arctangent formula returns a negative angle and it is necessary to add a further 180 degrees to calculate the correct standard angle. Likewise, when the real and imaginary components are both negative, that is, when the coordinates lie in the third quadrant, then the arctangent formula returns a positive angle and it is necessary to add 180 degrees from the angle to return the correct standard phase. Finally, when the real component is positive and the imaginary component is negative, that is, the data lies in the fourth quadrant, then the arctangent formula returns a negative angle. It is necessary to add 360 degrees to the angle to calculate the correct phase angle.

Therefore, the correct standard phase angle is dependent upon the sign of the real and imaginary component and is summarized in Table 7.

Once the magnitude of the impedance (|Z|) and the impedance phase angle (ZØ, in radians) are correctly calculated, it is possible to determine the magnitude of the real (resistive) and imaginary (reactive) component of the impedance ($Z_{UNKNOWN}$) by the vector projection of the impedance magnitude onto the real and imaginary impedance axis using the following formulas:

The real component is given by

$$|Z_{REAL}| = |Z| \times \cos(Z\text{Ø})$$

The imaginary component is given by

$$|Z_{IMAG}| = |Z| \times \sin(Z\text{Ø})$$

Table 7. Phase Angle

Real	Imaginary	Quadrant	Phase Angle
Positive	Positive	First	$\tan^{-1}(I/R) \times \frac{180°}{\pi}$
Negative	Positive	Second	$180° + \left(\tan^{-1}(I/R) \times \frac{180°}{\pi} \right)$
Negative	Negative	Third	$180° + \left(\tan^{-1}(I/R) \times \frac{180°}{\pi} \right)$
Positive	Negative	Fourth	$360° + \left(\tan^{-1}(I/R) \times \frac{180°}{\pi} \right)$

PERFORMING A FREQUENCY SWEEP

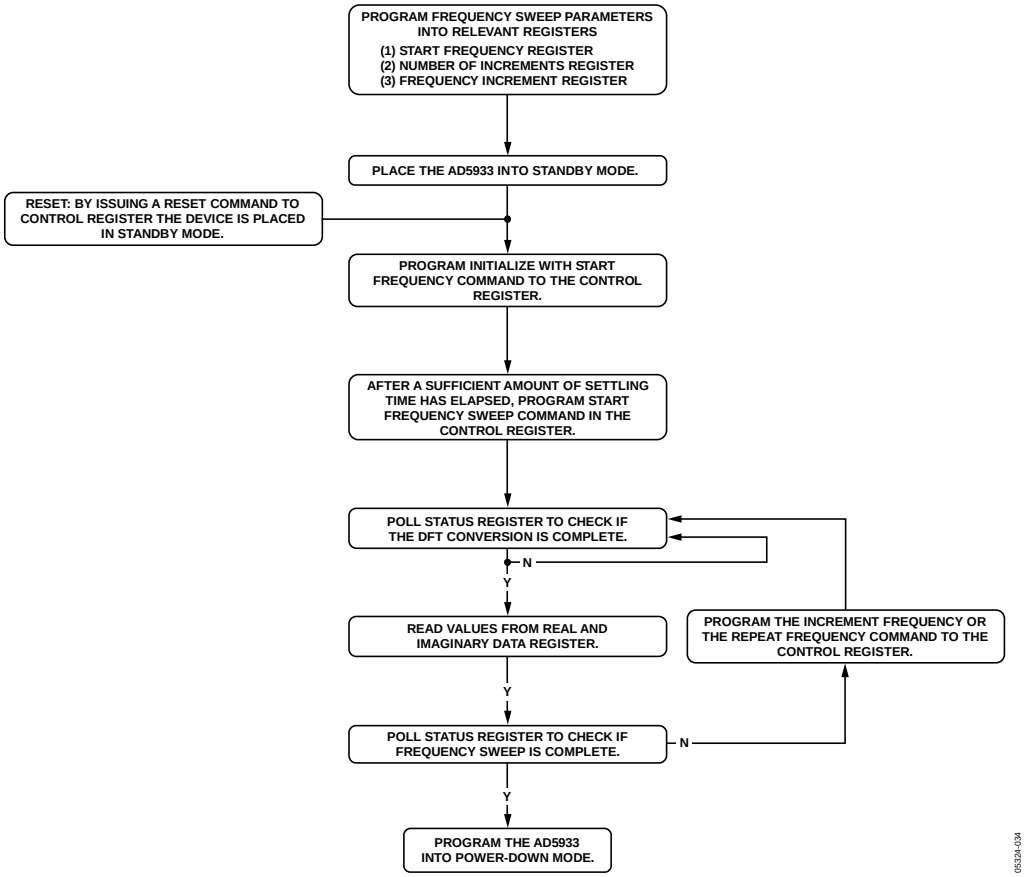

Figure 28. Frequency Sweep Flow Chart

REGISTER MAP

Table 8.

Register	Name	Register Data	Function
0x80	Control	D15 to D8	Read/write
0x81		D7 to D0	Read/write
0x82	Start frequency	D23 to D16	Read/write
0x83		D15 to D8	Read/write
0x84		D7 to D0	Read/write
0x85	Frequency increment	D23 to D16	Read/write
0x86		D15 to D8	Read/write
0x87		D7 to D0	Read/write
0x88	Number of increments	D15 to D8	Read/write
0x89		D7 to D0	Read/write
0x8A	Number of settling time cycles	D15 to D8	Read/write
0x8B		D7 to D0	Read/write
0x8F	Status	D7 to D0	Read only
0x92	Temperature data	D15 to D8	Read only
0x93		D7 to D0	Read only
0x94	Real data	D15 to D8	Read only
0x95		D7 to D0	Read only
0x96	Imaginary data	D15 to D8	Read only
0x97		D7 to D0	Read only

CONTROL REGISTER (REGISTER ADDRESS 0x80, REGISTER ADDRESS 0x81)

The AD5933 has a 16-bit control register (Register Address 0x80 and Register Address 0x81) that sets the AD5933 control modes. The default value of the control register upon reset is as follows: D15 to D0 reset to 0xA000 upon power-up.

The four MSBs of the control register are decoded to provide control functions, such as performing a frequency sweep, powering down the part, and controlling various other functions defined in the control register map.

The user may choose to write only to Register Address 0x80 and not to alter the contents of Register Address 0x81. Note that the control register should not be written to as part of a block write command. The control register also allows the user to program the excitation voltage and set the system clock. A reset command to the control register does not reset any programmed values associated with the sweep (that is, start frequency, number of increments, frequency increment). After a reset command, an initialize with start frequency command must be issued to the control register to restart the frequency sweep sequence (see Figure 28).

Table 9. Control Register Map (D15 to D12)

D15	D14	D13	D12	Function
0	0	0	0	No operation
0	0	0	1	Initialize with start frequency
0	0	1	0	Start frequency sweep
0	0	1	1	Increment frequency
0	1	0	0	Repeat frequency
1	0	0	0	No operation
1	0	0	1	Measure temperature
1	0	1	0	Power-down mode
1	0	1	1	Standby mode
1	1	0	0	No operation
1	1	0	1	No operation

Table 10. Control Register Map (D10 to D9)

D10	D9	Range No.	Output Voltage Range
0	0	1	2.0 V p-p typical
0	1	4	200 mV p-p typical
1	0	3	400 mV p-p typical
1	1	2	1.0 V p-p typical

Table 11. Control Register Map (D11, D8 to D0)

Bits	Description
D11	No operation
D8	PGA gain; 0 = ×5, 1 = ×1
D7	Reserved; set to 0
D6	Reserved; set to 0
D5	Reserved; set to 0
D4	Reset
D3	External system clock; set to 1
	Internal system clock; set to 0
D2	Reserved; set to 0
D1	Reserved; set to 0
D0	Reserved; set to 0

Control Register Decode

Initialize with Start Frequency

This command enables the DDS to output the programmed start frequency for an indefinite time. It is used to excite the unknown impedance initially. When the output unknown impedance has settled after a time determined by the user, the user must initiate a start frequency sweep command to begin the frequency sweep.

Start Frequency Sweep

In this mode the ADC starts measuring after the programmed number of settling time cycles has elapsed. The user has the ability to program an integer number of output frequency cycles (settling time cycles) to Register Address 0x8A and Register Address 0x8B before the commencement of the measurement at each frequency point (see Figure 28).

Increment Frequency

The increment frequency command is used to step to the next frequency point in the sweep. This usually happens after data from the previous step has been transferred and verified by the DSP. When the AD5933 receives this command, it waits for the programmed number of settling time cycles before beginning the ADC conversion process.

Repeat Frequency

The AD5933 has the facility to repeat the current frequency point measurement by issuing a repeat frequency command to the control register. This has the benefit of allowing the user to average successive readings.

Measure Temperature

The measure temperature command initiates a temperature reading from the part. The part does not need to be in power-up mode to perform a temperature reading. The block powers itself up, takes the reading, and then powers down again. The temperature reading is stored in a 14-bit, twos complement format at Register Address 0x92 and Register Address 0x93.

Power-Down Mode

The default state on power-up of the AD5933 is power-down mode. The control register contains the code 1010,0000,0000,0000 (0xA000). In this mode, both the VOUT and VIN pins are connected internally to GND.

Standby Mode

This mode powers up the part for general operation; in standby mode the VIN and VOUT pins are internally connected to ground.

Output Voltage Range

The output voltage range allows the user to program the excitation voltage range at VOUT.

PGA Gain

The PGA gain allows the user to amplify the response signal into the ADC by a multiplication factor of ×5 or ×1.

Reset

A reset command allows the user to interrupt a sweep. The start frequency, number of increments, and frequency increment register contents are not overwritten. An initialize with start frequency command is required to restart the frequency sweep command sequence.

START FREQUENCY REGISTER (REGISTER ADDRESS 0x82, REGISTER ADDRESS 0x83, REGISTER ADDRESS 0x84)

The default value of the start frequency register upon reset is as follows: D23 to D0 are not reset on power-up. After a reset command, the contents of this register are not reset.

The start frequency register contains the 24-bit digital representation of the frequency from where the subsequent frequency sweep is initiated. For example, if the user requires the sweep to start from frequency 30 kHz (using a 16.0 MHz clock), then the user programs the value of 0x0F to Register Address 0x82, the value of 0x5C to Register Address 0x83, and the value of 0x28 to Register Address 0x84. This ensures the output frequency starts at 30 kHz.

The code to be programmed to the start frequency register is

$$Start\ Frequency\ Code = \left(\frac{30\ \text{kHz}}{\left(\frac{16\ \text{MHz}}{4} \right)} \right) \times 2^{27} \equiv 0\text{x}0\text{F}5\text{C}28$$

FREQUENCY INCREMENT REGISTER (REGISTER ADDRESS 0x85, REGISTER ADDRESS 0x86, REGISTER ADDRESS 0x87)

The default value upon reset is as follows: D23 to D0 are not reset on power-up. After a reset command, the contents of this register are not reset.

The frequency increment register contains a 24-bit representation of the frequency increment between consecutive frequency points along the sweep. For example, if the user requires an increment step of 10 Hz using a 16.0 MHz clock, the user should program the value of 0x00 to Register Address 0x85, the value of 0x01 to Register Address 0x86m, and the value of 0x4F to Register Address 0x87.

The formula for calculating the increment frequency is given by

$$Frequency\ Increment\ Code = \left(\frac{10\ \text{Hz}}{\left(\frac{16\ \text{MHz}}{4} \right)} \right) \times 2^{27} \equiv 0\text{x}00014\,\text{F}$$

The user programs the value 0x00 to Register Address 0x85, the value 0x01 to Register Address 0x86, and the value 0x4F to Register Address 0x87.

NUMBER OF INCREMENTS REGISTER (REGISTER ADDRESS 0x88, REGISTER ADDRESS 0x89)

The default value upon reset is as follows: D8 to D0 are not reset on power-up. After a reset command, the contents of this register are not reset.

Table 12. Number of Increments Register

Reg	Bits	Description	Function	Format
0x88	D15 to D9	Don't care	Read or write	Integer number stored in binary format
	D8	Number of increments	Read or write	
0x89	D8 to D0	Number of increments	Read or write	Integer number stored in binary format

This register determines the number of frequency points in the frequency sweep. The number of points is represented by a 9-bit word, D8 to D0. D15 to D9 are don't care bits. This register, in conjunction with the start frequency register and the increment frequency register, determines the frequency sweep range for the sweep operation. The maximum number of increments that can be programmed is 511.

NUMBER OF SETTLING TIME CYCLES REGISTER (REGISTER ADDRESS 0x8A, REGISTER ADDRESS 0x8B)

The default value upon reset is as follows: D10 to D0 are not reset on power-up. After a reset command, the contents of this register are not reset (see Table 13).

This register determines the number of output excitation cycles that are allowed to pass through the unknown impedance, after receipt of a start frequency sweep, increment frequency, or repeat frequency command, before the ADC is triggered to perform a conversion of the response signal. The number of settling time cycles register value determines the delay between a start frequency sweep/increment frequency /repeat frequency command and the time an ADC conversion commences. The number of cycles is represented by a 9-bit word, D8 to D0. The value programmed into the number of settling time cycles register can be increased by a factor of 2 or 4 depending upon the status of bits D10 to D9. The five most significant bits, D15 to D11, are don't care bits. The maximum number of output cycles that can be programmed is 511 × 4 = 2044 cycles. For example, consider an excitation signal of 30 kHz. The maximum delay between the programming of this frequency and the time that this signal is first sampled by the ADC is ≈ 511 × 4 × 33.33 µs = 68.126 ms. The ADC takes 1024 samples, and the result is stored as real data and imaginary data in Register Address 0x94 to Register Address 0x97. The conversion process takes approximately 1 ms using a 16.777 MHz clock.

Table 13. Number of Settling Times Cycles Register

Register	Bits	Description			Function	Format
0x8A	D15 to D11	Don't care			Read or write	Integer number stored in binary format
	D10 to D9	2-bit decode				
		D10	**D9**	**Description**		
		0	0	Default		
		0	1	No. of cycles × 2		
		1	0	Reserved		
		1	1	No. of cycles × 4		
	D8	MSB number of settling time cycles				
0x8B	D7 to D0	Number of settling time cycles			Read or write	

STATUS REGISTER (REGISTER ADDRESS 0x8F)

The status register is used to confirm that particular measurement tests have been successfully completed. Each of the bits from D7 to D0 indicates the status of a specific functionality of the AD5933.

Bit D0 and Bit D4 to Bit D7 are treated as don't care bits These bits do not indicate the status of any measurement.

The status of Bit D1 indicates the status of a frequency point impedance measurement. This bit is set when the AD5933 has completed the current frequency point impedance measurement. This bit indicates that there is valid real data and imaginary data in Register Address 0x94 to Register Address 0x97. This bit is reset on receipt of a start frequency sweep, increment frequency, repeat frequency, or reset command. This bit is also reset on power-up.

The status of Bit D2 indicates the status of the programmed frequency sweep. This bit is set when all programmed increments to the number of increments register are complete. This bit is reset on power-up and on receipt of a reset command.

Table 14. Status Register (Register Address 0x8F)

Control Word	Function
0000 0001	Valid temperature measurement
0000 0010	Valid real/imaginary data
0000 0100	Frequency sweep complete
0000 1000	Reserved
0001 0000	Reserved
0010 0000	Reserved
0100 0000	Reserved
1000 0000	Reserved

Valid Temperature Measurement

The valid temperature measurement control word is set when a valid temperature conversion is complete indicating that valid temperature data is available for reading at Register Address 0x92 and Register Address 0x93. It is reset when a temperature measurement takes place as a result of a measure temperature command having been issued to the control register (Register Address 0x80 and Register Address 0x81) by the user.

Valid Real/Imaginary Data

D1 is set when data processing for the current frequency point is finished, indicating real/imaginary data available for reading. D1 is reset when a start frequency sweep/increment frequency/repeat frequency DDS start/increment/repeat command is issued. D1 is reset to 0 when a reset command is issued to the control register.

Frequency Sweep Complete

D2 is set when data processing for the last frequency point in the sweep is complete. This bit is reset when a start frequency sweep command is issued to the control register. This bit is also reset when a reset command is issued to the control register.

TEMPERATURE DATA REGISTER (16 BITS—REGISTER ADDRESS 0x92, REGISTER ADDRESS 0x93)

These registers contain a digital representation of the temperature of the AD5933. The values are stored in 16-bit, twos complement format. Bit D15 and Bit D14 are don't care bits. Bit 13 is the sign bit. To convert this number to an actual temperature, refer to the Temperature Conversion Formula section.

REAL AND IMAGINARY DATA REGISTERS (16 BITS—REGISTER ADDRESS 0x94, REGISTER ADDRESS 0x95, REGISTER ADDRESS 0x96, REGISTER ADDRESS 0x97)

The default value upon reset is as follows: these registers are not reset on power-up or on receipt of a reset command. Note that the data in these registers is valid only if Bit D1 in the status register is set, indicating that the processing at the current frequency point is complete.

These registers contain a digital representation of the real and imaginary components of the impedance measured for the current frequency point. The values are stored in 16-bit, twos complement format. To convert this number to an actual impedance value, the magnitude—$\sqrt{(Real^2 + Imaginary^2)}$—must be multiplied by an admittance/code number (called a gain factor) to give the admittance, and the result inverted to give impedance. The gain factor varies for each ac excitation voltage/gain combination.

SERIAL BUS INTERFACE

Control of the AD5933 is carried out via the I²C-compliant serial interface protocol. The AD5933 is connected to this bus as a slave device under the control of a master device. The AD5933 has a 7-bit serial bus slave address. When the device is powered up, it has a default serial bus address, 0001101 (0x0D).

GENERAL I²C TIMING

Figure 29 shows the timing diagram for general read and write operations using the I²C-compliant interface.

The master initiates data transfer by establishing a start condition, defined as a high-to-low transition on the serial data line (SDA), while the serial clock line (SCL) remains high. This indicates that a data stream follows. The slave responds to the start condition and shifts in the next 8 bits, consisting of a 7-bit slave address (MSB first) plus an R/W bit that determines the direction of the data transfer—that is, whether data is written to or read from the slave device (0 = write, 1 = read).

The slave responds by pulling the data line low during the low period before the ninth clock pulse, known as the acknowledge bit, and holding it low during the high period of this clock pulse. All other devices on the bus remain idle while the selected device waits for data to be read from or written to it. If the R/W bit is 0, then the master writes to the slave device. If the R/W bit is 1, the master reads from the slave device.

Data is sent over the serial bus in sequences of nine clock pulses, eight bits of data followed by an acknowledge bit, which can be from the master or slave device. Data transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, because a low-to-high transition when the clock is high may be interpreted as a stop signal. If the operation is a write operation, the first data byte after the slave address is a command byte. This tells the slave device what to expect next. It may be an instruction telling the slave device to expect a block write, or it may be a register address that tells the slave where subsequent data is to be written. Because data can flow in only one direction as defined by the R/W bit, it is not possible to send a command to a slave device during a read operation. Before performing a read operation, it is sometimes necessary to perform a write operation to tell the slave what sort of read operation to expect and/or the address from which data is to be read.

When all data bytes have been read or written, stop conditions are established. In write mode, the master pulls the data line high during the 10th clock pulse to assert a stop condition. In read mode, the master device releases the SDA line during the low period before the ninth clock pulse, but the slave device does not pull it low. This is known as a no acknowledge. The master then takes the data line low during the low period before the 10th clock pulse, then high during the 10th clock pulse to assert a stop condition.

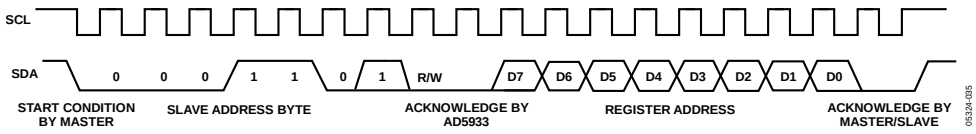

Figure 29. Timing Diagram

WRITING/READING TO THE AD5933

The interface specification defines several different protocols for different types of read and write operations. This section describes the protocols used in the AD5933. The figures in this section use the abbreviations shown in Table 15.

Table 15. I²C Abbreviation Table

Abbreviation	Condition
S	Start
P	Stop
R	Read
W	Write
A	Acknowledge
$\overline{A}$	No acknowledge write byte/command byte

User Command Codes

The command codes in Table 16 are used for reading/writing to the interface. They are further explained in this section, but are grouped here for easy reference.

Table 16. Command Codes

Command Code	Code Name	Code Description
1010 0000	Block write	This command is used when writing multiple bytes to the RAM; see the Block Write section.
1010 0001	Block read	This command is used when reading multiple bytes from RAM/memory; see the Block Read section.
1011 0000	Address pointer	This command enables the user to set the address pointer to any location in the memory. The data contains the address of the register to which the pointer should be pointing reworded

Write Byte/Command Byte

In this operation, the master device sends a byte of data to the slave device. The write byte can either be a data byte write to a register address or can be a command operation. To write data to a register, the command sequence is as follows (see Figure 30):

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts an acknowledge on SDA.
4. The master sends a register address.
5. The slave asserts an acknowledge on SDA.
6. The master sends a data byte.
7. The slave asserts an acknowledge on SDA.
8. The master asserts a stop condition on SDA to end the transaction.

Figure 30. Writing Register Data to Register Address

The write byte protocol is also used to set a pointer to an address (see Figure 31). This is used for a subsequent single-byte read from the same address or block read or block write starting at that address.

To set a register pointer, the following sequence is applied:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts an acknowledge on SDA.
4. The master sends a pointer command code (see Table 16; a pointer command = 1011 0000).
5. The slave asserts an acknowledge on SDA.
6. The master sends a data byte (a register address to where the pointer is to point).
7. The slave asserts an acknowledge on SDA.
8. The master asserts a stop condition on SDA to end the transaction.

Figure 31. Setting Address Pointer to Register Address

BLOCK WRITE

In this operation, the master device writes a block of data to a slave device (see Figure 32). The start address for a block write must previously have been set. In the case of the AD5933 this is done by setting a pointer to set the register address.

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts an acknowledge on SDA.
4. The master sends an 8-bit command code (1010 0000) that tells the slave device to expect a block write.
5. The slave asserts an acknowledge on SDA.
6. The master sends a data byte that tells the slave device the number of data bytes to be sent to it.
7. The slave asserts an acknowledge on SDA.
8. The master sends the data bytes.
9. The slave asserts an acknowledge on SDA after each data byte.
10. The master asserts a stop condition on SDA to end the transaction.

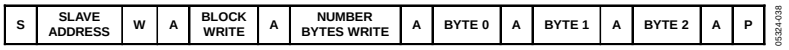

Figure 32. Writing a Block Write

READ OPERATIONS

The AD5933 uses two I²C read protocols: receive byte and block read.

Receive Byte

In the AD5933, the receive byte protocol is used to read a single byte of data from a register address whose address has previously been set by setting the address pointer.

In this operation, the master device receives a single byte from a slave device as follows (see Figure 33):

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the read bit (high).
3. The addressed slave device asserts an acknowledge on SDA.
4. The master receives a data byte.
5. The master asserts a no acknowledge on SDA (the slave needs to check that master has received data).
6. The master asserts a stop condition on SDA and the transaction ends.

Figure 33. Reading Register Data

Block Read

In this operation, the master device reads a block of data from a slave device (see Figure 34). The start address for a block read must previously have been set by setting the address pointer.

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts an acknowledge on SDA.
4. The master sends a command code (1010 0001) that tells the slave device to expect a block read.
5. The slave asserts an acknowledge on SDA.
6. The master sends a byte-count data byte that tells the slave how many data bytes to expect.
7. The slave asserts an acknowledge on SDA.
8. The master asserts a repeat start condition on SDA. This is required to set the read bit high.
9. The master sends the 7-bit slave address followed by the read bit (high).
10. The slave asserts an acknowledge on SDA.
11. The master receives the data bytes.
12. The master asserts an acknowledge on SDA after each data byte.
13. A no acknowledge is generated after the last byte to signal the end of the read.
14. The master asserts a stop condition on SDA to end the transaction.

Figure 34. Performing a Block Read

TYPICAL APPLICATIONS

MEASURING SMALL IMPEDANCES

The AD5933 is capable of measuring impedance values up to 10 MΩ if the system gain settings are chosen correctly for the impedance subrange of interest.

If the user places a small impedance value (≤500 Ω over the sweep frequency of interest) between the VOUT and VIN pins, it results in an increase in signal current flowing through the impedance for a fixed excitation voltage in accordance with Ohm's law. The output stage of the transmit side amplifier available at the VOUT pin may not be able to provide the required increase in current through the impedance. To have a unity gain condition about the receive side I-V amplifier, the user needs to have a similar small value of feedback resistance for system calibration as outlined in the Gain Factor Setup Configuration section. The voltage presented at the VIN pin is hard biased at VDD/2 due to the virtual earth on the receive side I-V amplifier. The increased current sink/source requirement placed on the output of the receive side I-V amplifier may also cause the amplifier to operate outside of the linear region. This causes significant errors in subsequent impedance measurements.

The value of the output series resistance, R_{OUT}, (see Figure 35) at the VOUT pin must be taken into account when measuring small impedances ($Z_{UNKNOWN}$), specifically when the value of the output series resistance is comparable to the value of the impedance under test ($Z_{UNKNOWN}$). If the R_{OUT} value is unaccounted for in the system calibration (that is, the gain factor calculation) when measuring small impedances, there is an introduced error into any subsequent impedance measurement that takes place. The introduced error depends on the relative magnitude of the impedance being tested compared to the value of the output series resistance.

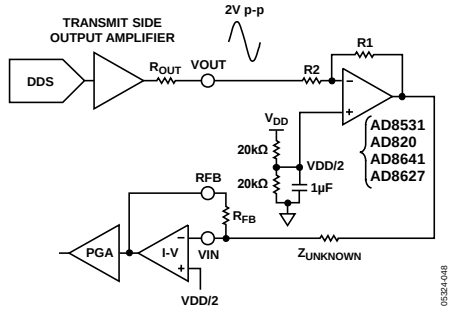

Figure 35. Additional External Amplifier Circuit for Measuring Small Impedances

The value of the output series resistance depends upon the selected output excitation range at VOUT and has a tolerance from device to device like all discrete resistors manufactured in a silicon fabrication process. Typical values of the output series resistance are outlined in Table 17.

Table 17. Output Series Resistance (R_{OUT}) vs. Excitation Range

Parameter	Value (Typ)	Output Series Resistance Value
Range 1	2 V p-p	200 Ω typ
Range 2	1 V p-p	2.4 kΩ typ
Range 3	0.4 V p-p	1.0 kΩ typ
Range 4	0.2 V p-p	600 Ω typ

Therefore, to accurately calibrate the AD5933 to measure small impedances, it is necessary to reduce the signal current by attenuating the excitation voltage sufficiently and also account for the R_{OUT} value and factor it into the gain factor calculation (see the Gain Factor Calculation section).

Measuring the R_{OUT} value during device characterization is achieved by selecting the appropriate output excitation range at VOUT and sinking and sourcing a known current at the pin (for example, ±2 mA) and measuring the change in dc voltage. The output series resistance can be calculated by measuring the inverse of the slope (that is, 1/slope) of the resultant I-V plot.

A circuit that helps to minimize the effects of the issues previously outlined is shown in Figure 35. The aim of this circuit is to place the AD5933 system gain within its linear range when measuring small impedances by using an additional external amplifier circuit along the signal path. The external amplifier attenuates the peak-to-peak excitation voltage at VOUT by a suitable choice of resistors (R1 and R2), thereby reducing the signal current flowing through the impedance and minimizing the effect of the output series resistance in the impedance calculations.

In the circuit shown in Figure 35, $Z_{UNKNOWN}$ recognizes the output series resistance of the external amplifier which is typically much less than 1 Ω with feedback applied depending upon the op amp device used (for example, AD820, AD8641, AD8531) as well as the load current, bandwidth, and gain.

The key point is that the output impedance of the external amplifier in Figure 35 (which is also in series with $Z_{UNKNOWN}$) has a far less significant effect on gain factor calibration and subsequent impedance readings in comparison to connecting the small impedance directly to the VOUT pin (and directly in series with R_{OUT}). The external amplifier buffers the unknown impedance from the effects of R_{OUT} and introduces a smaller output impedance in series with $Z_{UNKNOWN}$.

For example, if the user measures $Z_{UNKNOWN}$ that is known to have a small impedance value within the range of 90 Ω to 110 Ω over the frequency range of 30 kHz to 32 kHz, the user may not be in a position to measure R_{OUT} directly in the factory/lab. Therefore, the user may choose to add on an extra amplifier circuit like that shown in Figure 35 to the signal path of the AD5933. The user must ensure that the chosen external amplifier has a sufficiently low output series resistance over the bandwidth of interest in comparison to the impedance range under test (for an op amp selection guide, see www.analog.com/opamps). Most amplifiers from Analog Devices have a curve of closed loop output impedance vs. frequency at different amplifier gains to determine the output series impedance at the frequency of interest.

The system settings are

VDD = 3.3 V

VOUT = 2 V p-p

R2 = 20 kΩ

R1 = 4 kΩ

Gain setting resistor = 500 Ω

$Z_{UNKNOWN}$ = 100 Ω

PGA setting = ×1

To attenuate the excitation voltage at VOUT, choose a ratio of R1/R2. With the values of R1 = 4 kΩ and R2 = 20 kΩ, attenuate the signal by 1/5th of 2 V p-p = 400 mV. The maximum current flowing through the impedance is 400 mV/90 Ω = 4.4 mA.

The system is subsequently calibrated using the usual method with a midpoint impedance value of 100 Ω, a calibration resistor, and a feedback resistor at a midfrequency point in the sweep. The dynamic range of the input signal to the receive side of the AD5933 can be improved by increasing the value of the I-V gain resistor at the RFB pin. For example, increasing the I-V gain setting resistor at the RFB pin increases the peak-to-peak signal presented to the ADC input from 400 mV (RFB = 100 Ω) to 2 V p-p (RFB = 500 Ω).

The gain factor calculated is for a 100 Ω resistor connected between VOUT and VIN, assuming the output series resistance of the external amplifier is small enough to be ignored.

When biasing the circuit shown in Figure 35, note that the receive side of the AD5933 is hard-biased about VDD/2 by design. Therefore, to prevent the output of the external amplifier (attenuated AD5933 Range 1 excitation signal) from saturating the receive side amplifiers of the AD5933, a voltage equal to VDD/2 must be applied to the noninverting terminal of the external amplifier.

BIOMEDICAL: NONINVASIVE BLOOD IMPEDANCE MEASUREMENT

When a known strain of a virus is added to a blood sample that already contains a virus, a chemical reaction takes place whereby the impedance of the blood under certain conditions changes. By characterizing this effect across different frequencies, it is possible to detect a specific strain of virus. For example, a strain of the disease exhibits a certain characteristic impedance at one frequency but not at another; therefore, the requirement is to sweep different frequencies to check for different viruses. The AD5933, with its 27-bit phase accumulator, allows for subhertz frequency tuning.

The AD5933 can be used to inject a stimulus signal through the blood sample via a probe. The response signal is analyzed, and the effective impedance of the blood is tabulated. The AD5933 is ideal for this application because it allows the user to tune to the specific frequency required for each test.

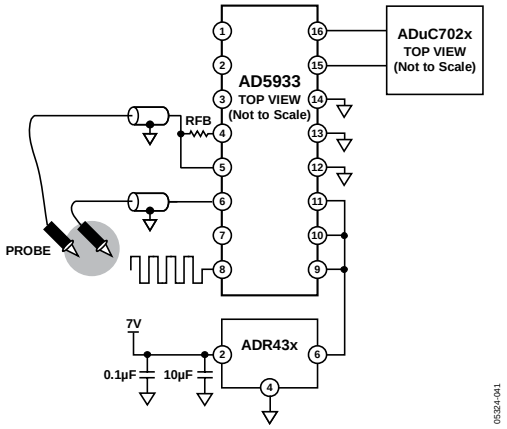

Figure 36. Measuring a Blood Sample for a Strain of Virus

SENSOR/COMPLEX IMPEDANCE MEASUREMENT

The operational principle of a capacitive proximity sensor is based on the change of a capacitance in an RLC resonant circuit. This leads to changes in the resonant frequency of the RLC circuit, which can be evaluated as shown Figure 37.

It is first required to tune the RLC circuit to the area of resonance. At the resonant frequency, the impedance of the RLC circuit is at a maximum. Therefore, a programmable frequency sweep and tuning capability is required, which is provided by the AD5933.

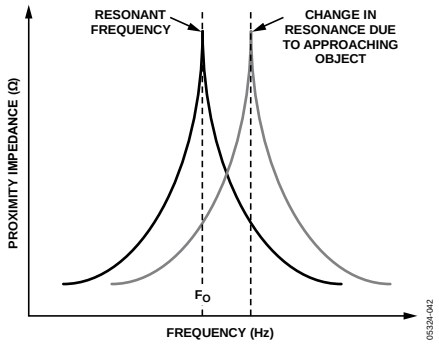

Figure 37. Detecting a Change in Resonant Frequency

An example of the use of this type of sensor is for a train proximity measurement system. The magnetic fields of the train approaching on the track change the resonant frequency to an extent that can be characterized. This information can be sent back to a mainframe system to show the train location on the network.

Another application for the AD5933 is in parked vehicle detection. The AD5933 is placed in an embedded unit connected to a coil of wire underneath the parking location. The AD5933 outputs a single frequency within the 80 kHz to 100 kHz frequency range, depending upon the wire composition. The wire can be modeled as a resonant circuit. The coil is calibrated with a known impedance value and at a known frequency. The impedance of the loop is monitored constantly. If a car is parked over the coil, the impedance of the coil changes and the AD5933 detects the presence of the car.

ELECTRO-IMPEDANCE SPECTROSCOPY

The AD5933 has found use in the area of corrosion monitoring. Corrosion of metals, such as aluminum and steel, can damage industrial infrastructures and vehicles such as aircraft, ships, and cars. This damage, if left unattended, may lead to premature failure requiring expensive repairs and/or replacement. In many cases, if the onset of corrosion can be detected, it can be arrested or slowed, negating the requirement for repairs or replacement. At present, visual inspection is employed to detect corrosion; however, this is time consuming, expensive, and cannot be employed in hard-to-access areas.

An alternative to visual inspection is automated monitoring using corrosion sensors. Monitoring is cheaper, less time consuming, and can be deployed where visual inspections are impossible. Electrochemical impedance spectroscopy (EIS) has been used to interrogate corrosion sensors, but at present large laboratory test instruments are required. The AD5933 offers an accurate and compact solution for this type of measurement, enabling the development of field deployable sensor systems that can measure corrosion rates autonomously.

Mathematically, the corrosion of aluminum is modeled using an RC network that typically consists of a resistance, R_S, in series with a parallel resistor and capacitor, R_P and C_P. A system metal would typically have values as follows: R_S is 10 Ω to 10 kΩ, R_P 1 is kΩ to 1 MΩ, and C_P is 5 µF to 70 µF. Figure 38 shows a typical Bode plot, impedance modulus, and phase angle vs. frequency, for an aluminum corrosion sensor.

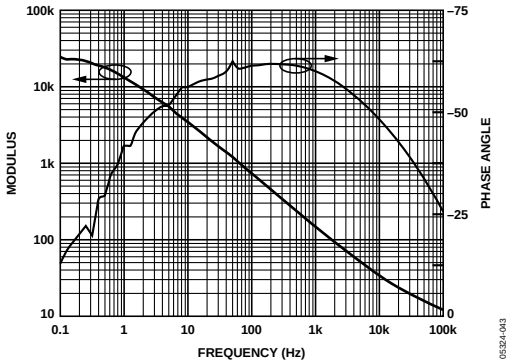

Figure 38. Bode Plot for Aluminum Corrosion Sensor

To make accurate measurements of these values, the impedance needs to be measured over a frequency range of 0.1 Hz to 100 kHz. To ensure that the measurement itself does not introduce a corrosive effect, the metal needs to be excited with minimal voltage, typically in the ±20 mV range. A nearby processor or control unit such as the ADuC702x would log a single impedance sweep from 0.1 kHz to 100 kHz every 10 minutes and download the results back to a control unit. To achieve system accuracy from the 0.1 kHz to 1 kHz range, the system clock needs to be scaled down from the 16.776 MHz nominal clock frequency to 500 kHz, typically. The clock scaling can be achieved digitally using an external direct digital synthesizer like the AD9834 as a programmable divider, which supplies a clock signal to MCLK and which can be controlled digitally by the nearby microprocessor.

LAYOUT AND CONFIGURATION

POWER SUPPLY BYPASSING AND GROUNDING

When accuracy is important in a circuit, carefully consider the power supply and ground return layout on the board. The printed circuit board containing the AD5933 should have separate analog and digital sections, each having its own area of the board. If the AD5933 is in a system where other devices require an AGND-to-DGND connection, the connection should be made at one point only. This ground point should be as close as possible to the AD5933.

The power supply to the AD5933 should be bypassed with 10 μF and 0.1 μF capacitors. The capacitors should be physically as close as possible to the device, with the 0.1 μF capacitor ideally right up against the device. The 10 μF capacitors are the tantalum bead type. It is important that the 0.1 μF capacitor have low effective series resistance (ESR) and effective series inductance (ESI); common ceramic types of capacitors are suitable. The 0.1 μF capacitor provides a low impedance path to ground for high frequencies caused by transient currents due to internal logic switching.

The power supply line itself should have as large a trace as possible to provide a low impedance path and reduce glitch effects on the supply line. Clocks and other fast switching digital signals should be shielded from other parts of the board by digital ground. Avoid crossover of digital and analog signals if possible. When traces cross on opposite sides of the board, ensure that they run at right angles to each other to reduce feedthrough effects on the board. The best board layout technique is the microstrip technique where the component side of the board is dedicated to the ground plane only, and the signal traces are placed on the solder side. However, this is not always possible with a two-layer board.

EVALUATION BOARD

The AD5933 evaluation board allows designers to evaluate the high performance AD5933 impedance converter with minimum effort.

The evaluation board interfaces to the USB port of a PC. It is possible to power the entire board from the USB port.

The impedance converter evaluation kit includes a populated and tested AD5933 printed circuit board. The EVAL-AD5933EB kit is shipped with a CD-ROM that includes self-installing software. Connect the PC to the evaluation board using the supplied cable.

The software is compatible with Microsoft® Windows® 2000 and Windows XP and Windows 7.

A schematic of the evaluation board is shown in Figure 39 and Figure 40.

USING THE EVALUATION BOARD

The AD5933 evaluation board is a test system designed to simplify the evaluation of the AD5933. The evaluation board data sheet is also available with the evaluation board that gives full information on operating the evaluation board. Further evaluation information is available from www.analog.com.

PROTOTYPING AREA

An area is available on the evaluation board for the user to add additional circuits to the evaluation test set. Users may want to include switches for multiple calibration use.

CRYSTAL OSCILLATOR (XO) vs. EXTERNAL CLOCK

A 16 MHz oscillator is included on the evaluation board. However, this oscillator can be removed and, if required, an external CMOS clock can be connected to the part.

SCHEMATICS

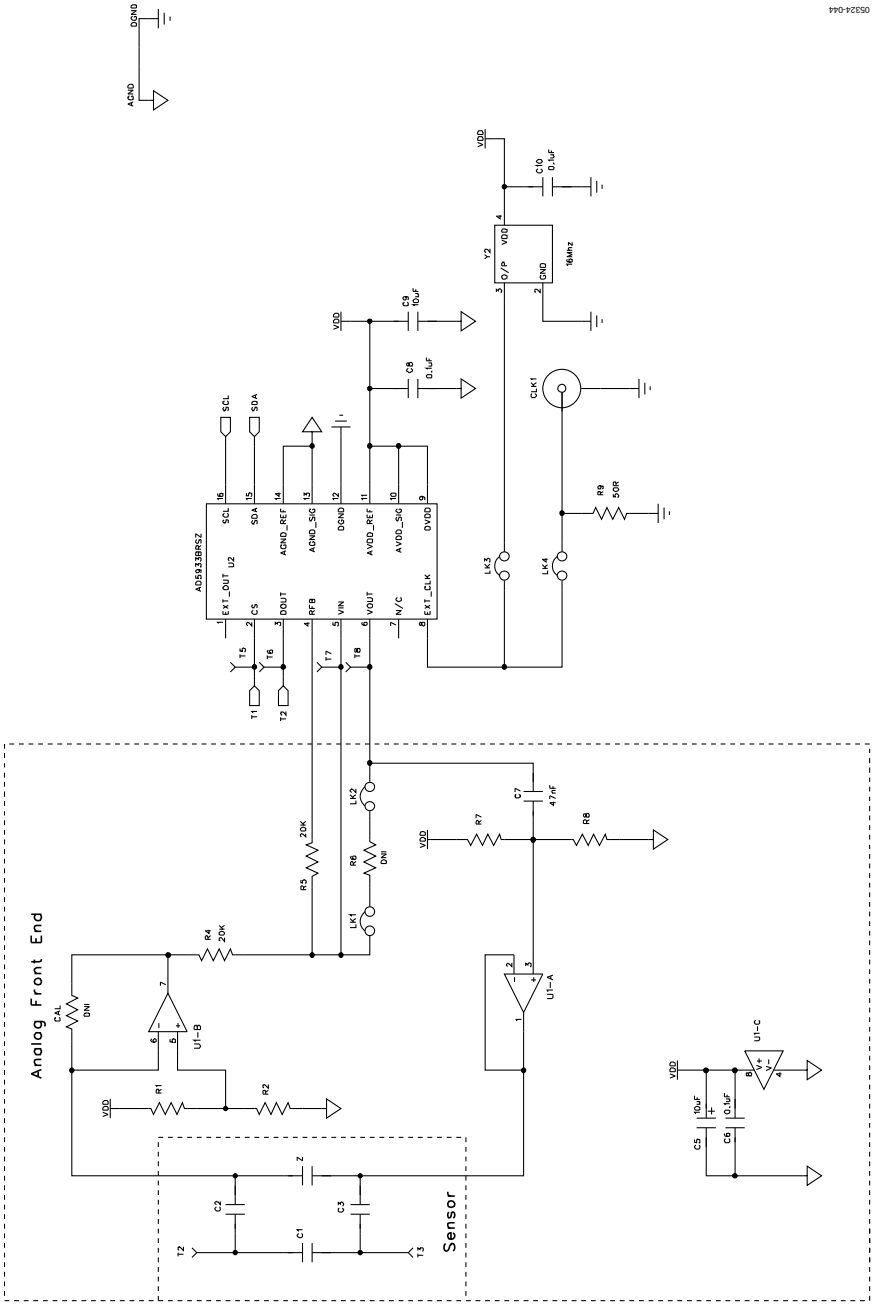

Figure 39. EVAL-AD5933EBZ USB Schematic

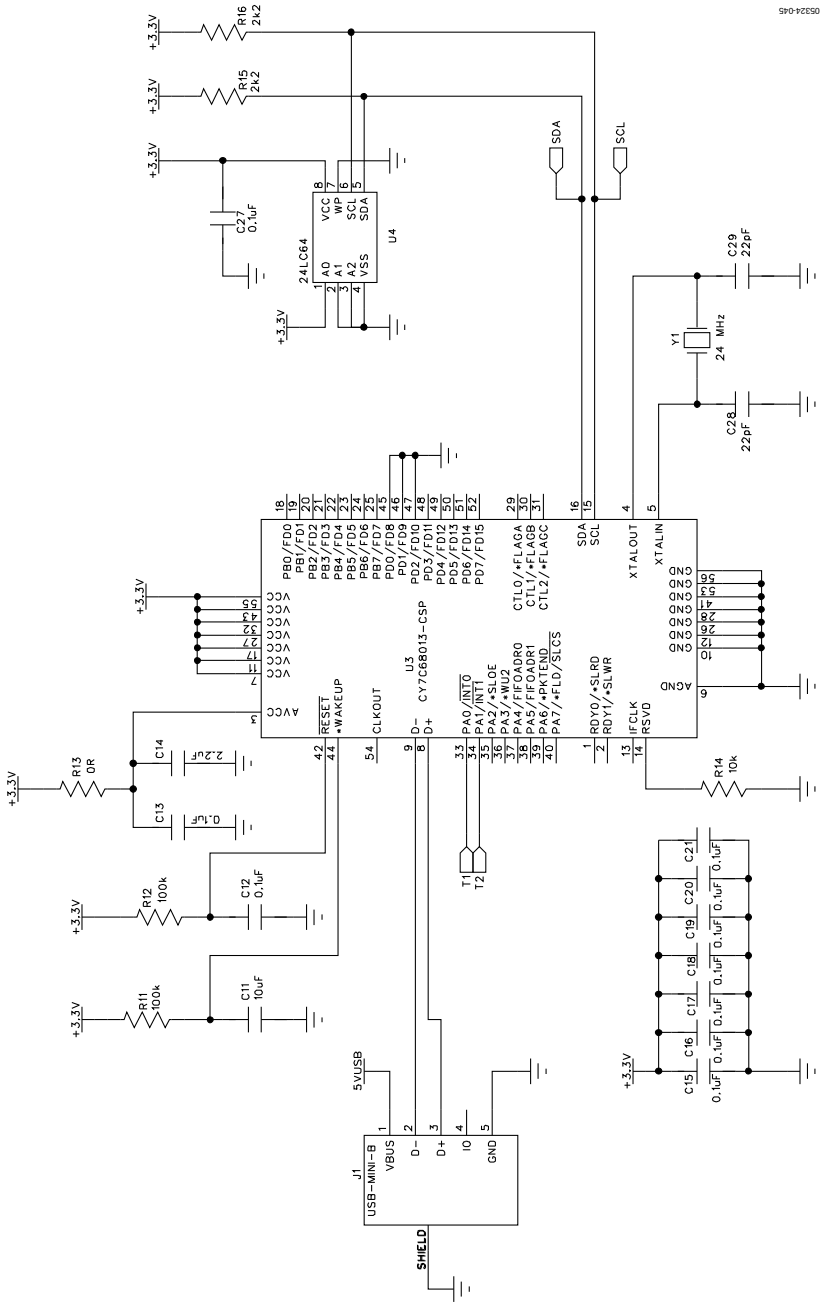

Figure 40. EVAL-AD5933EBZ Schematic

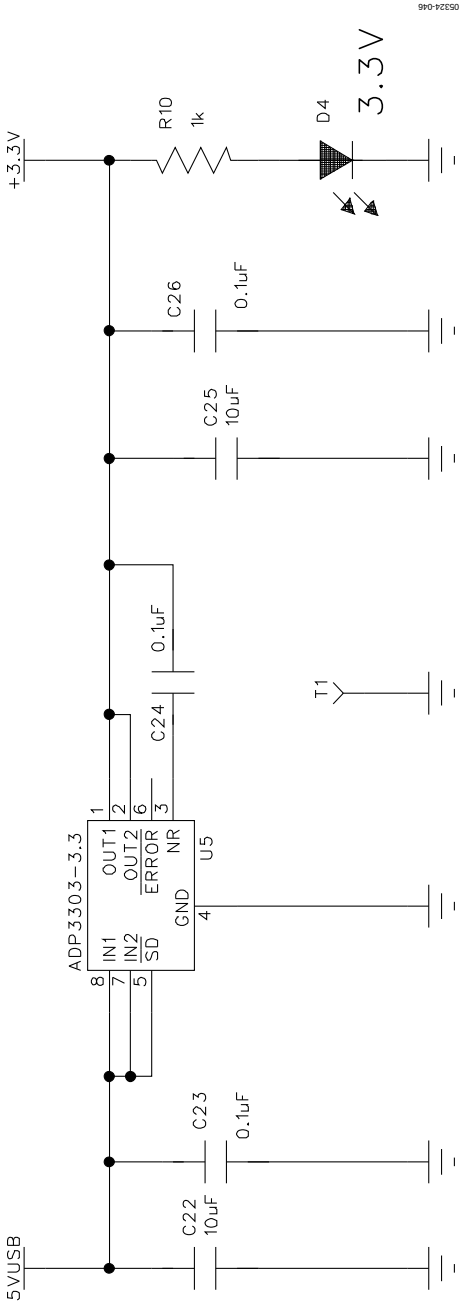

Figure 41. Linear Regulator on the EVAL-AD5933EB Evaluation Board

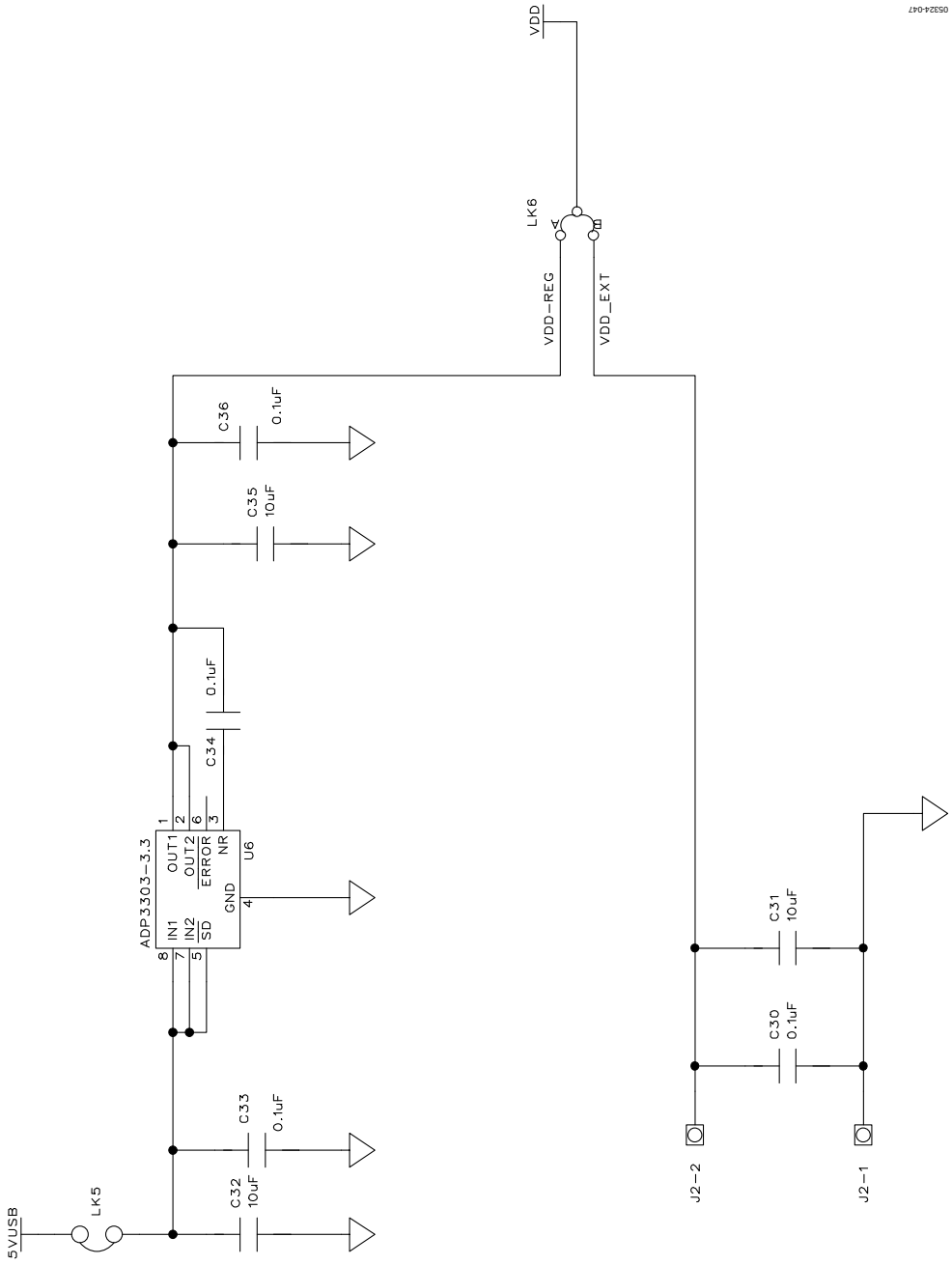

Figure 42. Decoupling on the EVAL-AD5933EB Evaluation Board

OUTLINE DIMENSIONS

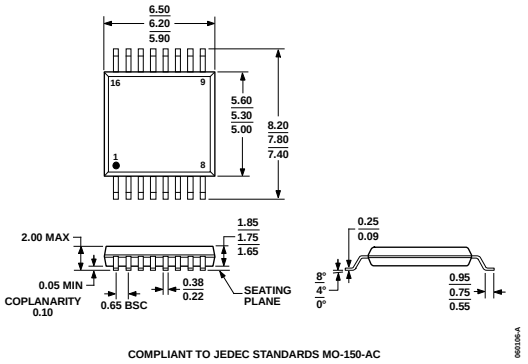

Figure 43. 16-Lead Shrink Small Outline Package [SSOP]
(RS-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
AD5933YRSZ	−40°C to +125°C	16-Lead Shrink Small Outline Package (SSOP)	RS-16
AD5933YRSZ-REEL7	−40°C to +125°C	16-Lead Shrink Small Outline Package (SSOP)	RS-16
AD5933WYRSZ-REEL7	−40°C to +125°C	16-Lead Shrink Small Outline Package (SSOP)	RS-16
EVAL-AD5933EBZ	−40°C to +125°C	Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The AD5933W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

A.2 AD8421

ANALOG DEVICES

3 nV/√Hz, Low Power Instrumentation Amplifier

Enhanced Product

AD8421-EP

FEATURES

- **Specified from −55°C to 125°C**
  - **0.9 µV/°C maximum input offset voltage drift**
  - **5 ppm/°C maximum gain drift (G = 1)**
- **Low power**
  - **2.3 mA maximum supply current**
- **Low noise**
  - **3.2 nV/√Hz maximum input voltage noise at 1 kHz**
  - **200 fA/√Hz current noise at 1 kHz**
- **Excellent ac specifications**
  - **2 MHz bandwidth (G = 100)**
  - **0.6 µs settling time to 0.001% (G = 10)**
  - **80 dB minimum CMRR at 20 kHz (G = 1)**
- **High precision dc performance**
  - **84 dB CMRR minimum (G = 1)**
  - **2 nA maximum input bias current**
- **Inputs protected to 40 V from opposite supply**
- **Gain set with a single resistor (G = 1 to 10,000)**

ENHANCED PRODUCT FEATURES

- **Supports defense and aerospace applications (AQEC standard)**
- **Military temperature range (−55°C to +125°C)**
- **Controlled manufacturing baseline**
- **One assembly/test site**
- **One fabrication site**
- **Enhanced product change notification**
- **Qualification data available on request**

PIN CONNECTION DIAGRAM

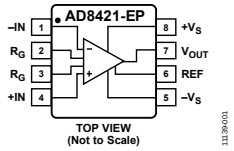

Figure 1.

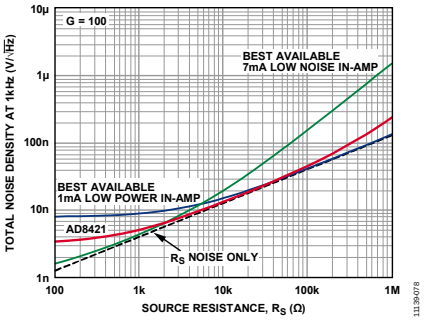

Figure 2. Noise Density vs. Source Resistance

GENERAL DESCRIPTION

The AD8421-EP is a low cost, low power, extremely low noise, ultralow bias current, high speed instrumentation amplifier that is ideally suited for a broad spectrum of signal conditioning and data acquisition applications. This product features extremely high CMRR, allowing it to extract low level signals in the presence of high frequency common-mode noise over a wide temperature range.

The 10 MHz bandwidth, 35 V/µs slew rate, and 0.6 µs settling time to 0.001% (G = 10) allow the AD8421-EP to amplify high speed signals and excel in applications that require high channel count, multiplexed systems. Even at higher gains, the current feedback architecture maintains high performance; for example, at G = 100, the bandwidth is 2 MHz and the settling time is 0.8 µs. The AD8421-EP has excellent distortion performance, making it suitable for use in demanding applications such as vibration analysis.

The AD8421-EP delivers 3 nV/√Hz input voltage noise and 200 fA/√Hz current noise with only 2 mA quiescent current, making it an ideal choice for measuring low level signals. For applications with high source impedance, the AD8421-EP employs innovative process technology and design techniques to provide noise performance that is limited only by the sensor.

The AD8421-EP uses unique protection methods to ensure robust inputs while still maintaining very low noise. This protection allows input voltages up to 40 V from the opposite supply rail without damage to the part.

A single resistor sets the gain from 1 to 10,000. The reference pin can be used to apply a precise offset to the output voltage.

The AD8421-EP is specified over the military temperature range of −55°C to +125°C. It is available in an 8-lead MSOP package.

Additional application and technical information can be found in the AD8421 data sheet.

Rev. 0 **Document Feedback**

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Tel: 781.329.4700 **Technical Support**

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REVISION HISTORY

5/13—Revision 0: Initial Version

SPECIFICATIONS

V_S = ±15 V, V_{REF} = 0 V, T_A = 25°C, G = 1, R_L = 2 kΩ, unless otherwise noted.

Table 1.

Parameter	Test Conditions/ Comments	Min	Typ	Max	Unit
COMMON-MODE REJECTION RATIO (CMRR)					
CMRR DC to 60 Hz with 1 kΩ Source Imbalance	V_{CM} = −10 V to +10 V				
G = 1		84			dB
G = 10		104			dB
G = 100		124			dB
G = 1000		134			dB
Over Temperature, G = 1	T_A = −55°C to +125°C	80			dB
CMRR at 20 kHz	V_{CM} = −10 V to +10 V				
G = 1		80			dB
G = 10		90			dB
G = 100		100			dB
G = 1000		100			dB
NOISE					
Voltage Noise, 1 kHz[1]	V_{IN}+, V_{IN}− = 0 V				
Input Voltage Noise, e_{ni}			3	3.2	nV/√Hz
Output Voltage Noise, e_{no}				60	nV/√Hz
Peak to Peak, RTI	f = 0.1 Hz to 10 Hz				
G = 1			2		µV p-p
G = 10			0.5		µV p-p
G = 100 to 1000			0.07		µV p-p
Current Noise					
Spectral Density	f = 1 kHz		200		fA/√Hz
Peak to Peak, RTI	f = 0.1 Hz to 10 Hz		18		pA p-p
VOLTAGE OFFSET[2]					
Input Offset Voltage, V_{OSI}	V_S = ±5 V to ±15 V			70	µV
Over Temperature	T_A = −55°C to +125°C			160	µV
Average TC				0.9	µV/°C
Output Offset Voltage, V_{OSO}				600	µV
Over Temperature	T_A = −55°C to +125°C			1.5	mV
Average TC				9	µV/°C
Offset RTI vs. Supply (PSR)	V_S = ±2.5 V to ±18 V				
G = 1		90	120		dB
G = 10		110	120		dB
G = 100		124	130		dB
G = 1000		130	140		dB
INPUT CURRENT					
Input Bias Current			1	2	nA
Over Temperature	T_A = −55°C to +125°C			8	nA
Average TC			50		pA/°C
Input Offset Current			0.5	2	nA
Over Temperature	T_A = −55°C to +125°C			3	nA
Average TC			1		pA/°C

Parameter	Test Conditions/ Comments	Min	Typ	Max	Unit
DYNAMIC RESPONSE					
Small Signal Bandwidth	−3 dB				
G = 1			10		MHz
G = 10			10		MHz
G = 100			2		MHz
G = 1000			0.2		MHz
Settling Time 0.01%	10 V step				
G = 1			0.7		µs
G = 10			0.4		µs
G = 100			0.6		µs
G = 1000			5		µs
Settling Time 0.001%	10 V step				
G = 1			1		µs
G = 10			0.6		µs
G = 100			0.8		µs
G = 1000			6		µs
Slew Rate					
G = 1 to 100			35		V/µs
GAIN[3]	$G = 1 + (9.9\ k\Omega/R_G)$				
Gain Range		1		10,000	V/V
Gain Error	$V_{OUT} = \pm 10$ V				
G = 1				0.05	%
G = 10 to 1000				0.3	%
Gain Nonlinearity	$V_{OUT} = -10$ V to +10 V				
G = 1	$R_L \geq 2\ k\Omega$			1	ppm
	$R_L = 600\ \Omega$		1	3	ppm
G = 10 to 1000	$R_L \geq 600\ \Omega$		30	50	ppm
	$V_{OUT} = -5$ V to +5 V		5	10	ppm
Gain vs. Temperature[3]					
G = 1				5	ppm/°C
G > 1				−80	ppm/°C
INPUT					
Input Impedance					
Differential			30‖3		GΩ‖pF
Common Mode			30‖3		GΩ‖pF
Input Operating Voltage Range[4]	$V_S = \pm 2.5$ V to ±18 V	$-V_S + 2.3$		$+V_S - 1.8$	V
Over Temperature	$T_A = -55°C$	$-V_S + 2.5$		$+V_S - 2.0$	V
	$T_A = +125°C$	$-V_S + 2.1$		$+V_S - 1.8$	V
OUTPUT	$R_L = 2\ k\Omega$				
Output Swing	$V_S = \pm 2.5$ V to ±18 V	$-V_S + 1.2$		$+V_S - 1.7$	V
Over Temperature	$T_A = -55°C$ to +125°C	$-V_S + 1.4$		$+V_S - 1.9$	V
Short-Circuit Current			65		mA
REFERENCE INPUT					
R_{IN}			20		kΩ
I_{IN}	$V_{IN}+, V_{IN}- = 0$ V		20	24	µA
Voltage Range		$-V_S$		$+V_S$	V
Reference Gain to Output			1 ± 0.0001		V/V

Parameter	Test Conditions/ Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range	Dual supply	±2.5		±18	V
	Single supply	5		36	V
Quiescent Current			2	2.3	mA
Over Temperature	T_A = −55°C to +125°C			2.8	mA
TEMPERATURE RANGE					
For Specified Performance		−55		+125	°C

[1] Total voltage noise = $\sqrt{(e_{ni}^2 + (e_{no}/G)^2 + e_{RG}^2)}$. See the AD8421 data sheet for more information.
[2] Total RTI $V_{OS} = (V_{OSI}) + (V_{OSO}/G)$.
[3] These specifications do not include the tolerance of the external gain setting resistor, R_G. For G > 1, add R_G errors to the specifications given in this table.
[4] Input voltage range of the AD8421-EP input stage only. The input range can depend on the common-mode voltage, differential voltage, gain, and reference voltage. See the Typical Performance Characteristics section for more information.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	±18 V
Output Short-Circuit Current Duration	Indefinite
Maximum Voltage at −IN or +IN[1]	$-V_S$ + 40 V
Minimum Voltage at −IN or +IN	$+V_S$ − 40 V
Maximum Voltage at REF[2]	$+V_S$ + 0.3 V
Minimum Voltage at REF	$-V_S$ − 0.3 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Maximum Junction Temperature	150°C
ESD	
Human Body Model	2 kV
Charged Device Model	1.25 kV
Machine Model	0.2 kV

[1] For voltages beyond these limits, use input protection resistors. See the AD8421 data sheet for more information.
[2] There are ESD protection diodes from the reference input to each supply, so REF cannot be driven beyond the supplies in the same way that +IN and −IN can. See the AD8421 data sheet for more information.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for a device in free air using a 4-layer JEDEC printed circuit board (PCB).

Table 3.

Package	θ_{JA}	Unit
8-Lead MSOP	138.6	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

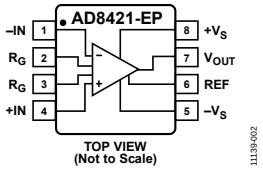

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	–IN	Negative Input Terminal.
2, 3	R_G	Gain Setting Terminals. Place resistor across the R_G pins to set the gain. G = 1 + (9.9 kΩ/R_G).
4	+IN	Positive Input Terminal.
5	$-V_S$	Negative Power Supply Terminal.
6	REF	Reference Voltage Terminal. Drive this terminal with a low impedance voltage source to level shift the output.
7	V_{OUT}	Output Terminal.
8	$+V_S$	Positive Power Supply Terminal.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = ±15 V, V_{REF} = 0 V, R_L = 2 kΩ, unless otherwise noted.

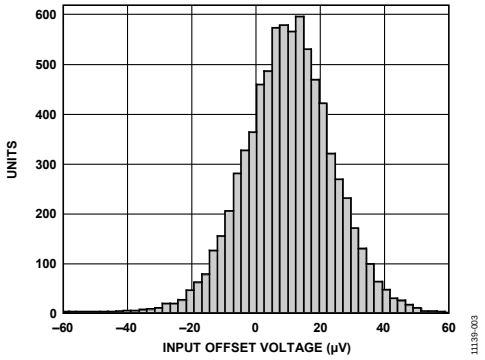

Figure 4. Typical Distribution of Input Offset Voltage

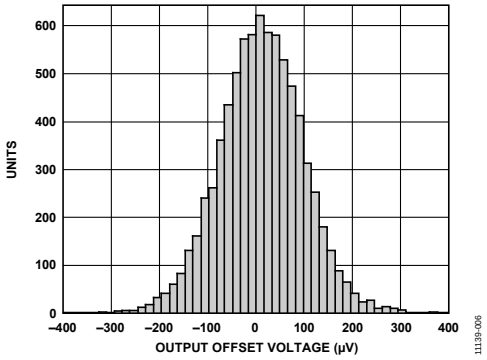

Figure 7. Typical Distribution of Output Offset Voltage

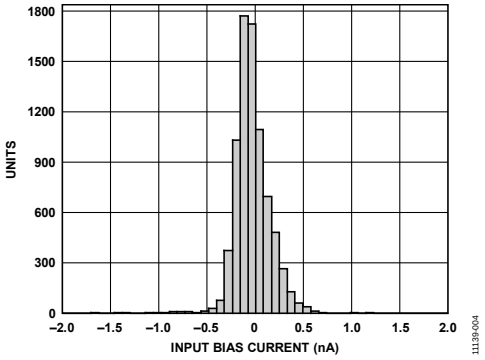

Figure 5. Typical Distribution of Input Bias Current

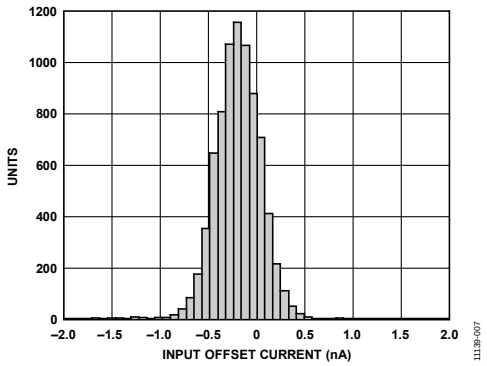

Figure 8. Typical Distribution of Input Offset Current

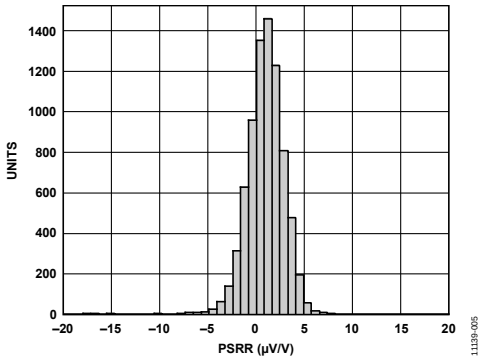

Figure 6. Typical Distribution of PSRR (G = 1)

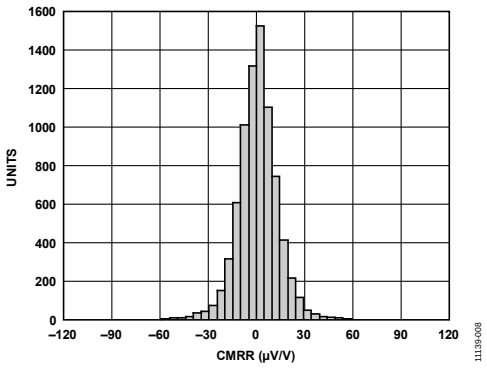

Figure 9. Typical Distribution of CMRR (G = 1)

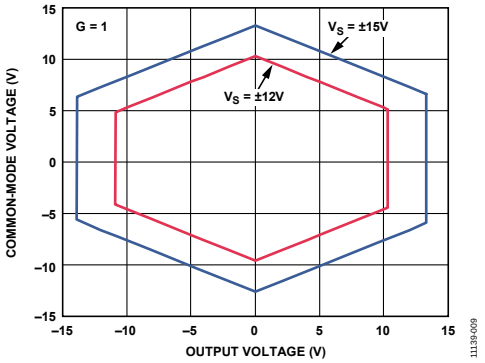

Figure 10. Input Common-Mode Voltage vs. Output Voltage; V_S = ±12 V and ±15 V (G = 1)

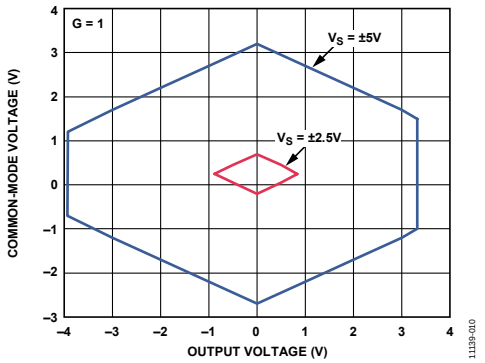

Figure 11. Input Common-Mode Voltage vs. Output Voltage; V_S = ±2.5 V and ±5 V (G = 1)

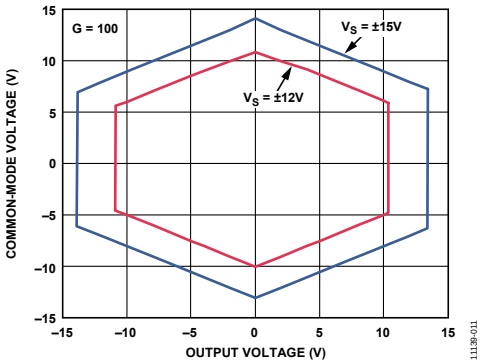

Figure 12. Input Common-Mode Voltage vs. Output Voltage; V_S = ±12 V and ±15 V (G = 100)

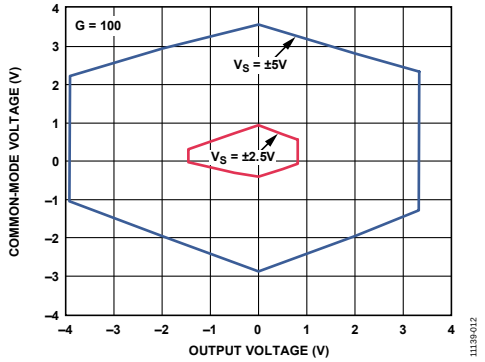

Figure 13. Input Common-Mode Voltage vs. Output Voltage; V_S = ±2.5 V and ±5 V (G = 100)

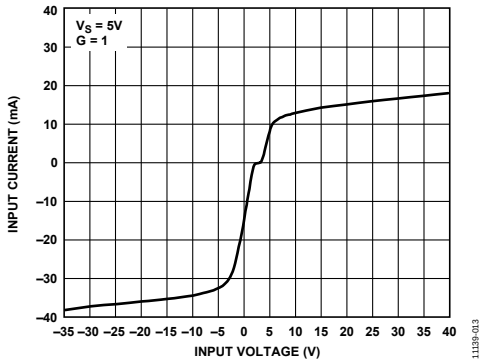

Figure 14. Input Overvoltage Performance; G = 1, $+V_S$ = 5 V, $-V_S$ = 0 V

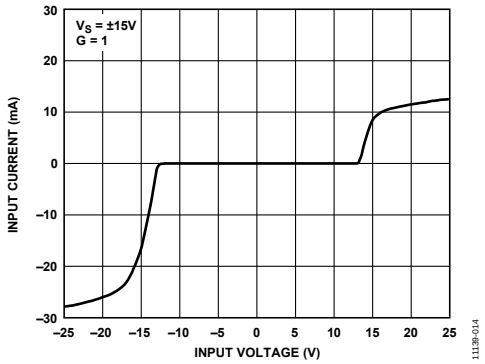

Figure 15. Input Overvoltage Performance; G = 1, V_S = ±15 V

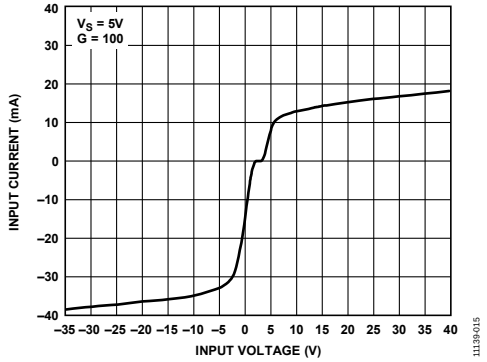

Figure 16. Input Overvoltage Performance; $+V_S$ = 5 V, $-V_S$ = 0 V, G = 100

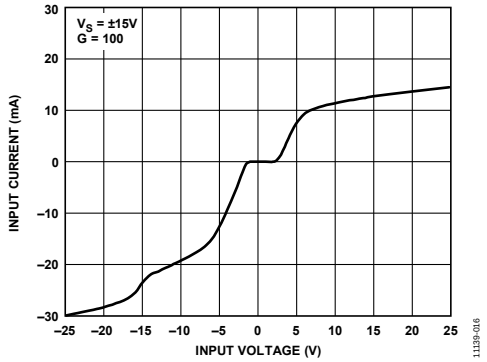

Figure 17. Input Overvoltage Performance; V_S = ±15 V, G = 100

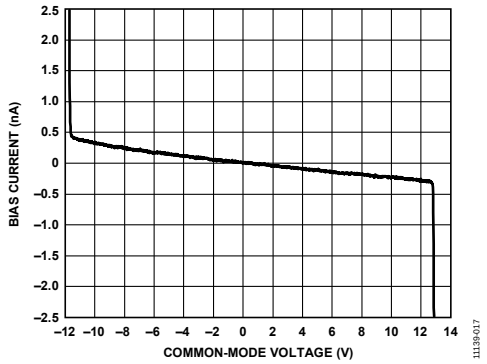

Figure 18. Input Bias Current vs. Common-Mode Voltage

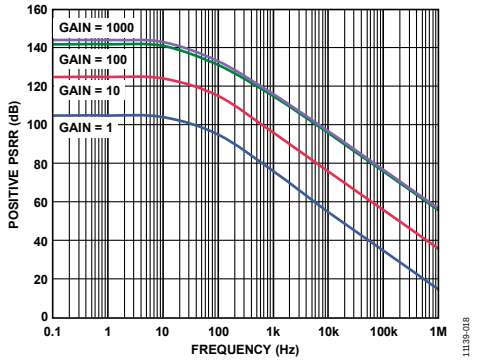

Figure 19. Positive PSRR vs. Frequency

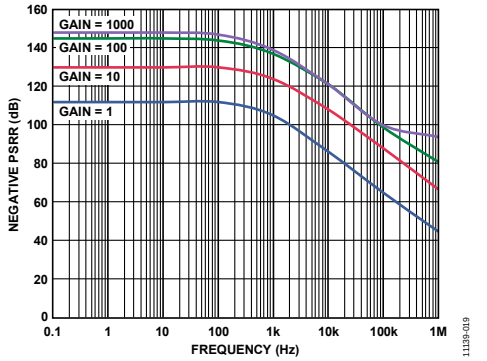

Figure 20. Negative PSRR vs. Frequency

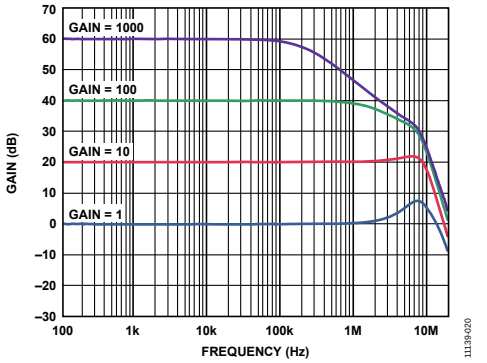

Figure 21. Gain vs. Frequency

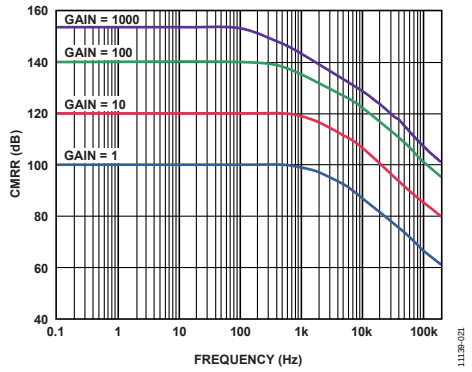

Figure 22. CMRR vs. Frequency

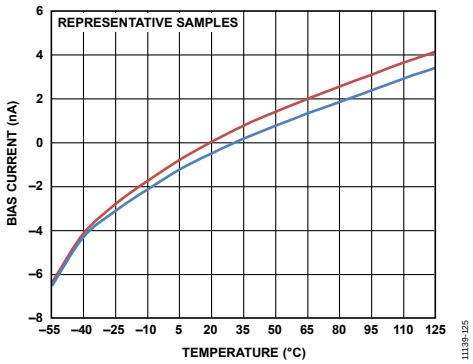

Figure 25. Input Bias Current vs. Temperature

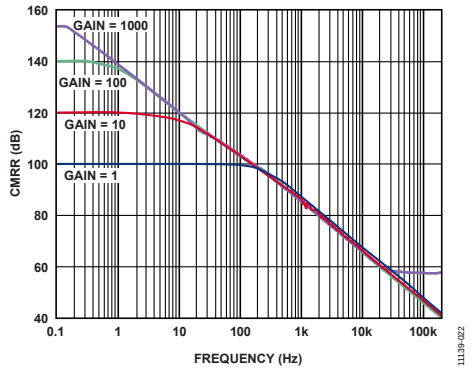

Figure 23. CMRR vs. Frequency, 1 kΩ Source Imbalance

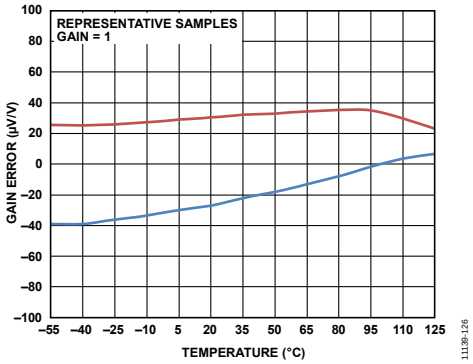

Figure 26. Gain vs. Temperature (G = 1)

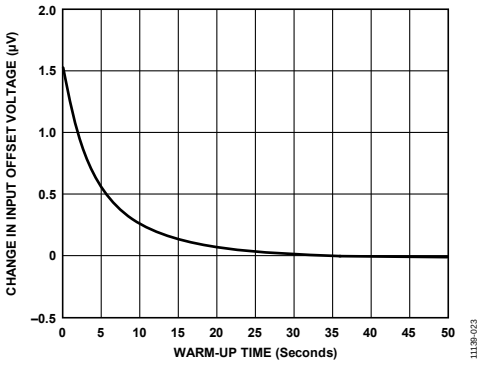

Figure 24. Change in Input Offset Voltage (V_{OSI}) vs. Warm-Up Time

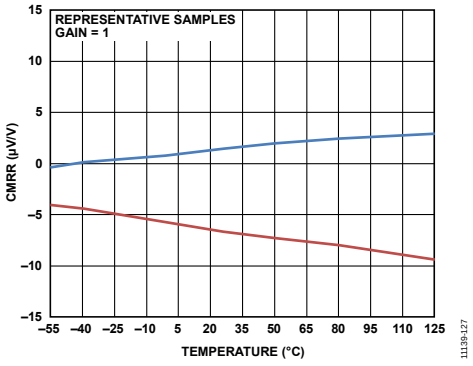

Figure 27. CMRR vs. Temperature (G = 1)

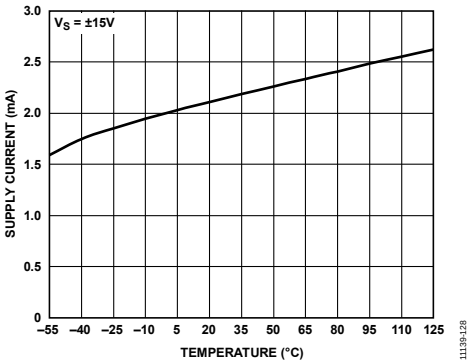

Figure 28. Supply Current vs. Temperature (G = 1)

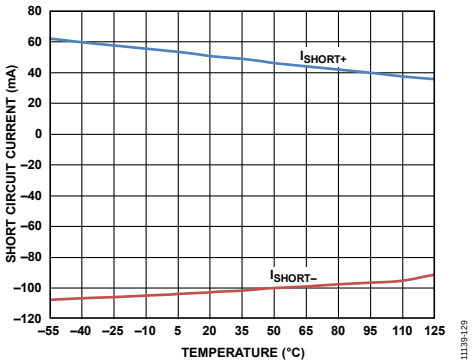

Figure 29. Short-Circuit Current vs. Temperature (G = 1)

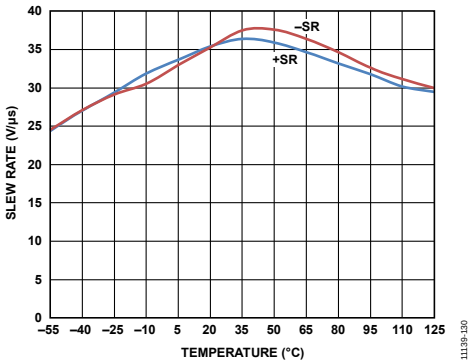

Figure 30. Slew Rate vs. Temperature, V_S = ±15 V (G = 1)

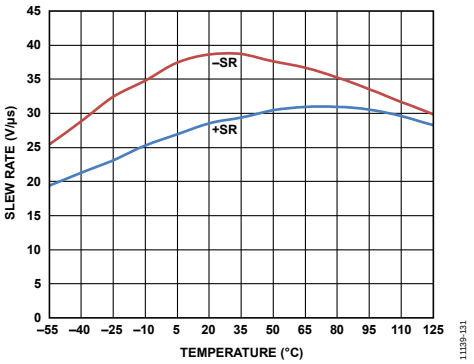

Figure 31. Slew Rate vs. Temperature, V_S = ±5 V (G = 1)

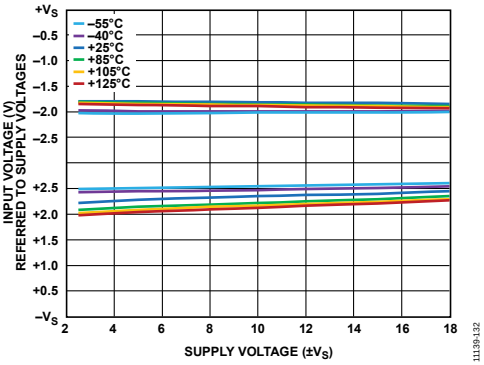

Figure 32. Input Voltage Limit vs. Supply Voltage

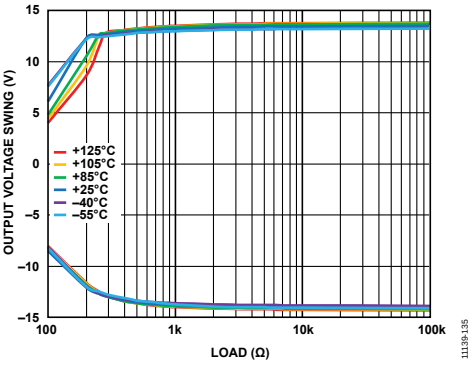

Figure 33. Output Voltage Swing vs. Load Resistance

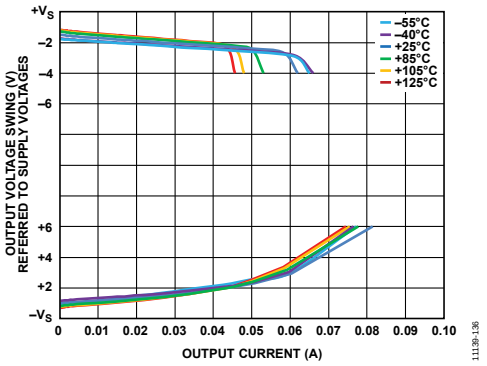

Figure 34. Output Voltage Swing vs. Output Current

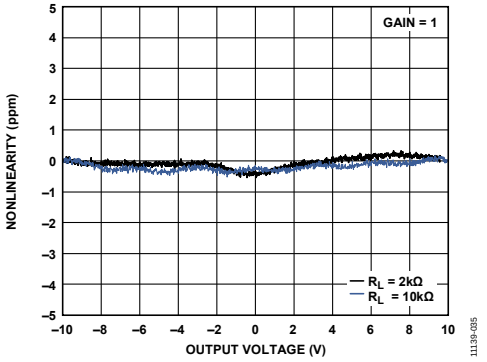

Figure 35. Gain Nonlinearity (G = 1), R_L = 10 kΩ, 2 kΩ

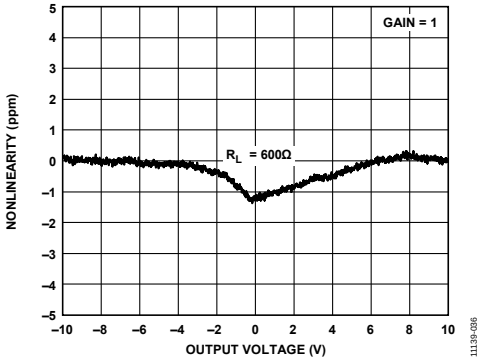

Figure 36. Gain Nonlinearity (G = 1), R_L = 600 Ω

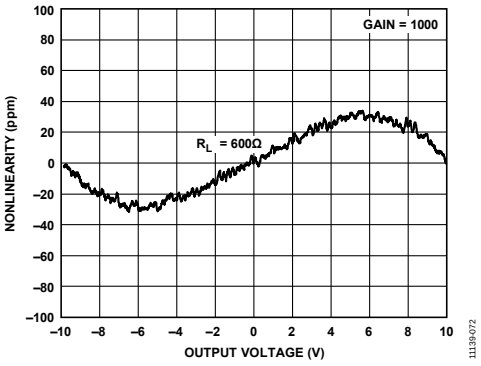

Figure 37. Gain Nonlinearity (G = 1000), R_L = 600 Ω, V_{OUT} = ±10 V

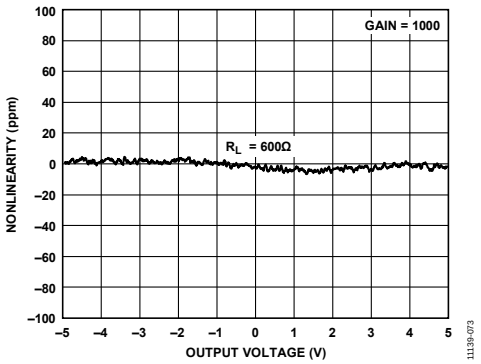

Figure 38. Gain Nonlinearity (G = 1000), R_L = 600 Ω, V_{OUT} = ±5 V

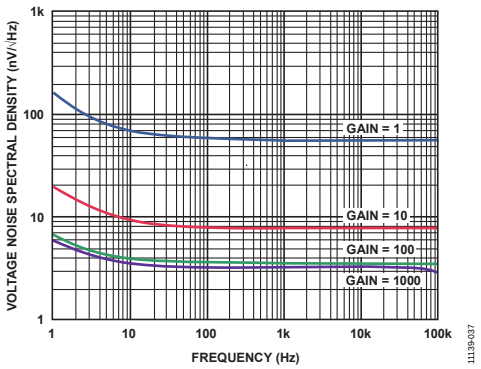

Figure 39. RTI Voltage Noise Spectral Density vs. Frequency

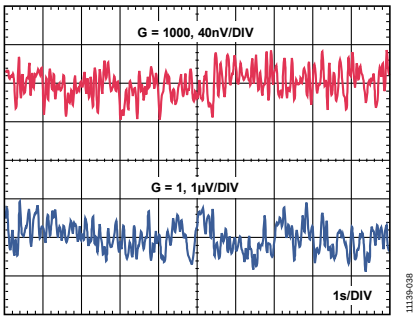

Figure 40. 0.1 Hz to 10 Hz RTI Voltage Noise (G = 1, G = 1000)

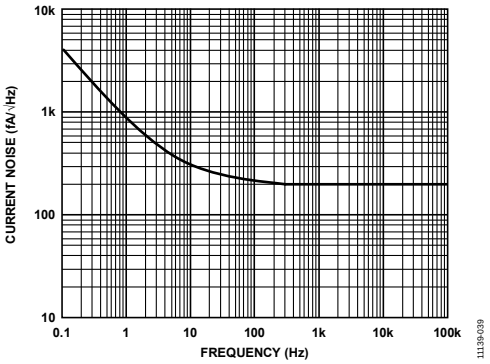

Figure 41. Current Noise Spectral Density vs. Frequency

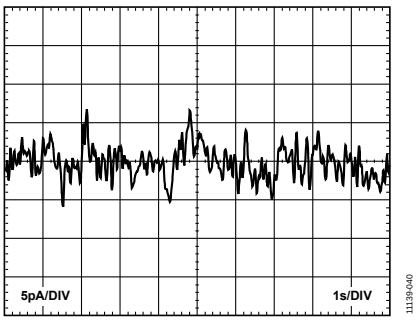

Figure 42. 0.1 Hz to 10 Hz Current Noise

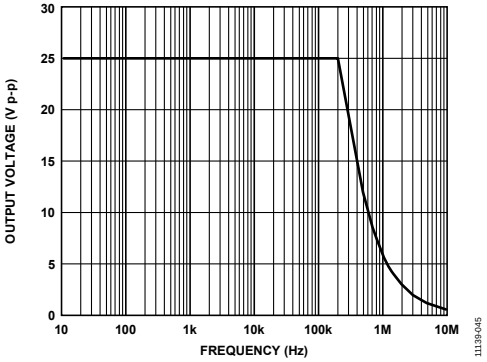

Figure 43. Large Signal Frequency Response

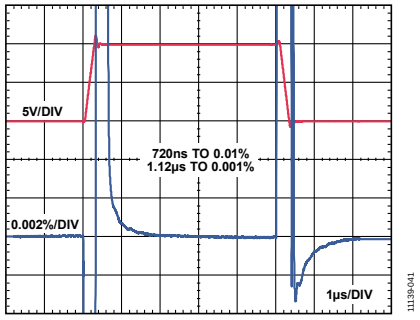

Figure 44. Large Signal Pulse Response and Settling Time (G = 1), 10 V Step, V_S = ±15 V, R_L = 2 kΩ, C_L = 100 pF

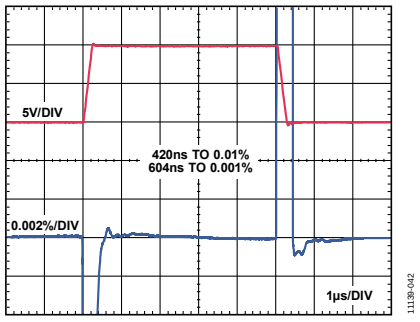

Figure 45. Large Signal Pulse Response and Settling Time (G = 10), 10 V Step, V_S = ±15 V, R_L = 2 kΩ, C_L = 100 pF

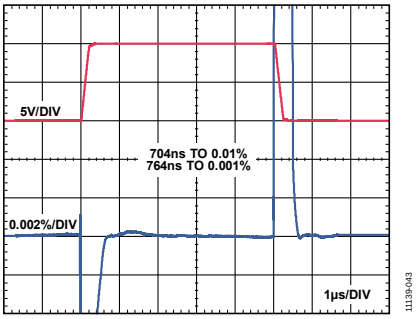

Figure 46. Large Signal Pulse Response and Settling Time (G = 100), 10 V Step, V_S = ±15 V, R_L = 2 kΩ, C_L = 100 pF

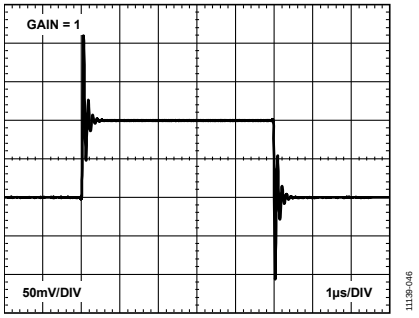

Figure 49. Small Signal Pulse Response (G = 1), R_L = 600 Ω, C_L = 100 pF

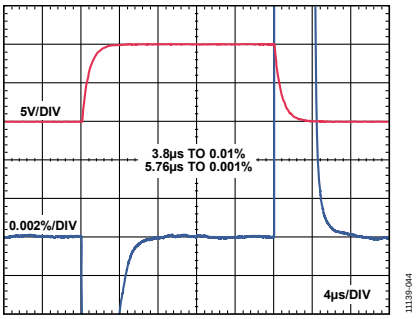

Figure 47. Large Signal Pulse Response and Settling Time (G = 1000), 10 V Step, V_S = ±15 V, R_L = 2 kΩ, C_L = 100 pF

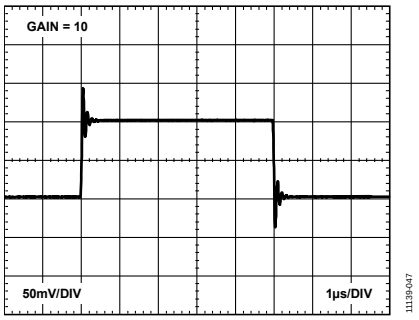

Figure 50. Small Signal Pulse Response (G = 10), R_L = 600 Ω, C_L = 100 pF

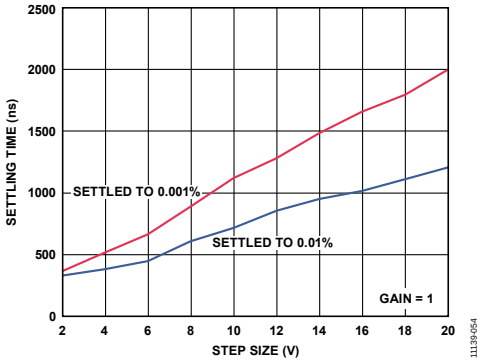

Figure 48. Settling Time vs. Step Size (G = 1), R_L = 2 kΩ, C_L = 100 pF

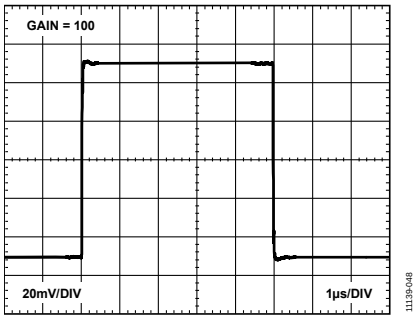

Figure 51. Small Signal Pulse Response (G = 100), RL = 600 Ω, CL = 100 pF

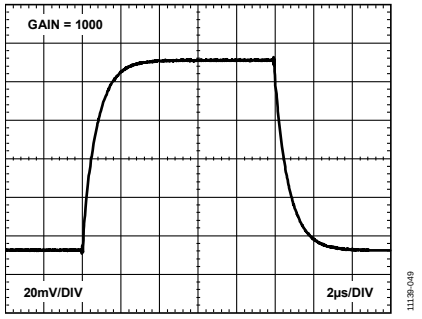

Figure 52. Small Signal Pulse Response (G = 1000), R_L = 600 Ω, C_L = 100 pF

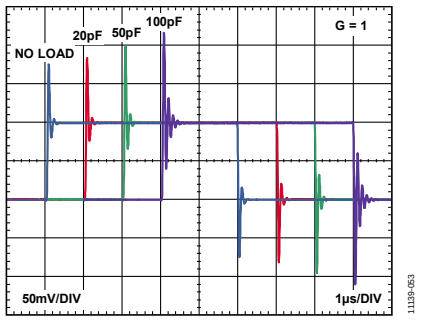

Figure 53. Small Signal Response with Various Capacitive Loads (G = 1), R_L = Infinity

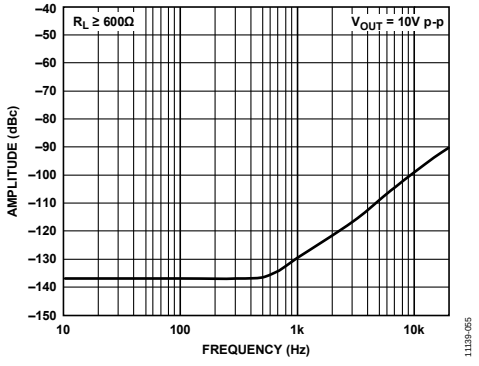

Figure 54. Second Harmonic Distortion vs. Frequency (G = 1)

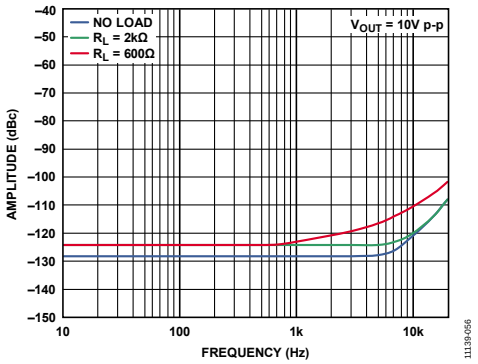

Figure 55. Third Harmonic Distortion vs. Frequency (G = 1)

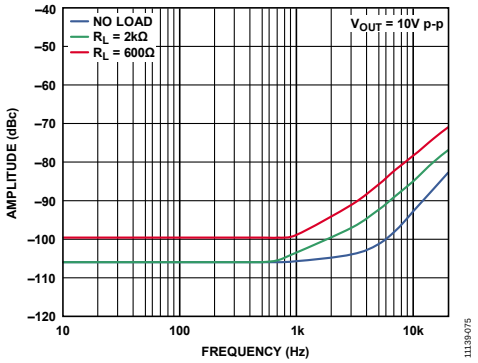

Figure 56. Second Harmonic Distortion vs. Frequency (G = 1000)

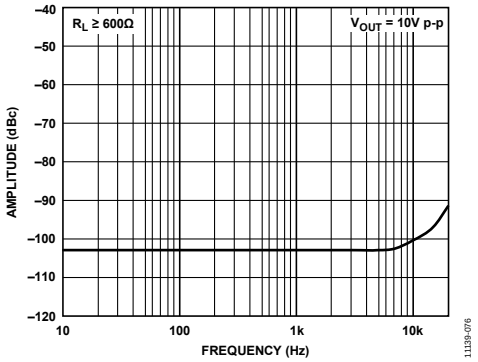

Figure 57. Third Harmonic Distortion vs. Frequency (G = 1000)

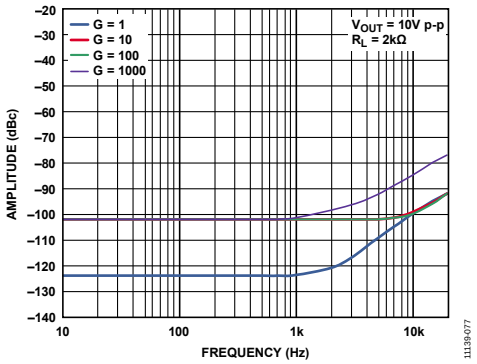

Figure 58. THD vs. Frequency

OUTLINE DIMENSIONS

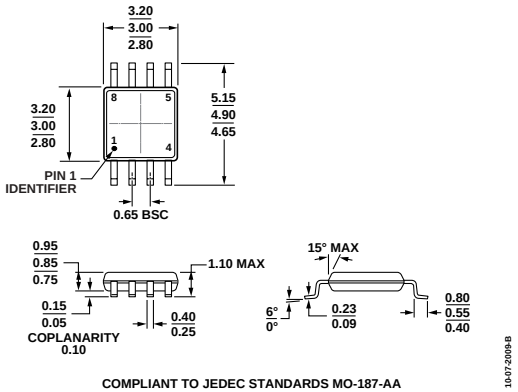

Figure 59. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
AD8421TRMZ-EP	−55°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	Y4T
AD8421TRMZ-EP-R7	−55°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	Y4T

[1] Z = RoHS Compliant Part.

NOTES

NOTES

A.3 AD8606

Precision, Low Noise, CMOS, Rail-to-Rail, Input/Output Operational Amplifiers

Data Sheet **AD8605/AD8606/AD8608**

FEATURES

- Low offset voltage: 65 µV maximum
- Low input bias currents: 1 pA maximum
- Low noise: 8 nV/√Hz
- Wide bandwidth: 10 MHz
- High open-loop gain: 1000 V/mV
- Unity gain stable
- Single-supply operation: 2.7 V to 5.5 V
- 5-ball WLCSP for single (AD8605) and 8-ball WLCSP for dual (AD8606)

APPLICATIONS

- Photodiode amplification
- Battery-powered instrumentation
- Multipole filters
- Sensors
- Barcode scanners
- Audio

GENERAL DESCRIPTION

The AD8605, AD8606, and AD8608[1] are single, dual, and quad rail-to-rail input and output, single-supply amplifiers. They feature very low offset voltage, low input voltage and current noise, and wide signal bandwidth. They use the Analog Devices, Inc. patented DigiTrim® trimming technique, which achieves superior precision without laser trimming.

The combination of low offsets, low noise, very low input bias currents, and high speed makes these amplifiers useful in a wide variety of applications. Filters, integrators, photodiode amplifiers, and high impedance sensors all benefit from the combination of performance features. Audio and other ac applications benefit from the wide bandwidth and low distortion. Applications for these amplifiers include optical control loops, portable and loop-powered instrumentation, and audio amplification for portable devices.

The AD8605, AD8606, and AD8608 are specified over the extended industrial temperature range (−40°C to +125°C). The AD8605 single is available in 5-lead SOT-23 and 5-ball WLCSP packages. The AD8606 dual is available in an 8-lead MSOP, an 8-ball WLSCP, and a narrow SOIC surface-mounted package. The AD8608 quad is available in a 14-lead TSSOP package and a narrow 14-lead SOIC package. The 5-ball and 8-ball WLCSP offer the smallest available footprint for any surface-mounted operational amplifier. The WLCSP, SOT-23, MSOP, and TSSOP versions are available in tape-and-reel only.

[1] Protected by U.S. Patent No. 5,969,657.

PIN CONFIGURATIONS

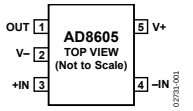

Figure 1. 5-Lead SOT-23 (RJ Suffix)

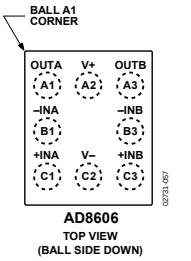

Figure 2. 8-Ball WLCSP (CB Suffix)

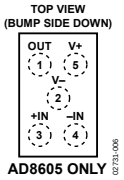

Figure 3. 5-Ball WLCSP (CB Suffix)

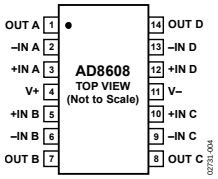

Figure 4. 14-Lead SOIC_N (R Suffix)

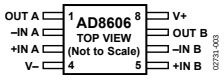

Figure 5. 8-Lead MSOP (RM Suffix), 8-Lead SOIC_N (R Suffix)

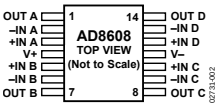

Figure 6. 14-Lead TSSOP (RU Suffix)

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Technical Support www.analog.com

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5 V ELECTRICAL SPECIFICATIONS

V_S = 5 V, V_{CM} = V_S/2, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}					
AD8605/AD8606 (Except WLCSP)		V_S = 3.5 V, V_{CM} = 3 V		20	65	µV
AD8608		V_S = 3.5 V, V_{CM} = 2.7 V		20	75	µV
AD8605/AD8606/AD8608		V_S = 5 V, V_{CM} = 0 V to 5 V		80	300	µV
		−40°C < T_A < +125°C			750	µV
Input Bias Current	I_B			0.2	1	pA
AD8605/AD8606		−40°C < T_A < +85°C			50	pA
AD8605/AD8606		−40°C < T_A < +125°C			250	pA
AD8608		−40°C < T_A < +85°C			100	pA
AD8608		−40°C < T_A < +125°C			300	pA
Input Offset Current	I_{OS}			0.1	0.5	pA
		−40°C < T_A < +85°C			20	pA
		−40°C < T_A < +125°C			75	pA
Input Voltage Range			0		5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 5 V	85	100		dB
		−40°C < T_A < +125°C	75	90		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = 0.5 V to 4.5 V	300	1000		V/mV
Offset Voltage Drift						
AD8605/AD8606	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C		1	4.5	µV/°C
AD8608	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C		1.5	6.0	µV/°C
INPUT CAPACITANCE						
Common-Mode Input Capacitance	C_{COM}			8.8		pF
Differential Input Capacitance	C_{DIFF}			2.6		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1 mA	4.96	4.98		V
		I_L = 10 mA	4.7	4.79		V
		−40°C < T_A < +125°C	4.6			V
Output Voltage Low	V_{OL}	I_L = 1 mA		20	40	mV
		I_L= 10 mA		170	210	mV
		−40°C < T_A < +125°C			290	mV
Output Current	I_{OUT}			±80		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		1		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR					
AD8605/AD8606		V_S = 2.7 V to 5.5 V	80	95		dB
AD8605/AD8606 WLCSP		V_S = 2.7 V to 5.5 V	75	92		dB
AD8608		V_S = 2.7 V to 5.5 V	77	92		dB
		−40°C < T_A < +125°C	70	90		dB
Supply Current/Amplifier	I_{SY}	I_{OUT} = 0 mA		1	1.2	mA
		−40°C < T_A < +125°C			1.4	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ, C_L = 16 pF		5		V/µs
Settling Time	t_S	To 0.01%, 0 V to 2 V step, A_V = 1		<1		µs
Unity Gain Bandwidth Product	GBP			10		MHz
Phase Margin	Φ_M			65		Degrees

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
NOISE PERFORMANCE						
Peak-to-Peak Noise	e_n p-p	f = 0.1 Hz to 10 Hz		2.3	3.5	μV p-p
Voltage Noise Density	e_n	f = 1 kHz		8	12	nV/√Hz
	e_n	f = 10 kHz		6.5		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.01		pA/√Hz

2.7 V ELECTRICAL SPECIFICATIONS

V_S = 2.7 V, V_{CM} = V_S/2, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}					
AD8605/AD8606 (Except WLCSP)		V_S = 3.5 V, V_{CM} = 3 V		20	65	µV
AD8608		V_S = 3.5 V, V_{CM} = 2.7 V		20	75	µV
AD8605/AD8606/AD8608		V_S = 2.7 V, V_{CM} = 0 V to 2.7 V		80	300	µV
		−40°C < T_A < +125°C			750	µV
Input Bias Current	I_B			0.2	1	pA
AD8605/AD8606		−40°C < T_A < +85°C			50	pA
AD8605/AD8606		−40°C < T_A < +125°C			250	pA
AD8608		−40°C < T_A < +85°C			100	pA
AD8608		−40°C < T_A < +125°C			300	pA
Input Offset Current	I_{OS}			0.1	0.5	pA
		−40°C < T_A < +85°C			20	pA
		−40°C < T_A < +125°C			75	pA
Input Voltage Range			0		2.7	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 2.7 V	80	95		dB
		−40°C < T_A < +125°C	70	85		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = 0.5 V to 2.2 V	110	350		V/mV
Offset Voltage Drift						
AD8605/AD8606	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C		1	4.5	µV/°C
AD8608	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C		1.5	6.0	µV/°C
INPUT CAPACITANCE						
Common-Mode Input Capacitance	C_{COM}			8.8		pF
Differential Input Capacitance	C_{DIFF}			2.6		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1 mA	2.6	2.66		V
		−40°C < T_A < +125°C	2.6			V
Output Voltage Low	V_{OL}	I_L = 1 mA		25	40	mV
		−40°C < T_A < +125°C			50	mV
Output Current	I_{OUT}			±30		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		1.2		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR					
AD8605/AD8606		V_S = 2.7 V to 5.5 V	80	95		dB
AD8605/AD8606 WLCSP		V_S = 2.7 V to 5.5 V	75	92		dB
AD8608		V_S = 2.7 V to 5.5 V	77	92		dB
		−40°C < T_A < +125°C	70	90		dB
Supply Current/Amplifier	I_{SY}	I_{OUT} = 0 mA		1.15	1.4	mA
		−40°C < T_A < +125°C			1.5	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ, C_L = 16 pF		5		V/µs
Settling Time	t_S	To 0.01%, 0 V to 1 V step, A_V = 1		<0.5		µs
Unity Gain Bandwidth Product	GBP			9		MHz
Phase Margin	Φ_M			50		Degrees

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
NOISE PERFORMANCE						
Peak-to-Peak Noise	e_n p-p	f = 0.1 Hz to 10 Hz		2.3	3.5	μV p-p
Voltage Noise Density	e_n	f = 1 kHz		8	12	nV/√Hz
	e_n	f = 10 kHz		6.5		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.01		pA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	GND to V_S
Differential Input Voltage	6 V
Output Short-Circuit Duration to GND	Observe Derating Curves
Storage Temperature Range	
All Packages	−65°C to +150°C
Operating Temperature Range	
All Packages	−40°C to +125°C
Junction Temperature Range	
All Packages	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4.

Package Type	θ_{JA}[1]	θ_{JC}	Unit
5-Ball WLCSP (CB)	170		°C/W
5-Lead SOT-23 (RJ)	240	92	°C/W
8-Ball WLCSP (CB)	115		°C/W
8-Lead MSOP (RM)	206	44	°C/W
8-Lead SOIC_N (R)	157	56	°C/W
14-Lead SOIC_N (R)	105	36	°C/W
14-Lead TSSOP (RU)	148	23	°C/W

[1] θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

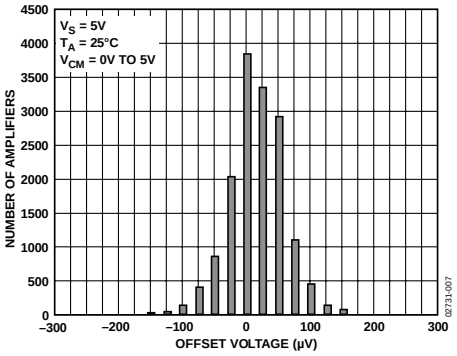


Figure 7. Input Offset Voltage Distribution

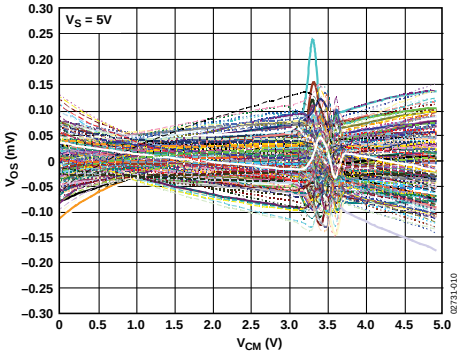


Figure 10. Input Offset Voltage vs. Common-Mode Voltage (200 Units, 5 Wafer Lots, Including Process Skews)

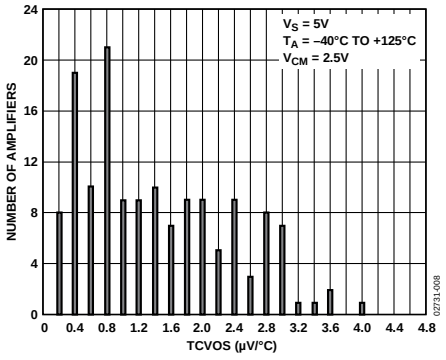


Figure 8. AD8608 Input Offset Voltage Drift Distribution

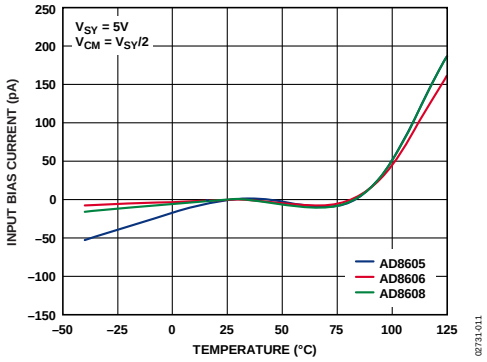


Figure 11. Input Bias Current vs. Temperature

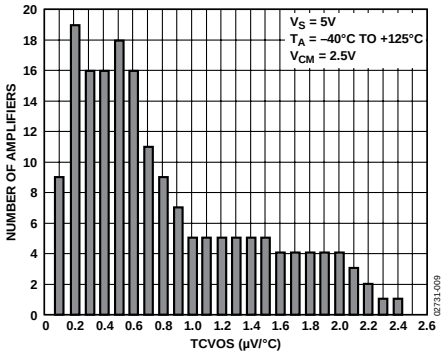


Figure 9. AD8605/AD8606 Input Offset Voltage Drift Distribution

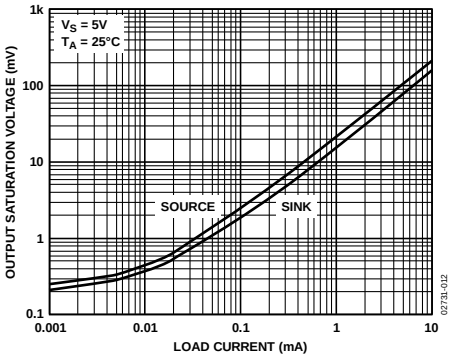


Figure 12. Output Saturation Voltage vs. Load Current

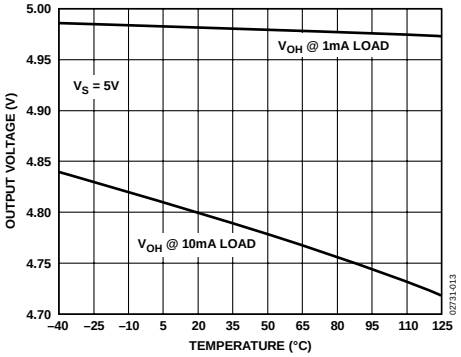


Figure 13. Output Voltage Swing High vs. Temperature

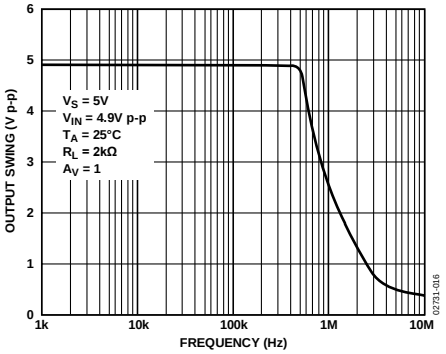


Figure 16. Closed-Loop Output Voltage Swing (FPBW)

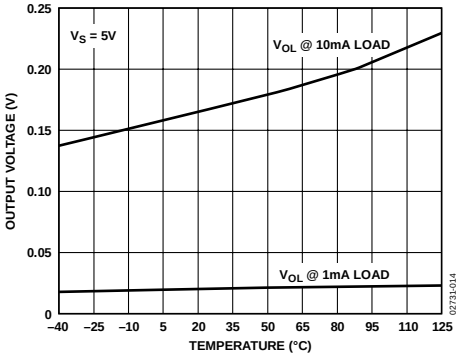


Figure 14. Output Voltage Swing Low vs. Temperature

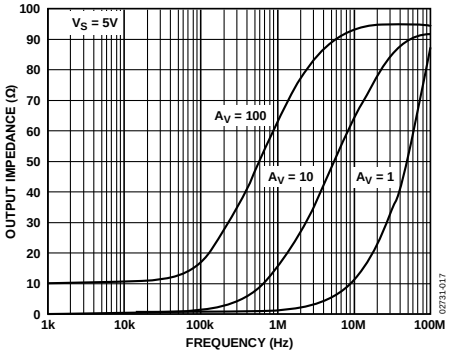


Figure 17. Output Impedance vs. Frequency

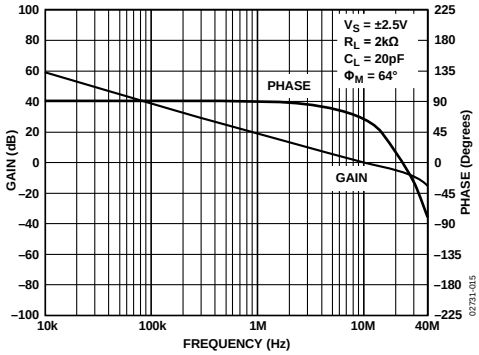


Figure 15. Open-Loop Gain and Phase vs. Frequency

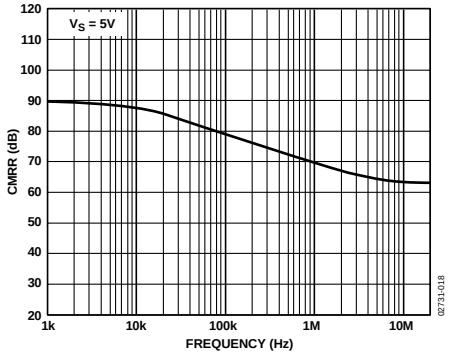


Figure 18. Common-Mode Rejection Ratio (CMRR) vs. Frequency

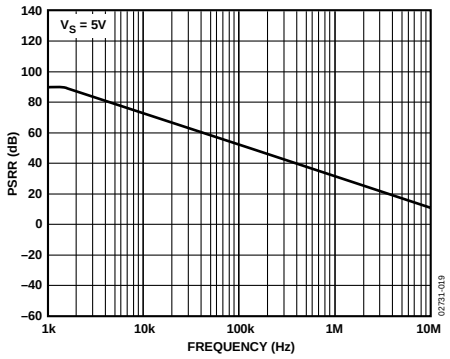


Figure 19. PSRR vs. Frequency

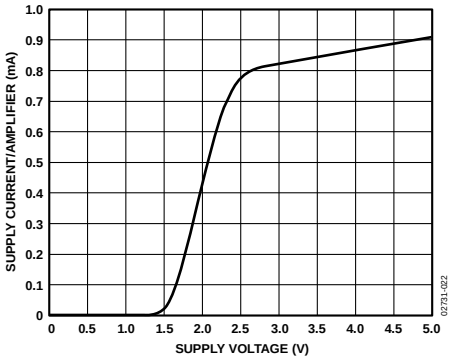


Figure 22. Supply Current/Amplifier vs. Supply Voltage

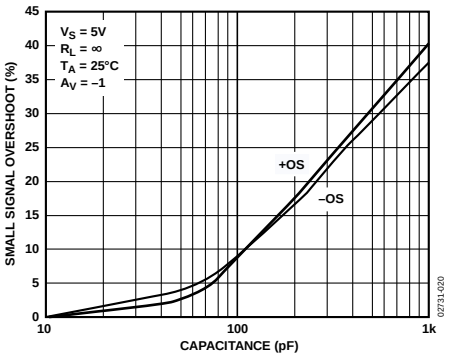


Figure 20. Small Signal Overshoot vs. Load Capacitance

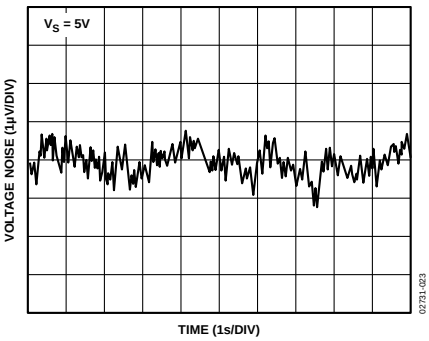


Figure 23. 0.1 Hz to 10 Hz Input Voltage Noise

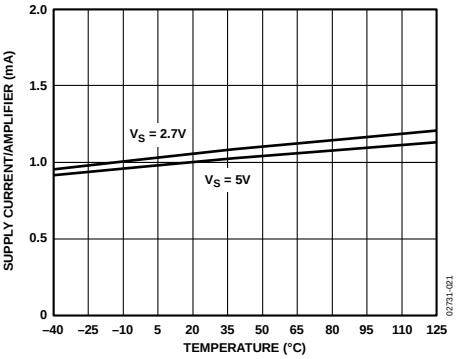


Figure 21. Supply Current/Amplifier vs. Temperature

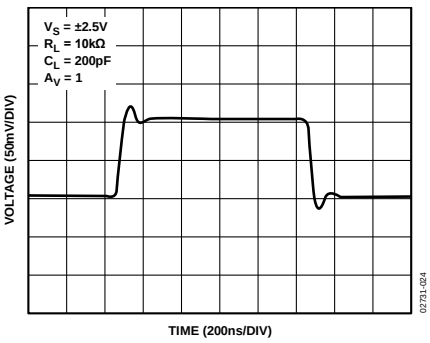


Figure 24. Small Signal Transient Response

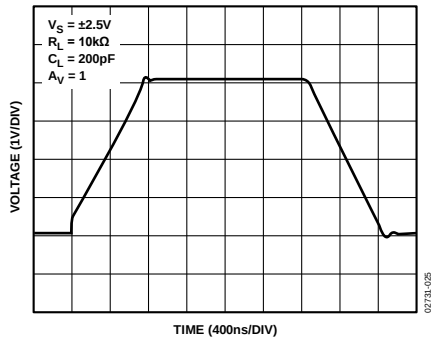


Figure 25. Large Signal Transient Response

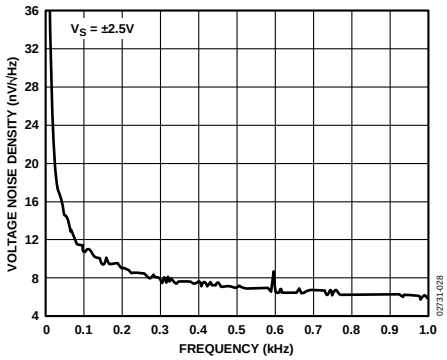


Figure 28. Voltage Noise Density vs. Frequency

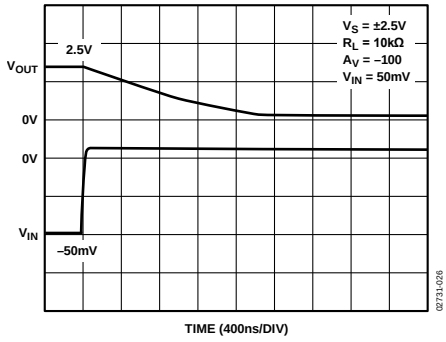


Figure 26. Positive Overload Recovery

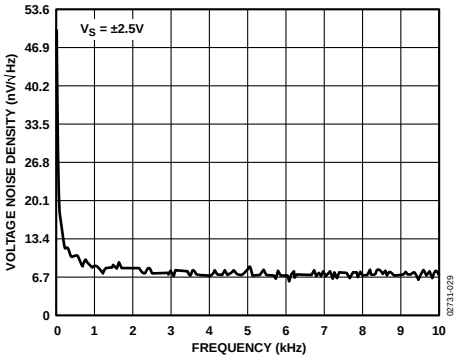


Figure 29. Voltage Noise Density vs. Frequency

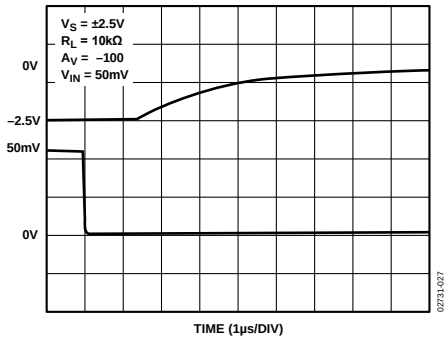


Figure 27. Negative Overload Recovery

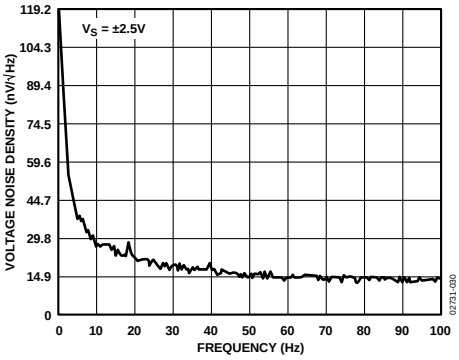


Figure 30. Voltage Noise Density vs. Frequency

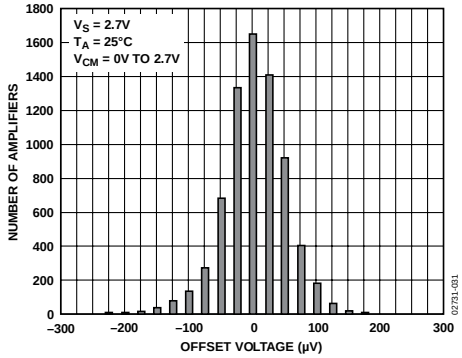


Figure 31. Input Offset Voltage Distribution

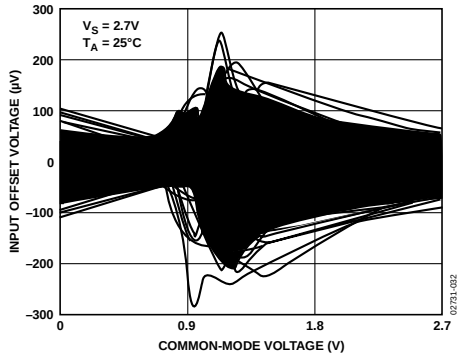


Figure 32. Input Offset Voltage vs. Common-Mode Voltage (200 Units, 5 Wafer Lots, Including Process Skews)

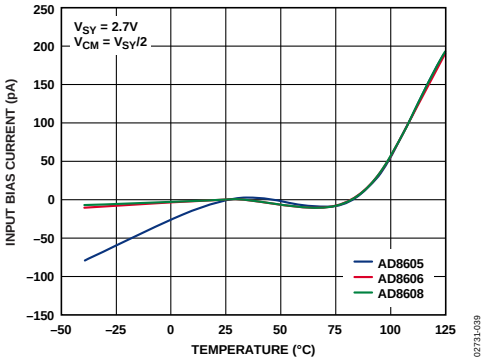


Figure 33. Input Bias Current vs. Temperature

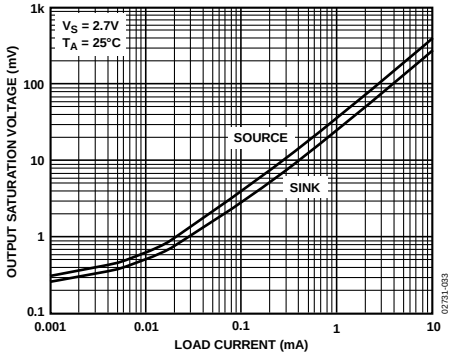


Figure 34. Output Saturation Voltage vs. Load Current

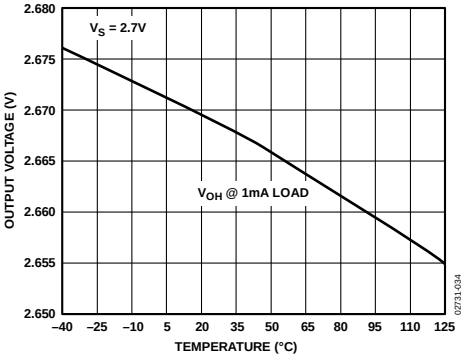


Figure 35. Output Voltage Swing High vs. Temperature

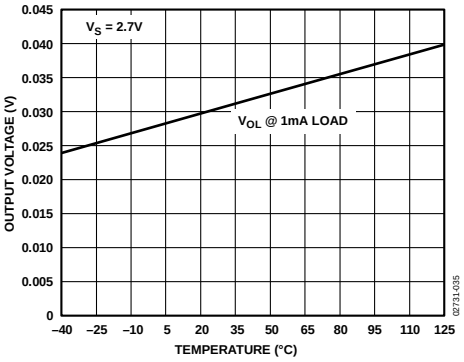


Figure 36. Output Voltage Swing Low vs. Temperature

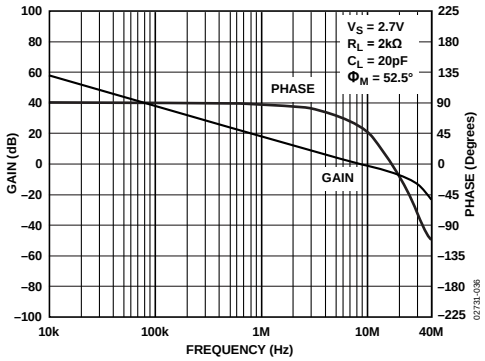


Figure 37. Open-Loop Gain and Phase vs. Frequency

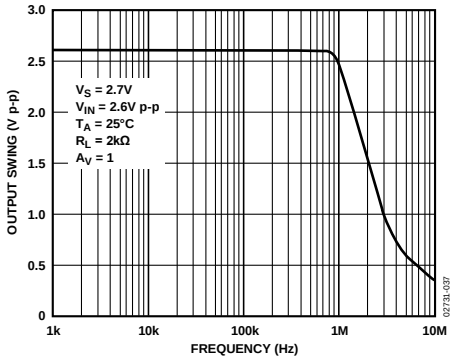


Figure 38. Closed-Loop Output Voltage Swing vs. Frequency (FPBW)

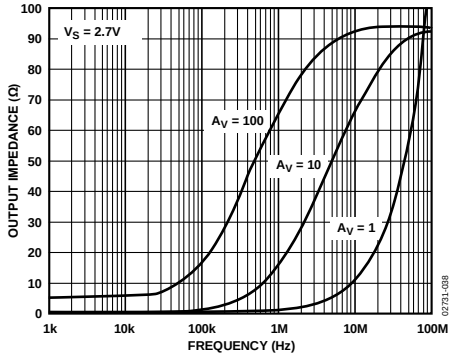


Figure 39. Output Impedance vs. Frequency

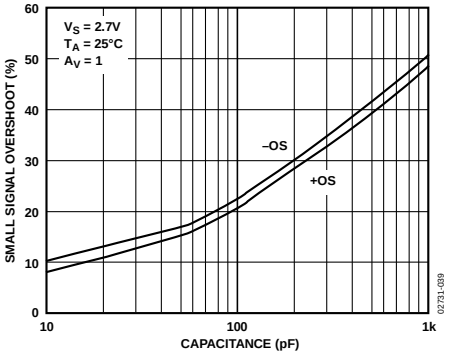


Figure 40. Small Signal Overshoot vs. Load Capacitance

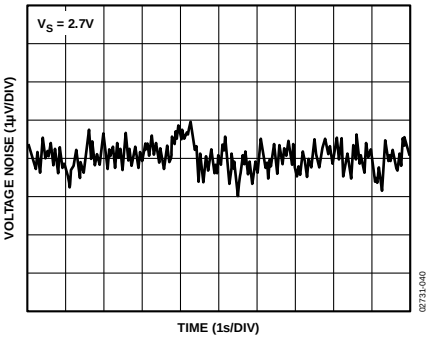


Figure 41. 0.1 Hz to 10 Hz Input Voltage Noise

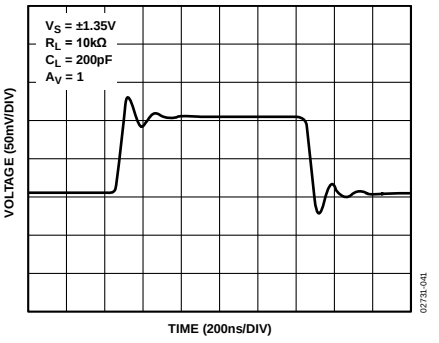


Figure 42. Small Signal Transient Response

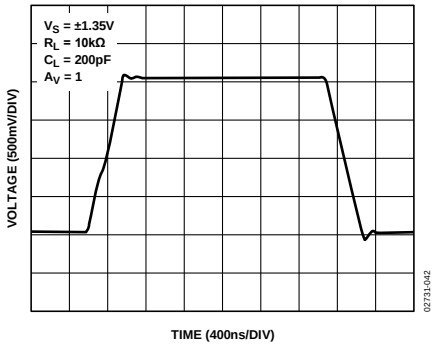


Figure 43. Large Signal Transient Response

APPLICATIONS INFORMATION

OUTPUT PHASE REVERSAL

Phase reversal is defined as a change in polarity at the output of the amplifier when a voltage that exceeds the maximum input common-mode voltage drives the input.

Phase reversal can cause permanent damage to the amplifier; it can also cause system lockups in feedback loops. The AD8605 does not exhibit phase reversal even for inputs exceeding the supply voltage by more than 2 V.

MAXIMUM POWER DISSIPATION

Power dissipated in an IC causes the die temperature to increase, which can affect the behavior of the IC and the application circuit performance.

The absolute maximum junction temperature of the AD8605/AD8606/AD8608 is 150°C. Exceeding this temperature could damage or destroy the device.

The maximum power dissipation of the amplifier is calculated according to

$$P_{DISS} = \frac{T_J - T_A}{\theta_{JA}}$$

where:
T_J is the junction temperature.
T_A is the ambient temperature.
θ_{JA} is the junction-to-ambient thermal resistance.

Figure 45 compares the maximum power dissipation with temperature for the various AD860x family packages.

INPUT OVERVOLTAGE PROTECTION

The AD860x has internal protective circuitry. However, if the voltage applied at either input exceeds the supplies by more than 0.5 V, external resistors should be placed in series with the inputs. The resistor values can be determined by

$$\frac{V_{IN} - V_S}{R_S} \leq 5\text{mA}$$

The remarkable low input offset current of the AD860x (<1 pA) allows the use of larger value resistors. With a 10 kΩ resistor at the input, the output voltage has less than 10 nV of error voltage. A 10 kΩ resistor has less than 13 nV/√Hz of thermal noise at room temperature.

THD + NOISE

Total harmonic distortion is the ratio of the input signal in V rms to the total harmonics in V rms throughout the spectrum. Harmonic distortion adds errors to precision measurements and adds unpleasant sonic artifacts to audio systems.

The AD860x has a low total harmonic distortion. Figure 46 shows that the AD8605 has less than 0.005% or −86 dB of THD + N over the entire audio frequency range. The AD8605 is configured in positive unity gain, which is the worst case, and with a load of 10 kΩ.

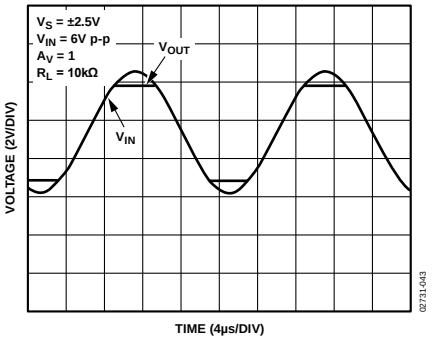


Figure 44. No Phase Reversal

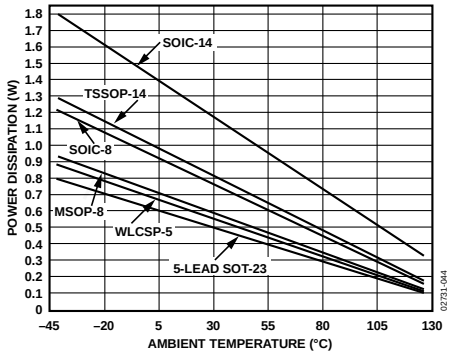


Figure 45. Maximum Power Dissipation vs. Ambient Temperature

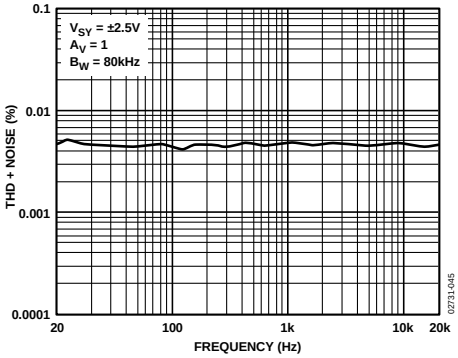


Figure 46. THD + Noise vs. Frequency

TOTAL NOISE INCLUDING SOURCE RESISTORS

The low input current noise and input bias current of the AD860x make it the ideal amplifier for circuits with substantial input source resistance, such as photodiodes. Input offset voltage increases by less than 0.5 nV per 1 kΩ of source resistance at room temperature and increases to 10 nV at 85°C. The total noise density of the circuit is

$$e_{n,TOTAL} = \sqrt{e_n^2 + (i_n R_S)^2 + 4kTR_S}$$

where:
e_n is the input voltage noise density of the AD860x.
i_n is the input current noise density of the AD860x.
R_S is the source resistance at the noninverting terminal.
k is Boltzmann's constant (1.38×10^{-23} J/K).
T is the ambient temperature in Kelvin (T = 273 + °C).

For example, with R_S = 10 kΩ, the total voltage noise density is roughly 15 nV/√Hz.

For R_S < 3.9 kΩ, e_n dominates and $e_{n,TOTAL} \approx e_n$.

The current noise of the AD860x is so low that its total density does not become a significant term unless R_S is greater than 6 MΩ.

The total equivalent rms noise over a specific bandwidth is expressed as

$$E_n = (e_{n,TOTAL})\sqrt{BW}$$

where BW is the bandwidth in hertz.

Note that the previous analysis is valid for frequencies greater than 100 Hz and assumes relatively flat noise, above 10 kHz. For lower frequencies, flicker noise (1/f) must be considered.

CHANNEL SEPARATION

Channel separation, or inverse crosstalk, is a measure of the signal feed from one amplifier (channel) to another on the same IC.

The AD8606 has a channel separation of greater than −160 dB up to frequencies of 1 MHz, allowing the two amplifiers to amplify ac signals independently in most applications.

CAPACITIVE LOAD DRIVE

The AD860x can drive large capacitive loads without oscillation. Figure 48 shows the output of the AD8606 in response to a 200 mV input signal. In this case, the amplifier is configured in positive unity gain, worst case for stability, while driving a 1000 pF load at its output. Driving larger capacitive loads in unity gain can require the use of additional circuitry.

A snubber network, shown in Figure 49, helps reduce the signal overshoot to a minimum and maintain stability. Although this circuit does not recover the loss of bandwidth induced by large capacitive loads, it greatly reduces the overshoot and ringing. This method does not reduce the maximum output swing of the amplifier.

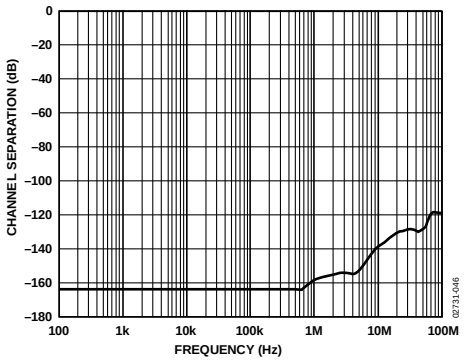


Figure 47. Channel Separation vs. Frequency

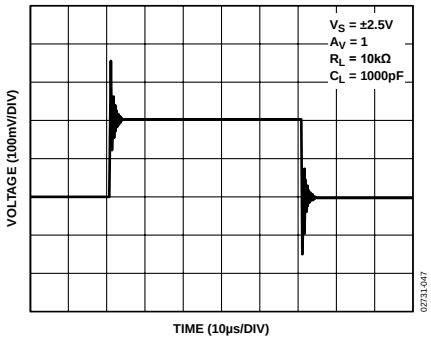


Figure 48. AD8606 Capacitive Load Drive Without Snubber

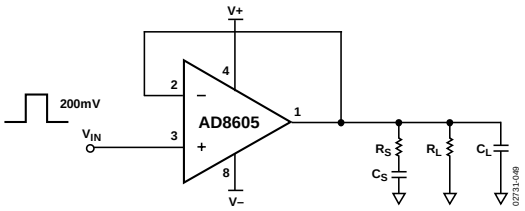


Figure 49. Snubber Network Configuration

Figure 50 shows a scope of the output at the snubber circuit. The overshoot is reduced from over 70% to less than 5%, and the ringing is eliminated by the snubber. Optimum values for R_S and C_S are determined experimentally.

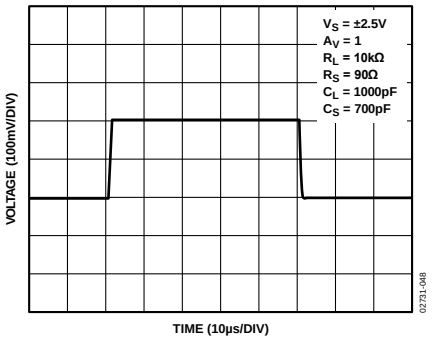


Figure 50. Capacitive Load Drive with Snubber

Table 5 summarizes a few optimum values for capacitive loads.

Table 5.

C_L (pF)	R_S (Ω)	C_S (pF)
500	100	1000
1000	70	1000
2000	60	800

An alternate technique is to insert a series resistor inside the feedback loop at the output of the amplifier. Typically, the value of this resistor is approximately 100 Ω. This method also reduces overshoot and ringing but causes a reduction in the maximum output swing.

LIGHT SENSITIVITY

The AD8605ACB (WLCSP package option) is essentially a silicon die with additional postfabrication dielectric and intermetallic processing designed to contact solder bumps on the active side of the chip. With this package type, the die is exposed to ambient light and is subject to photoelectric effects. Light sensitivity analysis of the AD8605ACB mounted on standard PCB material reveals that only the input bias current (I_B) parameter is impacted when the package is illuminated directly by high intensity light. No degradation in electrical performance is observed due to illumination by low intensity (0.1 mW/cm^2) ambient light. Figure 51 shows that I_B increases with increasing wavelength and intensity of incident light; I_B can reach levels as high as 4500 pA at a light intensity of 3 mW/cm^2 and a wavelength of 850 nm. The light intensities shown in Figure 51 are not normal for most applications, that is, even though direct sunlight can have intensities of 50 mW/cm^2, office ambient light can be as low as 0.1 mW/cm^2.

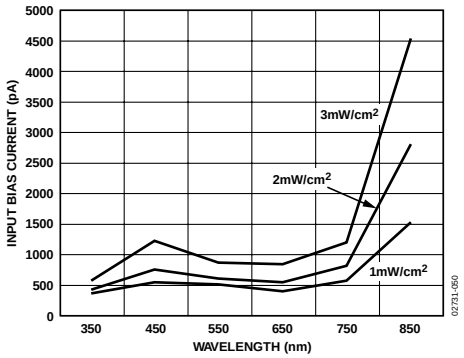


Figure 51. AD8605ACB Input Bias Current Response to Direct Illumination of Varying Intensity and Wavelength

When the WLCSP package is assembled on the board with the bump side of the die facing the PCB, reflected light from the PCB surface is incident on active silicon circuit areas and results in the increased I_B. No performance degradation occurs due to illumination of the backside (substrate) of the AD8605ACB. The AD8605ACB is particularly sensitive to incident light with wavelengths in the near infrared range (NIR, 700 nm to 1000 nm). Photons in this waveband have a longer wavelength and lower energy than photons in the visible (400 nm to 700 nm) and near ultraviolet (NUV, 200 nm to 400 nm) bands; therefore, they can penetrate more deeply into the active silicon. Incident light with wavelengths greater than 1100 nm has no photoelectric effect on the AD8605ACB because silicon is transparent to wavelengths in this range. The spectral content of conventional light sources varies. Sunlight has a broad spectral range, with peak intensity in the visible band that falls off in the NUV and NIR bands; fluorescent lamps have significant peaks in the visible but not the NUV or NIR bands.

Efforts have been made at a product level to reduce the effect of ambient light; the under bump metal (UBM) has been designed to shield the sensitive circuit areas on the active side (bump side) of the die. However, if an application encounters any light sensitivity with the AD8605ACB, shielding the bump side of the WLCSP package with opaque material should eliminate this effect. Shielding can be accomplished using materials such as silica-filled liquid epoxies that are used in flip-chip underfill techniques.

WLCSP ASSEMBLY CONSIDERATIONS

For detailed information on the WLCSP PCB assembly and reliability, see Application Note AN-617, *MicroCSP™ Wafer Level Chip Scale Package*.

I-V CONVERSION APPLICATIONS

PHOTODIODE PREAMPLIFIER APPLICATIONS

The low offset voltage and input current of the AD8605 make it an excellent choice for photodiode applications. In addition, the low voltage and current noise make the amplifier ideal for application circuits with high sensitivity.

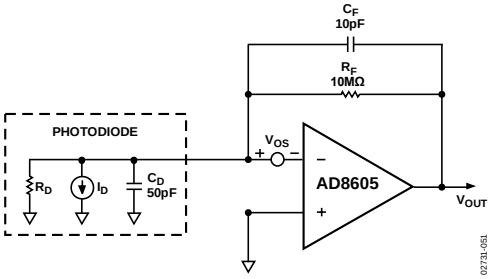


Figure 52. Equivalent Circuit for Photodiode Preamp

The input bias current of the amplifier contributes an error term that is proportional to the value of R_F.

The offset voltage causes a dark current induced by the shunt resistance of the Diode R_D. These error terms are combined at the output of the amplifier. The error voltage is written as

$$E_O = V_{OS}\left(1+\frac{R_F}{R_D}\right)+R_F I_B$$

Typically, R_F is smaller than R_D, thus R_F/R_D can be ignored.

At room temperature, the AD8605 has an input bias current of 0.2 pA and an offset voltage of 100 µV. Typical values of R_D are in the range of 1 GΩ.

For the circuit shown in Figure 52, the output error voltage is approximately 100 µV at room temperature, increasing to about 1 mV at 85°C.

The maximum achievable signal bandwidth is

$$f_{MAX} = \sqrt{\frac{f_t}{2\pi R_F C_F}}$$

where f_t is the unity gain frequency of the amplifier.

AUDIO AND PDA APPLICATIONS

The low distortion and wide dynamic range of the AD860x make it a great choice for audio and PDA applications, including microphone amplification and line output buffering.

Figure 53 shows a typical application circuit for headphone/line-out amplification.

R1 and R2 are used to bias the input voltage at half the supply, which maximizes the signal bandwidth range. C1 and C2 are used to ac couple the input signal. C1, R1, and R2 form a high-pass filter whose corner frequency is 1/[2π(R1||R2)C1].

The high output current of the AD8606 allows it to drive heavy resistive loads.

The circuit in Figure 53 is tested to drive a 16 Ω headphone. The THD + N is maintained at approximately −60 dB throughout the audio range.

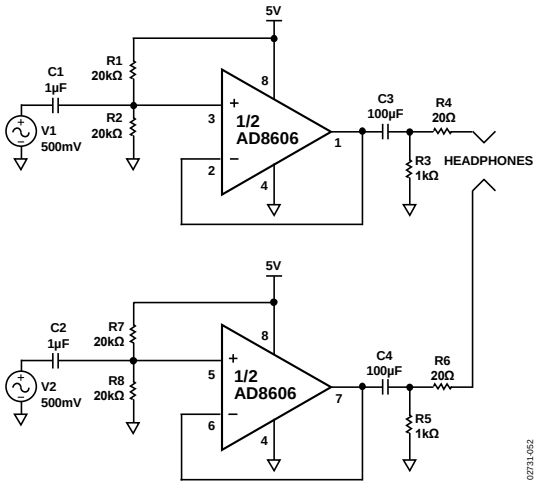


Figure 53. Single-Supply Headphone/Speaker Amplifier

INSTRUMENTATION AMPLIFIERS

The low offset voltage and low noise of the AD8605 make it an ideal amplifier for instrumentation applications.

Difference amplifiers are widely used in high accuracy circuits to improve the common-mode rejection ratio. Figure 54 shows a simple difference amplifier. Figure 55 shows the common-mode rejection for a unity gain configuration and for a gain of 10.

Making (R4/R3) = (R2/R1) and choosing 0.01% tolerance yields a CMRR of 74 dB and minimizes the gain error at the output.

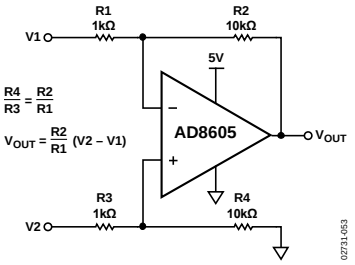


Figure 54. Difference Amplifier, A_V = 10

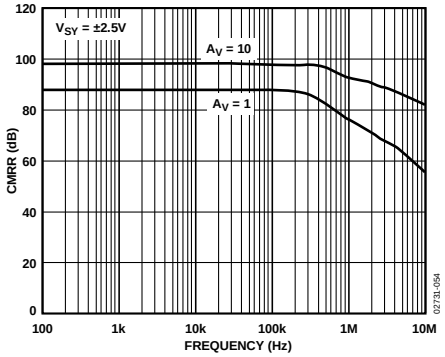


Figure 55. Difference Amplifier CMRR vs. Frequency

DAC CONVERSION

The low input bias current and offset voltage of the AD8605 make it an excellent choice for buffering the output of a current output DAC.

Figure 56 shows a typical implementation of the AD8605 at the output of a 12-bit DAC.

The DAC8143 output current is converted to a voltage by the feedback resistor. The equivalent resistance at the output of the DAC varies with the input code, as does the output capacitance.

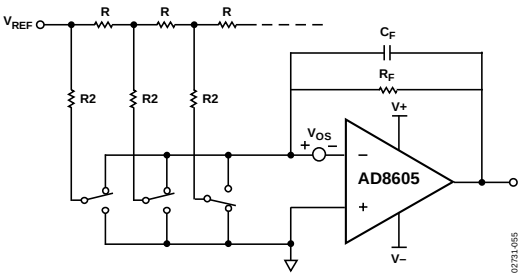


Figure 56. Simplified Circuit of the DAC8143 with AD8605 Output Buffer

To optimize the performance of the DAC, insert a capacitor in the feedback loop of the AD8605 to compensate the amplifier for the pole introduced by the output capacitance of the DAC. Typical values for C_F range from 10 pF to 30 pF; it can be adjusted for the best frequency response. The total error at the output of the op amp can be computed by

$$E_O = V_{OS}\left(1 + \frac{R_F}{Req}\right)$$

where *Req* is the equivalent resistance seen at the output of the DAC. As previously mentioned, Req is code dependent and varies with the input. A typical value for Req is 15 kΩ. Choosing a feedback resistor of 10 kΩ yields an error of less than 200 µV.

Figure 57 shows the implementation of a dual-stage buffer at the output of a DAC. The first stage is used as a buffer. Capacitor C1 with Req creates a low-pass filter, and thus, provides phase lead to compensate for frequency response. The second stage of the AD8606 is used to provide voltage gain at the output of the buffer.

Grounding the positive input terminals in both stages reduces errors due to the common-mode output voltage. Choosing R1, R2, and R3 to match within 0.01% yields a CMRR of 74 dB and maintains minimum gain error in the circuit.

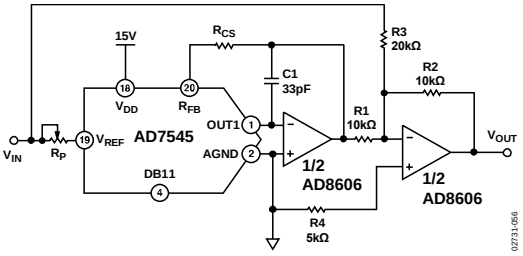


Figure 57. Bipolar Operation

OUTLINE DIMENSIONS

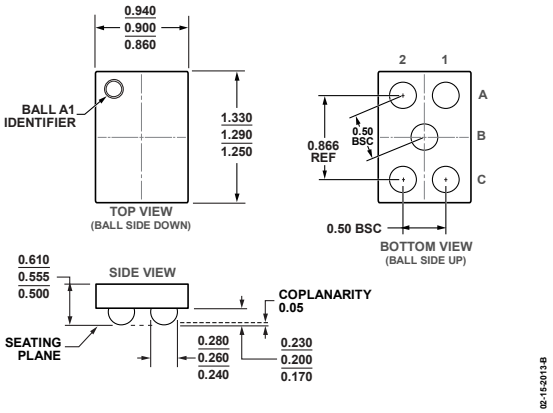
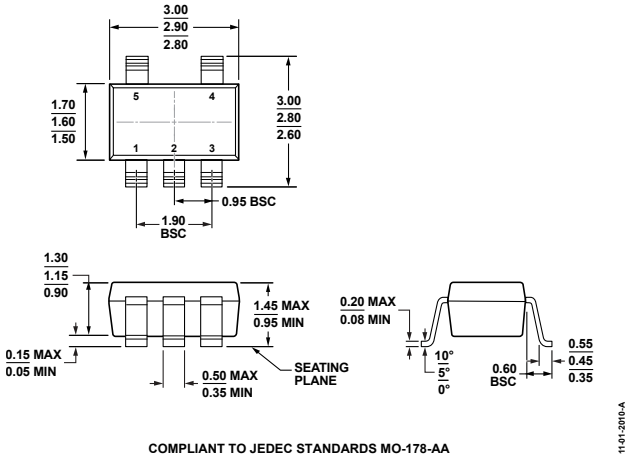
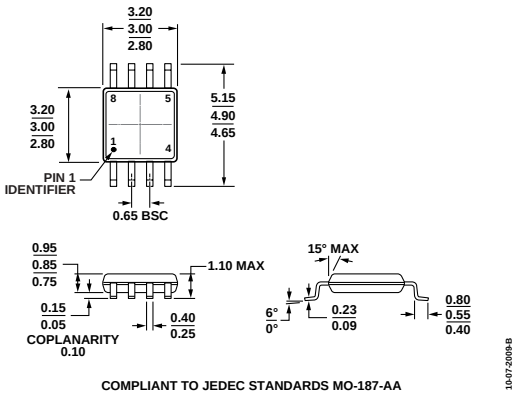


Figure 58. 5-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-5-1)
Dimensions shown in millimeters



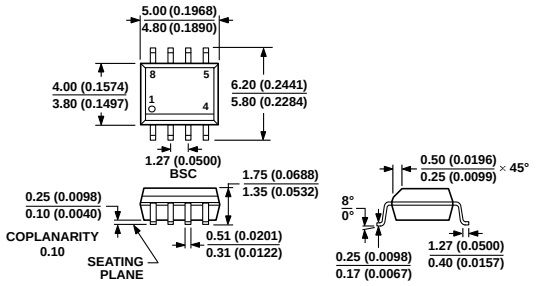
COMPLIANT TO JEDEC STANDARDS MO-178-AA

Figure 59. 5-Lead Small Outline Transistor Package [SOT-23]
(RJ-5)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 60. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 61. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)

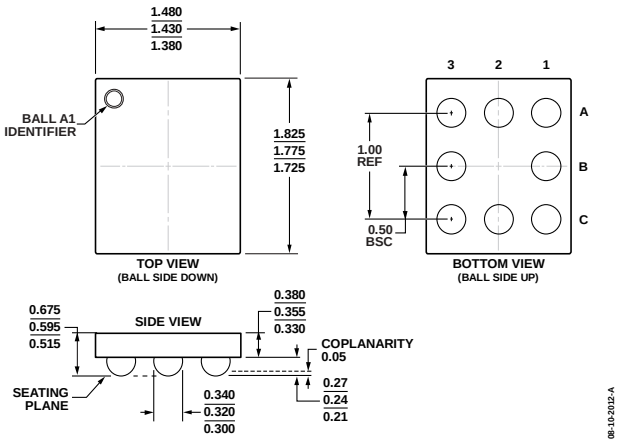
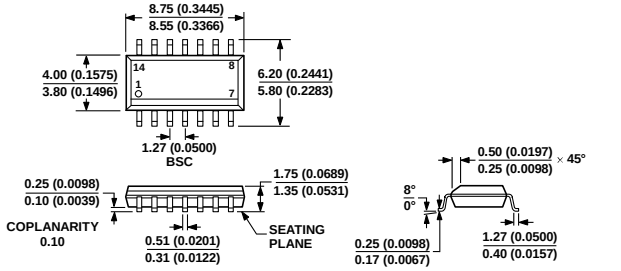


Figure 62. 8-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-8-1)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AB
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 63. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-14)
Dimensions shown in millimeters and (inches)

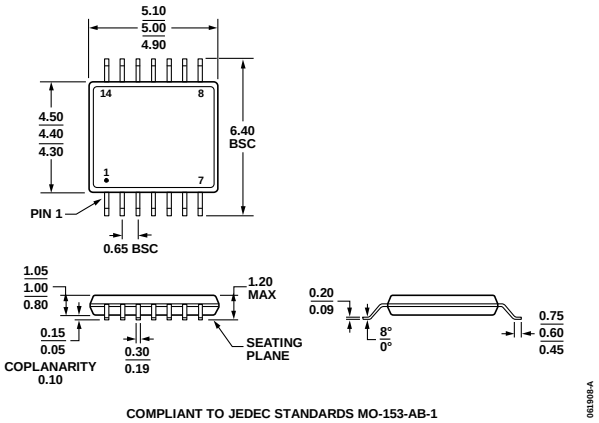


Figure 64. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
AD8605ACBZ-REEL	−40°C to +125°C	5-Ball WLCSP	CB-5-1	A1J
AD8605ACBZ-REEL7	−40°C to +125°C	5-Ball WLCSP	CB-5-1	A1J
AD8605ART-REEL	−40°C to +125°C	5-Lead SOT-23	RJ-5	B3A
AD8605ARTZ-R2	−40°C to +125°C	5-Lead SOT-23	RJ-5	B3A#
AD8605ARTZ-REEL	−40°C to +125°C	5-Lead SOT-23	RJ-5	B3A#
AD8605ARTZ-REEL7	−40°C to +125°C	5-Lead SOT-23	RJ-5	B3A#
AD8606ARM-REEL	−40°C to +125°C	8-Lead MSOP	RM-8	B6A
AD8606ARMZ-R7	−40°C to +125°C	8-Lead MSOP	RM-8	B6A#
AD8606ARMZ-REEL	−40°C to +125°C	8-Lead MSOP	RM-8	B6A#
AD8606AR	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8606AR-REEL	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8606AR-REEL7	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8606ARZ	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8606ARZ-REEL	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8606ARZ-REEL7	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8606ACBZ-REEL7	−40°C to +125°C	8-Ball WLCSP	CB-8-1	B6A#
AD8608ARZ	−40°C to +125°C	14-Lead SOIC_N	R-14	
AD8608ARZ-REEL	−40°C to +125°C	14-Lead SOIC_N	R-14	
AD8608ARZ-REEL7	−40°C to +125°C	14-Lead SOIC_N	R-14	
AD8608ARUZ	−40°C to +125°C	14-Lead TSSOP	RU-14	
AD8608ARUZ-REEL	−40°C to +125°C	14-Lead TSSOP	RU-14	

[1] Z = RoHS Compliant Part, # denotes RoHS compliant product (except for CB-5-1) may be top or bottom marked.

B Codes

B.1 Atmega328p Code


```
#include "Wire.h"
#include "SoftwareSerial.h"
//Register locations
#define SLAVEADDR 0x0D
#define ADDRPTR 0xB0
#define STARTFREQ_R1 0x82
#define STARTFREQ_R2 0x83
#define STARTFREQ_R3 0x84
#define FREGINCRE_R1 0x85
#define FREGINCRE_R2 0x86
#define FREGINCRE_R3 0x87
#define NUMINCRE_R1 0x88
#define NUMINCRE_R2 0x89
#define NUMSCYCLES_R1 0x8A
#define NUMSCYCLES_R2 0x8B
#define REDATA_R1 0x94
#define REDATA_R2 0x95
#define IMGDATA_R1 0x96
#define IMGDATA_R2 0x97
#define TEMPR1 0x92
#define TEMPR2 0x93
#define CTRLREG 0x80
#define CTRLREG2 0x81
#define STATUSREG 0x8F
const float MCLK = 16.776*pow(10,6); // AD5933 Internal Clock Speed 16.776 MHz
const float startfreq = 5*pow(10,3); // Set start freq, < 100Khz
const float increfreq = 1*pow(10,3); // Set freq increment
const int increnum = 95; // Set number of increments; < 511
SoftwareSerial Bluetooth(10, 11); // RX, TX
char state;
int count=0;
void setup() {
  Wire.begin();
  Bluetooth.begin(9600);
  //nop - clear ctrl-reg
  writeData(CTRLREG,0x01);
  //reset ctrl register
  writeData(CTRLREG2,0x10);
  programReg();
}
void loop(){
         /////Programming Device Registers/////
          programReg();
          //run sweep
          runSweep();
          //wait 1000 before restarting
          delay(1000);
}
void programReg(){
  // Set Range 1, PGA gain 1
  writeData(CTRLREG,0x01);
  // Set settling cycles
  writeData(NUMSCYCLES_R1, 0x07);
```

```
  writeData(NUMSCYCLES_R2, 0xFF);
  // Start frequency of 5kHz
  writeData(STARTFREQ_R1, getFrequency(startfreq,1));
  writeData(STARTFREQ_R2, getFrequency(startfreq,2));
  writeData(STARTFREQ_R3, getFrequency(startfreq,3));
  // Increment by 1 kHz
  writeData(FREGINCRE_R1, getFrequency(increfreq,1));
  writeData(FREGINCRE_R2, getFrequency(increfreq,2));
  writeData(FREGINCRE_R3, getFrequency(increfreq,3));
  // Points in frequency sweep (95), max 511
  writeData(NUMINCRE_R1, (increnum & 0x001F00)>>0x08 );
  writeData(NUMINCRE_R2, (increnum & 0x0000FF));
}
void runSweep() {
  short re;
  short img;
  double freq;
  double mag;
  double phase;
  double sys_phase;
  double gain;
  double impedance;
  int i=0;
  programReg();
  // 1. Standby '10110000' Mask D8-10 of avoid tampering with gains
  writeData(CTRLREG,(readData(CTRLREG) & 0x07) | 0xB0);
  // 2. Initialize sweep
  writeData(CTRLREG,(readData(CTRLREG) & 0x07) | 0x10);
  // 3. Start sweep
  writeData(CTRLREG,(readData(CTRLREG) & 0x07) | 0x20);
  while((readData(STATUSREG) & 0x07) < 4 ) {  // Check that status reg != 4, sweep not complete
    delay(100); // delay between measurements
    //reads imaginary and real data
    int flag = readData(STATUSREG)& 2;
    if (flag==2) {
      byte R1 = readData(REDATA_R1);
      byte R2 = readData(REDATA_R2);
      re = (R1 << 8) | R2;
      R1  = readData(IMGDATA_R1);
      R2  = readData(IMGDATA_R2);
      img = (R1 << 8) | R2;
      freq = startfreq + i*increfreq;
      //save real and imaginary to seperate double variables to ensure correct transmission
      with matlab code
      mag=re;
      phase=img;
        //print Freg,Real and Imaginary
      if(freq/1000==5){
        Bluetooth.println('*');
      }
       Bluetooth.println(freq/1000);
       Bluetooth.println(mag);
       Bluetooth.println(phase);
```

```
      //Increment frequency
      if((readData(STATUSREG) & 0x07) < 4 ){
        writeData(CTRLREG,(readData(CTRLREG) & 0x07) | 0x30);
        i++;
      }

    }
  }
  writeData(CTRLREG,(readData(CTRLREG) & 0x07) | 0xA0);
}
void writeData(int addr, int data) {
 Wire.beginTransmission(SLAVEADDR);
 Wire.write(addr);
 Wire.write(data);
 Wire.endTransmission();
 delay(1);
}
int readData(int addr){
  int data;
  Wire.beginTransmission(SLAVEADDR);
  Wire.write(ADDRPTR);
  Wire.write(addr);
  Wire.endTransmission();
  delay(1);
  Wire.requestFrom(SLAVEADDR,1);
  if (Wire.available() >= 1){
    data = Wire.read();
  }
  else {
    data = -1;
  }
  delay(1);
  return data;
}
byte getFrequency(float freq, int n){
  long val = long((freq/(MCLK/4)) * pow(2,27));
  byte code;
    switch (n) {
      case 1:
        code = (val & 0xFF0000) >> 0x10;
        break;
      case 2:
        code = (val & 0x00FF00) >> 0x08;
        break;
      case 3:
        code = (val & 0x0000FF);
        break;
      default:
        code = 0;
    }
  return code;
}
```

B.2 MATLAB Code


```
RC=1;%Testing with RC Parallel load 1 for YES ANYTHIng ELSE=NO
%TYPE IN YOUR R AND C PARALLEL LOAD VALUES HERE
Rtheo=1980;
Ctheo=5.34E-9;
% Stage Zero - Theoretical
%generates theoretical phase and magnitude of the impedance if not human
%testing
if RC==1
for i=1:96
    format long, ImpTheo(i)=1/(sqrt(((1/Rtheo)^2)+((2*pi*((i+4)*1000)*Ctheo)^2)));
    format long, PhaTheo(i)=(atan(-2*pi*((i+4)*1000)*Ctheo*Rtheo))*360/(2*pi);
end
else
    ImpTheo=0;
    PhaTheo=0;
end
%%
% Stage One - Receiver
% Bluetoooth Receiver
% Outputs Received Data converted to Doubles
DATA=Bluetooth_Receive();
%%
%Stage Two - Set up Frame
%Finds Locatations of NaN's as Delimitter
%Outputs Data From first to second Nan (One Full Trasission)
DATA3=Seperator(DATA);
%Stage Three - Set up Useful Data
%Takes one Complete Data Set
%Outputs Frequency, Real, and Imaginary Values In Seperate Arrays
[FREQ, REAL, IMAG]=SETUP(DATA3);
%%
%Stage Four - Project Calculations
%Takes Real and Imaginary Data
%Outputs Calculated Phase and Impedance
% if(RC==1)
%     [ImpVar, PhaVar] = Calb(RCalb,Ccalb,REAL,IMAG);
% end
load('905Dtermpha.mat')
load('905DterMimp.mat')
[Phase, Impedance]=ProjCalc( REAL, IMAG,PhaVar,ImpVar);
%% Graphing
% DESCRIPTIVE TEXT
%Stage Five - Project Plotting
%Takes Phase Impedance and Frequency
%Creates Graphs
ProjGraph(FREQ,Impedance,Phase,ImpTheo,PhaTheo,RC);
%Stage Six - Error Anlysis
%Takes in Phase Impedance and Frequency
%Outputs graphs/Data showing Relationship between Experimental and
%Theoretical
%Shows error analysis and save error data to variables
if RC==1
[Erimp,erpha] =ErrorAN(FREQ,Impedance,Phase,ImpTheo,PhaTheo);
```

```
meanImpedancepercenterror = mean(Erimp);
meanPhasemeanerror = mean(erpha);
[MaxIMPpercenterror, IIMP] = max(Erimp);
[MaxPhaerror, IPha] = max(erpha);
stddevImpedance = std(Erimp);
stddevPhase = std(erpha);
end

function DATA = Bluetooth_Receive()
%Tyler Newman 2016
%Function Prototype
%Receives Bluetooth data from MQP PCB board
%outputs large enough data frame to get all correct values to be decoded
%later
    %b = Bluetooth('HC-06',1);
        b = Bluetooth('MQPLow2',1);
    %Sets up Bluetooth Connection
    %String is name of Bluetooth device
    fopen(b);
    for i= 1:1000;
        y=fscanf(b);
        x(i)=str2double(y);
    end
    %For 1000 iterations saves the data from the HC-06
    %To the array y
    DATA=x;
    fclose(b);
end

function [ DATA3 ] = Seperator( DATA )
%Seperates Data Stream into correct Arrays
%Makes use of Unique Starting Code '*' that is Represented by
%NaN at this point
DATA2=isnan(DATA);
I=find(DATA2==1);
Begin=I(1)+1;
End=I(2)-1;
DATA3=DATA(Begin:End);
end

function [ Freq, Real, Imag ] = SETUP( DATA3 )
%SEPERATES DATA INTO FREQ, IMAGINARY and REAL
    for(i=1:96)
        Freq(i)=DATA3(i+2*(i-1));
        Real(i)=DATA3(i+2*(i-1)+1);
        Imag(i)=DATA3(i+2*(i-1)+2);
    end
end

function [ Phase, Impedance ] = ProjCalc(  Real, Imag, PhaVar, ImpVar)
%Calculates Phase and impedance of unknown source
Impedance=(ImpVar.*sqrt((Real.^2)+(Imag.^2)));
for i=1:3
```

```
    Impedance(i)=Impedance(i)+10.5;
end
for i=14:96
    Impedance(i)=Impedance(i)-10.5;
end
for i=1:96
    if(Real(i)>=0 && Imag(i)>=0)
        Phase(i)=(atan(Real(i)/Imag(i))*180/pi);
    elseif(Real(i)<0 && Imag(i)>=0)
        Phase(i)=(atan(Real(i)/Imag(i))*180/pi)+178;
    elseif(Real(i)<0 && Imag(i)<0)
        Phase(i)=(atan(Real(i)/Imag(i))*180/pi)-2;
    elseif(real(i)>=0 && Imag(i)<0)
        Phase(i)=(atan(Real(i)/Imag(i))*180/pi)-180;
    end
    Phase(i)=Phase(i)-PhaVar(i);
end
end

function [ ] = ProjGraph( FREQ,Impedance,Phase,ImpTheo,PhaTheo, RC)
%UNTITLED2 Summary of this function goes here
%   Plots Phase vs frequency
%           Impedance vs Freq
% on both graphs plots the theroetical values also
figure(1)
loglog(FREQ,Impedance,'rs')
hold on
if RC==1
loglog(FREQ,ImpTheo,'b')
end
title('Impedance Vs Frequency')
xlabel('Frequency (kHz)')
ylabel('Impedance (Ohms)')
if RC==1
legend('Experimental','Theoretical')
end
hold off
figure(2)
semilogx(FREQ,Phase,'rs')
hold on
if RC==1
semilogx(FREQ,PhaTheo,'b')
end
title('Phase vs Frequency')
xlabel('Frequency (kHz)')
ylabel('Phase (degrees)')
if RC==1
legend('Experimental','Theoretical')
end
hold off
end

function [ ErrorIMPer, ErrorPhase] = ErrorAN(FREQ,Impedance,Phase,ImpTHEO,PhaTHEO)
```

```
%Calculates %error for impedance and Relative signed error for phase and
%plots thems
ErrorIMP=ImpTHEO-Impedance;
ErrorPhase=PhaTHEO-Phase;
ErrorIMPer=ErrorIMP./ImpTHEO*100;
ErrorPhaseer=ErrorPhase./PhaTHEO*100;
figure(4)
plot(FREQ,ErrorPhase,'r-s')
title('Differential Phase Error At Each Frequency')
xlabel('Frequency (kHz)')
ylabel('Error (Degrees)')
figure(5)
plot(FREQ,ErrorIMPer,'r-s')
title(' Impedance Error At Each Frequency')
xlabel('Frequency (kHz)')
ylabel('Error (%)')
end
```

C IRB Approval

Informed Consent Agreement for Participation

Investigator: Muhammad Abid, Tyler Newman, Sara Kim and Sebastian Rojas

Contact Information: mqp-lpbio@wpi.edu

Title of Research Study: Low Power Biomedical Sensor

Introduction You are being asked to participate in a research study. Before you agree, however, you must be fully informed about the purpose of the study, the procedures to be followed, and any benefits, risks or discomfort that you may experience as a result of your participation. This form presents information about the study so that you may make a fully informed decision regarding your participation.

Purpose of the study: The purpose of this study is to investigate and develop a skin impedance meter. Human skin impedance is widely used to evaluate body composition (Bioelectrical Impedance Analysis). It also can be indicators of many diseases such as skin cancer and diabetes. We will be verifying the functionality of the device by testing with human subject.

Procedures to be followed: We have built a skin impedance spectrometer that sends a current signal through tissue under test (TUT) and measures voltage across the TUT. First, a pair of electrodes will be attached to a forearm of a participant. Then, whenever the participant is ready, the device will send an AC current signal of maximum peak value of 200μA (very low DC current included, less then ±25μA) through the electrodes and measure the voltage value. The current signal sent through is below the safety limit which is 9mA DC and 1.8mA AC @ 60Hz[1]. This process will take less than 10 seconds, and the participant is free to take off the electrodes.

Risks to study participants: It is possible that a participant feels a minor discomfort when injecting the current signal.

Benefits to research participants and others: Your participation will not have a immediate benefit to a participant. However, this experiment will be helpful in verifying the functionality of the device developed in the research.

Record keeping and confidentiality: Some of the biological information including gender and age will be collected along with the skin impedance value. Collected data will be included in the project report. The information is only for research purpose and will not contain any reference that can make the information identifiable.

Compensation or treatment in the event of injury: The research will not cause more than a minimal risk. In case of an injury, you will be treated with proper procedure to

[1] Environment, Safety, and Health Manual, Volume II, Part 16.1, U.S. Dept. of Energy at University of California Lawrence Livermore National Laboratory, Contract W-7405-ENG-48, Feb 1996

Approved by
WPI IRB 1
3/3/16 - 3/2/17

reduce discomfort and heal any wound. You do not give up any of your legal rights by signing this statement.

For more information about this research or about the rights of research participants, or in case of research-related injury, contact:
Student Investigator, Muhammad Abid, Email: meabid@wpi.edu
Student Investigator, Tyler Newman, Email: tjnewman@wpi.edu
Student Investigator, Sara Kim, Email: skim@wpi.edu
Student Investigator, Sebastian Rojas, Email: srojas2@wpi.edu
Project Advisor, John McNeill, Email: mcneill@wpi.edu
WPI IRB Chair, Professor Kent Rissmiller, Tel. 508-831-5019, Email: kjr@wpi.edu
University Compliance Officer, Jon Bartelson, Tel. 508-831-5725, Email: jonb@wpi.edu

Your participation in this research is voluntary. Your refusal to participate will not result in any penalty to you or any loss of benefits to which you may otherwise be entitled. You may decide to stop participating in the research at any time without penalty or loss of other benefits. The project investigators retain the right to cancel or postpone the experimental procedures at any time they see fit.

By signing below, you acknowledge that you have been informed about and consent to be a participant in the study described above. Make sure that your questions are answered to your satisfaction before signing. You are entitled to retain a copy of this consent agreement.

_____ Date: _____
Study Participant Signature

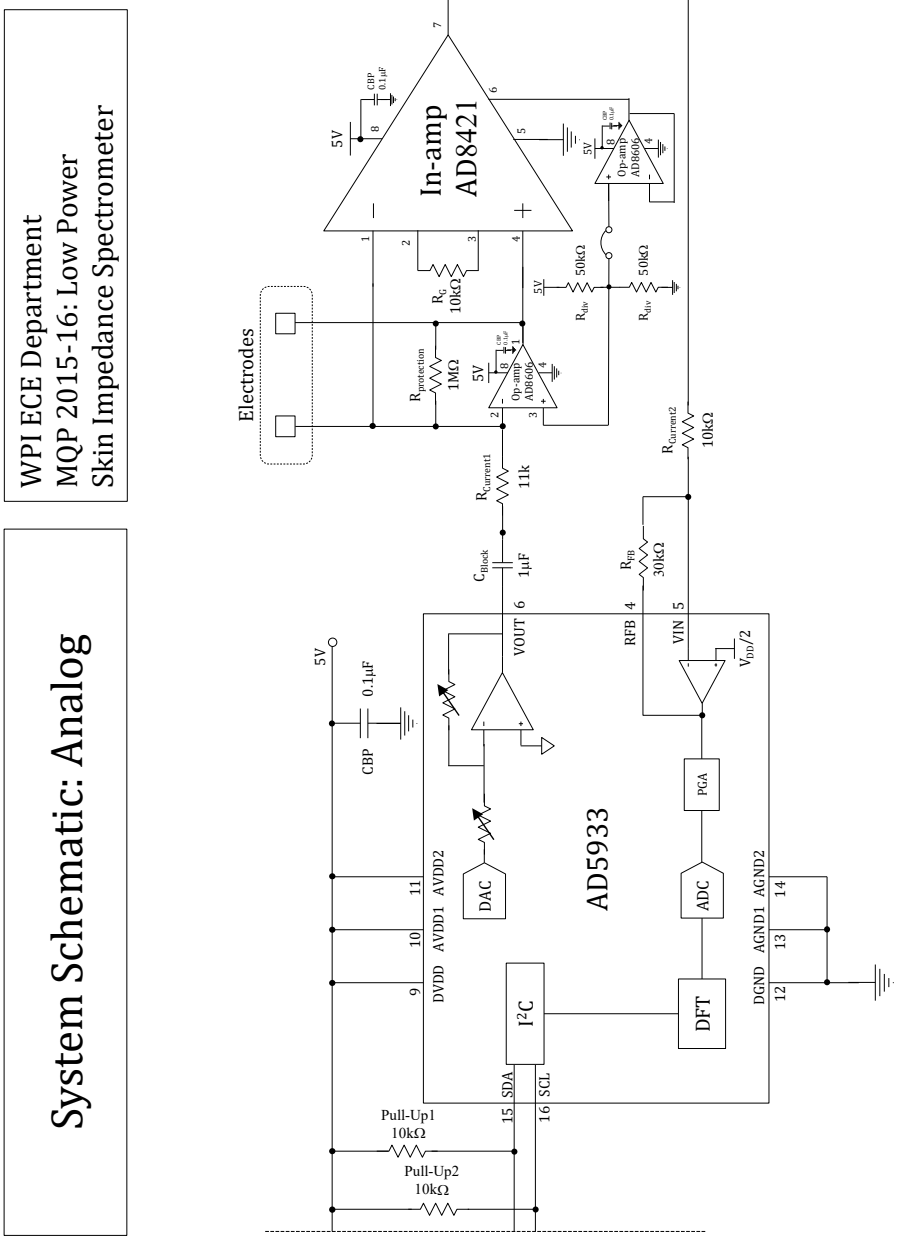
_____
Study Participant Name (Please print)

_____ Date: _____
Signature of Person who explained this study

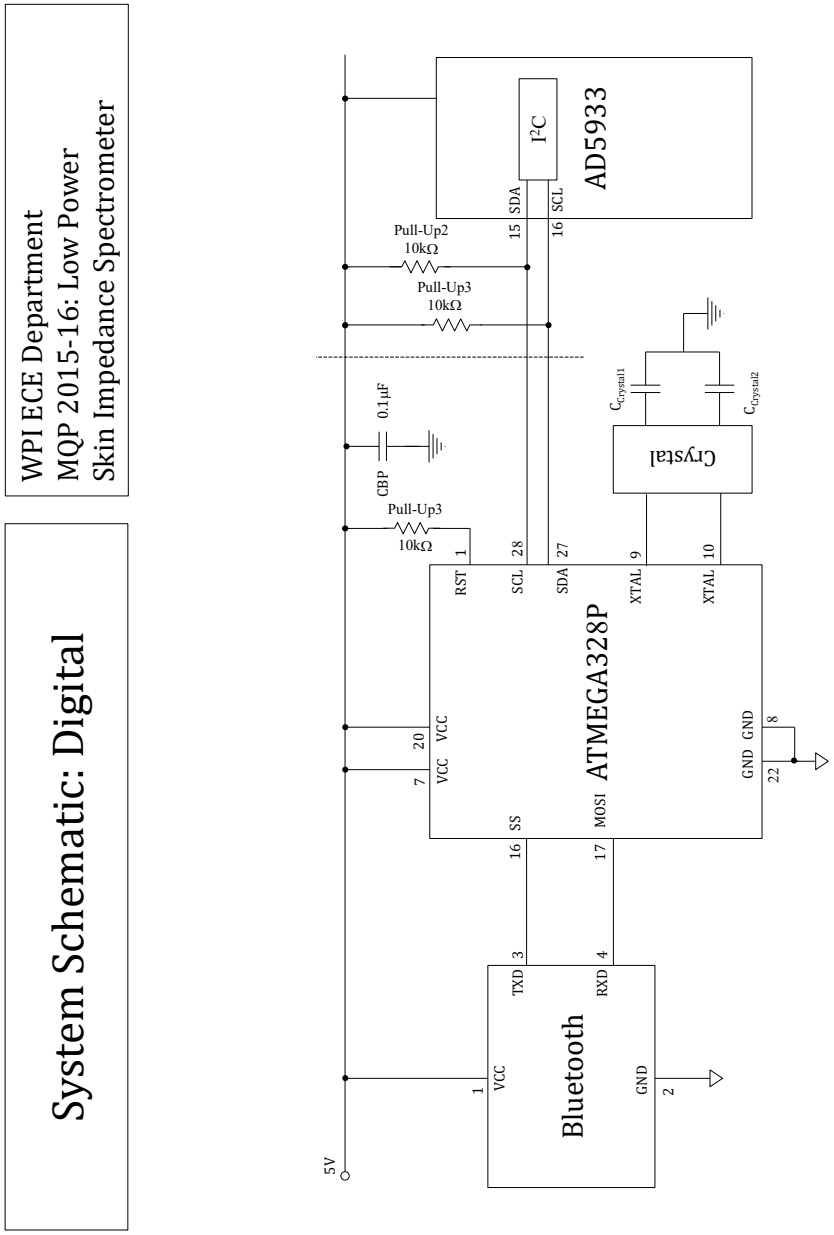
Approved by
WPI IRB 1
3/3/16 - 3/2/17

D Schematics

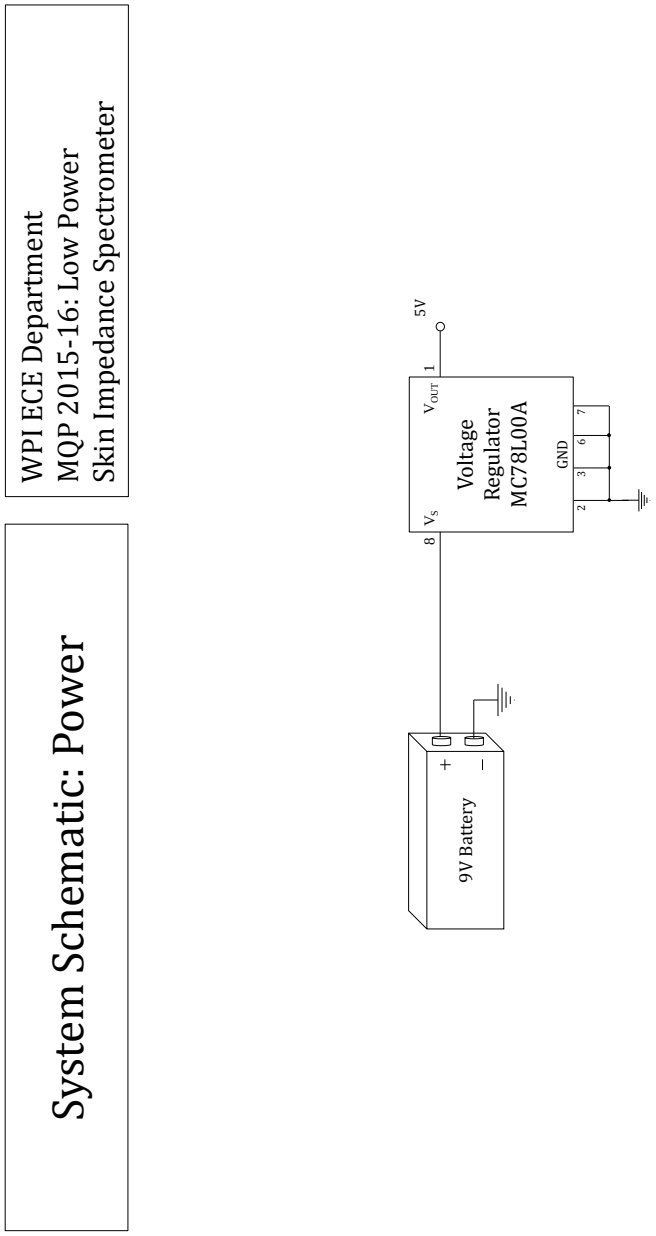
D.1 Analog



D.2 Digital


System Schematic: Digital
WPI ECE Department
MQP 2015-16: Low Power
Skin Impedance Spectrometer
AD5933
I²C
SDA
SCL
15
16
Pull-Up2
10kΩ
Pull-Up3
10kΩ
0.1µF
CBP
Pull-Up3
10kΩ
Crystal
C_Crystal1
C_Crystal2
RST
SCL
SDA
XTAL
XTAL
1
28
27
9
10
ATMEGA328P
VCC
VCC
GND
GND
20
7
8
22
SS
MOSI
16
17
Bluetooth
TXD
RXD
VCC
GND
3
4
1
2
5V

D.3 Power


System Schematic: Power
WPI ECE Department
MQP 2015-16: Low Power
Skin Impedance Spectrometer
9V Battery
+
–
8
V_S
Voltage
Regulator
MC78L00A
V_{OUT}
1
5V
GND
2
3
6
7