Universal Evaluation Platform

A Major Qualifying Project

Advisor:

Professor Susan M. Jarvis

Submitted By:

Sagar Mahurkar

Dylan Baranik

Erik Paulson

Jorgo Mihallari

Abstract

Universal Evaluation Platform (UEP), the lab bench on a board, seeks to streamline the process of testing new integrated circuit products. It replaces costly custom test fixtures, and allows test engineers to fully characterize new devices before datasheets exist. Features include fixed and adjustable voltage supplies, common digital communication protocols, filter generation via digital signal processing, and a user interface. Communication and digital signal processing were implemented on an FPGA, while power supplies were assembled through custom circuitry. The platform aims to save engineering time and resources, while accommodating testing of a wide array of products.

Acknowledgements

The Universal Evaluation Platform team would like to thank the people who provided support and guidance necessary to make this project possible: Project advisors Professor Susan Jarvis and Professor Jahangir Rahman for their feedback in weekly meetings, design reviews and valuable comments on project reports. Professor R. James Duckworth for lending the team a Kintex-7 KC705 FPGA, as well as for helping the team tackle roadblocks with digital design. Lastly, the WPI Electrical and Computer Engineering Department for supporting project costs.

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List of Commonly Used Acronyms

AC – Alternating Current

ACK – Acknowledgement

ADC – Analog to Digital Converter

AI – Artificial Intelligence

BJT – Bipolar Junction Transistor

CAD – Computer Aided Design

CMOS – Complimentary MOS (MOSFET)

CS – Chip Select (SPI)

DAC – Digital to Analog Converter

DC – Direct Current-------

DSP – Digital Signal Processing

DUT – Device Under Test

FIR – Finite Impulse Response (DSP)

FMC – FPGA Mezzanine Card

FPGA – Field Programmable Gate Array

GUI – Graphical User Interface

IC – Integrated Circuit

I2C – Inter-Integrated Circuit

IIR – Infinite Impulse Response (DSP)

LDO – Low Drop-Out (referring to Linear Regulators)

LVDS – Low Voltage Differential Signal

LSB – Least Significant Bit

MISO – Master In, Slave Out (SPI)

MOSFET – Metal Oxide Silicon Field Effect Transistor

MOSI – Master Out, Slave In (SPI)

MQP – Major Qualifying Project

MSB – Most Significant Bit

NAK – Negative Acknowledgement

NMOS – N-Channel MOSFET

PCB – Printed Circuit Board

RDAC – Resistive Digital to Analog Converter

RX - Receive

SCL – Serial Clock Line (I2C)

SCLK – Serial Clock (SPI)

SDA – Serial Data (I2C)

SDI – Serial Data In (SPI)

SDO – Serial Data Out (SPI)

SPI – Serial Peripheral Interface

TX – Transmit

UART – Universal Asynchronous Receive Transmit

UEP – Universal Evaluation Platform

UI – User Interface

USB – Universal Serial Bus

VI – LabVIEW Virtual Instrument

WPI – Worcester Polytechnic Institute

Authorship

This report was a collaborative effort between all the members of the Universal Evaluation Platform team. All members contributed equally to the research and development of this project, and are collectively responsible for all sections of this report.

Meet the team: Left to Right: Sagar Mahurkar, Erik Paulson, Jorgo Mihallari, Dylan Baranik

Executive Summary

Product/Test engineers build a custom testing platform to test, evaluate and debug every product before a datasheet exists to quantify its characteristics. Not only is building a new platform for every product time consuming, but it is also expensive. A survey of these engineers was conducted. It was discovered that the cost associated with evaluation platforms varied from $1,000 to $200,000, median being $50,000. The Universal Evaluation Platform allows automated and streamlined verification testing that would save engineers time and companies valuable resources. A generic and customizable evaluation platform can be used multiple times for a variety of components and designs. The versatility that comes from the customization aspect can save companies and engineers resources and time that would have been used to develop new evaluation platforms.

The main features of the Evaluation Platform include fixed and variable power supplies, common IC digital communication protocols, and digital signal processing for real-time digital filter implementation.

The power supply systems were built to allow configurable power provisioning to a device under test. Fixed power supply rails of 5V, 3.3V, 2.5V and 1.8V are provided for reliable power output to a device. These rails were made using multiple LP3962 1.5A Fast Linear Regulators from Texas Instruments were optimized for stability under loads up to 1A. The adjustable power supply allows for a range of 0V to 4V output. This is aimed to test the spectrum of voltages over which the devices would operate maintaining expected behavior. This was accomplished with the LT3083 3A single resistor linear regulator from Linear Technology. The power supplies allow for configurability under testing conditions and emulate the operation of a lab power supply.

Digital communications consisted of the following serial protocols: Serial Peripheral Interface (SPI), Universal Asynchronous Receive Transmit (UART), and Inter-Integrated Circuit (I2C).

The SPI is implemented in Verilog on the Xilinx Kintex-7 FPGA KC705 evaluation kit. The interface allows both read and write. SPI is a loosely defined interface, thus the Verilog code was designed to offer flexibility. Configurable clock edges for read and write, chip select, sync signal, and length of data were offered.

The UART interface was implemented by leveraging the soft-core processor MicroBlaze offered by Xilinx. Through the MicroBlaze wizard, the baud rate can be set, and interrupts for receive and transmit can be enabled. By default, the UART module communicates at a baud rate of 9600 baud.

The I2C bus, implemented in Verilog and VHDL (VHSIC Hardware Description Language), on the Xilinx Kintex-7 FPGA KC705 enables a single master device to communicate with any number of slave devices via a single two-wire bus. The user control capabilities allow three I2C commands to be specified and sent repeatedly.

All the subsystems are managed from a user interface. This panel is a simple text based command window in PuTTY which communicates via serial to MicroBlaze, a soft-core processor on the FPGA. When the user opens up the control panel, they are greeted with the main menu where they are asked to select which subsystem they wish to set parameters for. The user has the capability to return to the main menu at any point by pressing the “c” key. After the completion of a submenu the user is returned to the main menu where they can select a different subsystem.

The Universal Evaluation Platform is a lab bench on a board that offers multiple communication protocols to support a wide array of products, fixed power supplies to output

stable voltages, an adjustable power supply to support a spectrum of supply testing, and a user interface to support easy interaction with the features.

1. Introduction

As the electronics engineering industry matures, it is important to spend less time (engineering dollars) while evaluating circuit components. For product and test engineers, a design goes through several phases. One of these phases is testing the product for its expected properties and performance, before a datasheet exists, to quantify these characteristics. Product/Verification Engineers build a custom testing platform to test, evaluate and debug every product. This testing ensures that the design performs as expected.

A device under test (DUT) is verified for expected outputs and behaviors with test inputs. Manual and semi-automated testing processes can be cumbersome and time consuming. Such exhaustive testing is required to ensure that the design performs as expected. Current testing platforms are almost always exclusively designed for a specific product, and hence not reusable for different versions or entirely different products. Automated and streamlined verification testing would save engineers time and companies valuable resources. A generic and configurable evaluation platform can be used multiple times for a variety of components and designs. This Major Qualifying Project has developed the Universal Evaluation Platform to address this problem. The versatility that comes from the configurable aspect of the Universal Evaluation Platform allows it to be used as a test and evaluation platform for a large variety of products. Thus, it can save companies and engineers resources and time that would otherwise be spent on development of new evaluation platforms. The UEP configurable evaluation platform can act as a ‘lab bench on a board’.

2. Background

The testing of electronic components has been required as long as electronic devices have been under production. Modern test equipment automates and enhances manufacturing, design and testing processes. This increases yield and quality of product, while improving customer satisfaction by mitigating the number of malfunctioning components. Testing provides the entire engineering process with a feedback loop, allowing engineers to find potential issues more quickly and easily. Testing is broken into phases based on the lifecycle of the device under test (DUT).

The number of different test phases typically varies from company to company, but most institute a model where testing is conducted throughout the design chain. There are several levels of testing that companies will employ to ensure that a product is optimized at each level. These testing phases include manufacturing testing, testing for yield, and evaluation testing for debugging. Evaluation platforms are most useful where initial behavioral characteristics have been described and need to be verified. While manufacturing testing can be fully automated, verification engineering before manufacturing stages is more complex and must often be completed manually.

With the complexity of devices continuously on the rise, testing processes become more complex and implementation-specific. In many cases, a specific evaluation platform must be developed in order to conduct production testing in a meaningful fashion. These specific cases require a great investment, both monetarily and in manpower. At the time of this writing, conducting a LinkedIn job search for “Electrical Test Engineer” yields 7,538 open positions in the United States alone.

The variety of test methods is expanding, due to the number of different devices now available on the electronics market. Some electrical components, like MOSFETs and BJTs

are relatively simple, and therefore require little testing. The testing for these parts can be easily automated. Other parts have a long tenure, such as the 741 op-amp, first created in 1968, and are well characterized and understood. New components are often much more complex, with many different applications within a single IC. These kinds of components can be programmable, perform multiple functions and work as a major operating block within a system. Many parts now utilize high-speed communications buses like I2C, or SPI. With the complexity of these devices, verification testing can take a long time and use extensive amounts of resources. To ease the process of verification, some companies target the automatic testing market, providing platforms to test components and systems.

2.1 Existing Solutions and Market

There are existing companies who work on automating system testing platforms. Some examples are ARC Technology Solutions, Bloomy, Astronics, and Test Systems Inc. The existing test platforms are used for ICs and larger scale systems in the domains of digital, analog, RF, microwave, mixed signal, and electro-mechanical. The commercial testing platforms offered are not only expensive, but also segregated. In most cases, every feature requires a separate system for testing. These systems leave little room for further development on the consumer end.

The Universal Evaluation Platform major qualifying project (MQP) has created a flexible system suitable for testing and debugging of many types of ICs and other electrical components. It allowed the end user to customize and manipulate circuit routing and features to sufficiently test upcoming products.

A survey was conducted by the team by sending a questionnaire to test engineering professionals. The survey inquired about the cost of evaluation platforms, importance of

features, and inquired about specifications wanted for the subsystems of the Universal Evaluation Platform. The questions and results are attached in Appendix E.

The cost of evaluation platforms ranged from $1,000 to $200,000, with the median being $50,000. This demonstrates the versatility of test platforms and high costs associated with them. The survey asked the participants to rate importance of each feature of the evaluation platform. Table 1 shows the results for this question. 100% of the responses indicated that a configurable power supply was important, and 75% of the responses indicated that digital communication interfaces with DUT were important. These two subsystems were chosen as the most important requirements for the platform. The Universal Evaluation platform supports features to test and debug products at a stage that the datasheets are not ready. For this, the features were made as configurable as possible.

Table 2.1 Survey Results for importance of features

Question	**Important**	**Moderately Important**	**Not Important**
Configurable Real Time Digital Filters	0.00%	87.50%	12.50%
Digital communication interfaces with DUT	75%	12.50%	12.50%
Configurable power supply settings	100%	0%	0%
Simple Function Generator	50.00%	50.00%	0%
LabVIEW UI	62.50%	25%	12.50%
LVDS Amplifier	12.50%	62.50%	25%
Artificial Intelligence for Testing suggestions	12.50%	25%	62.50%

3. System Overview

The design of the Universal Evaluation Platform addresses the wide array of electrical components available on the market by making use of several robust and flexible subsystems. The subsystems are hosted on three main blocks: the field programmable gate array (FPGA), user interface, and custom hardware (figure 3.1).

An FPGA was chosen for implementation of digital design instead of a microprocessor in order to allow large amounts of parallel processing, and support a plethora of IO pins. The Kintex-7 KC705 FPGA Evaluation Kit was lent to the team by Prof. R. James Duckworth. This FPGA was chosen for its provision of a high pin count FPGA Mezzanine Card (FMC) connector, exposing a total of 400 IO pins. Additionally, the FPGA supported 407,600 Slice Registers, 203,800 Slice Look up Tables, and the soft core processor Microblaze [1].

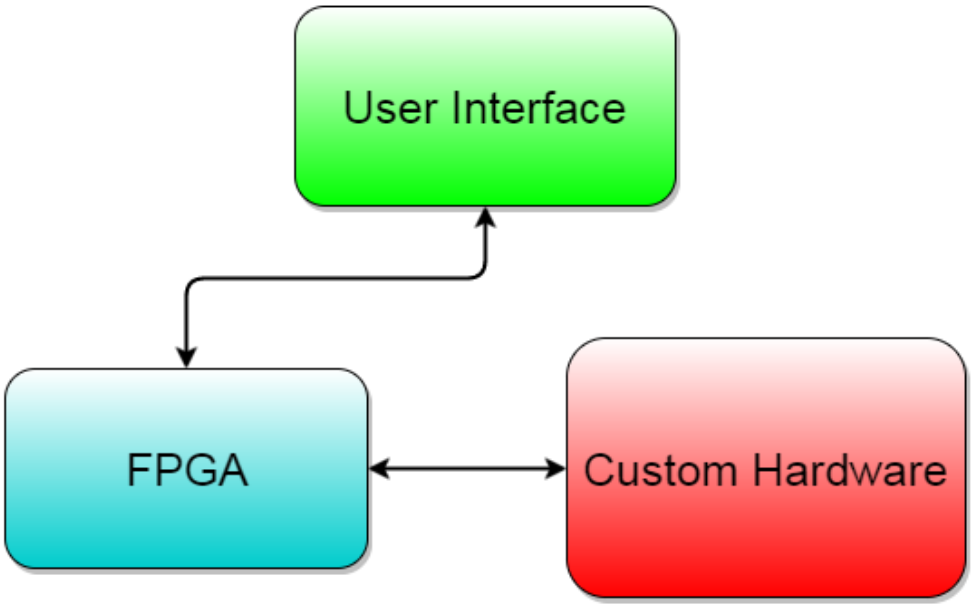

Figure 3.1 Universal Evaluation Platform System Level Block Diagram

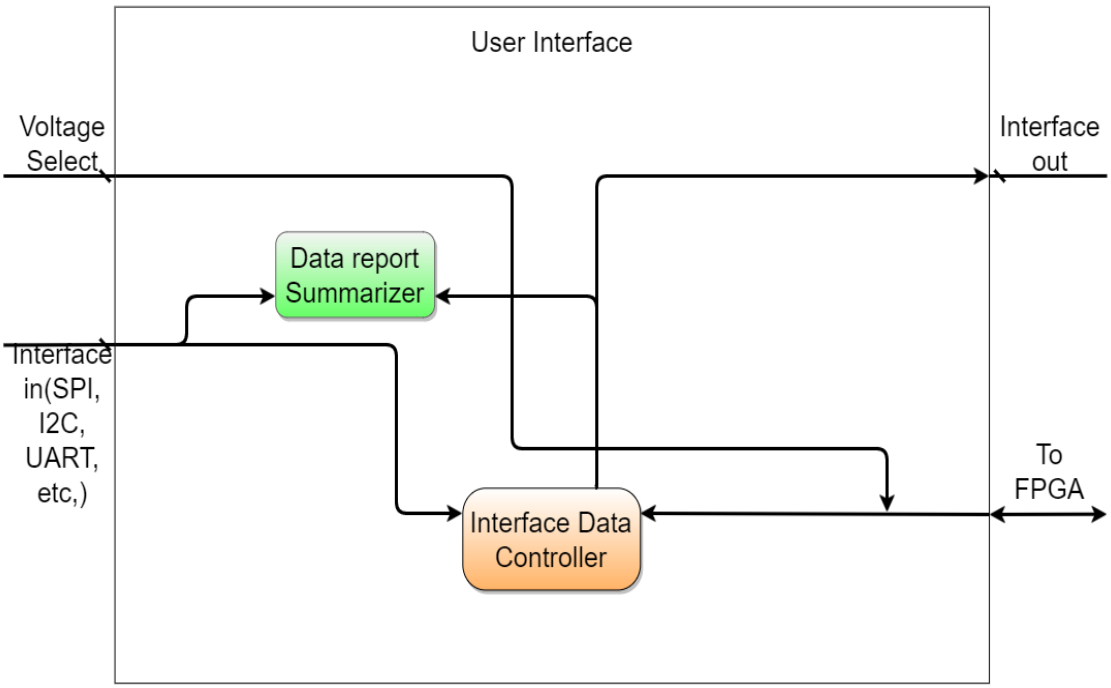

Figure 3.2 User Interface Block Diagram

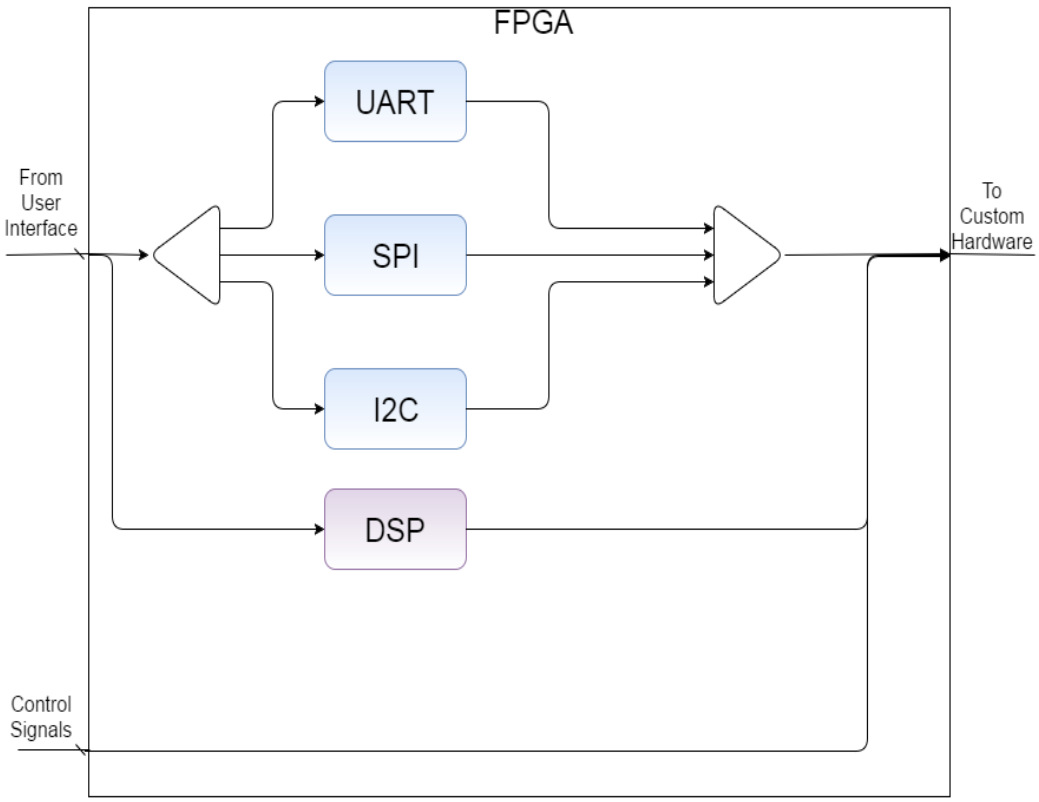

Figure 3.3 FPGA Digital Communications and Controls Block Diagram

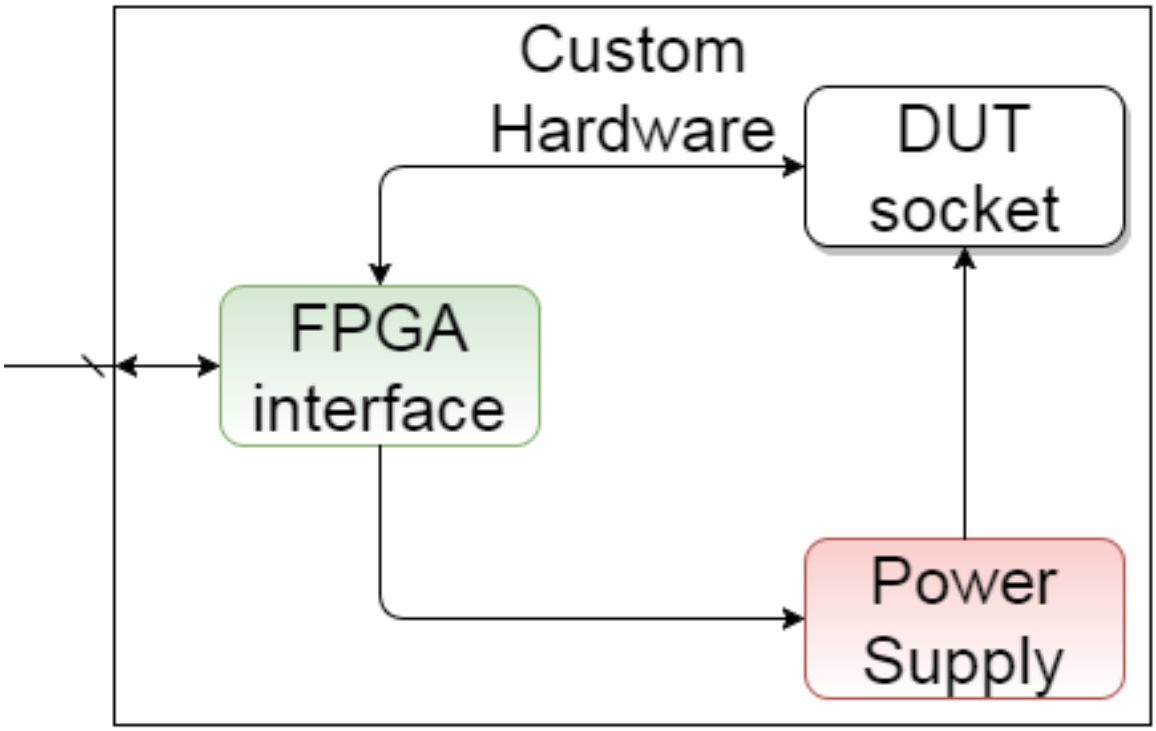

Figure 3.4 PCB Implementing Interface to the DUT, and the Power Supply

The complexity of all the project goals required that a tiered structure be deployed for project management. The structure consisted of three levels. The first level (L1) addressed aspects of the project which were of critical need to the final product. The second level (L2) involved subsystems which were believed to be more complex to execute and would be logical to work on only once the L1 subsystems were complete. Finally, the third level (L3) referred to components of the project which fell into two categories. These components were either very difficult to accomplish given limited time, or they were not important for the final product. The level assignments corresponded to the results obtained for importance of subsystems from the survey.

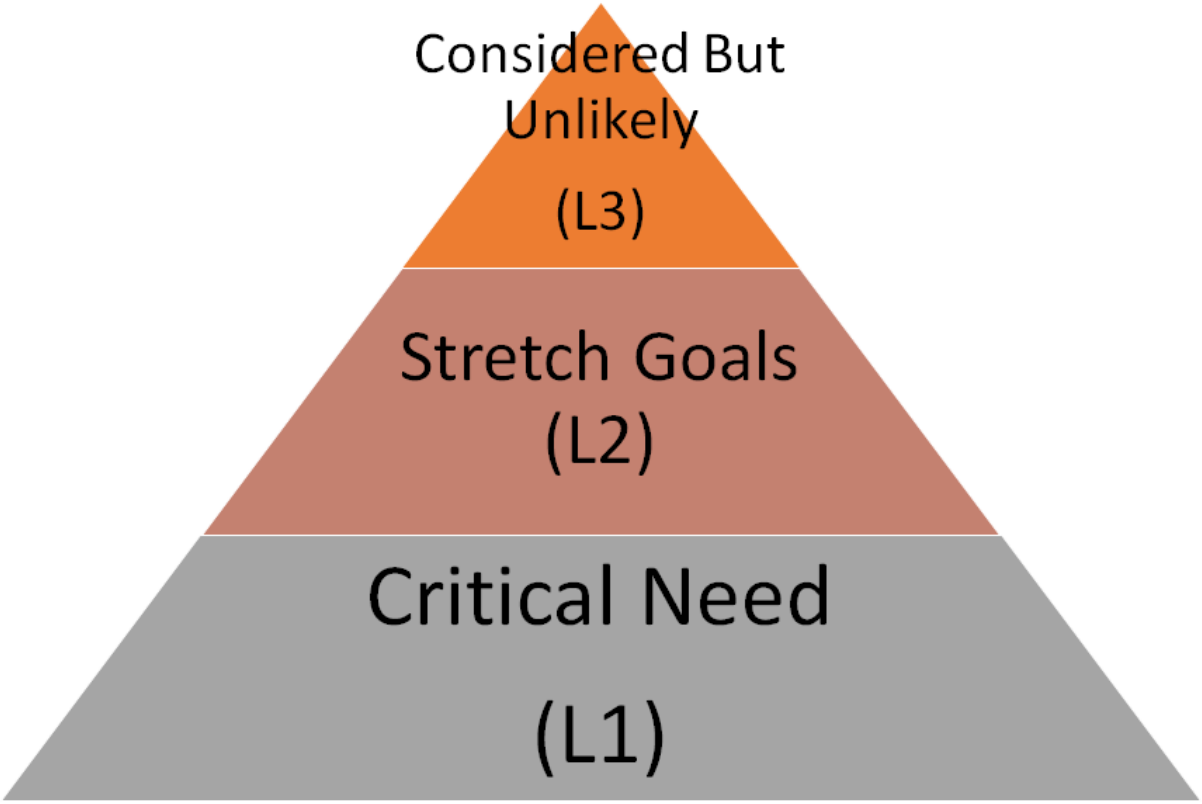

Figure 3.5 Tiered Structure for Importance of Subsystems

3.1 Critical Needs (L1)

The following list of subsystems are components which are critical to the project and received foremost attention. Their development formed the basis upon which the rest of the project was built upon. Two subsystems composed this L1 category, they were the precision DC power supply and flexible digital communication interface.

3.1.1 Precision DC Power Supply

The Universal Evaluation Platform implemented several operating voltages in order to interface with devices of varying architecture and power requirements. To achieve this, the platform implemented precision power supplies, both in variable and fixed formats. Variable power supplies allow ICs to be tested under corner cases such as under voltage and

overvoltage conditions. Otherwise, fixed power supplies can drive ICs at common levels, including 1V8, 2V5, 3V3, and 5V.

3.1.2 Flexible Digital Communication

Flexible communication interfaces are required in order to make use of complex digital ICs. These ICs often implement serial communications protocols such as I2C, SPI, and UART which must be included in the evaluation platform to facilitate communication. These modules were customized such that the signals and associated clocks can be routed to different pins. Additionally, flexibility in timing and clocking is important to interface with a variety of ICs.

3.2 Stretch Goal Subsystems (L2)

Stretch goals, or L2 subsystems are those which will serve as beneficial add-ons to the final product. These items are not absolutely essential, however. As such, their development fell secondary to the previously listed critical systems. Stretch goals include pattern generation, digital signal processing and a user interface (UI), further explained below.

3.2.1 Digital Signal Processing

Digital signal processing can be used to perform any necessary signal conditioning. This may be useful for test engineers that would like to isolate or separate frequency ranges for debugging and noise cancellation of signals being sent or received, with reference to a DUT.

3.2.2 User Interface

A user interface allows an engineer to set the parameters of their test to evaluate the DUT. A MicroBlaze was utilized to generate the user interface. MicroBlaze is a soft-core processor implemented on the FPGA. Xilinx provides support for a soft-core processor,

MicroBlaze, the hardware of which is implemented on the FPGA as well as a software development kit that supports C programming to control the MicroBlaze. The user interface is opened up in a PuTTY terminal that communicates via UART to the MicroBlaze, providing full control over the subsystems resident on the FPGA. All parameters were made easily adjustable requiring minimal effort on the part of the engineer.

3.2.3 Pattern Generation

A function generator is a crucial lab tool in order to test sensors and systems. A proposed feature of the system was a flexible pattern generator to create analog signals like sine waves, square waves, triangle waves and other patterns. These functions were planned to be implemented at various frequencies.

3.3 Reach Tasks (L3)

The following items were considered in the early stages of the project. They were determined to be too difficult in implementation, and therefore had a minimal priority. As such, potential implementations for these systems will not be discussed in any subsequent sections. However, prior thoughts on the usefulness of these systems are provided here.

3.3.1 LVDS Systems

Low Voltage Differential Signals operate at a low power and can run at very high speeds, using inexpensive twisted-pair copper cables. This standard is used in many communications applications. Unfortunately, this signal can be hard to capture due to its finicky nature and high speed. Usually, the signal is only valid for capture during a part of its period (~50%). An LVDS amplifier would help analyze the nature of the signal, and make data capture easier.

3.3.2 Artificial Intelligence

The main purpose of the evaluation platform is to be able to detect problems in the functioning of a product and help debug them. Many of the problems detected are something seen previously. However, this might be seen by some other team, at some other location, or in a previous version of the product. A large amount of time and resources are spent in solving the same problems multiple times.

An artificial intelligence would help optimize the process of debugging. It will sort errors based on factors such as locality, keywords of symptoms, rate of occurrence, and the most recent occurrence. Based on the symptoms provided by the engineer, it will suggest possible problems, checks and solutions.

4. Methodology

The following section discusses the challenges faced, and breakthroughs made by the Universal Evaluation Platform team during the course of this project.

4.1 Power Supply

The design and testing of the power supply was prioritized due to its status as an L1 subsystem. Power supply development immediately adopted into a two-pronged approach with both fixed and variable voltage supplies provisioned to the DUT. The first step of the design process was to determine the specification of each supply. Detailed specifications of the supplies are provided in a fact sheet in Appendix A.

4.1.1 Variable Power Supply

The requirements of the variable power supply were defined as follows:

- Percentage control over output level
- Fine control in voltage output via least-significant bit changes
- Clean output voltage

With the above criteria in mind, investigations into switching and linear supply technologies were conducted. It was immediately found that for a precise voltage output, linear regulation was preferable. While linear regulators produce more heat, they do not suffer from coupling switching noise into the output line. A diagram comparing the outputs of 12V switching and linear (LDO) supplies is provided in Figure 4.1.

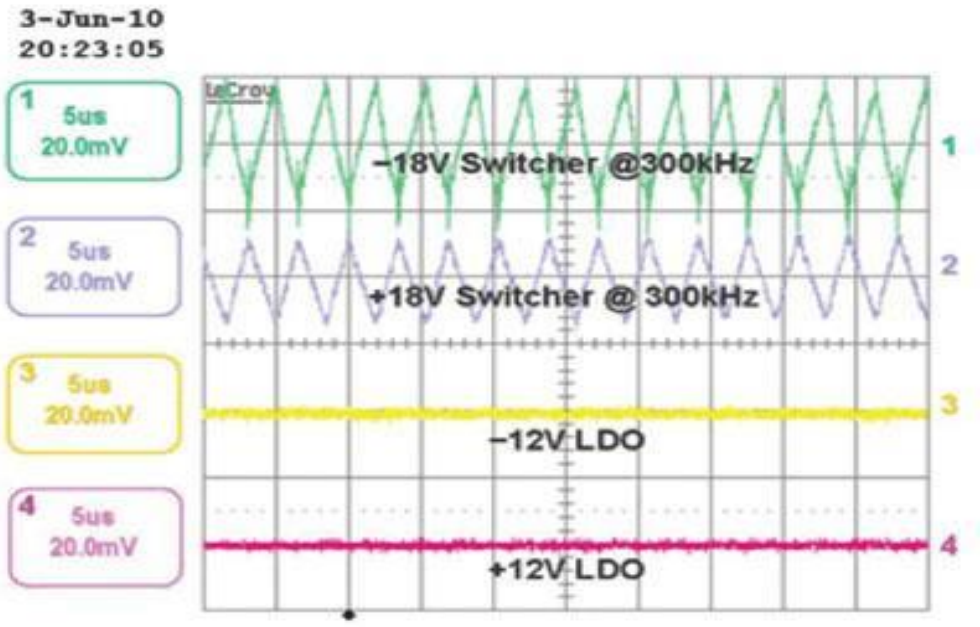

Figure 4.1 Voltage Ripple Comparison between Switching and Linear Power Supply Technology [2]

Modern linear regulators accomplish reasonable efficiency while providing sufficient amounts of current. Many of these are inherently variable, using a current source topology to set output voltage. An example of this type of device is the Linear Technology LT3080 [3] 1.1A low dropout voltage linear regulator [4]. Control of these regulators was established by putting a variable resistance in series with the current source, generating an output voltage across the output line. The chosen method to provide a variable resistance is with a digital potentiometer. The Analog Devices AD8400 [5] SPI 255 step digital potentiometer was selected for this application. This part provides a range of a 0Ω to 100kΩ. This allowed for an effective voltage range of 0V to 5V.

In Figures 4.2 and 4.3, a schematic capture and layout for the AD8400/LT3080 power supply combination are provided. These plans include capacitors for load line filtering and stability.

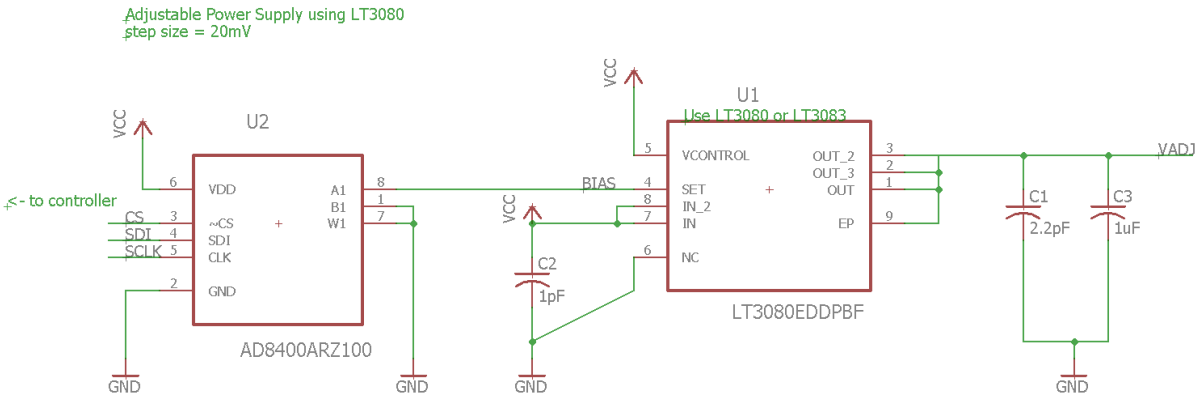

Figure 4.2 Revision 1 Variable Power Supply Schematic

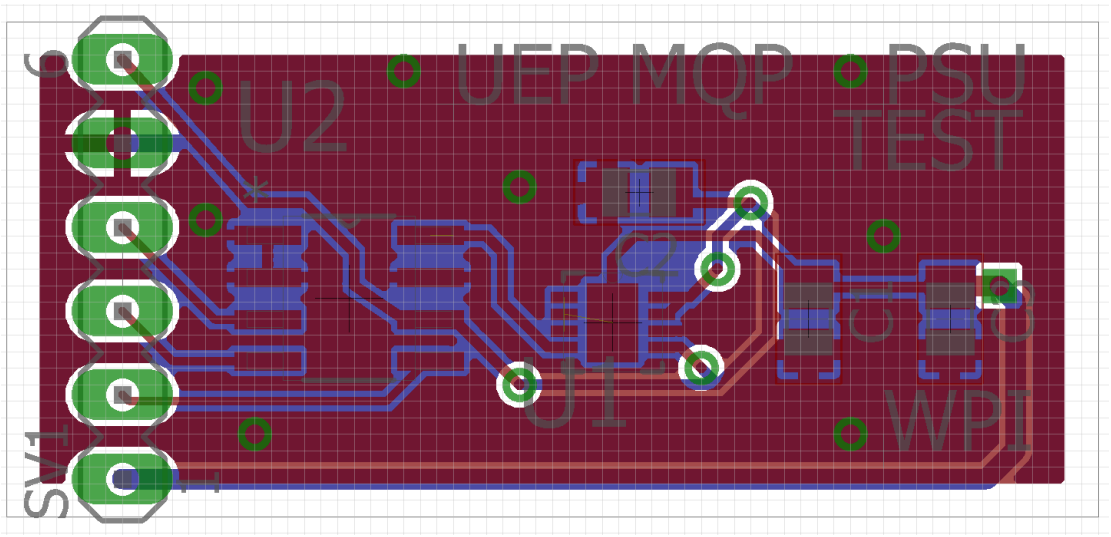

Figure 4.3 Revision 1 Variable Power Supply Layout

The original power supply design proved problematic as the package footprint for the LT3080 was incorrect. The MS08E package was too small for hand soldering and the exposed pad would not provide enough thermal transfer. As an alternative, a new design was proposed and then laid out using the same parts with different packages. For ease of verification, custom circuit symbols were created in Eagle [6] to keep packages consistent.

Further thermal considerations prompted the team to develop robust power dissipation guidelines. For user and component safety, the 5DD-PAK of the new LT3080 should remain at or below 60 degrees Celsius even during extended high current testing. For an input voltage of 6V, an output voltage of 1V, and the maximum current draw of 0.5A, this meant

that the package would need to dissipate 2.5W safely. Power estimations revealed the following [4].

$$T_J = T_A + P_{TOTAL} * \theta_{JA}$$

$$where\ T_A = 25\ ℃, P = 2.5W, \theta_{JA} = 35℃/W$$

$$T_J = 147.5\ ℃$$

This thermal junction temperature was unacceptable. In order to resolve this, two parallel power resistors are placed in series with the IN terminal of the device. This limits the voltage dissipation over the pass transistor based on current throughput. The resistors are determined as follows [4].

$$R_S = 2\ \Omega\ meant\ a\ Vdrop\ of\ 1V\ across\ pass\ transistor$$

$$Now, P_{TOTAL} \sim = 1V * 0.5A = 0.5W,\ T_J \sim = 50\ ℃\ (safe)$$

$$remaining\ dissipated\ across\ resistors$$

In the final design the load is shared across two 4Ω resistors in order to equally distribute power dissipation. Therefore, the remaining power of 2W is 1W per resistor. The resistors chosen are rated for 3W each so they should provide satisfactory heat transfer with this distributed method.

The schematic was revised as shown in Figure 4.4. Note the addition of R1 and R2 as explained above.

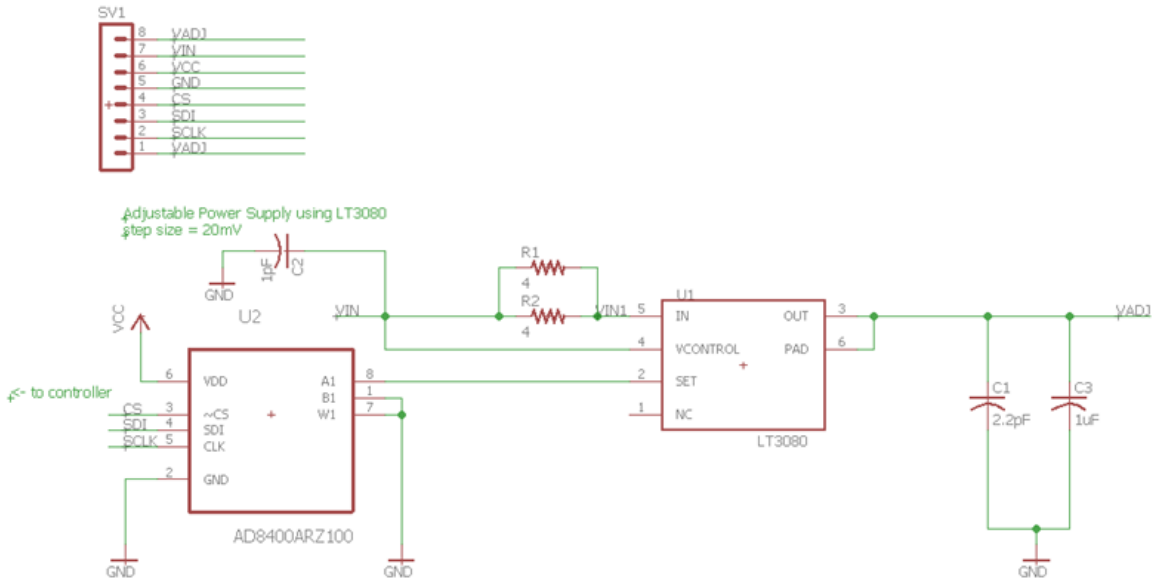

Figure 4.4 Revision 2 Adjustable Power Supply Schematic

The board layout was also revised as shown in Figure 4.5. The new board layout accommodates much wider PCB traces and includes split ground planes for thermal and connectivity reasons. Current carrying traces were increased in width to match pad size. Signal traces remained mainly the same as the previous design. Finally, the planes are double-sided in order to assist in the thermal conductivity of the part.

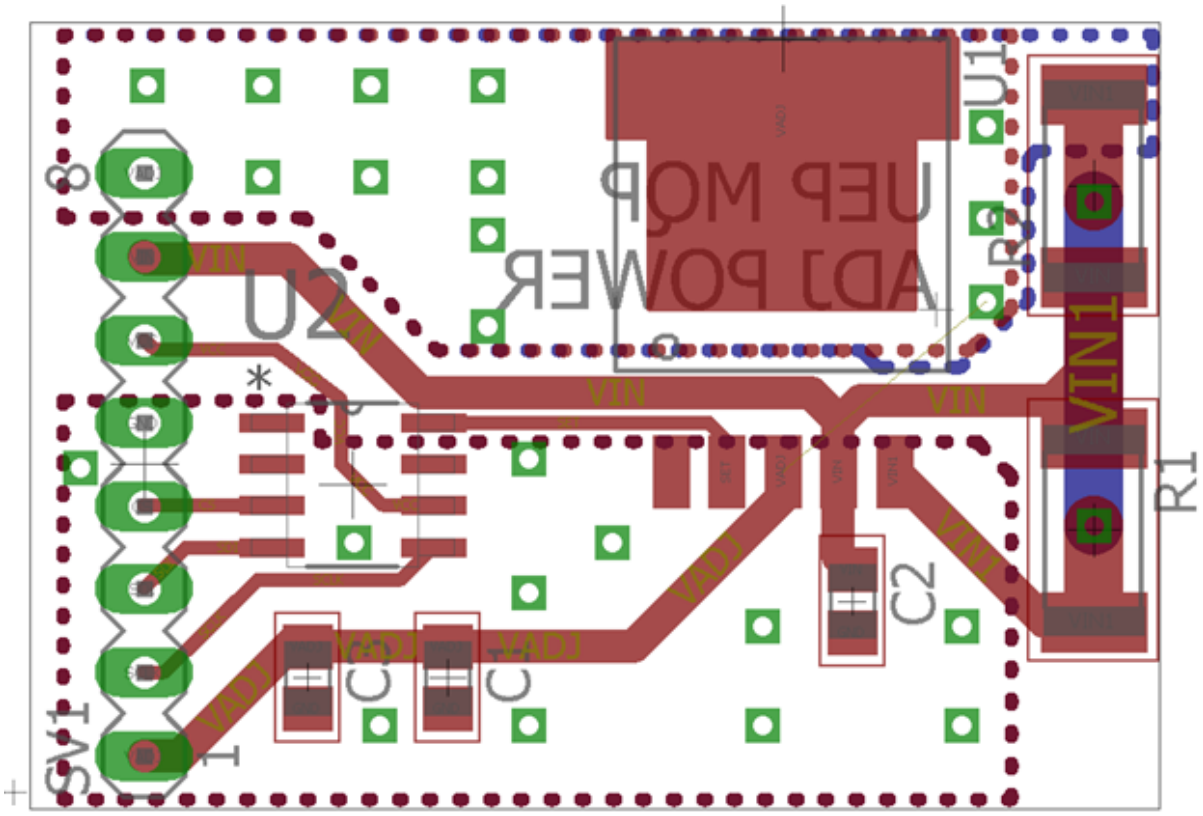

Figure 4.5 Revision 2 Adjustable Power Supply Layout

The revised design of the adjustable power supply has been fabricated and assembled (Figure 4.6).

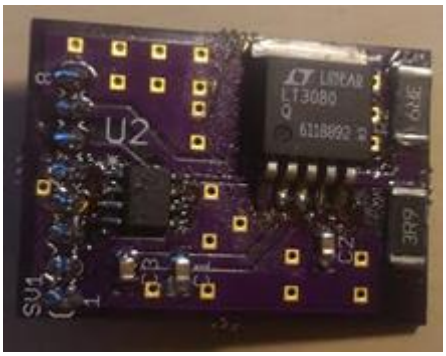

Figure 4.6 Adjustable Supply Assembled on Printed Circuit Board

Preliminary testing of the adjustable power supply indicated several items that were to be improved. The AD8400 is a SPI device which can have its values selected programmatically. First, the digital potentiometer, AD8400, was tested without the linear regulator with a microcontroller-based system (MSP430). This initial testing yielded useful knowledge about the AD8400's SPI transaction structure (see Figure 4.7 below). This SPI

transaction includes two address bits (A1, A0) setting the output channel of multi-channel RDACs, and eight data bits (D7 - D0) for the value. Some strange results were found while testing the system using the microcontroller, as it did not perfectly implement these 10-bit SPI transactions.

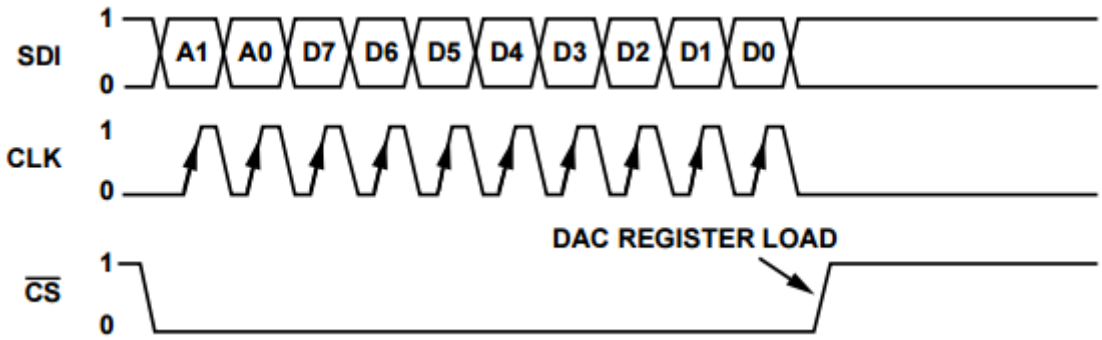

Figure 4.7 AD8400 SPI Timing Diagram

In order to implement the SPI transaction testing, the firmware was ported to the FPGA platform. On the FPGA, finer detail and control could be exercised with the SPI structure. The adjustable power supply verification began successfully once the SPI hardware on the FPGA was available for this use. In order to make testing as easy as possible, the user interface features of the project were built at this time. SPI transaction verification was assured using the oscilloscope.

The performance of the RDAC was evaluated next by testing the resistances given specific SPI transactions (codes). The linearity and repeatability of some common values were tested and verified to match the AD8400 datasheet specifications. The remaining components of the adjustable supply were then assembled and tested.

Initial verification of the entire system did not match original design expectations. With most RDAC values, the linear regulator would saturate at roughly 1V below the supply voltage. Given the supply voltage of 6V, the output would be stuck at 4.7V. The linear regulator was allowed to float without proper loading. Certain values changed the output, but the expected range of 0V to 5V was not available. The circuit needed troubleshooting.

A critical oversight was discovered with the choice of the LT3080 voltage regulator. In order to set the output voltage, the LT3080 exposes a 10µA current source to an external pin, which is connected to the RDAC. Using Ohm's law, it's easy to find the first problem. A 100kΩ potentiometer and a 10µA current source produces a voltage of 1V. This is far below the expected range. Fortunately, Linear Technology offers a regulator with identical topology to the LT3080 which uses a 50µA current source. The LT3083 [7] 3-amp regulator was chosen to replace the LT3080. While more expensive, the use of this new part also improved expected performance characteristics. The revised schematic is as follows: the circuit implements an LT3083 with the AD8400. This schematic sees added bypass capacitance for the ICs (see Figure 4.8).

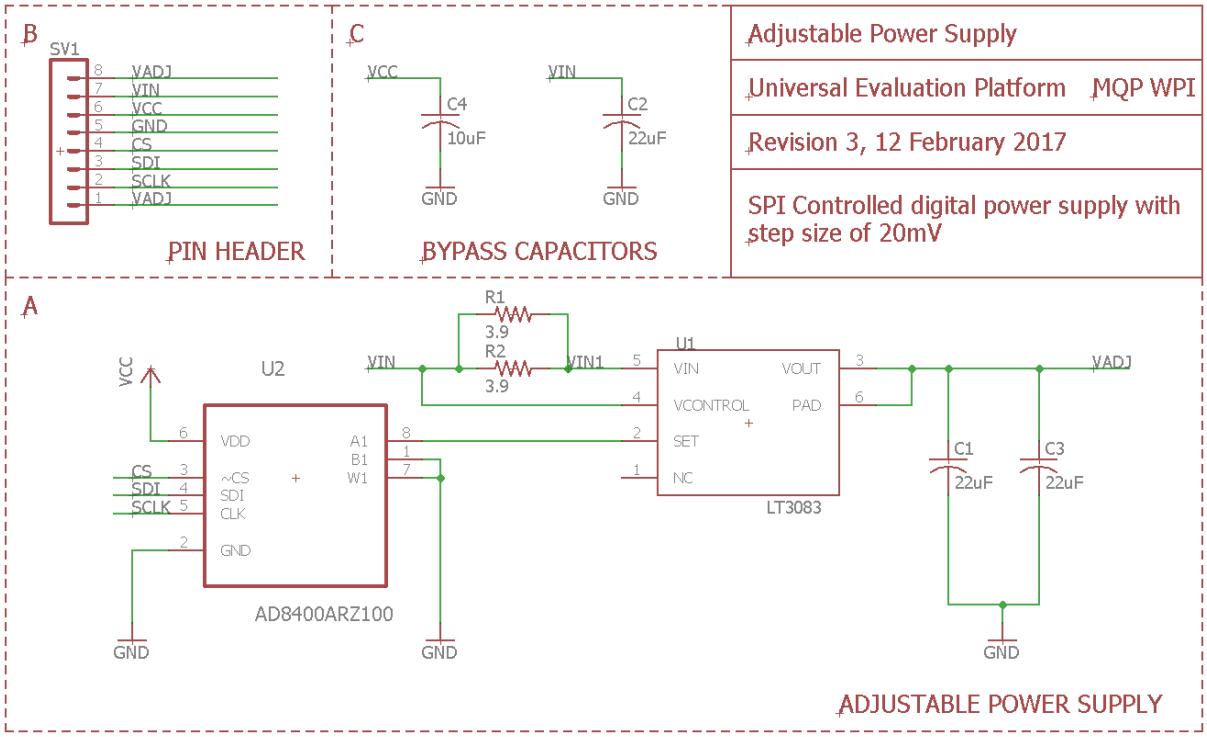

Figure 4.8 Revision 3 Adjustable Power Supply Schematic

The adjustable power supply underwent further testing, as it still provided unexpected values while not connected to any load devices. The next reasonable troubleshooting step was to apply a load to the power supply and measure performance. Under these conditions, it was possible to characterize the adjustable power supply. As such, testing will apply to loaded

conditions only. As current approaches 0A, the adjustable power supply may perform outside of specifications.

A few modifications were made to the schematic which were not possible to bring up in an additional revision of the board. This is the addition of more bypass capacitance for ICs. The slight modification can be seen in the final assembled board in Figure 4.9.

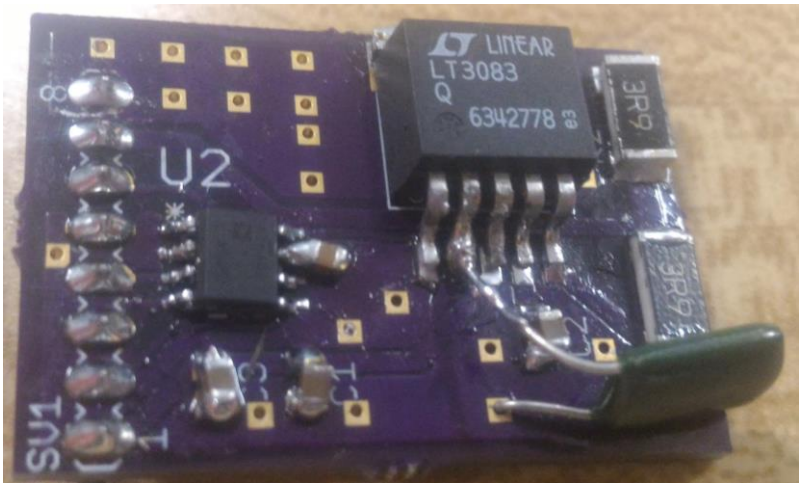

Figure 4.9 Revision 3 modifications without respinning PCB

The final design of the adjustable power supply board allowed for the circuit to function effectively. At this point, the circuit test methodology (discussed in Section 5.1) was applied and results were collected.

4.1.2 Fixed Power Supply

In the case of the fixed power supply both switching and linear topologies were pursued due to less constraining control requirements. It was decided however that a linear topology would be more desirable since it makes the design simpler and leaves less concern over unexpected behavior. This is critical for a power supply which will be provisioning supply voltages to many of the DUTs and control logic for other systems. The first IC to be considered was the Texas Instruments LP8728 [8] which provides four rails from 1V2 to 3V3, largely satisfying the power requirements of normal logic devices. This device

however, was abandoned after realization that the available package was too small and would be very difficult to properly solder to the board.

Further investigation into other ICs which would meet our requirements was done. The Texas Instruments LP3962 [9] is a linear regulator which met all the requirements and was large enough to easily work with and manually solder onto the board. The package came in four different variations each providing four different voltage outputs, these being 1V8, 2V5, 3V3, and 5V. The IC also features a shutoff pin making turning on and off each IC individually a simple task. A schematic of the 5V fixed rail is shown in Figure 4.10. As seen in the schematic a simple NMOS transistor is connected to pin1 which is the shutdown pin. The NMOS is controlled by the FPGA allowing individual control of the ICs to be turned on and off. Our design specifications report that the fixed rails will have the ability to provide a maximum of 1A of current. The LP3962 is capable of producing a total of 1.5A which surpasses the original requirements. This large current output however raises a major concern about proper heat distribution and management. For this reason, the team decided to take a cascaded approach to the fixed power supply. This means that the output of each voltage level becomes the input the next lower voltage level. For example, the 5V output becomes the input to the 3V3 IC. This means that in order to provide the lowest voltage output, in our case 1V8, we need to have all four power ICs turned on. A full schematic of the fixed power supply is provided in the Appendix which demonstrates this cascaded approach clearly.

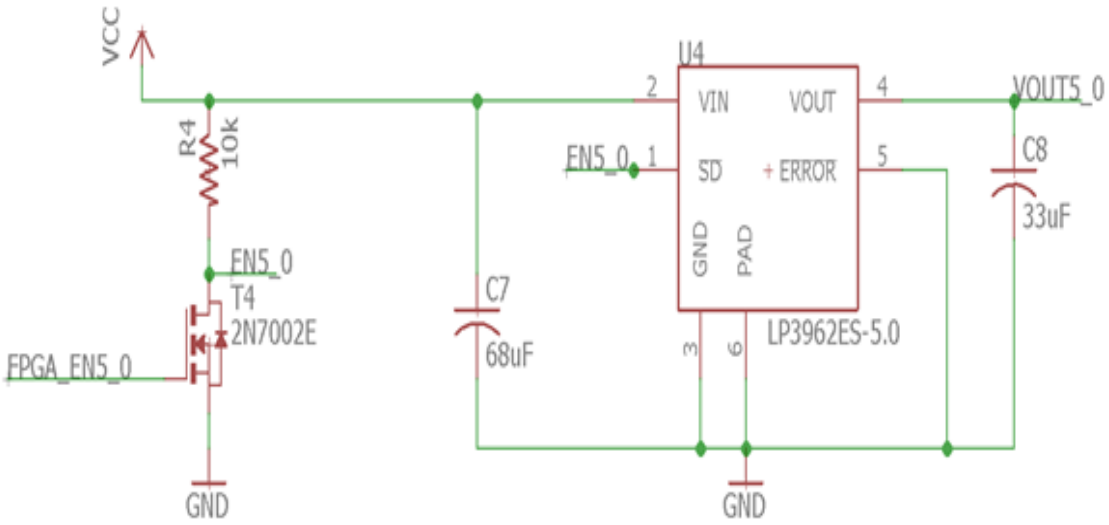

Figure 4.10 Fixed Power Supply 5V Rail

Once the schematic was finished the next steps taken were turning it into a PCB layout, taking into consideration the best way to deal with the potential heat that our board may produce. An image of the final PCB layout is provided below. The layout was designed in Eagle CAD and the board is a two-layer board. As can be seen, vias have been placed throughout the board wherever possible. This is to help with heat dissipation if a test engineer is required to use the 1A capability that this board can provide. The final fixed power supply PCB is shown below in Figures 4.11 and 4.12.

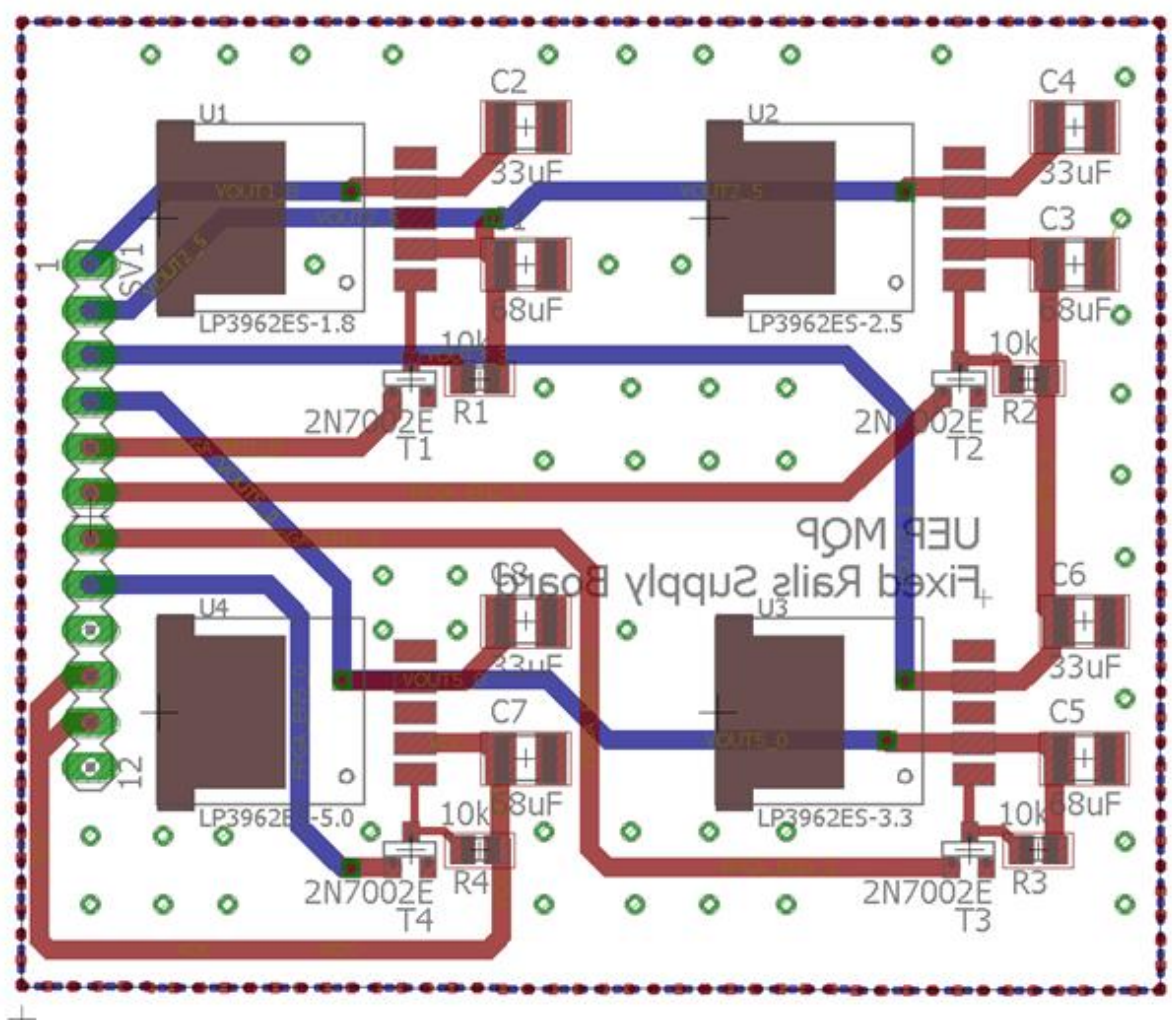

Figure 4.11 Layout Fixed Supply 4 Rails

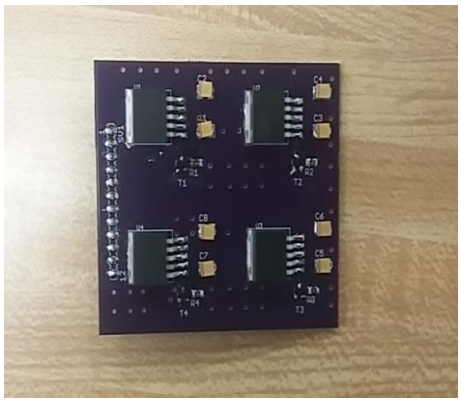

Figure 4.12 Fixed Power Supply Assembled Board

Preliminary testing yielded that each regulator was providing the correct voltages when 6V was supplied to the inputs, and the FPGA was able to bring the NMOS high, pulling down the shutdown pin and shutting the regulators off. At this point, the test methodologies

described in Section 5.1 were applied to the subsystem for performance characterization under varied conditions.

4.2 Digital Communications

It was decided that Serial Digital Communication interfaces will be implemented using the FPGA to interface with the DUTs. Serial Peripheral Interface (SPI), Universal Asynchronous Receiver and Transmitter (UART), and Inter-Integrated Circuit (I2C) were chosen to be implemented.

4.2.1 Serial Peripheral Interface (SPI)

The SPI Interface [10] was designed using Xilinx ISE Tools and Verilog. The SPI interface was classified into two parts with respect to functionality: Transmit and Receive.

The Transmit part was responsible for sending data from the FPGA to the DUT, while the Receive part was responsible for capturing data from the DUT on the FPGA. The design parameters shown in Table 4.1 were chosen for the SPI interface.

Table 4.1 SPI Design Parameters

Parameter	**Min**	**Typical**	**Max**	**Unit**	**Comments**
SDI Number of Bits in SPI	1	8	32	bits	The number of bits received by the SPI module
SDO Number of Bits in SPI	1	8	32	bits	The number of bits transmitted by the SPI module
Frequency of SCLK in SPI			100	MHz	The SCLK can operate on frequencies up to 500 MHz

For transmit module, the following inputs were provided:

- Number of bits of output: Size of output to be sent in bits
- Clock: Clock for Serial Clock

- Value of Output: Data to be sent to DUT
- Active Sync: Choice of having Sync high or low for the duration that data is sent out
- Reset: To reset the module
- Load: To load the data to be sent
- Tx Enable: To enable the module to transmit
- Active CS: Choice of having CS active high or low

Outputs of Transmit were sync, chip select (CS), serial clock (SCLK), and serial data out (SDO). For processing in the module, a counter was used to keep track of the bit to be transmitted. The Sync and CS signals would be active for the period that data was being sent out. SCLK was set to be the same frequency as input clock. Two different modules were created to send data on the positive and negative edges of the clock.

For the receive part, following inputs were provided:

- Number of bits of input: Size of input to be captured
- Clock: Clock for Serial Clock
- SDI: Bitwise data from DUT to FPGA
- Active Sync: Choice of having Sync high or low for the duration that data is captured
- Reset: To reset the module
- Load: To load the data to be sent
- Tx Enable: To enable the module to transmit
- Active CS: Choice of having CS active high or low

Outputs of Receive were sync, chip select (CS), serial clock (SCLK), and data captured. The bit to be captured was monitored using a counter. The Sync and CS signals would be active for the period that data was being received. SCLK was the same frequency as

the input clock. Two different modules were created to receive data on the positive and negative edges of the clock.

SPI was the first Verilog module implemented on the FPGA. Interfacing with the FPGA was a challenge on many frontiers. The Kintex-7 KC705 FPGA only supports LVDS clocks. A Digital Clock Manager was used to convert LVDS clock to a single-ended clock output. The FMC IO pins were not easily accessible to probe. For this purpose, an FMC breakout board which allows easier access to the IO pins was purchased. It was found that the FMC pins have a fixed IO Standard of LVCMOS25. To use other logic levels, level shifters need to be used. The ordering of pins on the FMC breakout board was unclear. The numbering convention was discovered through trial and error. The FMC breakout board consists primarily of three sets of 2x20 pins. Originally the team thought that each pair of pins represented a positive and negative differential pair. Counterintuitively it was discovered that the differential pairs were aligned lengthwise.

4.2.2 Universal Asynchronous Receiver and Transmitter (UART)

The UART Interface was initially designed in Verilog. The original simulation is displayed in Figure 4.13 and 4.14. Figure 4.15 shows the ideal UART pattern. The following inputs were provided to the simulation:

- Number of bits of input: 8
- Number of bits of output: 8
- Value of Input: 10101011 (LSB first)
- Output to be captured: 01001111 (LSB first)
- Master: FPGA

The following results were obtained while testing Transmitter using simulation:

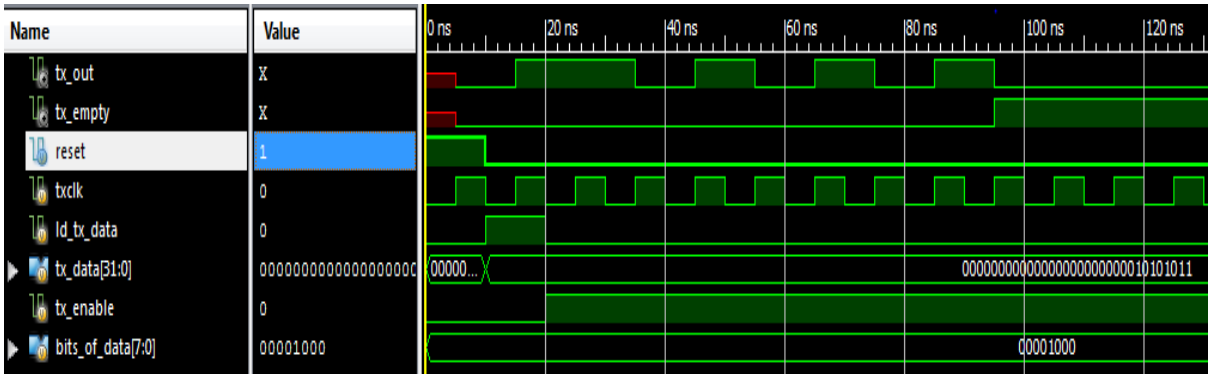

Figure 4.13 Results of TX in simulation (Top to Bottom: Data Out, Transmit Empty (not part of functionality), Reset, Serial Clock (not part of functionality), Load Transmit Data, Data to be transmitted, Transmit Enable, Number of bits of Data)

The following results were obtained while testing Receiver using simulation:

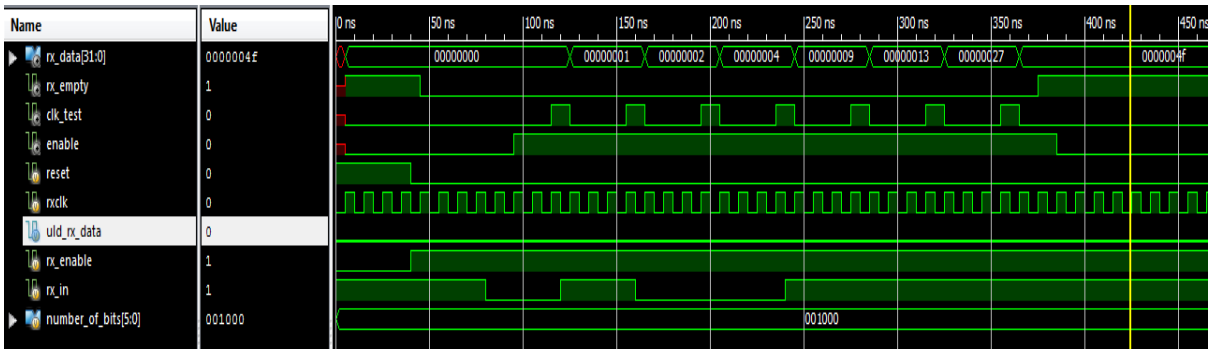

Figure 4.14 Results of RX in simulation(Top to Bottom: Data Captured, Receive Empty (not part of functionality), Serial Clock (not part of functionality), Enable, Reset, Rx Fast Clock (not part of functionality), Unload RX Data, Receive Enable, Data Input , Number of bits of data)

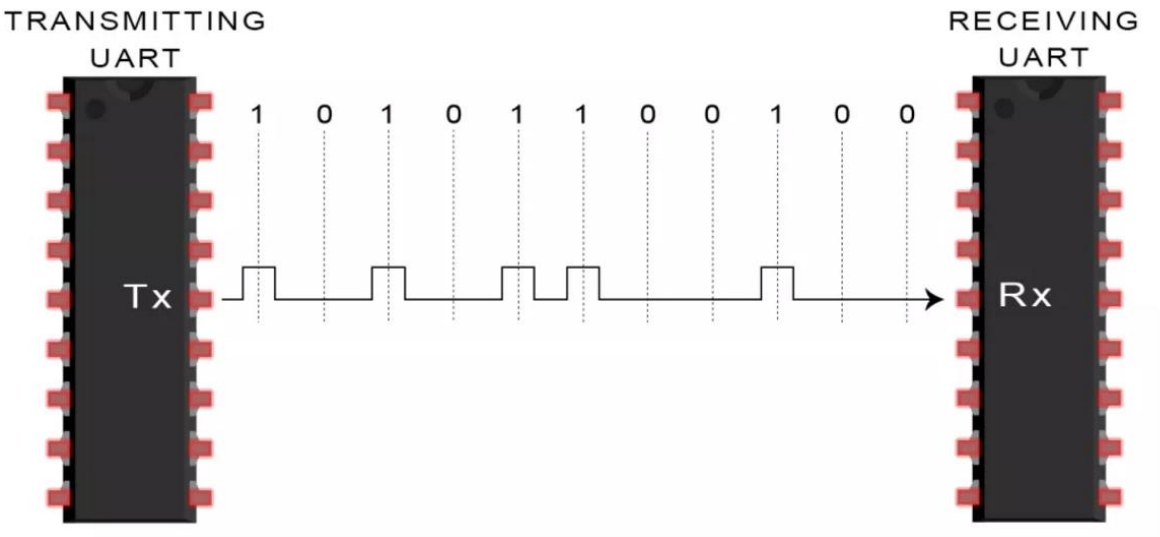

Figure 4.15 Correct UART Protocol [11] (Data being transmitted from UART TX to UART RX)

However, it was discovered that MicroBlaze, a soft core processor designed by Xilinx offered UART capabilities. This was leveraged to implement the final UART module. The baud rate can be modified through the MicroBlaze setup wizard, and interrupts can be enabled. UART interrupts were enabled, and the default baud rate was set to 9600 baud.

Interfacing with the UART from MicroBlaze was a challenge. The naming convention for Transmit and Receive on the Universal Constraints File (UCF) provided by Xilinx were reversed from the perspective of MicroBlaze.

4.2.3 Inter-Integrated Circuit (I2C)

I2C is a digital communication protocol which allows for many devices to communicate through a two-wire bus consisting of a clock line (SCL) and a data line (SDA). Both lines are connected to pull-up resistors so that their default state is logic high when not being driven low. The device designations in this protocol are master-transmitter/receiver or slave-transmitter/receiver. The protocol dictates an optional feature of allowing for more than one master device, in which a timing arbitration scheme decides what device will control the lines, however multi-master capability is not currently in the scope of this project. [12]

In order to implement I2C, a first attempt was made using a VHDL module, i2c_master.vhd [13], however due to a misunderstanding of its use, only a partially successful simulation of the module was performed as given in the following simulation (Figure 4.16).

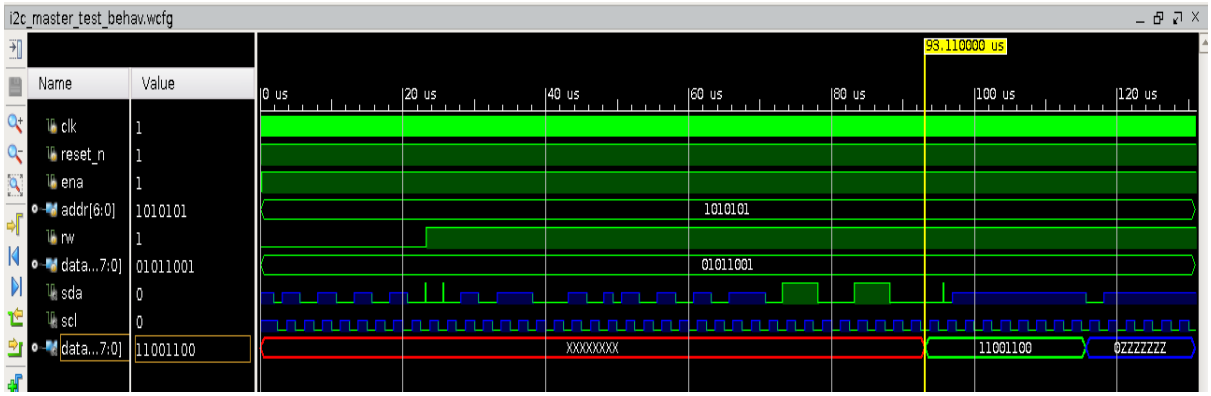

Figure 4.16 Simulation of VHDL I2C Module (Top to Bottom: System Clock, Reset, Enable, Address, Read/Write bit, Data, SDA, SCL)

Note that in the above simulation, the transaction does not correctly terminate. This is due entirely to improper use of the module at the time and will soon be elaborated on.

When it was believed that i2c_master.vhd was not functional, an attempt was made to write an implementation of it in Verilog using an eight state finite state machine. In this attempt, the states were IDLE, START, ADDR, RW, ACK, DATA, ACK2, END. While these states were not invalid, they were deemed insufficient for the needs of this subsystem because the module did not release control of the line (high impedance) but incorrectly drove the line to logic 1. At the same time, i2c_master.vhd was scrutinized further to see if it was still viable to modify it into a usable form. However, it was discovered that the importance of the busy signal provided by the VHDL module was not appropriately understood.

The proper use of i2c_master.vhd required keeping track of the number of times the busy signal transitions from low to high, depending on how many commands are desired in a given transaction. This is because the module waits until the enable signal goes high, at which point it will latch in the 7-bit address, R/W bit, and 8-bit data to be written (must be specified even if performing a read command). Once these fields are latched in, the busy signal is asserted. At this point, if there is another command in the transaction, then the enable signal should remain asserted and the new address, R/W, and data to write should be set and held until the busy signal once again transitions from low to high. Once all commands

for the transaction have been sent, the final command will be to simply de-assert the enable signal and i2c_master.vhd will create the end bit once ready. The i2c_master.vhd will handle all necessary logic to create the repeated start bit, therefore the control logic can be kept based entirely upon the enable, busy, address, R/W, and data to write signals.

For this project, three commands may be specified for an I2C transaction, but the control logic in Verilog can be easily modified to allow a user to specify the number of commands desired.

In order to verify the ultimate functionality of this system, a Sunfounder PCF8591 [14] AD/DA I2C device equipped with an on board potentiometer connected to input channel 1 was tested on a Raspberry Pi so that an oscilloscope capture of the expected functionality could be identified and compared to later. Once performance benchmarks were verified on the Raspberry Pi with the PCF8591 board, master-receiver and master-transmitter tests were conducted on a Spartan 6 Nexys 3 FPGA board using i2c_master.vhd and the Verilog control logic written for it.

Once the functionality was verified on the Spartan 6 Nexys 3, The Verilog code was transferred to the Kintex-7 KC705 FPGA board for final testing by comparing its performance against that of the Raspberry Pi.

4.3 Digital Signal Processing

The firmware for the digital signal processing system was developed such that a user could connect hardware and interface with the filters. The DSP subsystem was developed to take a sample-by-sample approach to digital filtering, using linear discrete convolution shown in Figure 4.17.

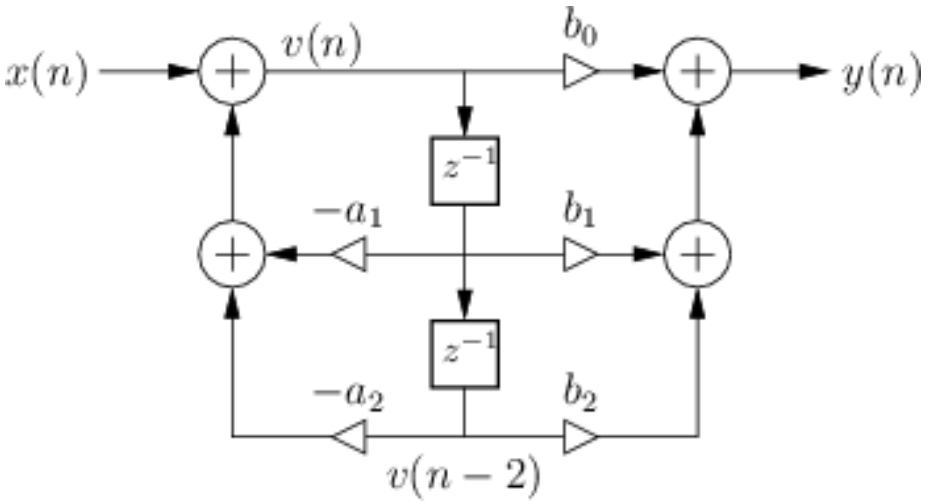

Figure 4.17 Second Order IIR Filter Signal Flow Diagram [15] w will be used instead of v to denote the intermediate variable

Since the computation is being performed on a MicroBlaze soft core embedded processor inside the FPGA, which is not particularly well optimized for digital signal processing. To curb this limitation, the following logical progression occurred: The DSP will only be applied for signal filtering. For an IIR filter defined by coefficients *a* of length *M* and *b* of length *L* allowed for some mathematical optimization of the IIR filtering method which is given as follows:

$$w_n = x_n - \sum_{m=1}^{M-1} w_{n-m} * a_m\,, \quad y = \sum_{l=0}^{L-1} w_{n-l} * b_l = w_n * b_0 + \sum_{l=1}^{L-1} w_{n-l} * b_l$$

$$assuming\ L = M\ \ldots$$

$$y = \underbrace{\left(x_n - \sum_{m=1}^{M-1} [w_{n-m} * a_m]\right)}_{w_n} * b_0 + \sum_{m=1}^{M-1} [w_{n-m} * b_m]$$

$$distributing\ b_0\ and\ combining\ the\ two\ sums\ \ldots$$

$$y = b_0 x_n + \sum_{m=1}^{M-1} \left[w_{n-m} \left(b_m - \underbrace{b_0 a_m}_{precompute} \right) \right]$$

It is worth noting that w_n refers to the n^{th} value of the intermediate variable w. This optimization simply reveals that two sets of multiply-accumulate operations here simplifies to one set of a subtract-multiply-accumulate operation if each coefficient, a_m is scaled by b_0.

Additionally, the computations performed by this system are 16 bit fixed point operations which assume Q-12 filter coefficients to speed up the computation of any DSP operations.

4.4 Command Line User Interface

A central panel was developed to easily control all of the subsystems in the project. A GUI developed in LabVIEW was contemplated due to its nice aesthetics. An interface was developed to support LabVIEW FPGA communication, which can be leveraged by the user to build a GUI.

The following LabVIEW Virtual Instrument (VI) is an example of what the final user interface was originally intended to look like providing control to all the subsystems. This VI had each subsystem placed in its own panel allowing the user to easily view all options and parameters (Figure 4.18).

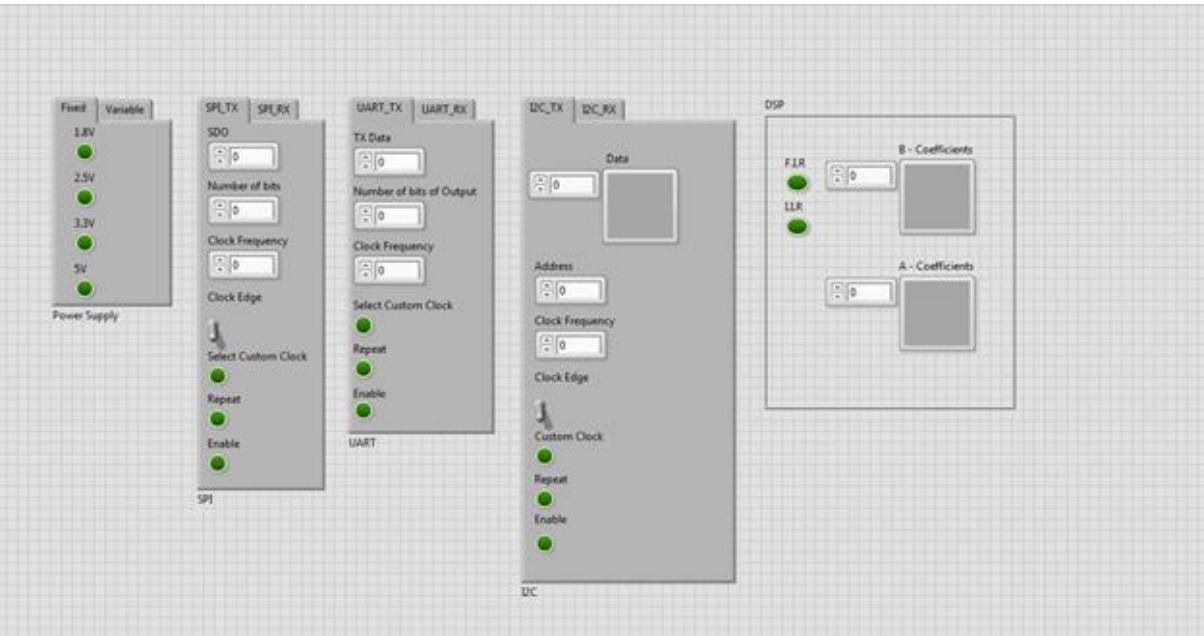

Figure 4.18 LabVIEW GUI mock up

Under development, the LabVIEW VI seen in Figure 4.19 was capable of sending and receiving data bits. It also had control of the fixed power supply and was completed with the full capability to turn on and off each linear regulator independently. The VI works by first selecting the port number to which the FPGA is connected and then the baud rate is selected. For the Kintex-7 KC705 FPGA, a baud rate of 9600 baud was chosen. Each different power rail is turned off by turning on the corresponding buttons. As described in Section 4.1.2 once a rail like the 3V3 is turned off all voltages below that are also turned off. There is also a textbox which allows the FPGA to send string characters to the user which will be used to send important test data. The LabVIEW communication was not in order when strings were being transmitted. In order to fix this issue an acknowledgement protocol utilizing ACKs and NAKs would have needed to be developed. Further development of this however, was stopped due to the simpler implementation of the command line UI in the MicroBlaze itself.

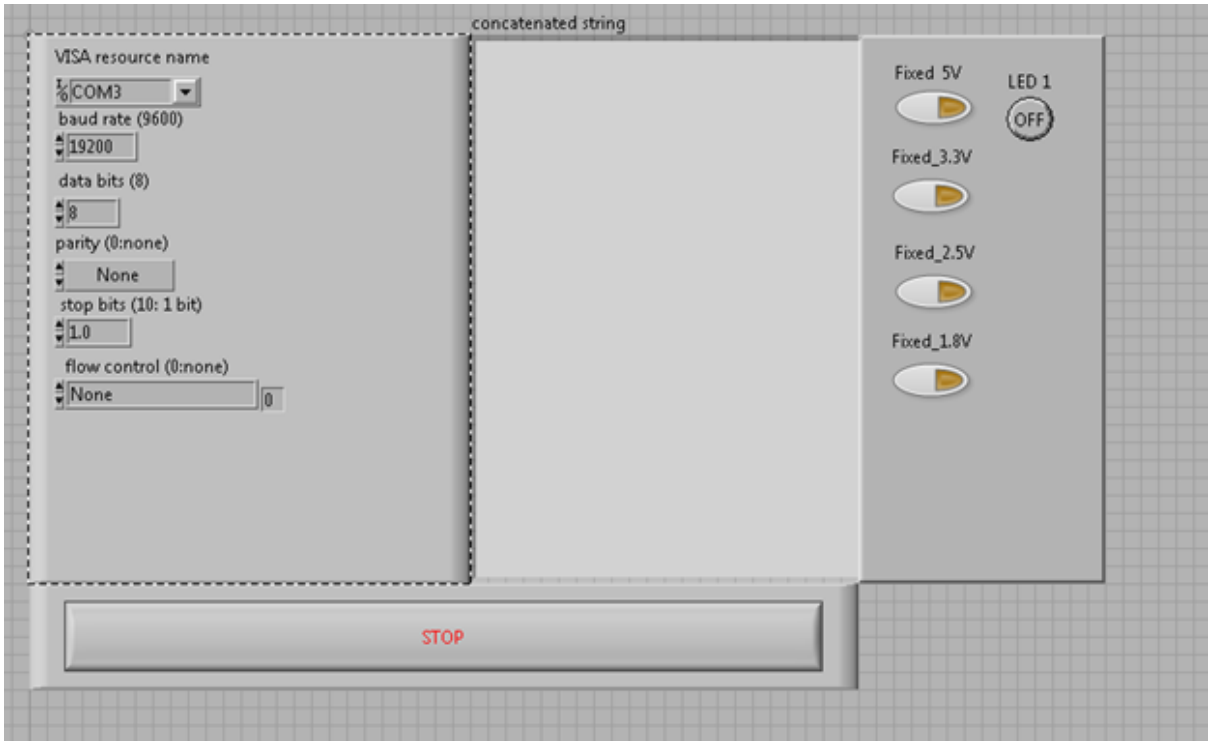

Figure 4.19 LabVIEW Fixed Power Supply Control Panel

Many engineers are familiar with a console based UI. An implementation of a menu-driven user interface enabled the user to change platform operation. The UI provides control over the subsystems including power supply and digital communications. The following image shows the main menu of the interface. From here, the user will select a sub-menu to specify system parameters (Figure 4.20).

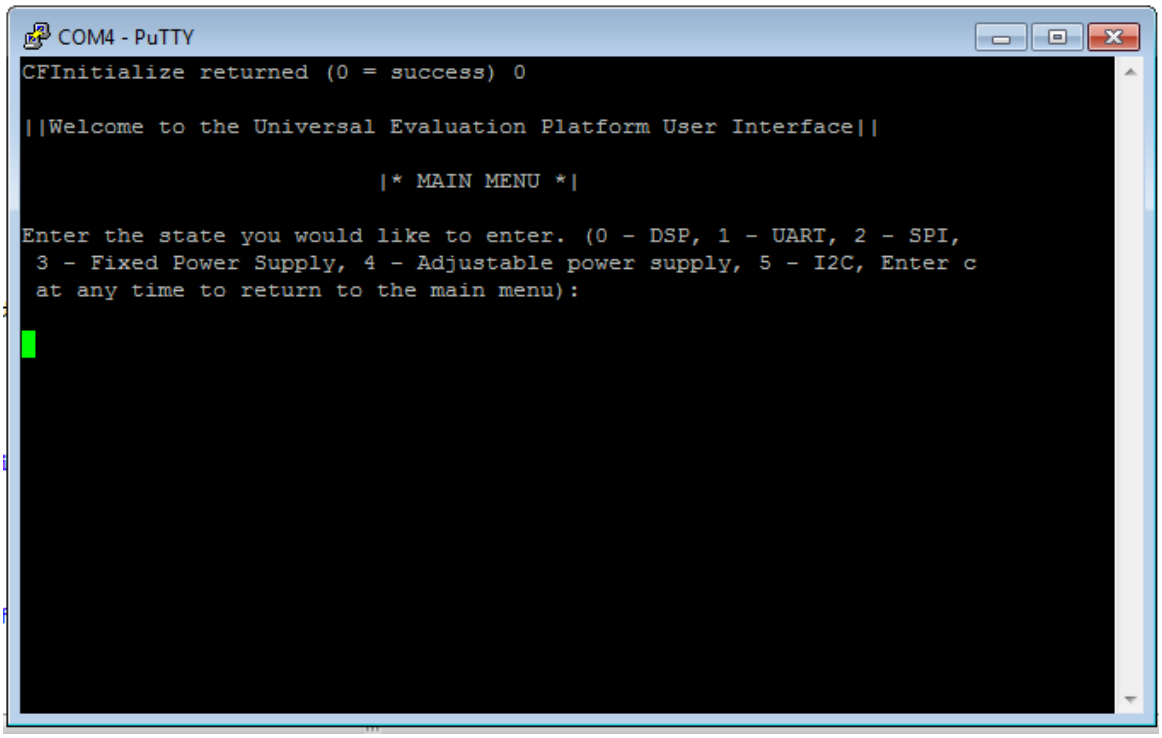

Figure 4.20 Console UI Main Menu

As an example, the process of setting parameters in the fixed power supply submenu is shown below in Figure 4.21. The user is first asked whether they would like to enable or disable one of the voltage lines. Once the user has entered an input, they are asked which voltage line they would like to toggle. At this point the user is returned to the main menu.

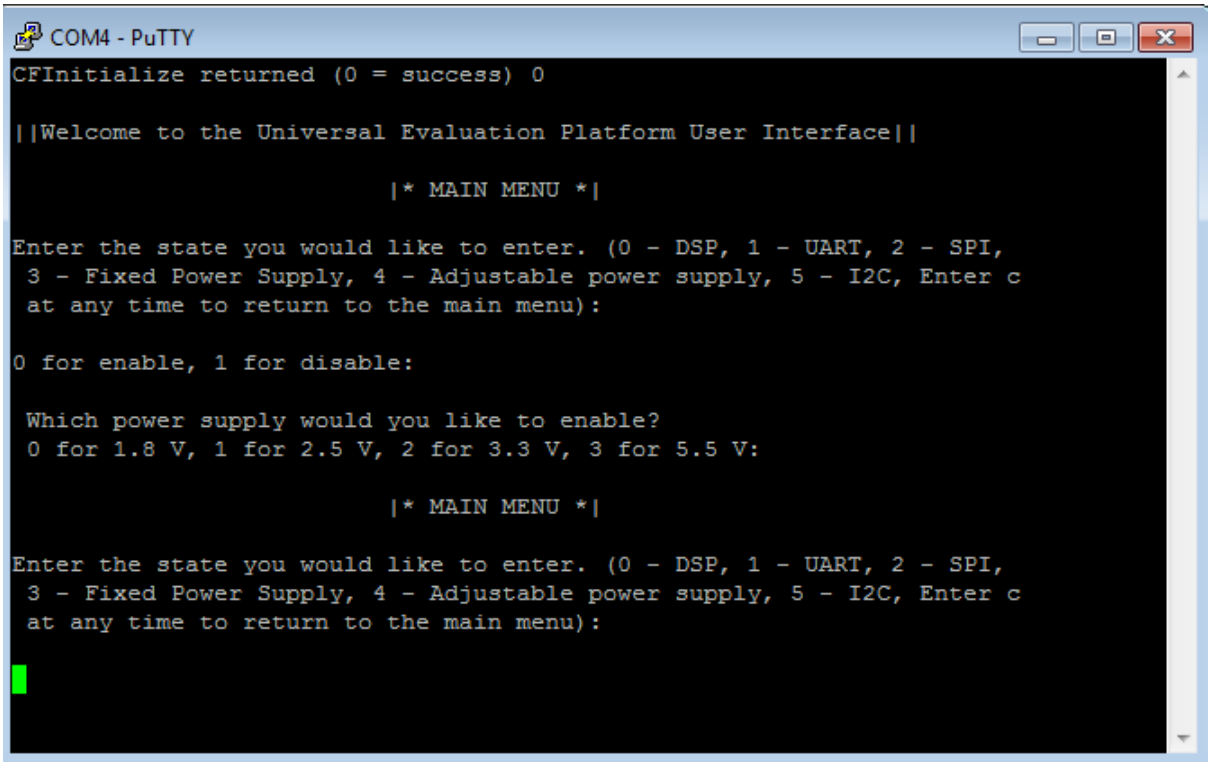

Figure 4.21 Fixed Power Supply Sub-Menu

4.5 Pattern Generation

The function generator (L2) is very useful for testing sensors and systems. A proposed pattern generator was built using a DAC paired with the FPGA. At this time, a potential DAC has been determined. The Analog Devices AD9744 [16] is a 14-bit parallel data DAC capable of sample output rates up to 210MSPS. These capabilities should meet the specifications provided fully in Appendix C, but summarized in Table 4.2.

Table 4.2 Pattern Generator Specifications, Tabulated

Parameter	**Min**	**Typical**	**Max**	**Unit**	**Comments**
Resolution		14		bits	
Supply Voltage		3.3		V	supply voltage for DAC, reference voltage based on full scale output

Sample Frequency		125		MSPS	
Signal Development					Sinusoid, triangle, sawtooth, square, modulation

Additionally, the AD9744 has high performance characteristics including spurious free dynamic range and linearity. This DAC provides parallel input which will be much more useful for high speed applications. Finally, it provides current sourced differential outputs which can be combined using an op-amp to single ended signals.

A schematic and board layout has been generated for the AD9744-based function generator. Many components have been based on suggestions from the datasheet, including several components of the layout. The schematic is presented in Figure 4.22.

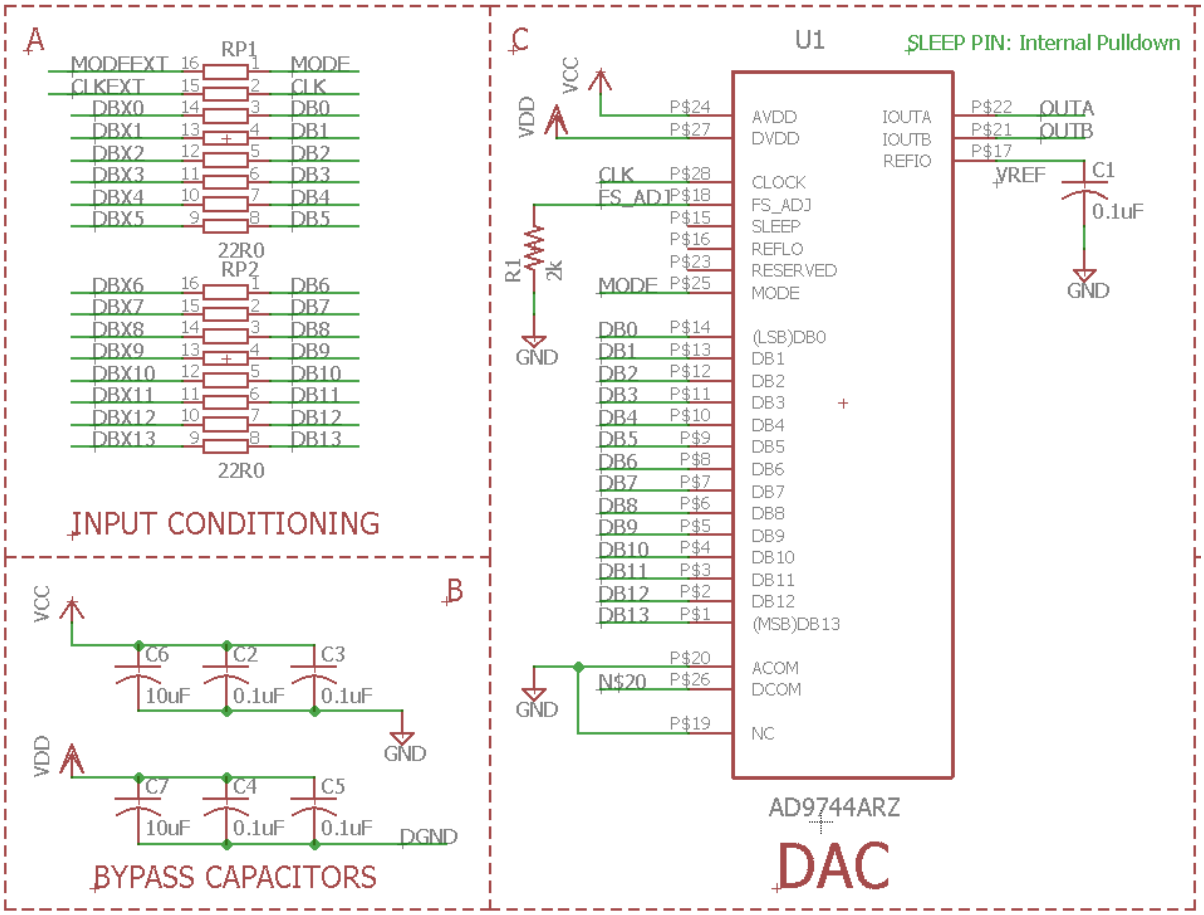

Figure 4.22 Pattern Generator Schematic

The AD9744 is presented at the center of the schematic. Its 14-bit data input along with power, ground, and reference connections are on the left side. The data pins, mode pin and clock pin pass through a 22Ω resistor network. The voltage and ground pins are decoupled through capacitive networks. Finally, the differential output is made single-ended by a subtraction amplifier with a gain of 2. This amplification is provided by the AD8041, a 170MHz capable op-amp with fast response.

The layout of the function generator also follows recommendations provided in the AD9744 datasheet, which includes a split ground plane as well as trace size matching. The clock and mode pins may have some crosstalk. The mode pin are pulled to ground most of the time, so this is less of a concern. The layout of the pattern generator is provided in Figure 4.23.

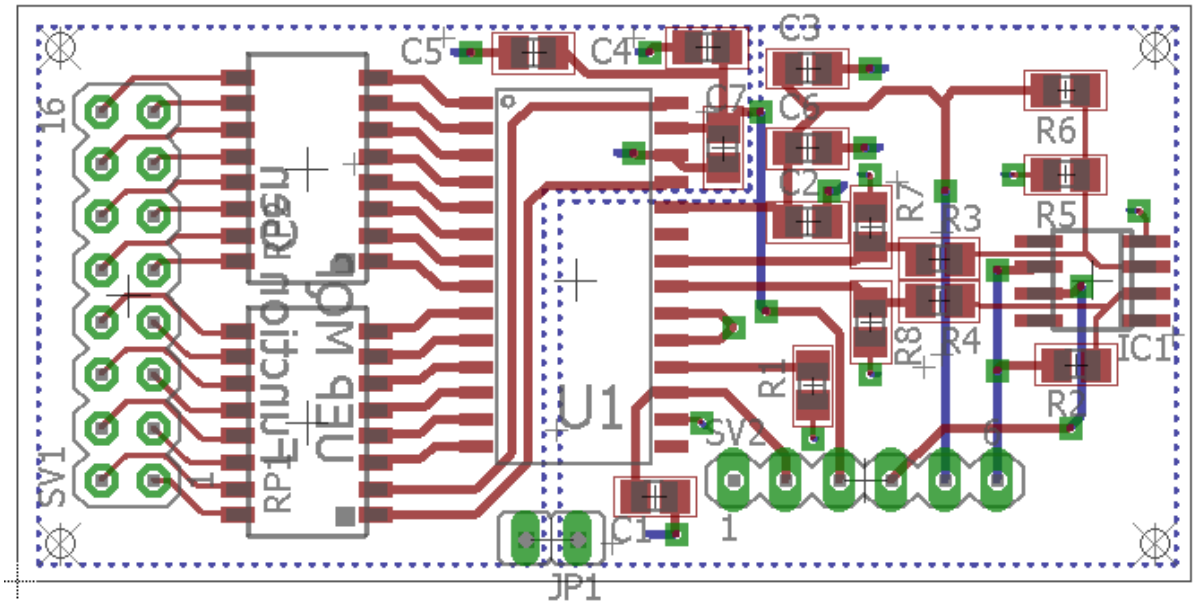

Figure 4.23 Pattern Generator Layout

Due to time limitations encountered by the team, the pattern generator subsystem was not fully realized. The power supplies required further attention than previously expected and it was preferred to effectively solve L1 subsystems versus the function generator.

5. Testing and Results

Testing has been conducted for all of the subsystems. The following section discusses the testing setups and results for each individual subsystem.

5.1 Power Supply

Significant testing was required in order to qualify the power supply boards as viable test equipment. In the original project proposal, specifications were developed for tolerances and expected performance from each of the systems. The fixed power supply was designed to output 5V, 3V3, 2V5. 1V8 and a max of 1A. The adjustable power supply was designed to have an output of 5V and 0.5A.

Both unloaded and load testing were required, and as such a constant current load device was built in order to test the power supply subsystems. The constant current load is assembled using an LM324AN op-amp, a 50kΩ potentiometer, an MTP3055 MOSFET, and 10x 10Ω power resistors. The schematic of this device matches up with a commonly available schematic. Figure 5.1 displays the schematic used for this test equipment. Figure 5.2 displays the tester assembled on a protoboard for ease of use.

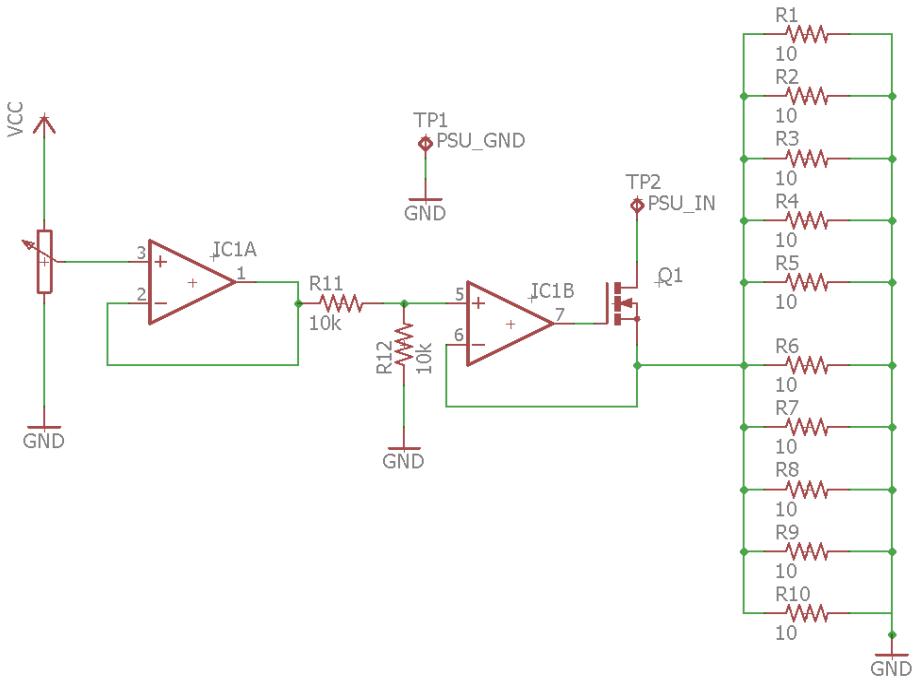

Figure 5.1 Constant Current Load Schematic

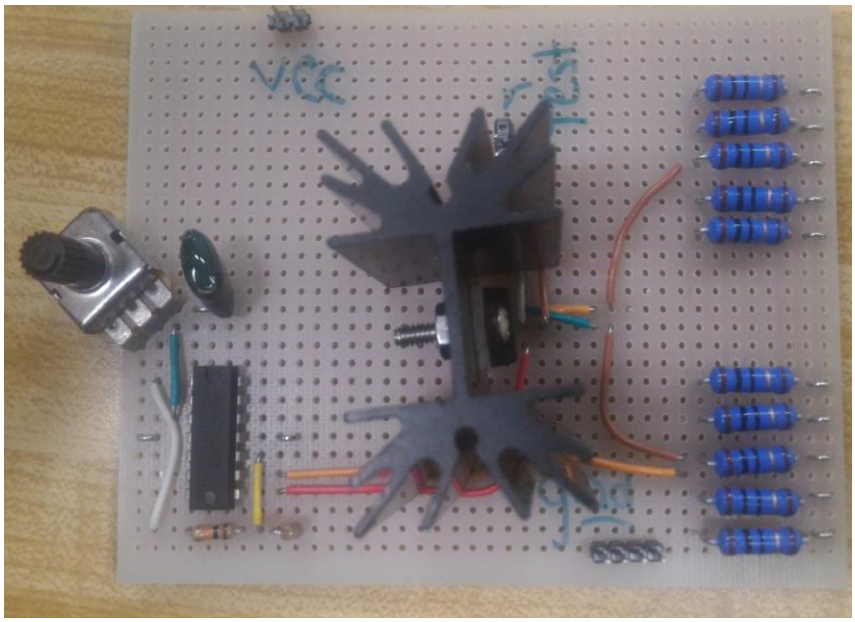

Figure 5.2 Constant Current Load Test Equipment

The constant current load provided a reliable way to test each regulator with varied load conditions. The MOSFET in the middle sinks the same amount of current through the resistors regardless of changes in voltage from the power supply test input. It was a valuable tool for characterization of the power supplies.

5.1.1 Adjustable Power Supply

Testing of the adjustable power supply had a wide range of requirements. Both current and voltage settings needed to be swept through, in order to characterize performance under load and different user settings. As discussed in the Methodology section, the adjustable power supply performs correctly under load. The adjustable power supply settings were mapped in order to find what output voltages corresponded with which input codes. These tests were conducted at a minimal but reasonable load of 5mA. Some useful values for common supply outputs are provided in Table 5.1. The entire results listing can be seen in Appendix F. A linearity plot is also provided.

Table 5.1 Useful Adjustable Power Supply Code Mapping Results (5mA load)

SPI Code	82	93	108	133	158	168	182	206	231
Output (V)	3.509	3.294	3.001	2.504	2.006	1.798	1.503	1.019	0.5076

The adjustable supply was next evaluated versus load at several common voltages obtained from the Table 5.1. The voltages included 3.3V, 2.5V, 1.8V, 1.0V, and 0.5V. Each voltage was tested with load conditions aligning with original specifications. For the adjustable supply, these conditions included 0mA, 200mA, and 500mA. The test results are provided in Table 5.2. Note that due to limitations of the MOSFET driving the constant current circuit, the 0.5V test is conducted only at 0.385A.

Table 5.2 Adjustable Power Supply Regulation Results using Lab Supply

Adjustable Power Supply Load Performance (6V Lab Supply)			
Vo = 3.3V		**SPI Code 92**	
Load Level (A)	**0**	**0.2**	**0.5**
Output Voltage (V)	3.312	3.309	3.3
Line Regulation (noise) (mV)	120	120	92

Percent Error %	0.36	0.27	0
Vo = 2.5V		**SPI Code 133**	
Load Level (A)	**0**	**0.2**	**0.5**
Output Voltage (V)	2.506	2.504	2.498
Line Regulation (noise) (mV)	132	100	100
Percent Error %	0.24	0.16	0.08
Vo = 1.8V		**SPI Code 168**	
Load Level (A)	**0**	**0.2**	**0.5**
Output Voltage (V)	1.799	1.8	1.804
Line Regulation (noise) (mV)	110	100	60
Percent Error %	0.06	0	0.22
Vo = 1.0V		**SPI Code 207**	
Load Level (A)	**0**	**0.2**	**0.5**
Output Voltage (V)	1.01	1.006	0.997
Line Regulation (noise) (mV)	110	100	96
Percent Error %	1	0.6	0.3
Vo = 500mV		**SPI Code 231**	
Load Level (A)	**0**	**0.2**	**0.385**
Output Voltage (V)	0.5133	0.5094	0.5059
Line Regulation (noise) (mV)	110	104	132
Percent Error %	2.6	1.8	1.2

No test equipment performs well only under best case conditions. A variety of test conditions were used to verify performance in worst case scenarios. The adjustable power supply was subjected to a secondary load test using a lower quality AC-DC switching converter. The results from this test are provided in Table 5.3.

Table 5.3 Adjustable Power Supply Regulation Results with AC-DC Converter

Adjustable Power Supply Load Performance (AC-DC Converter)			
Vo = 3.3V		**SPI Code 92**	
Load Level (A)	**0**	**0.2**	**0.5**
Output Voltage (V)	3.305	3.304	3.3
Line Regulation (noise) (mV)	110	114	118
Percent Error %	0.15	0.12	0
Vo = 2.5V		**SPI Code 133**	
Load Level (A)	**0**	**0.2**	**0.5**
Output Voltage (V)	2.509	2.502	2.495
Line Regulation (noise) (mV)	114	114	112
Percent Error %	0.36	0.08	0.2
Vo = 1.8V		**SPI Code 168**	
Load Level (A)	**0**	**0.2**	**0.5**
Output Voltage (V)	1.811	1.804	1.79
Line Regulation (noise) (mV)	108	104	104
Percent Error %	0.61	0.22	0.56
Vo = 1.0V		**SPI Code 207**	
Load Level (A)	**0**	**0.2**	**0.5**
Output Voltage (V)	1.005	0.998	0.982
Line Regulation (noise) (mV)	104	106	110
Percent Error %	0.5	0.2	1.8
Vo = 500mV		**SPI Code 231**	
Load Level (A)	**0**	**0.2**	**0.385**
Output Voltage (V)	0.5107	0.5024	0.4999
Line Regulation (noise) (mV)	106	100	102
Percent Error %	2.1	0.48	0.2

A final test of thermal drift performance was conducted as the adjustable power supply relies on power resistors to assist in power dissipation. Over time, these resistors heat up and their values drift. This means that the output voltage can change under high current tests. This testing was conducted under worst case current conditions for the original specifications, 0.5A. The voltage was varied and then results at time 0, 3 minutes, 5 minutes, and 10 minutes were logged. The resulting table is provided in Table 5.4.

Table 5.4 Thermal Testing Results for Adjustable Power Supply

0.5A load, Vo varied for time Adjustable Supply Thermal Test				
Vo = 3.3V				
Time (min)	0	3	5	10
Voltage	3.306	3.332	3.338	3.343
Percent Error	0.18	0.97	1.02	1.3
Vo = 2.5V				
Time (min)	0	3	5	10
Voltage	2.5	2.521	2.526	2.529
Percent Error	0	0.84	1.04	1.16
Vo = 1.8V				
Time (min)	0	3	5	10
Voltage	1.788	1.809	1.813	1.816
Percent Error	0.67	0.5	0.72	0.89
Vo = 1V				
Time (min)	0	3	5	10
Voltage	0.991	1.002	1.004	1.007
Percent Error	0.9	0.2	0.4	0.7

5.1.2 Fixed Power Supply

The initial functionality of the fixed power supply under no load was tested and verified. This included MOSFET shutdown switches controlled by the FPGA as well as regulation under no load conditions. Line regulation is confirmed in these no load conditions with all voltage regulators turned on. This verifies the performance of the design in the best case.

A variety of test conditions were used to verify performance in worst case scenarios, using equipment on hand in the lab. Initially, the power supplies are tasked with regulation from a pre-regulated source: a lab supply. Tables 5.5 and 5.6 were completed under various load conditions.

Table 5.5 Fixed Power Supply Regulation Results with Lab Supply

Regulator Performance with 6V Lab Power Supply				
Vo = 5V				
Load Level (A)	0	0.2	0.5	1
Output Voltage (V)	5.007	4.977	4.929	4.833
Output Voltage (V) (5 min)		4.974	4.920	4.845
Line Regulation (noise) (mV)	12	24	32	100
Percentage Error %	0.14	0.52	1.6	3.1
Vo = 3.3V				
Load Level (A)	0	0.2	0.5	1
Output Voltage (V)	3.305	3.270	3.214	3.120
Output Voltage (V) (5 min)		3.272	3.205	3.125
Line Regulation (noise) (mV)	12	28	68	60
Percentage Error %	0.15	0.85	2.9	5.3
Vo = 2.5V				
Load Level (A)	0	0.2	0.5	1
Output Voltage (V)	2.499	2.420	2.388	2.25
Output Voltage (V) (5 min)		2.43	2.394	2.21
Line Regulation (noise) (mV)	12	60	82	48
Percentage Error %	0.004	2.8	4.2	4.8
Vo = 1.8V				
Load Level (A)	0	0.2	0.5	1
Output Voltage (V)	1.799	1.753	1.728	1.700
Output Voltage (V) (5 min)		1.758	1.741	1.69
Line Regulation (noise) (mV)	12	80	130	100
Percentage Error %	0.005	2.33	3.3	6.1

Again, the platform should also be able to handle lower quality power inputs. Input voltage to the regulators must be kept to a minimum (even if low quality) to avoid thermal problems at high current loads. As such, the team found a 6V, 3A AC-DC converter and used it to test how transients may affect the system.

Table 5.6 Fixed Power Supply Performance with AC-DC Plug Pack

Regulator Performance with Lower Quality Supply				
Vo = 5V				
Load Level (A)	0	0.2	0.5	1
Output Voltage (V)	5.009	4.998	4.985	4.964
Output Voltage (V) (5 min)		4.999	4.985	4.977
Line Regulation (noise) (mV)	32	48	62	70
Percentage Error %	0.18	0.002	0.3	0.46
Vo = 3.3V				
Load Level (A)	0	0.2	0.5	1
Output Voltage (V)	3.307	3.295	3.283	3.260
Output Voltage (V) (5 min)		3.297	3.286	3.266
Line Regulation (noise) (mV)	28	64	144	152
Percentage Error %	0.2	0.009	0.04	1.0
Vo = 2.5V				
Load Level (A)	0	0.2	0.5	1
Output Voltage (V)	2.501	2.492	2.470	2.435
Output Voltage (V) (5 min)		2.490	2.470	2.446
Line Regulation (noise) (mV)	12	134	192	244
Percentage Error %	0.004	0.4	1.2	2.2
Vo = 1.8V				
Load Level (A)	0	0.2	0.5	1
Output Voltage (V)	1.803	1.795	1.790	1.773
Output Voltage (V) (5 min)		1.790	1.789	1.779

Line Regulation (noise) (mV)	12	56	204	208
Percentage Error %	0.17	0.55	0.61	1.2

5.2 Digital Communications

5.2.1 SPI Testing

Initial testing of the Verilog module for SPI was done using the Xilinx ISE simulation tools. The results of the simulation are shown in Figures 5.3 and 5.4. The following inputs were provided to the simulation:

- Number of bits of input: 8
- Number of bits of output: 8
- Clock speed: 100 MHz
- Value of Input: 10101011 (LSB first)
- Output to be captured: 10101011 (LSB first)
- Master: FPGA

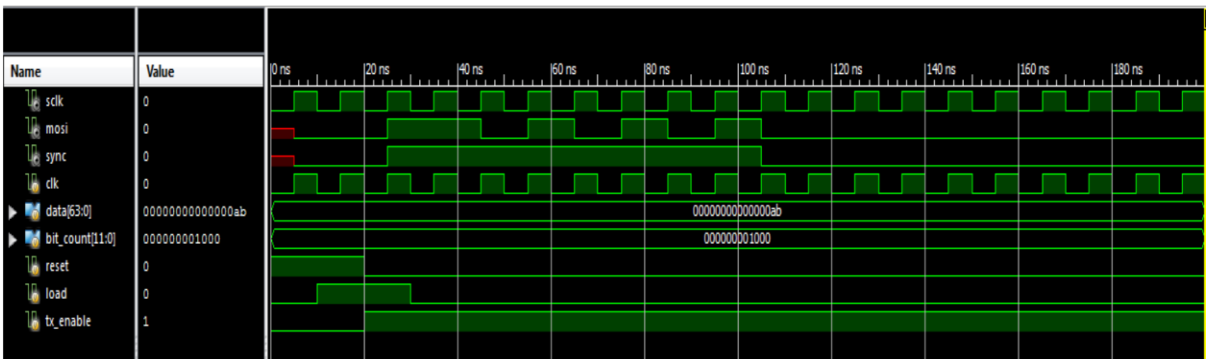

Figure 5.3 Results of SPI Transmit in simulation (Top to Bottom: Serial Clock, Master Out Slave In, Sync signal, Source Clock, Data to be sent, Number of bits, Reset, Load, Transmit Enable)

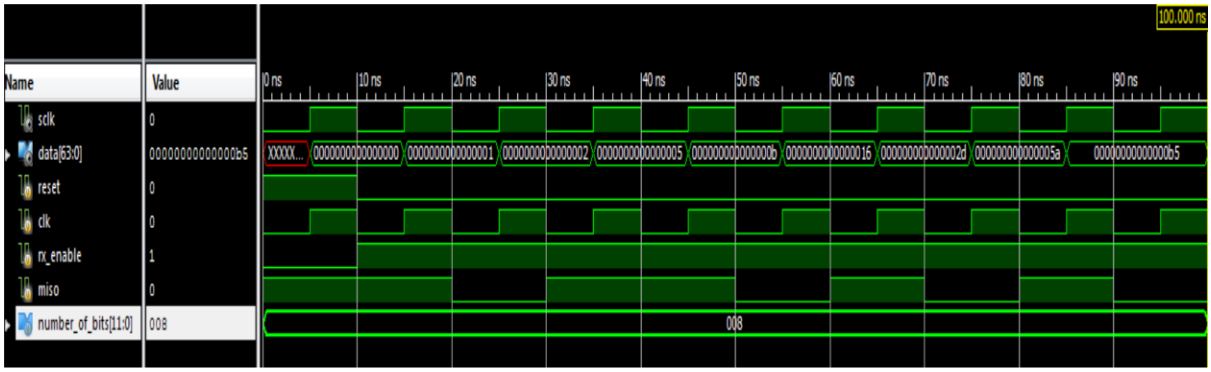

Figure 5.4 Results of SPI Receive in simulation (Top to Bottom: Serial Clock, Data Captured, Reset, Source Clock, Receive Enable, Master In Slave Out, Number of bits)

The SPI Transmit was then verified to work by sending an 8 bit pattern 10101011 to the oscilloscope, with Sync active high as shown in Figure 5.4.

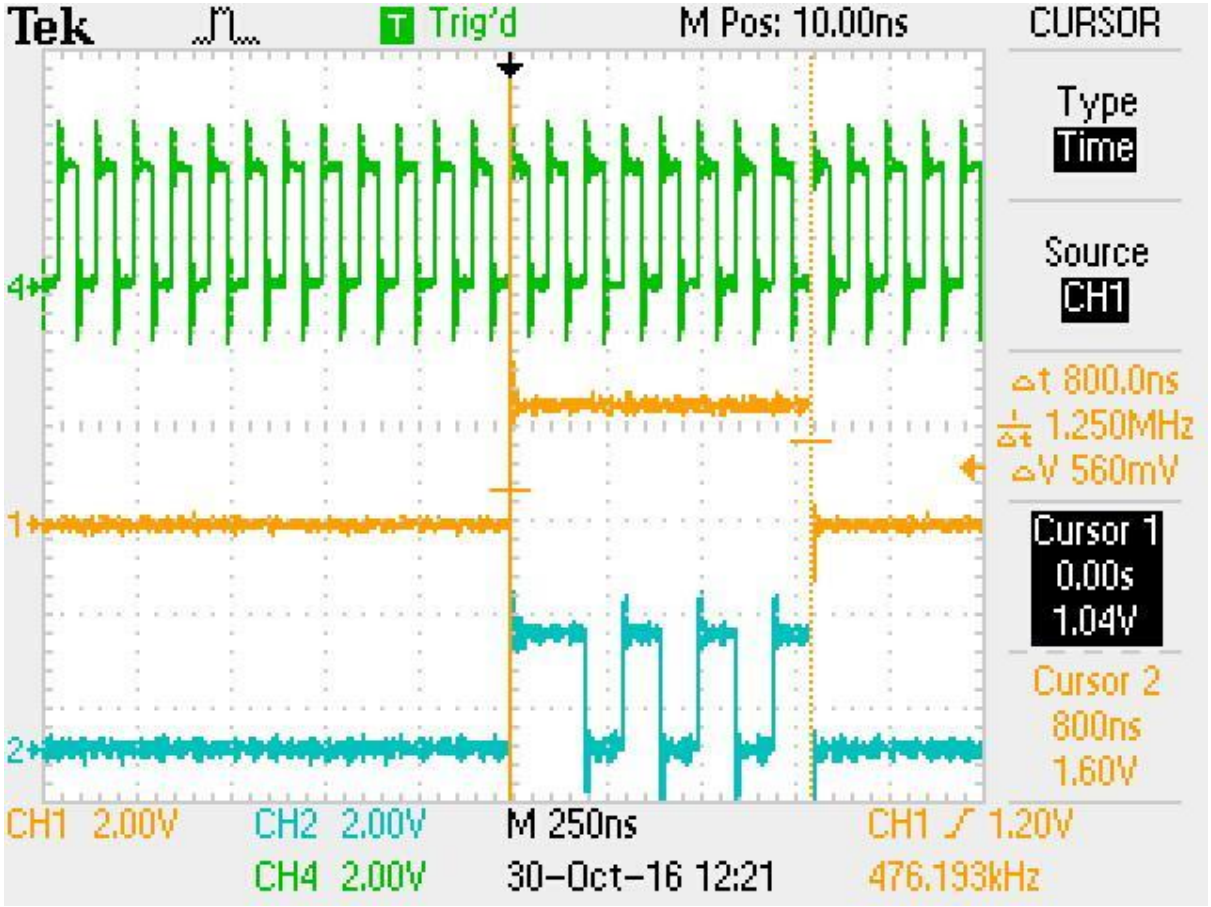

Figure 5.5 Results of SPI Transmit on Oscilloscope (Top to Bottom: Serial Clock, Chip Select (Active High), Serial Data Out)

After verifying that SPI transmit worked as expected on an oscilloscope, it was tested with a physical device. The FPGA was connected to an AD7303 [17] 8-bit SPI DAC and multiple SPI writes were conducted to produce a 16-step triangle wave. Examples of the writes are shown in Figures 5.6 and 5.7. The triangle wave is shown in Figure 5.8.

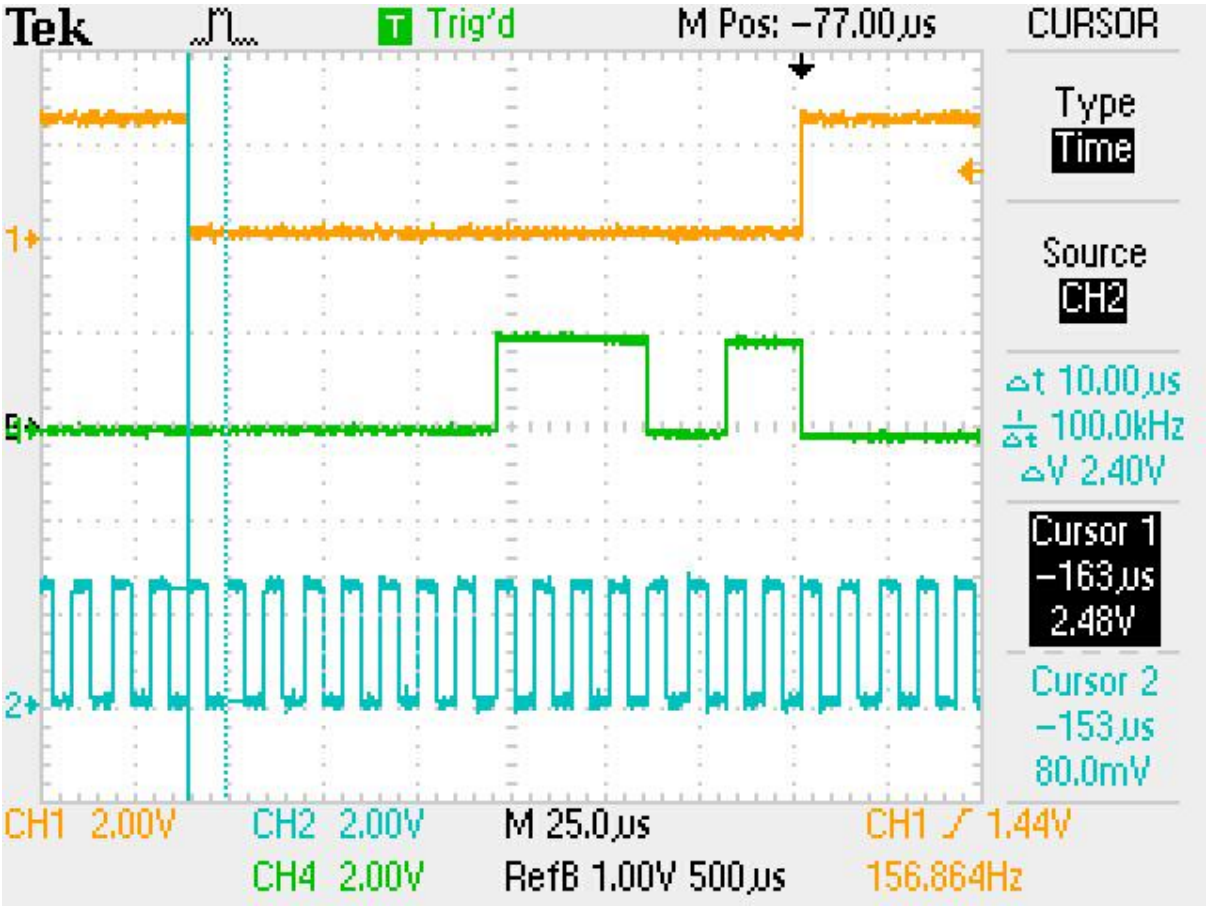

Figure 5.6 Results of SPI Write Using Spartan 6 on Oscilloscope (Top to Bottom: Chip Select (Active Low), Serial Data Out, Serial Clock)

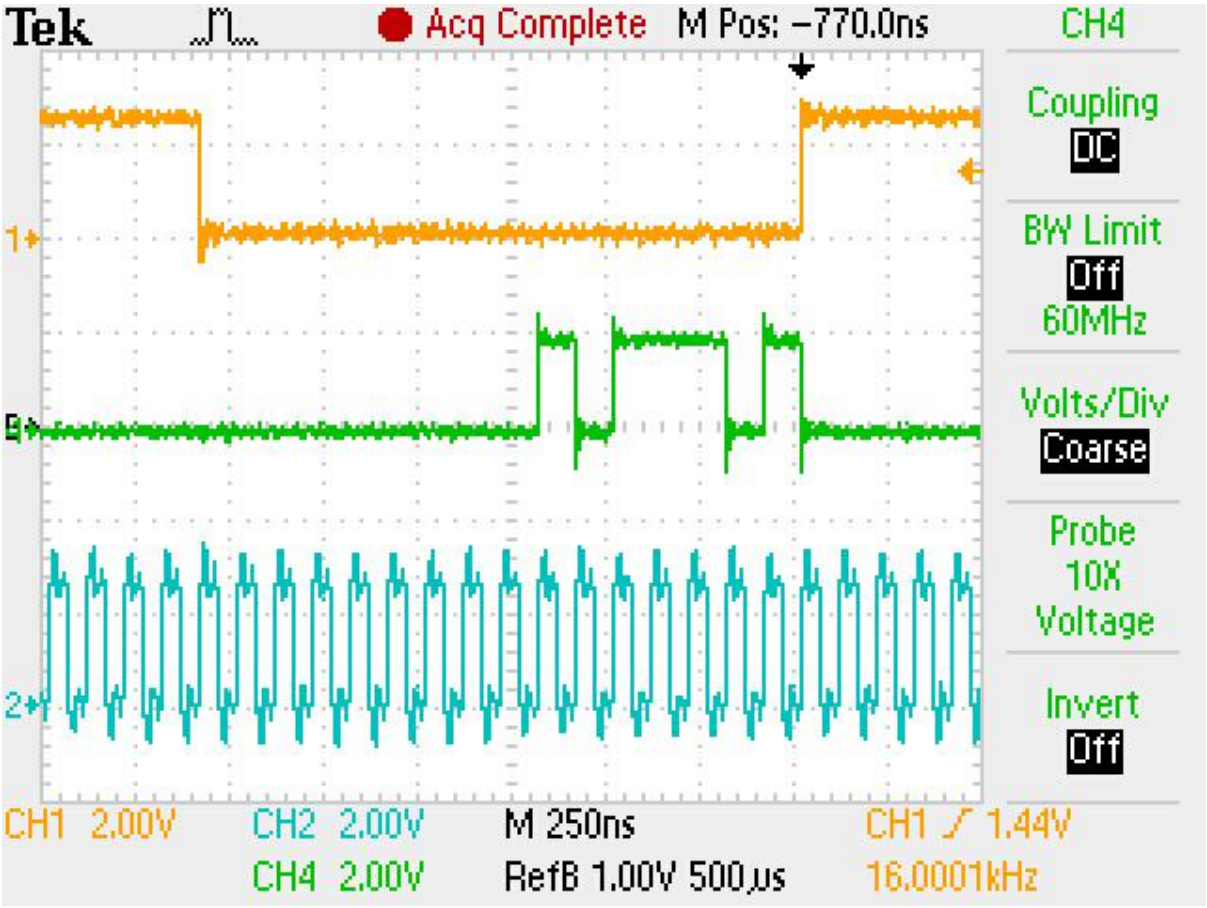

Figure 5.7 Results of SPI Write using Kintex-7 KC705 on Oscilloscope (Top to Bottom: Chip Select (Active Low), Serial Data Out, Serial Clock)

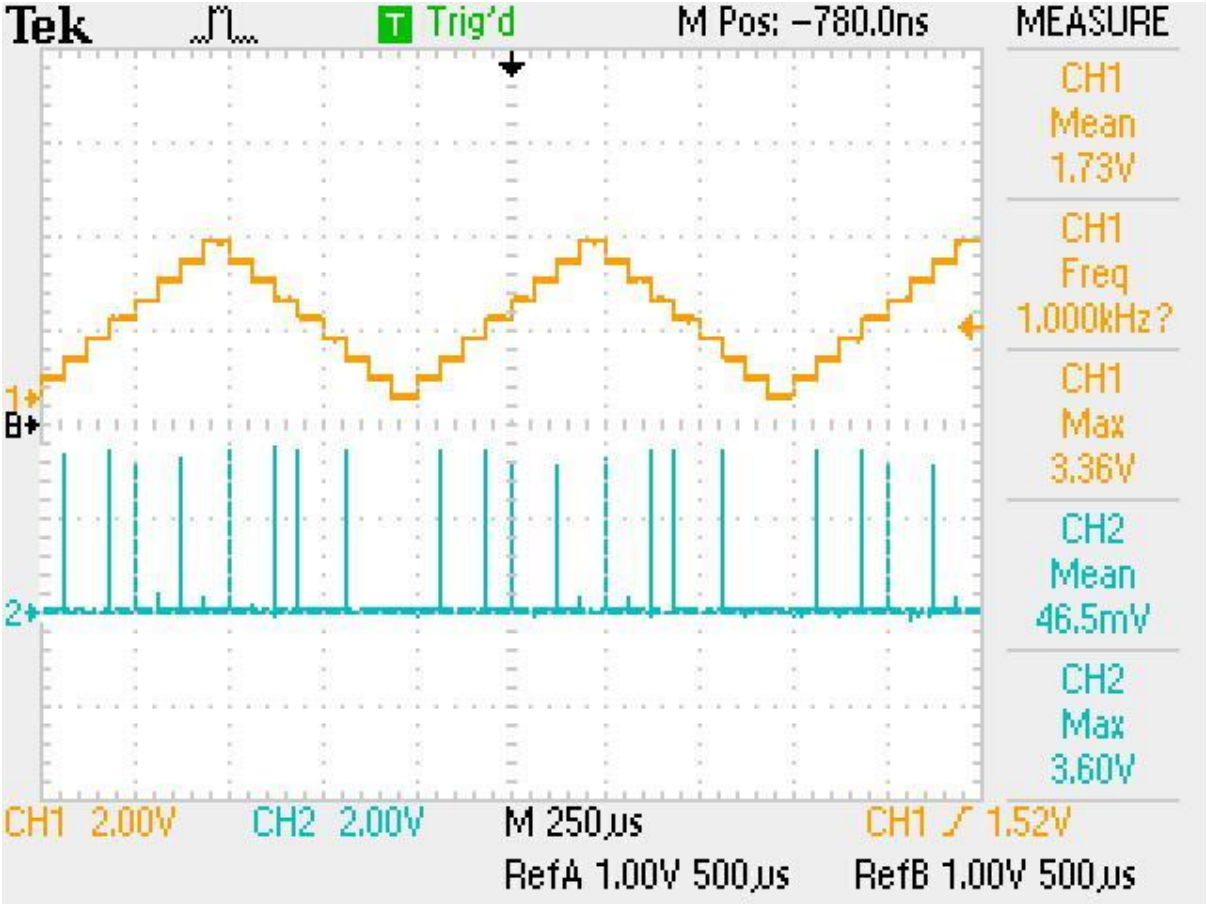

Figure 5.8 SPI Write Triangle Wave on Spartan 6 (Top Channel: DAC Output, Bottom Channel: Data Transmissions from FPGA)

The SPI Receive module was tested using an 8-bit MISO light sensor. The FPGA was the master, and the light sensor sent data to the FPGA Serial Data In (SDI) line. An oscillogram of the test results are shown in Figure 5.9.

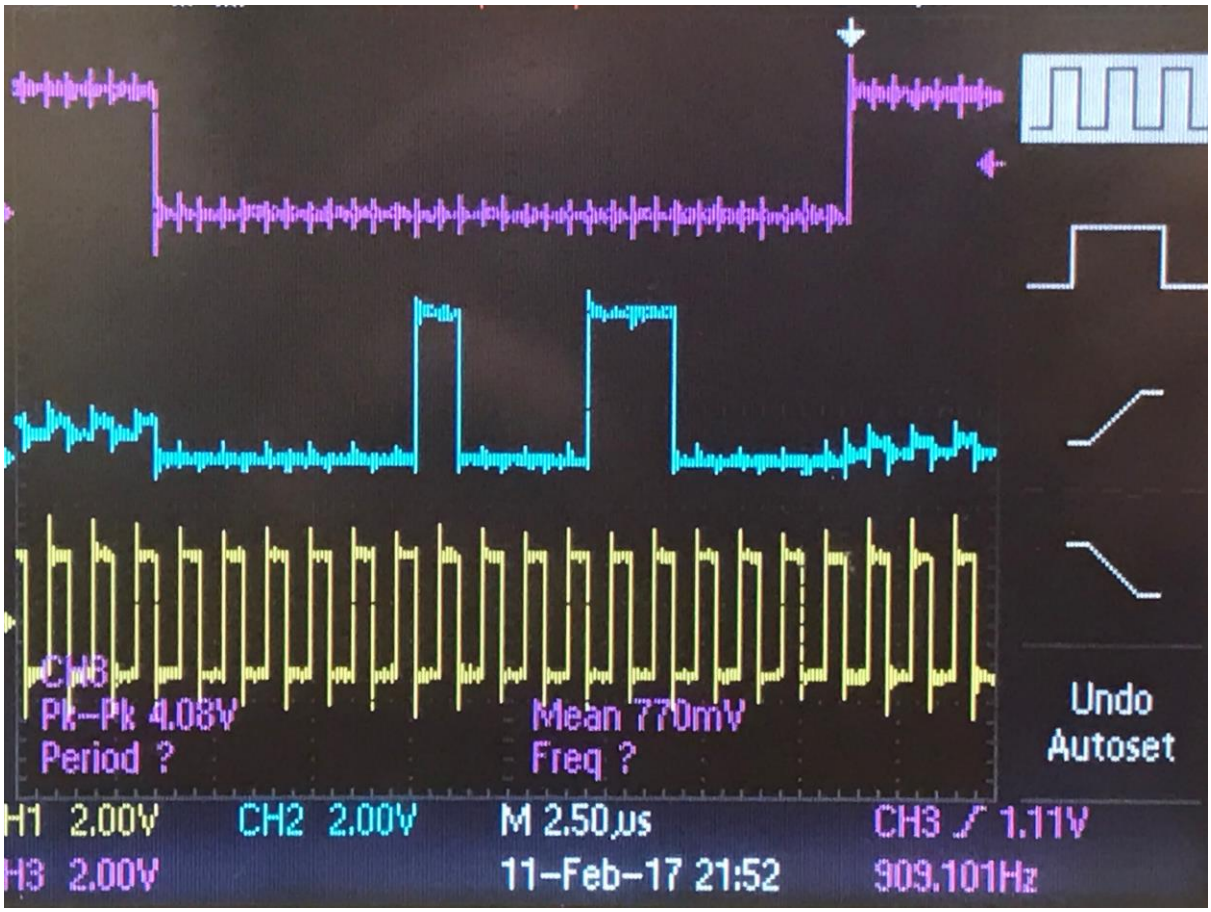

Figure 5.9 SPI Read on Scope (Top to Bottom: Chip Select (Active Low), Serial Data In, Serial Clock)

The SPI read was initially tested with ambient light, the value of the data captured was 31. When a flashlight was shined onto the sensor, the value of the data captured was 246. These results were recorded using PuTTY, and screenshots of the same are shown in Figures 5.10 and 5.11 for ambient light and flashlight respectively. This test helped verify the behavior of SPI read. The SPI transmit module has been tested to work up to 10 MHz frequency of the Serial Clock (SCLK), and the SPI receive module has been tested to work up to a 1 MHz SCLK. The limiting factors were the specifications of the DAC and the light sensor used to test these modules.

```
0 for send, 1 for receive:

 How many bytes will be received:

Do you want to receive on the positive edge or negative
                                                        edge of the clock ( 0 -
 negative edge, 1 - positive edge):

Would you like to sync low or high (0 - low, 1 - high):

Data received was 31

Data received was 31
```

Figure 5.10 SPI Read with ambient light on Light Sensor

```
0 for send, 1 for receive:

 How many bytes will be received:

Do you want to receive on the positive edge or negative
                                                        edge of the clock ( 0 -
 negative edge, 1 - positive edge):

Would you like to sync low or high (0 - low, 1 - high):

Data received was 246

Data received was 246
```

Figure 5.11 SPI Read with torch flashed on Light Sensor

5.2.2 UART

The UART module [11] was created using MicroBlaze. The MicroBlaze supports UART transmit and receive capabilities. The baud rate can be modified through the MicroBlaze wizard. By default, these UART pins are connected to USB_TX and USB_RX. For initial testing, the Transmit was connected to an FMC pin, and the output was observed on an oscilloscope. A data write was performed with the value 10101011 in binary. The

oscillogram of this test can be observed in Figure 5.12.

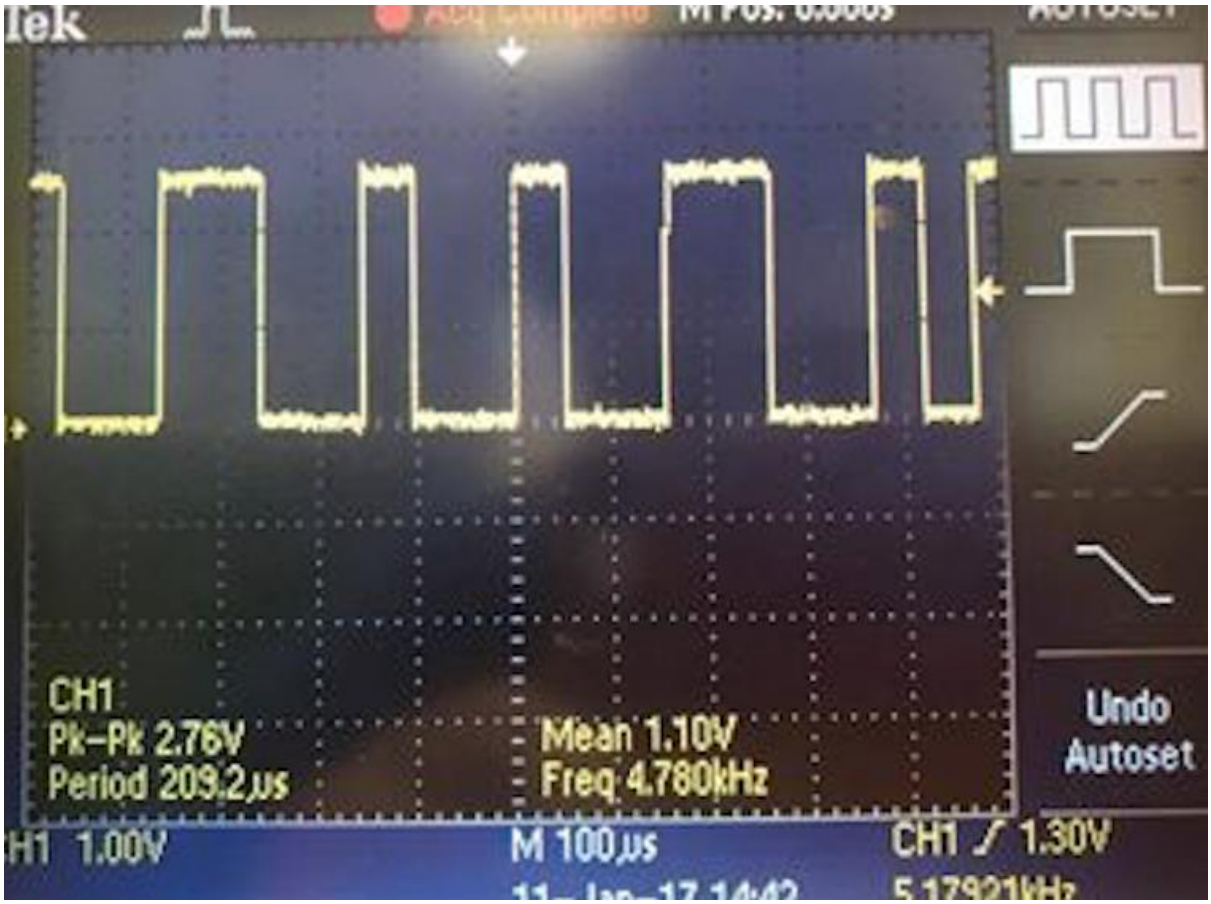

Figure 5.12 Oscillogram of UART Transmit

The UART module was further tested using serial read and writes performed through PuTTY. An example of the serial write is seen in Figure 5.13.

```
What byte would you like to send?

a was the byte sent
```

Figure 5.13 UART Transmit test using PuTTY

The character entered through PuTTY was written using UART transmit. For UART read, a character entered through PuTTY was captured using receive and displayed on the UI. The result of this test is shown in Figure 5.14.

```
Press 0 for send, 1 for receive:

The byte received was a
```

Figure 5.14 UART Receive test using PuTTY

5.2.3 I2C Testing

Initial testing for I2C was performed using Xilinx ISE design suite simulation tools. The test conditions were as follows:

- Command 1:
    - addr = 1010101
    - rw = 1
    - data_wr = 01011001
- Command 2 (to demonstrate repeated start by changing to a read command):
    - addr = 1010101
    - rw = 0
    - data_wr = 01011001 (not relevant in this command)
    - data_rd = 11001100

While the simulation was mostly correct, the only fault was the lack of de-assertion of the enable (ena) signal, therefore the transaction would not end and continued to re-perform the "read" command since i2c_master.vhd would not send the master NACK bit.

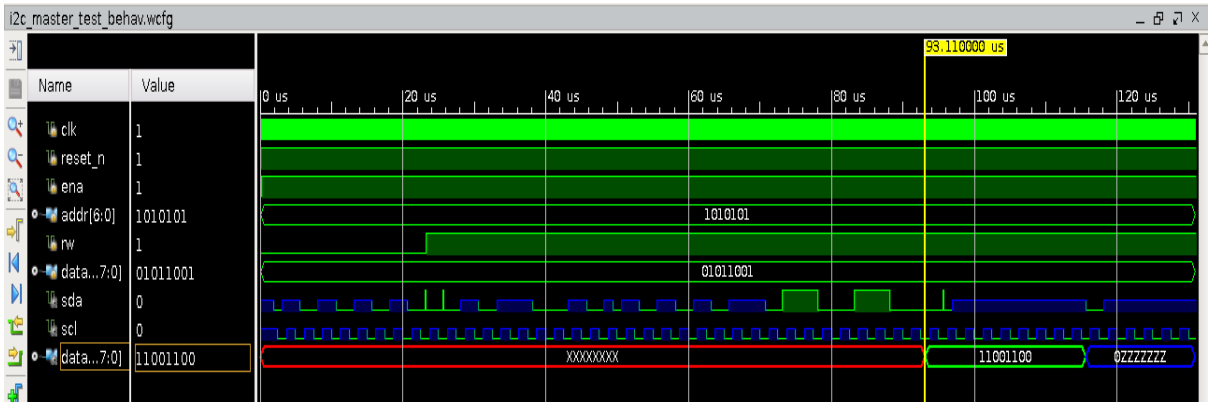

Figure 5.15 Simulation of i2c_master.vhd Demonstrating its Full Capabilities (Top to Bottom: Source Clock, Reset, Enable, Read/Write bit, Data, SDA, SCL, Data read)

Following simulation, tests were performed with a Raspberry Pi and a Sunfounder PCF8591 AD/DA I2C device with an on board potentiometer connected to input channel 1 of the device. Figure 5.16 shows the oscillogram of the transaction.

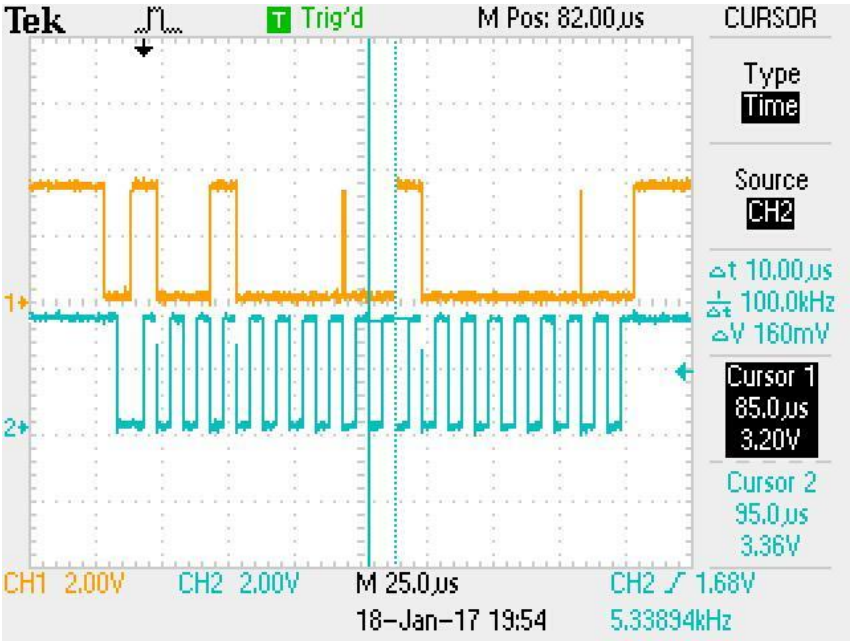

Figure 5.16 Raspberry Pi I2C Transaction with PCF8591 (Top: SDA, Bottom: SCL)

Here it is seen that the device address (in binary) is 100 1000 followed by a rw bit of 0, indicating a read command. The device then transmits a converted potentiometer value of 0100 0000 followed by an ACK bit and an end bit.

This was used as a performance benchmark to which the performance of the FPGA I2C implementation would be compared. The test was performed by reading converted potentiometer values from the device and then immediately transmitting them back to the device to be converted back to analog outputs. The results of the test are shown from Figure 5.17 to 5.19:

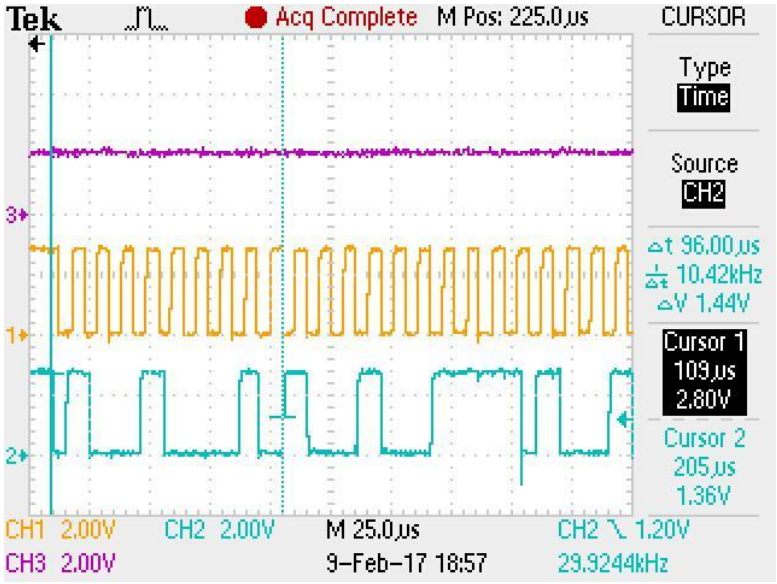

Figure 5.17 Addressing PCF8591 and Reading ADC value followed by Repeated Start (Top: DAC Output, Middle: SCL, Bottom: SDA)

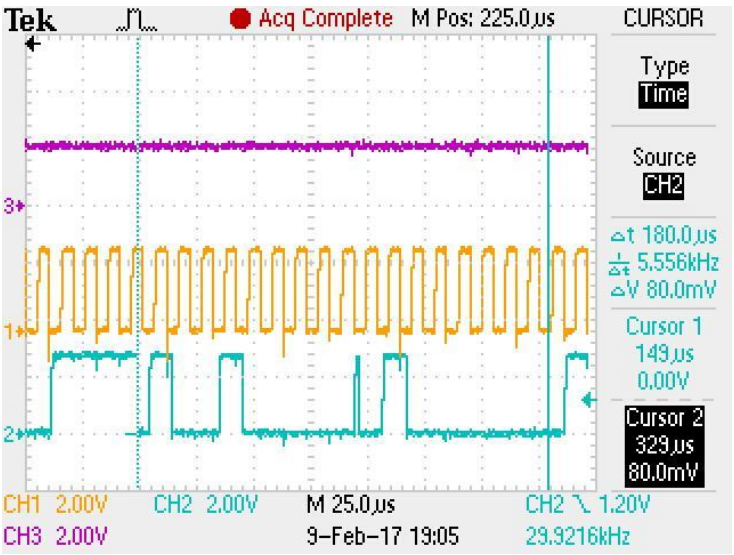

Figure 5.18 Repeated Start followed by Address again and Control Byte (Top: DAC Output, Middle: SCL, Bottom: SDA)

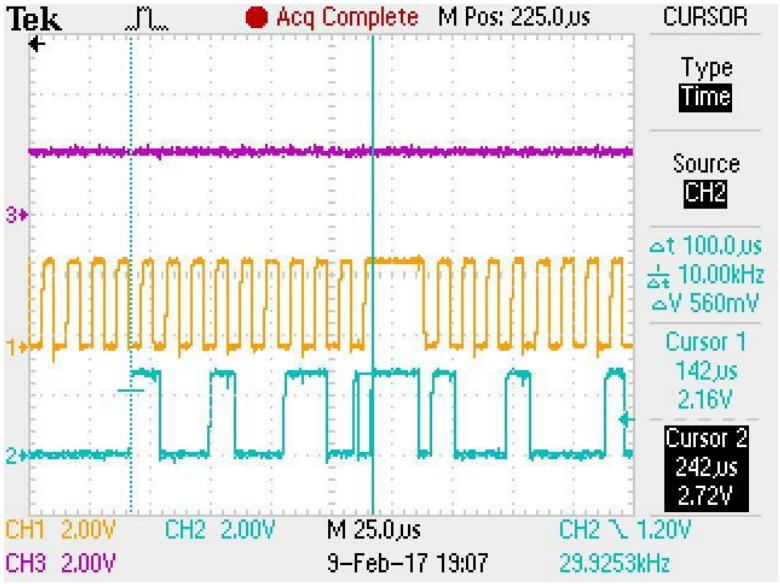

Figure 5.19 : Data Write followed by End Bit then looping back to start the whole Transaction again (Top: DAC Output, Middle: SCL, Bottom: SDA)

First in Figure 5.17, the device is addressed and read from. Then in Figure 5.18, a repeated start is used to change to a write command and the device is addressed again and sent a control byte to instruct the DAC to output on channel 0. Finally in Figure 5.19, the data that was read before is written back to the AD/DA device and the end bit is sent, thus ending the transaction. This transaction is continually repeated so that the potentiometer can be rotated and channel 3 on the oscillogram shows the analog output of the DAC.

5.3 Digital Signal Processing

The testing of Digital Signal Processing was conducted using mathematical modelling. Testing of the DSP subsystem was performed by creating two three-element arrays of Q-12 filter coefficients (A and B coefficients), nominally 4096, 8192, and 12288 (1.0, 2.0, and 3.0 in floating point) for both arrays then passing a Q-15 input 32768 (1.0 in floating point) as input into the IIR filtering function. This was done three times so that we could easily compute the expected three outputs by hand.

The function outputs three Q-15 32768s (1.0 in floating point) as expected, confirming the functionality of the filtering functions. This was then extended so that a user may provide a header file of a particular format to specify filter coefficients.

6. Recommendations and Future Work

The majority of the critical and stretch goals were achieved. As expected, the advanced reach goals could not be implemented due to time constraints. These reach goals have been discussed in the subsystem section of the report. The future work section will mainly focus on the possible improvements to the currently implemented subsections of the project.

6.1 Power Supplies

The fixed and adjustable power supply systems could be improved by increasing regulator output capability and stability. In current implementations, the power supplies have 1A and 0.5A output capabilities each. This may be improved to compare with bench power supplies more closely. However, the overall results are quite sufficient for testing of gate-based devices like digital systems. The fixed power supplies provide common CMOS voltages, where the adjustable power supply can sweep the common voltage range from 0V to 4V.

The power supplies were implemented with a minimalist approach. For the design, some assumptions had to be made. One of the assumptions made was overall input supply stability. The current supply boards accept an input of 6V, at 3A current. Nominally, the input supply should lack ripple, transient spikes, and other power quality issues, but this is not always the case. Some improvements to the supply filtering could be made to make the power supply subsystem more robust under transient conditions. In its current state, the adjustable power supply can accept transients up to 23V. The fixed power supplies can only accept up to 7.5V, so those are good candidates for further input safety and regulation.

Output safety features of the power supply were built in, including thermal shutdown and current limit protection from the regulators. However, further capacitance and filtering can be built in to minimize output ripple under poor input conditions. The adjustable supply thermal drift should be minimized.

6.2 Digital Communication Protocols

The Serial Peripheral Interface (SPI) is loosely defined, hence there is room for additional support features. The most significant one would be to allow a fixed number of continuous writes with configurable data. The FMC bank supports a fixed IOSTANDARD of LVCMOS25. Currently it is recommended to use logic level converters to support other standards. However, for a neater implementation, a TI PMBus controller could be used to change the reference voltage of the FMC bank programmatically.

The UART was implemented by leveraging the MicroBlaze. Implementing a UART module in Verilog would be encouraged, as it would decrease reliance on Xilinx tools and changing the UART settings such as baud rate would be achievable through the user interface, instead of the Xilinx MicroBlaze setup wizard.

The I2C subsystem was built upon the open source VHDL firmware: i2c_master.vhd module which currently only supports the 7-bit addressing mode of the I2C standard. Additionally, the Verilog control logic currently requires the user to specify three commands: each consisting of a 7 bit address, a read/write bit, and 8 bit data to write to the slave. Any data read from the slave device will be loaded into a single data bus - overwriting old read data. The control logic then ends the transaction and loops back to repeat this process ad infinitum until new commands are specified by the user. Therefore, the control logic should be modified so that the user can specify whether it should repeatedly send the same commands and the number of commands. The data read should also be stored before being

overwritten with new data. Additionally, multiple I2C speed modes may be provided by instantiating i2c_master.vhd with different SCLK parameters. A final change option is to modify the VHDL code of i2c_master.vhd to support 10 bit addressing of slave devices.

6.3 Digital Signal Processing

The DSP subsystem will need to have timer interrupts implemented so that proper sampling rates may be specified and processing will occur in an interrupt service routine. Additionally, an audio codec may be a useful component for DSP testing.

6.4 User Interface

The command line user interface has the capability to control all subsystem parameters. However, it is very simple and visually basic. The user interface does not always display the inputs that the user submitted, requiring the user to remember their parameters. One way to improve the system is to continually show or have a menu option that pulls up all the parameters that have been set. More future work that can be done on the user interface is with the implementation of LabVIEW. LabVIEW a very popular software for making graphical user interfaces was used to make a preliminary central panel to control the subsystems. The issue of sending and receiving data in correct order arose when the team was in the process of developing the LabVIEW user interface. In future work this can be resolved by implementing an acknowledgement system using NAKs and ACKs commonly utilized in data networks.

6.5 Function Generator

Time constraints in the project prohibited the completion of the function generator subsystem. The schematic and layout are complete. In order to move forward with this

portion of the project, Verilog listings for data generation must be completed. Additionally, the board for the function generator must be assembled. From this point, however, the function generator should be ready for testing through different clock speeds, functions, and magnitudes.

7. Conclusion

The Universal Evaluation platform is a tool for engineers which will simplify the validation and testing process. Features included fixed and adjustable power supply, common serial communications protocols, digital signal processing and a user interface. These features were based on research conducted on industry needs. The design and testing of these features was conducted by the MQP team over the period of A, B, and C terms 2016-2017.

The fixed power supply subsystem excelled when tested under both unloaded and loaded conditions. It fulfilled original expectations including 1A current availability, ±100mV load regulation, and safe thermal performance. Although it is not directly comparable to existing lab products for voltage testing, it provides useful performance for IC testing, particularly digital or mixed signal ICs.

The adjustable power supply subsystem also performed well under loaded conditions. The regulator is capable of up to 3A current availability, and the original 0.5A expectation was easily met. Safe thermal performance was met despite a maximum of 2.5W power dissipation. Again, this subsystem does not necessarily compare to existing lab products, but it can be highly useful for IC testing including corner cases for voltage inputs. In essence, the adjustable power supply provides a small footprint device for IC power testing.

The digital communication protocols were initially tested with simulations. The output of the communication modules were then verified on an oscilloscope. Finally physical devices were verified to work as expected after being controlled through the SPI, I2C, and UART modules. A majority of the proposed features were achieved. For SPI, transactions up to 32 bits were supported, and SPI read and write were tested for frequencies up to 1 MHz and 10 MHz respectively with a physical device. UART was built by leveraging MicroBlaze, and settings can be modified through the Xilinx MicroBlaze setup wizard. By default, 8 bit read and writes are offered at 9600 baud. I2C was tested using three commands or bytes of

data to read or write at the standard speed mode of 100 kbits/sec. Testing for higher speed modes could not be performed due to limitations on the I2C device being used to perform the tests.

The digital signal processing subsystem was tested using a straightforward mathematical check with a third order filter, and three inputs. The results were verified using mathematical modeling. Since polling was used instead of configuring timer interrupts on the MicroBlaze, no useful sampling frequency data could be obtained.

The Universal Evaluation Platform is a unique product that can improve the testing and debugging process in a revolutionary way before datasheets have been created. With the Universal Evaluation Platform, engineering time, lab space, lab equipment, and money can all be saved. A plethora of subsystems make the Universal Evaluation Platform a great product for evaluation of a wide variety of devices.

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Appendix A: Power Supply Fact Sheet

Parameter	Min	Typical	Max	Unit	Comments
Input Voltage		6	8	V	PSU input
Input Current		3		A	Up to
Current Availability		3		A	across all channels
Fixed Supplies Constant Voltage (CV) and Constant Current (CC)					
1.8V Tolerance		±50		mV	
2.5V Tolerance		±50		mV	
3.3V Tolerance		±100		mV	
5V Tolerance		±100		mV	
Current Availability		1		A	per channel
Regulation Type		Linear			Linear regulation for fixed supplies
Adjustable Supplies					
Output Tolerance		2		%	of output target voltage (or 20mV)
Regulation Type		Linear			Stability and simplicity maximized
Current Source Capability		500		mA	
Control Method		Resistive Divider			10MHz SPI Maximum Control
Power Supply Control Schema					
Fixed Supply Control					Toggled via transistor switches, controlled via SPI. Transistors will pull regulator inputs high.
Variable Supply Control					Resistive Divider has RDAC component, controlled via SPI. Fixed supply and adjustable supply may be turned on at the same time.

Appendix B: Flexible Digital Communication

Parameter	Min	Typical	Max	Unit	Comments
SDI Number of Bits in SPI	1	8	32	bits	The number of bits received by the SPI module
SDO Number of Bits in SPI	1	8	32	bits	The number of bits transmitted by the SPI module
Frequency of SCLK in SPI			100	MHz	The SCLK can operate on frequencies up to 500 MHz
TX/RX Number of Bits in UART		8		bits	The number of bits received by the UART module
Frequency of TX/RX in UART			57600	baud	The UART can operate on frequencies up to 57600 baud
I2C Number of Bytes	1	8	32	bytes	
I2C Speed Modes			3	MHz	All Speed modes up to 3 MHz are offered
Clock edge for transmit/receive in all Protocols					Configurable

Appendix C: Pattern Generation Fact Sheet

Parameter	Min	Typical	Max	Unit	Comments
Resolution		14		bits	
Supply Voltage		3.3		V	supply voltage for DAC, reference voltage based on full scale output
Current Output		10		mA	Drive strength of AD9744
Sample Frequency		125		MSPS	
Output Channels		2		#	
Signal Frequency	DC		25	MHz	
Signal Development					**Sinusoid, triangle, sawtooth, square, modulation (?)**
Current, Voltage Amplification					**Capable, adjustable**
Parameter	**Min**	**Typical**	**Max**	**Unit**	**Comments**
Resolution		14		bits	
Supply Voltage		3.3		V	supply voltage for DAC, reference voltage based on full scale output

Appendix D: Digital Signal Processing Fact Sheet

Parameter	Min	Typical	Max	Unit	Comments
Max Sampling Frequency			100	kHz	
Max Filter Order			64	#	
Supported Filters					FIR and IIR

Appendix E: Survey Results

Default Report MQP Survey November 21st 2016, 8:32 am MST

Q1 - What is your profession?

Engineer

Manufacturing Product Engineer

Electrical Engineer

Electrical Engineer

Electrical Engineer - System Integration & Test

Engineer

EE/Draper

Spartan (AKA embedded software engineer)

Q2 - What is the cost associated with your current evaluation platform (lab bench equipment, software)?

.dollars

$5000

>$50k

100000+

200,000

Just a computer. About 1000 I am guessing. Most software I use is free, like PuTTY.

Q3- Rate each feature

Important Moderately important Not important Total

Configurable real time digital filters 0.00% 0 87.50% 7 12.50% 1 8 Digital communication interfaces with DUT (SPI, UART, I2C)

75.00% 6 12.50% 1 12.50% 1 8

Configurable power supply settings (voltage, current sources)

100.00% 8 0.00% 0 0.00% 0 8

Simple function generator capability 50.00% 4 50.00% 4 0.00% 0 8 Labview user interface with test summary report

62.50% 5 25.00% 2 12.50% 1 8

LVDS amplifier 12.50% 1 62.50% 5 25.00% 2 8 Artificial intelligence for testing suggestions

12.50% 1 25.00% 2 62.50% 5 8

Q4 - How important would you rate the following features in a real time digital filtering system for a product evaluation platform?

Field Minimum Maximum Mean Std Deviation Variance Count

Configurable filter order and type 0.00 9.00 4.26 2.85 8.11 8

Anti-aliasing filtering 0.00 10.00 6.50 3.61 13.01 8

Adaptive Filtering options 0.00 10.00 6.60 3.12 9.72 8

Q6 - Beyond SPI, UART, I2C are there any other communication protocols you regularly use with DUTs?

Yes, custom product specific digital serial or parallel interface ports.

NA For ICs, those interfaces are probably fine. If you work with higher-level systems, consider RS232, RS422, and Ethernet Mostly uart, rs-232, rs-485

I2C seems most important to me. UART and serial things are good.

Q5 - Describe your desired power supply precision characteristics (voltage, current, load tolerance i.e. within 100mV of given voltage)?

Within 10mV

;alkdjf;djf

100mV

0-30VDC, 2A max, programmable by 10mV is usually fine

3.3, 2.5, 1.2

+-10mv, mostly care about dc ripple

For my kind of embedded design, 100mV would be the most precision needed.

Q6 - What do you consider the minimum specifications for a useful function generator?

N/A

Should be able to run at least 20MHz and 0 to 10 volts Frequency capability is important -- if RF ICs, make sure can handle those higher frequencies. If not RF ICs, upper limit can be lesser for cost savings fully configurable waveform, >10MHz

Agilent 33120A is our standard

ability to sync with external clock (typically use rebidium standard) Square wave, sine wave, amplitude, frequency. offset would not matter much.

Q7 - What information should be provided by the summary report?

N/A

Supply current, rdson, vector or scan pattern pass/fail data Date/time, user, IC name/model#, serial #, resistance measurements on each pin combo, voltage/current readings, input stimuli applied, output measured, SW version #, equipment model #s/calibration dates Pass / Fail output, test limits, actual value measured, power draw during test, test station ID, test location, test operator, Test date/time monitor all power and other voltages, digital signals

EVERYTHING ON SAME TIME STAMP I don't have enough experience to know for sure. If the evaluation occurs automatically, I would like to know all of the configuration that went into the test. I want to know unexpected values, and if space allows, the measurements of output shown in some simple manner.

Q8 - Do you have recommendations/additional features that you would like implemented on an evaluation platform?

this gets tight really fast

Eeprom for loading of scan vectors

Resistance measurements across each pin combo -- automated (with MUX) is desired goal, but manual is fine

I want it to look nice.

Is there a way to use this so that I can spy on an I2C bus and see the output as binary values?

Appendix F: Adjustable Power Supply Map and Linearity

Code	Output (V)	Code	Output (V)	Code	Output (V)	Code	Output (V)
0	3.863	34	3.847	68	3.761	102	3.119
1	3.863	35	3.846	69	3.749	103	3.099
2	3.863	36	3.845	70	3.735	104	3.079
3	3.862	37	3.845	71	3.719	105	3.06
4	3.862	38	3.844	72	3.702	106	3.041
5	3.862	39	3.843	73	3.684	107	3.021
6	3.861	40	3.841	74	3.665	108	3.001
7	3.861	41	3.84	75	3.645	109	2.982
8	3.86	42	3.839	76	3.626	110	2.962
9	3.86	43	3.838	77	3.606	111	2.943
10	3.859	44	3.836	78	3.587	112	2.925
11	3.859	45	3.836	79	3.567	113	2.905
12	3.859	46	3.834	80	3.548	114	2.885
13	3.858	47	3.833	81	3.529	115	2.866
14	3.857	48	3.833	82	3.509	116	2.846
15	3.857	49	3.832	83	3.489	117	2.827
16	3.858	50	3.83	84	3.47	118	2.807
17	3.857	51	3.829	85	3.451	119	2.788
18	3.857	52	3.827	86	3.431	120	2.768
19	3.856	53	3.825	87	3.412	121	2.749
20	3.855	54	3.823	88	3.392	122	2.729

21	3.855	55	3.821	89	3.373	123	2.71
22	3.854	56	3.819	90	3.353	124	2.69
23	3.854	57	3.816	91	3.333	125	2.67
24	3.852	58	3.814	92	3.314	126	2.651
25	3.852	59	3.811	93	3.294	127	2.631
26	3.852	60	3.807	94	3.275	128	2.602
27	3.851	61	3.804	95	3.255	129	2.583
28	3.85	62	3.8	96	3.236	130	2.563
29	3.85	63	3.796	97	3.216	131	2.544
30	3.849	64	3.793	98	3.197	132	2.524
31	3.848	65	3.786	99	3.177	133	2.504
32	3.849	66	3.779	100	3.157	134	2.485
33	3.848	67	3.771	101	3.138	135	2.465

Code	Output	Code	Output	Code	Output	Code	Output
136	2.446	170	1.76	204	1.058	238	0.3703
137	2.427	171	1.74	205	1.039	239	0.3503
138	2.407	172	1.72	206	1.019	240	0.3163
139	2.388	173	1.701	207	0.9992	241	0.2967
140	2.368	174	1.681	208	0.963	242	0.2767
141	2.348	175	1.661	209	0.9432	243	0.2571
142	2.329	176	1.621	210	0.9235	244	0.2374
143	2.309	177	1.601	211	0.9039	245	0.218
144	2.281	178	1.581	212	0.8843	246	0.1984
145	2.261	179	1.562	213	0.8649	247	0.1788
146	2.241	180	1.542	214	0.8453	248	0.1592
147	2.221	181	1.523	215	0.8257	249	0.1397

148	2.202	182	1.503	216	0.8061	250	0.1201
149	2.182	183	1.484	217	0.7866	251	0.1005
150	2.163	184	1.464	218	0.7671	252	0.0809
151	2.143	185	1.445	219	0.7475	253	0.0612
152	2.124	186	1.425	220	0.7279	254	0.0418
153	2.104	187	1.405	221	0.7082	255	0.0223
154	2.085	188	1.386	222	0.6885		
155	2.065	189	1.366	223	0.6687		
156	2.046	190	1.346	224	0.6449		
157	2.026	191	1.327	225	0.6251		
158	2.006	192	1.293	226	0.6054		
159	1.987	193	1.273	227	0.5859		
160	1.955	194	1.254	228	0.5662		
161	1.935	195	1.234	229	0.5467		
162	1.916	196	1.215	230	0.5272		
163	1.896	197	1.195	231	0.5076		
164	1.876	198	1.175	232	0.488		
165	1.857	199	1.156	233	0.4685		
166	1.837	200	1.136	234	0.4489		
167	1.818	201	1.117	235	0.4294		
168	1.798	202	1.097	236	0.4097		
169	1.779	203	1.078	237	0.39		

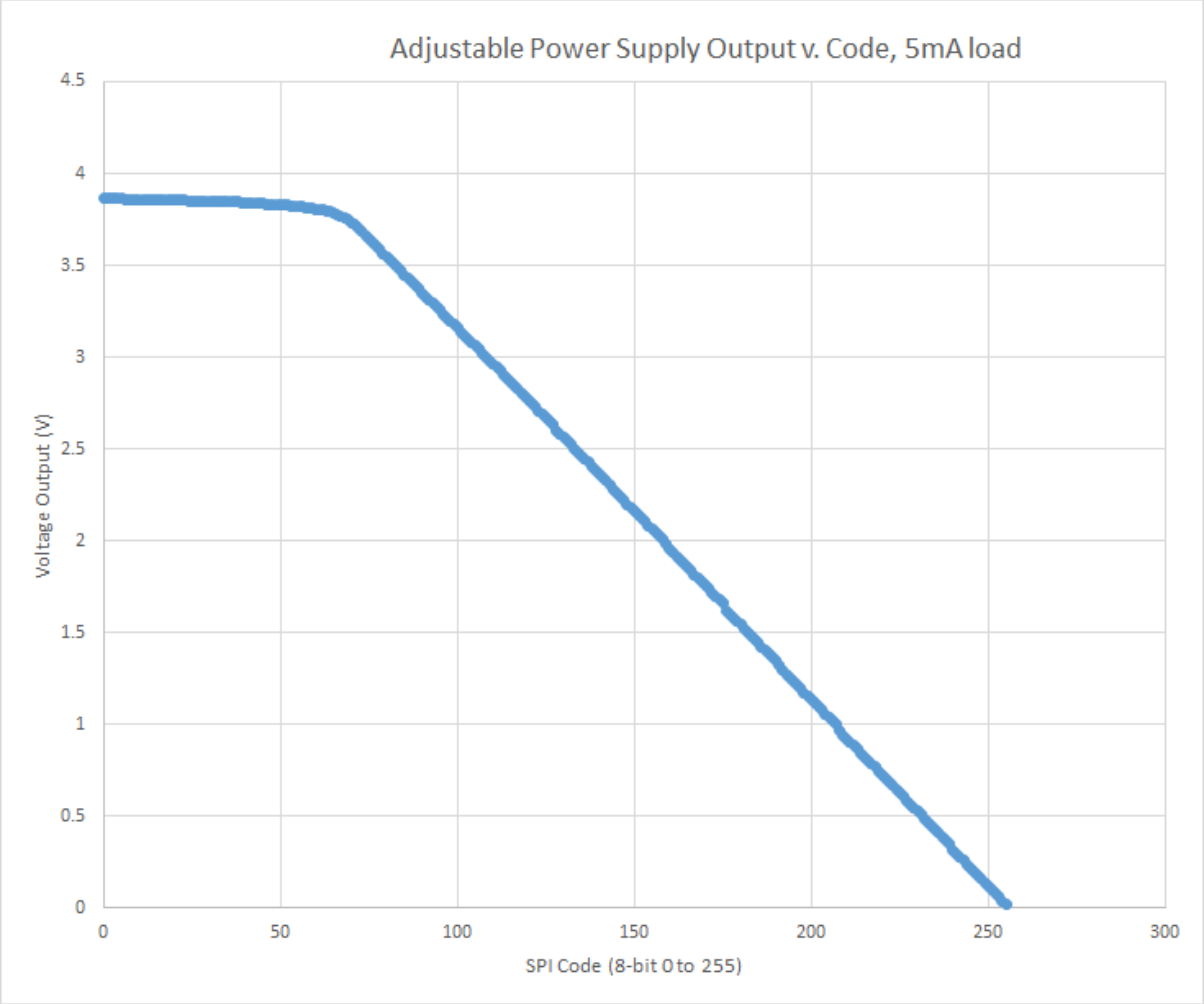

Figure 0.1 Adjustable Power Supply Output v. Code