

Accelerating Augmented Reality Video Processing with FPGAs

Anthony Dresser (CS, ECE), Lukas Hunker (CS, ECE), Andrew Weiler (ECE) Advisors: Professor Michael Ciaraldi (CS), Professor James Duckworth (ECE)

Background/Motivation

Virtual Reality is a fast growing field with several new systems shipping this year

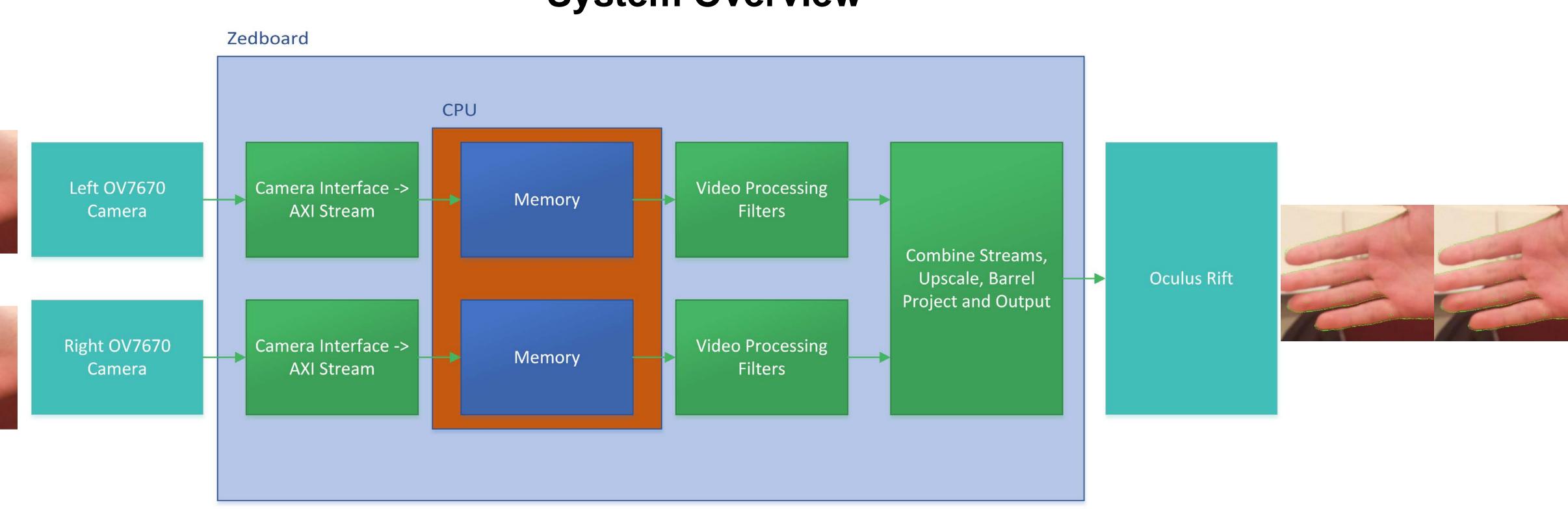
Currently \$1000+ gaming PC is needed in addition to VR hardware

FPGAs allow for efficient parallel video processing, making them an ideal candidate for VR/AR systems



https://www.flickr.com/photos/collinmel/14802996132

System Overview



Zedboard

Video Hardware

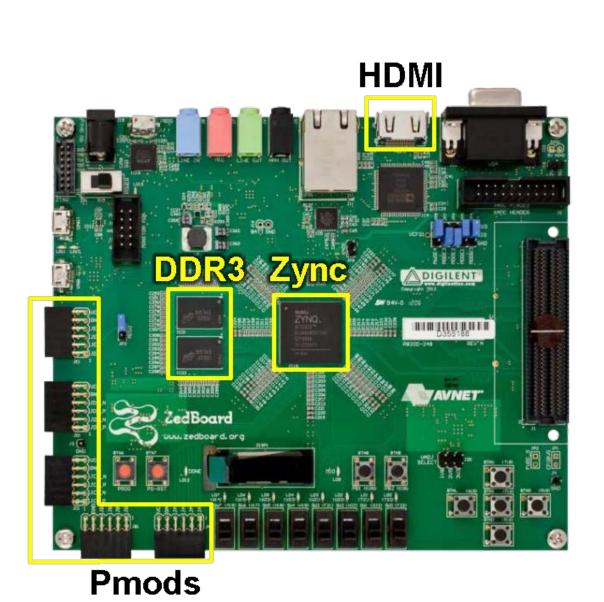
•1080 x 1920 resolution

•Interfaces over USB and HDMI

Oculus Rift DK2

OV7670 camera

serial port



Zync chip contains both an ARM Cortex A9 and a **FPGA**

512 MB of DDR3 memory

5 PMOD expansion ports

Video Filters

Original Image

 Comes in as a grayscale image for easier processing

Delta Frame Filter

 Processes what has changed between two frames by taking the absolute difference

Thresholding

 Removes any values below a threshold and sets the rest at maximum white

Median Filter

 Takes the median of each pixel to reduce noise

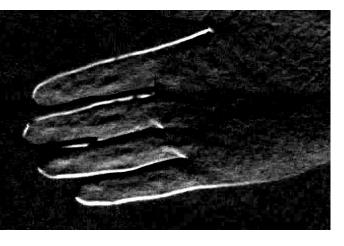
Sobel Filter

 Detects final edges on the objects found in the image

Overlay

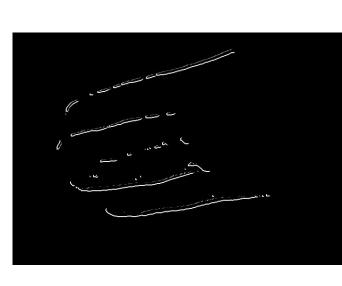
 Takes the information from the Sobel filter and writes it on top of the original image













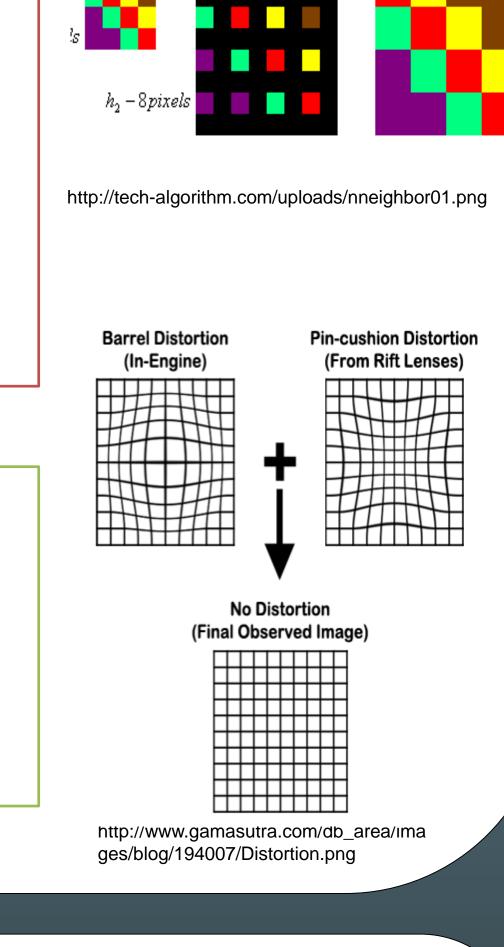
Barrel Projection and Scaling

Scaling

- Scales from 640x480 to 1080x960 for Oculus
- Uses nearest neighbor horizontally
- Duplicates each line

Barrel Projection

- Correct for Oculus lens distortion
- Maps radius of coordinates in polar space



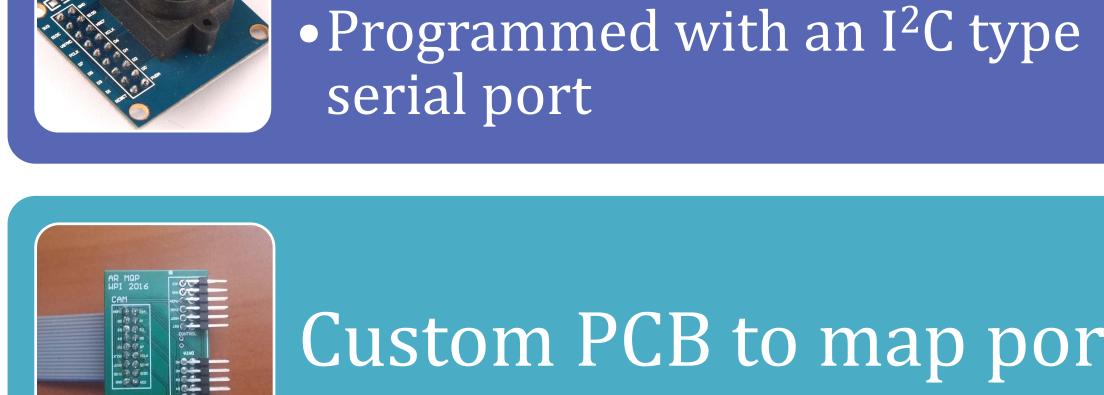
Accomplishments & Conclusions

Created working endto-end system

Developed filters for highlighting differences

Costs about half as much as a typical VR capable computer

Reduced size, weight and power consumption compared to a desktop PC



Custom PCB to map ports